Verilog coding Instructions

(CO202-Mini Project)

1. Verilog code file name: VerilogGM-102-205.v (Gate Modelling - GM), VerilogDM-102-205.v (Dataflow Modelling - DM) and VerilogBM-102-205.v (Behavioural Modelling - BM). Verilog code test-bench file name: Verilog-102-205.v and should be common for GM, DM and BM. (**Note:** Behavioural modelling is compulsory and Gate modeling or Dataflow modelling)
2. The name of the main module in GM, DM and BM should be VerilogGM_102_205, VerilogDM_102_205 and VerilogBM_102_205 respectively. The name of the test-bench module should be Verilog_102_205.
3. The name of the "vvp" output in GM, DM and BM should be VerilogGM-102-205.vcd, VerilogDM-102-205.vcd and VerilogBM-102-205.vcd respectively.
4. Additional README text file with the name Verilog-102-205.txt
5. Documents to be uploaded: Verilog code (2 files), test-bench code (1 file), "vvp" output (2 files) and README text file (1 file). Instead of uploading individual files, a team can also upload the "zip" file with the name Verilog-102-205.zip.
6. Verilog code (.v – 2 files) and test-bench (.v – 1 file) should start with comments indicating:
    - Title of the mini project:
    - Reg. No.:
    - Abstract:
    - Functionalities:
    - Brief descriptions on code:
7. Declarations of input and output (in small letters) should be done at the beginning of module(s) one per line with comment. Select meaningful names for variables reflecting its purpose.
8. Use proper indent for the proper formatting of code.
9. Start the Verilog code module with brief descriptions.
10. Write proper comments for conditional, looping and case statements.
11. Test-bench should include proper comments, indent, formatting and stimulus which demonstrates all the functionalities of your mini project.
12. To encourage the hardware model of mini project, a grace marks of maximum 10 (conditions apply) will be awarded in mini project (not exceeding 25) to a team, if a team

could demonstrate hardware model (build only by respective team members) on or before 15.11.2017. (**Note:** If a team is willing to demonstrate their hardware model of mini project, they should inform course instructor by 10.11.2017)

Verilog code Evaluation Scheme

(Mini Project)

Sl. No.	Items	Marks	Remarks
1	Follow up of above instructions *	4	Follow up of above 1-11 instructions
2	Demonstrations of all the functionalities	5	Demonstration of all the functionalities quoted in an abstract and DFD
3	Presentation	1	Your preparations and seriousness
Total		**10**	

Note: * - is mandatory for a team to proceed with the further evaluations

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