Mojo:

**Conclusion:**

still early in development, so wouldn’t suggest it yet. But in the future, when its more fleshed out/developed, yes.

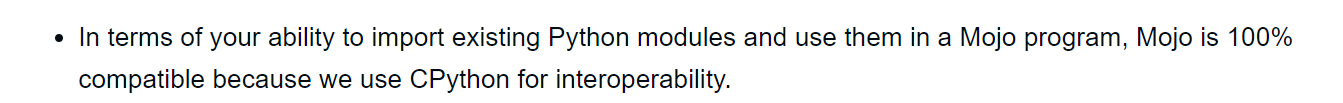
**Progress:**

need linux. in windows, use wsl. Got the environment working, but didn’t successfully convert python program to mojo yet.

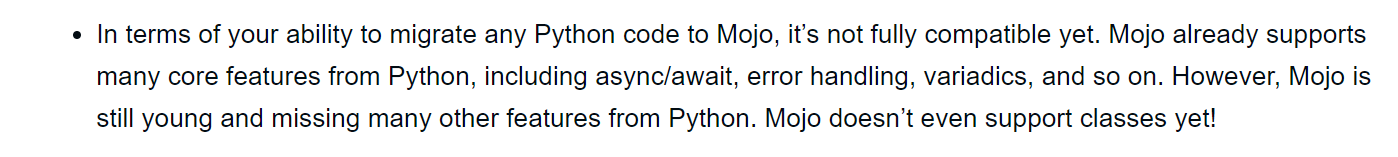
couldn’t get the python program converted to mojo yet even with from python import python. Had a problem with functions/variables

**Notes:**

* base lang is fully compatible with python. Mojo is a superset of python. Still use same libraries Supports libraries but not fully compatible. Ex numpy or scikitlearn



* few differences with python apparently, but wouldn’t suggest converting stuff/programming with it yet



A screenshot of a computer

Description automatically generated

-works with jupyter

Gem5:

you mentioned to read jbl files learn from phd student. But read in the message file

A screenshot of a computer screen

Description automatically generated

**Verification: verified most, it reads in the groups ✅**

('cpu0', 'dcache0', (10, 19, 20, 23, 26, 28, 38, 39, 40, 41, 52, 58, 64))

* 10:cpu0:dcache0:WriteReq
* 20:cpu0:dcache0:ReadReq
* 38:cpu0:dcache0:LockedRMWReadReq
* 40:cpu0:dcache0:LockedRMWWriteReq

('cpu0', 'icache0', (0, 9))

* 0:cpu0:icache0:ReadReq
* 9:icache0:cpu0:ReadResp

('cpu1', 'dcache1', (47, 50, 51, 57, 61, 69, 70, 71, 74, 88, 90, 101))

* 47:cpu1:dcache1:WriteReq
* 51:cpu1:dcache1:ReadReq
* 61:cpu1:dcache1:LockedRMWReadReq
* 70:cpu1:dcache1:LockedRMWWriteReq
* 50:dcache1:cpu1:WriteResp
* 57:dcache1:cpu1:ReadResp
* 69:dcache1:cpu1:LockedRMWReadResp
* 71:dcache1:cpu1:LockedRMWWriteResp
* 74:dcache1:cpu1:CleanEvict
* 88:dcache1:cpu1:ReadSharedReq
* 90:dcache1:cpu1:ReadExReq
* 101:dcache1:cpu1:UpgradeReq

('cpu1', 'icache1', (42, 46))

* 42:cpu1:icache1:ReadReq
* 46:icache1:cpu1:ReadResp

('cpu2', 'dcache2', (80, 83, 84, 87, 93, 96, 97, 98, 105, 108, 123, 133))

* 80:cpu2:dcache2:WriteReq
* 84:cpu2:dcache2:ReadReq
* 93:cpu2:dcache2:LockedRMWReadReq
* 97:cpu2:dcache2:LockedRMWWriteReq
* 83:dcache2:cpu2:WriteResp
* 87:dcache2:cpu2:ReadResp
* 96:dcache2:cpu2:LockedRMWReadResp
* 98:dcache2:cpu2:LockedRMWWriteResp
* 105:dcache2:cpu2:UpgradeReq
* 108:dcache2:cpu2:ReadSharedReq
* 123:dcache2:cpu2:ReadExReq
* 133:dcache2:cpu2:CleanEvict

('cpu2', 'icache2', (76, 79))

('cpu3', 'dcache3', (115, 118, 119, 122, 126, 129, 130, 131, 135, 138, 144, 146, 149))

* 115:cpu3:dcache3:WriteReq
* 119:cpu3:dcache3:ReadReq
* 126:cpu3:dcache3:LockedRMWReadReq
* 130:cpu3:dcache3:LockedRMWWriteReq
* 118:dcache3:cpu3:WriteResp
* 122:dcache3:cpu3:ReadResp
* 129:dcache3:cpu3:LockedRMWReadResp
* 131:dcache3:cpu3:LockedRMWWriteResp
* 135:dcache3:cpu3:WritebackDirty
* 138:dcache3:cpu3:ReadSharedReq
* 144:dcache3:cpu3:CleanEvict
* 146:dcache3:cpu3:UpgradeReq
* 149:dcache3:cpu3:ReadExReq

('cpu3', 'icache3', (111, 114))

('dcache0', 'l2bus', (12, 18, 21, 22, 27, 30, 34, 53, 55, 59, 60, 65, 67, 141, 142))

('dcache1', 'l2bus', (48, 49, 54, 56, 66, 68, 75, 89, 91, 92, 100, 102, 103, 107))

('dcache2', 'l2bus', (81, 82, 85, 86, 94, 95, 106, 109, 110, 124, 125, 132, 134))

('dcache3', 'l2bus', (116, 117, 120, 121, 127, 128, 136, 139, 140, 145, 147, 148, 150, 151))

* 116:dcache3:l2bus:ReadExReq
* 120:dcache3:l2bus:ReadSharedReq
* 127:dcache3:l2bus:UpgradeReq
* 136:dcache3:l2bus:WritebackDirty
* 140:dcache3:l2bus:ReadResp
* 148:dcache3:l2bus:UpgradeResp
* 151:dcache3:l2bus:ReadExResp
* 117:l2bus:dcache3:ReadExResp
* 121:l2bus:dcache3:ReadResp
* 128:l2bus:dcache3:UpgradeResp
* 139:l2bus:dcache3:ReadSharedReq
* 145:l2bus:dcache3:CleanEvict
* 147:l2bus:dcache3:UpgradeReq
* 150:l2bus:dcache3:ReadExReq

('dram', 'membus', (3, 5, 13, 15, 36))

('icache0', 'l2bus', (2, 8, 25, 33, 43))

('icache1', 'l2bus', (44, 45, 72, 73))

('icache2', 'l2bus', (77, 78, 99, 104))

('icache3', 'l2bus', (112, 113, 137, 152))

('l2bus', 'l2cache', (1, 7, 11, 17, 24, 29, 31, 35, 63, 143))

('l2cache', 'membus', (4, 6, 14, 16, 32, 37, 62, 153))