MP Assignment IV

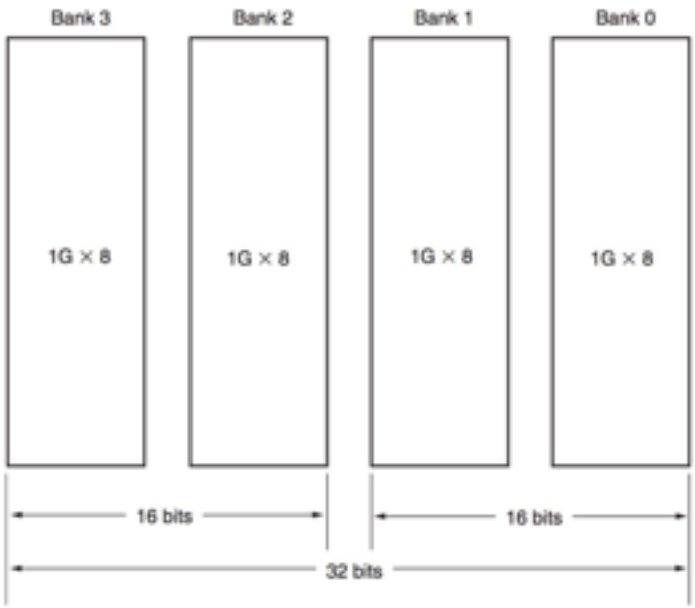
1. **A. Describe the 80386DX memory system and explain the purpose and operation of the bank selection signals.**

   The 80386 has a 32-bit data bus and four banks of memory.

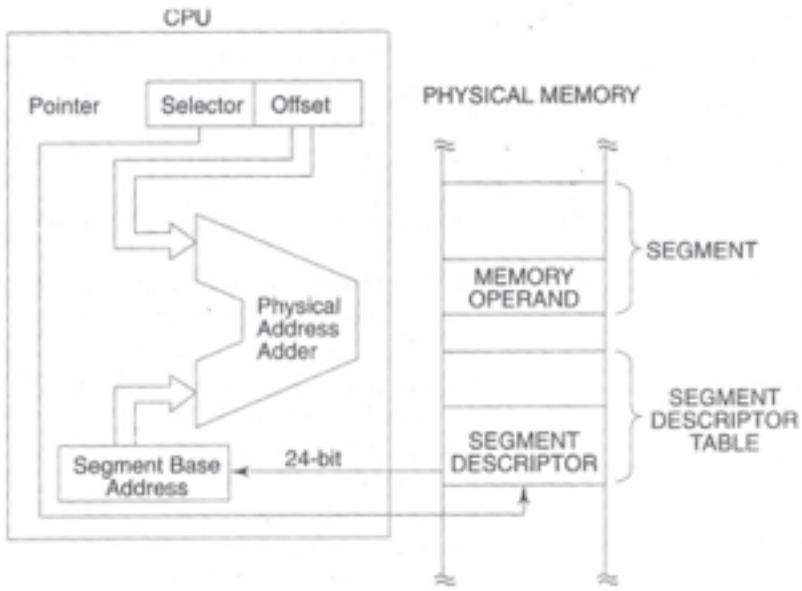
   A logical address specified in an instruction is first translated to a linear address by the segmenting hardware. This linear address is then translated to a physical address by the paging unit, which allows a virtual address of a program to be located in any portion of physical memory.

   The memory banks for 80386DX are large memory systems contain four 8-bit-wide banks that each contain up to 1GB of memory. Bank selection is accomplished by the bank selection signals BE_3, BE_2, BE_1, and BE_0. If a 32-bit number is transferred, all four banks are selected; if a 16-bit number is transferred, two banks (usually BE_3 and BE_2 or BE_1 and BE_0) are selected; and if 8 bits are transferred, a single bank is selected.

   Memory location 00000000H is in bank 0, location 00000001H is in bank 1, location 00000002H is in bank 2, and location 00000003H is in bank 3. The 80386 does not contain address connections A_1 and A_0 because these have been encoded as the bank enable signals.

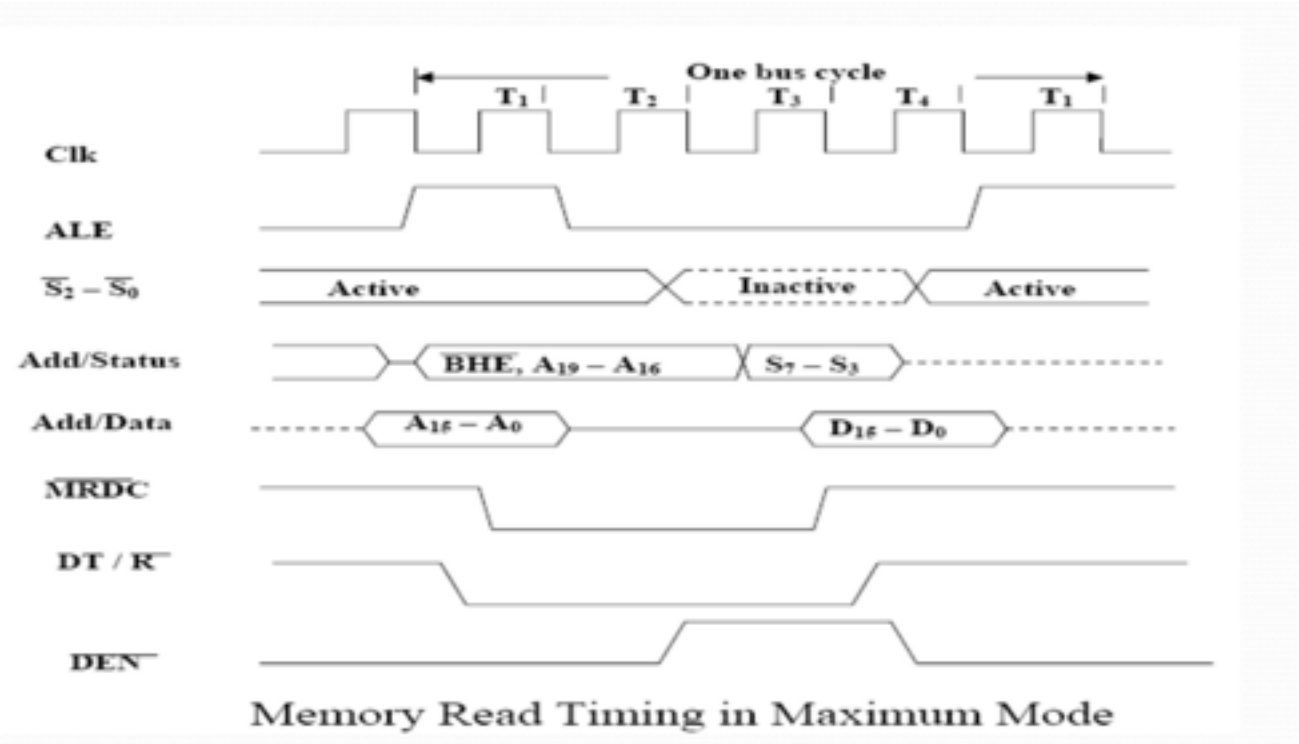


1. **B. With a neat diagram, explain how 24-bit physical address is generated in 80286 protected mode.**



The 80286's protected mode extends the processor's address space to 2^{24} bytes (16 megabytes), but not by adjusting the shift value. Instead, the 16-bit segment registers now contain an index into a table of segment descriptors containing 24-bit base addresses to which the offset is added. To support old software, the processor starts up in "real mode", a mode in which it uses the segmented addressing model of the 8086.

2. **A. Draw the timing diagram for 8086 maximum mode input operation. Include only the output signals of 8288 bus controller along with clock in the timing diagram.**



Memory Read Timing in Maximum Mode

2. B. Explain the following signal groups of 80386:

a. Bus control

BE_{3-0}# Bank Enable	Select the access of a byte, word, or double-word of data. These signals are generated internally by the microprocessor from address bits A_1 and A_0.
A_{31-2}	Connections address any of the 1G × 32 (4G bytes) memory locations found in the 80386 memory system. Note that A_0 and A_1 are encoded in the bus enable (BE3-BE0) to select any or all of the four bytes in a 32-bit-wide memory location.
D_{31-0}	Connections transfer data between the microprocessor and its memory and I/O system.

b. Bus cycle definition

W/R#	Indicates that the current bus cycle is a write when a logic 1 or a read when a logic 0.
D/C#	Indicates that the data bus contains data for or from memory or I/O when a logic 1. If D/C is a logic 0, the microprocessor is halted or executes an interrupt acknowledge.
M/IO#	Selects a memory device when a logic 1 or an I/O device when a logic 0. During the I/O operation, the address bus contains a 16-bit I/O address on address connections A_{15-2}.
LOCK#	Becomes a logic 0 whenever an instruction is prefixed with the LOCK: prefix. This is used most often during DMA accesses.

c. Coprocessor signaling

PEREQ#	The **coprocessor request** asks the 80386 to relinquish control and is a direct connection to the 80387 arithmetic coprocessor.
BUSY#	Input used by the WAIT or FWAIT instruction that waits for the coprocessor to become not busy. This is also a direct connection to the 80387 from the 80386.
ERROR#	Indicates to the microprocessor that an error is detected by the coprocessor.

3. A. i) Explain how TLB read and write operations are performed using the test registers in 80386.

READ

- Write TR_6 with the linear address, making sure that C = 1.
- Read both TR_6 and TR_7. If the PL bit indicates a hit, then the desired values of TR_6 and TR_7 indicate the contents of the TLB.

WRITE

- Write TR_7 for the desired physical address, PL, and REP values.
- Write TR_6 with the linear address, making sure that C = 0.

3. A. ii) Describe the role of following control bits in CR0 of 80386.

a. MP

Is set to indicate that the arithmetic **coprocessor is present** in the system.

b. PG

Selects **page table translation** of linear addresses into physical addresses when PG = 1. Page table translation allows any linear address to be assigned any physical memory location.

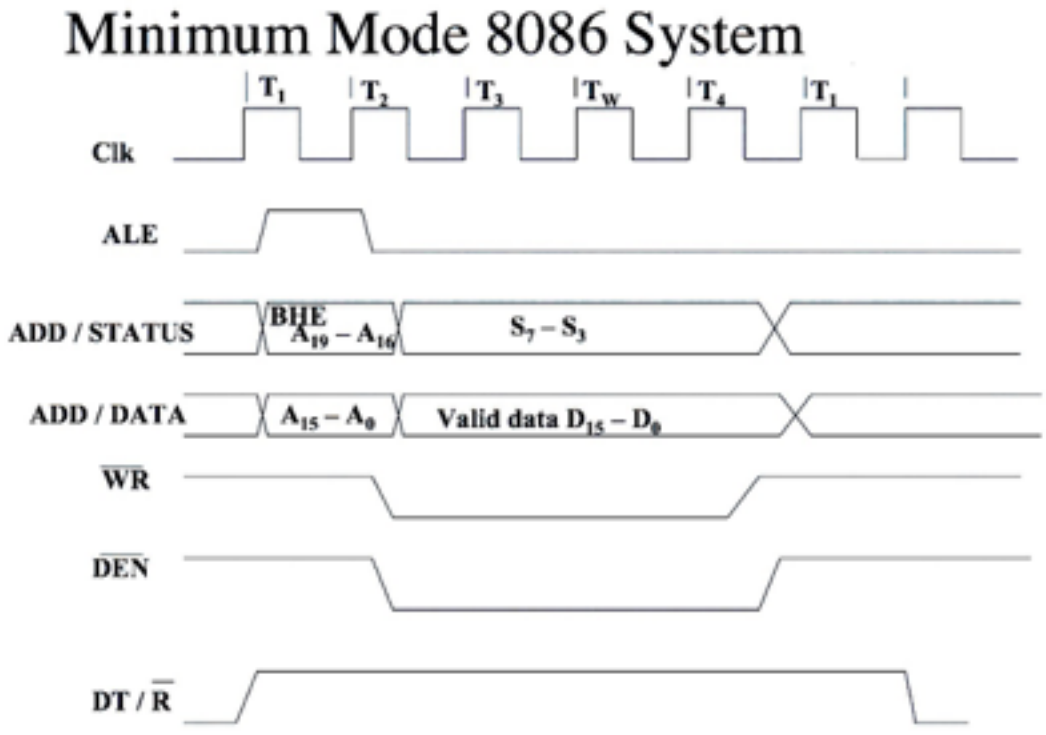
c. PE

Is set to select the **protected mode** of operation for the 80386. It may also be cleared to reenter the real mode. This bit can only be set in the 80286. The 80286 could not return to real mode without a hardware reset, which precludes its use in most systems that use protected mode.

d. ET

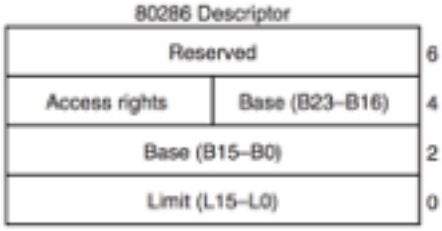
Selects the **80287 coprocessor** when ET 0 or the **80387 coprocessor** when ET I. This bit was installed because there was no 80387 available when the 80386 first appeared. In most systems, ET is set to indicate that an 80387 is present in the system.

3. B. Draw a neat sketch of 8086 minimum mode bus timing diagram for a write operation.



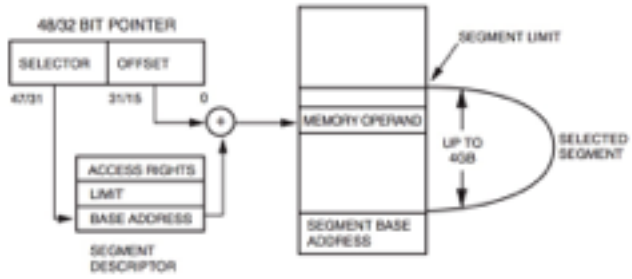
4. A. Distinguish 80286 and 80386 microprocessors with respect to descriptors and selectors. Also draw and explain the descriptor format for 80386.

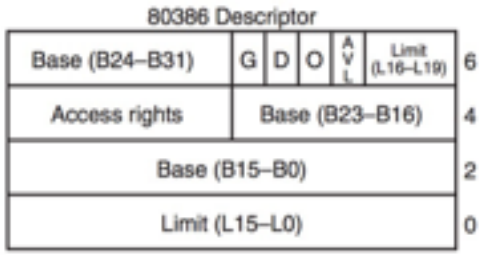
The main difference between the 80286 and 80386 is that the latter has two additional selectors (FS and GS) and the most significant two bytes of the descriptor are defined for the 80386. Another difference is that 80386 descriptors use a 32-bit base address and a 20-bit limit, instead of the 24-bit base address and a 16-bit limit found on the 80286.



The 80286 addresses a 16MB memory space with its 24-bit base address and has a segment length limit of 64K bytes, due to the 16-bit limit. The 80386 addresses a 4GB memory space with its 32-bit base address and has a segment length limit of 1MB or 4GB, due to a 20-bit limit that is used in two different ways. The 20-bit limit can access a segment with a length of 1M byte if the granularity bit (G) = 0. If G = 1, the 20-bit limit allows a segment length of 4G bytes.

The granularity bit is found in the 80386 descriptor. If G = 0, the number stored in the limit is interpreted directly as a limit, allowing it to contain any limit between 00000H and FFFFFH for a segment size up to 1MB. If G = 1, the number stored in the limit is interpreted as 00000XXXH-FFFFFXXXH, where the XXX is any value between 000H and FFFH.





4. B. Explain the various processing units in 80286 architecture.

Bus Unit (BU):

It has address latches, data transceivers, bus interface and circuitry, instruction pre-fetcher, processor extension interface and 6 byte instruction queue.

Functions :

- To perform all memory and I/O read and write.
- To pre-fetch the instruction bytes.
- To control the transfer of data to and from processor extension devices like 80287 math co-processor.
- Whenever BU is not using the buses for the operation, it pre-fetches the instruction bytes and put them is a 6 byte pre-fetch queue.

Instruction Unit (IU):

It has 3 decoded instruction queue and instruction decoder.

Functions :

- It fully decodes up to three prefetched instructions and holds them in a queue.
- So that EU can access them.
- It helps the processor to speed up, as pipelining of instruction is done.

Execution Unit (EU):

It includes ALU, registers and the Control unit. Registers are general purpose, index, pointer, flag register and 16 –bit Machine Status Word (MSW).

Functions :

- To sequentially execute the instructions received from the instruction unit.
- ALU result is either stored in register bank or sent over the data bus.

Address Unit (AU):

It consists of segment registers, offset address and a physical address adder.

Functions :

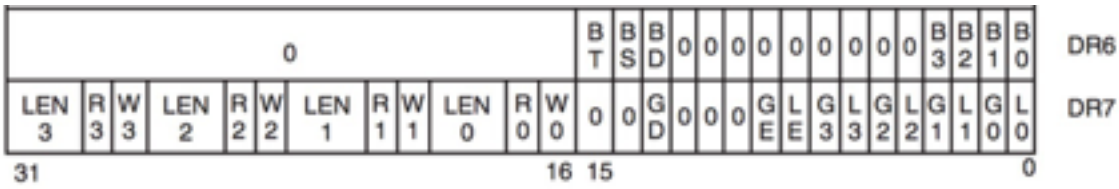
- Compute the physical address that will be sent out to the memory or I/O by BU.
- 80286 operate in two different modes
  1. real address mode
  2. Protected virtual address mode.
- When used in Real address mode, AU computes the address with segment base and offset like 8086. Segment register are CS, DS, ES and SS hold base address. IP, BP, SI, DI , SP hold offset.
- Maximum physical space allowed in this mode is 1MB.
- When 80286 operate in protected mode, the address unit acts as MMU.
- All 24 address lines used and can access up to 16MB of physical memory.
- If descriptor table scheme is used it can address up to 1GB of virtual memory.

5. A. Explain how an 80286 is switched from real address mode to protected virtual address mode and how it is switched back to real address mode operation.

80286 is switched from real mode to protected mode by setting the protection enable bit in the MSW. Bit 0 of the MSW is used to switch between real and protected mode. Once the desired word is loaded in a register or memory location, 80286 is switched to protected mode by executing LMSW (Load Machine Status Word). Finally, to get 80286 operating in protected mode, An inter-segment jump to the start of the main system is executed, flushing the instruction byte queue, as in protected mode the queue functions differently than in real mode.

Once it's in the virtual address mode, it can only be switched back by resetting the machine. It does not have any instruction to switch back, in accordance to the integrity protection in the Virtual Address Mode.

5. B. Discuss the various control bits in the Debug registers DR_6 and DR_7 with the aid of a neat diagram.



The control bits in DR_6 and DR_7 are defined as follows:

BT	If set = 1, the debug interrupt was caused by a task switch.
BS	If set, the debug interrupt was caused by the TF bit in the flag register.
BD	If set, the debug interrupt was caused by an attempt to read the debug register with the GD bit set. The GD bit protects access to the debug registers.
B_{3-0}	Indicate which of the four debug breakpoint addresses caused the debug interrupt.
LEN	Each of the four length fields pertains to each of the four breakpoint addresses stored in DR_0-DR_3. These bits further define the size of access at the breakpoint address as 00 (byte), 01 (word), or 11 (doubleword).
RW	Each of the four read/write fields pertains to each of the four breakpoint addresses stored in DR_0-DR_3. The RW field selects the cause of action that enabled a break- point address as 00 (instruction access), 01 (data write), and 11 (data read and write).
GD	If set, GD prevents any read or write of a debug register by generating the debug interrupt. This bit is automatically cleared during the debug interrupt so that the debug registers can be read or changed, if needed.
GE	If set, selects a global breakpoint address for any of the four breakpoint address registers.
LE	If set, selects a local breakpoint address for any of the four breakpoint address registers.