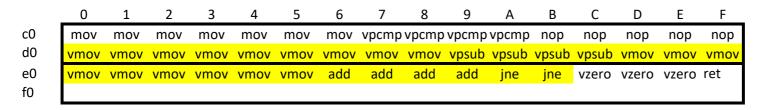
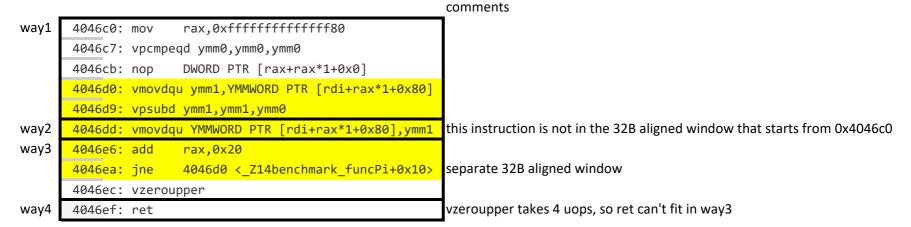
### baseline

#### Code layout



#### DSB layout

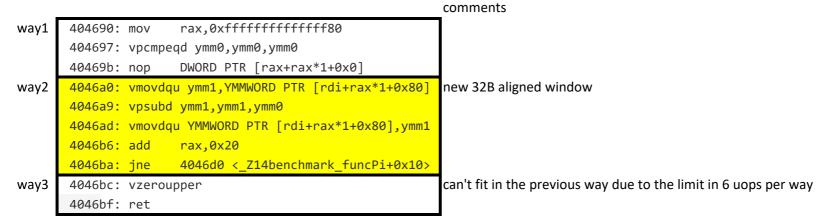


## no\_foo

### Code layout

_	0	1	2	3	4	5	6	7	8	9	Α	В	С	D	Ε	F
80																
90	mov	vpcmp	vpcmp	vpcmp	vpcmp	nop	nop	nop	nop	nop						
a0	vmov	vmov	vpsub	vpsub	vpsub	vpsub	vmov	vmov	vmov							
b0	vmov	vmov	vmov	vmov	vmov	vmov	add	add	add	add	jne	jne	vzero	vzero	vzero	ret
c0																
d0																

#### DSB layout

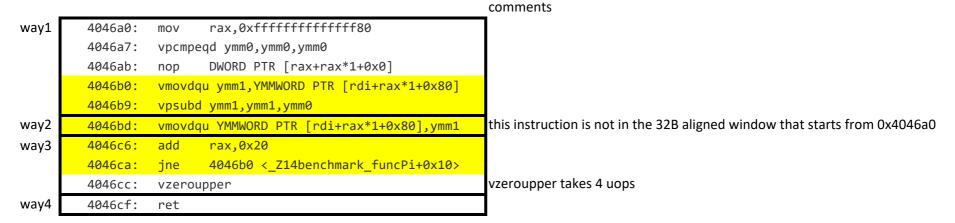


# aligned\_functions

### Code layout

_	0	1	2	3	4	5	6	7	8	9	Α	В	С	D	Ε	F
a0	mov	vpcmp	vpcmp	vpcmp	vpcmp	nop	nop	nop	nop	nop						
b0	vmov	vmov	vpsub	vpsub	vpsub	vpsub	vmov	vmov	vmov							
c0	vmov	vmov	vmov	vmov	vmov	vmov	add	add	add	add	jne	jne	vzero	vzero	vzero	ret
d0																

### DSB layout



# aligned\_blocks

### Code layout

	0	1	2	3	4	5	6	7	8	9	Α	В	С	D	Е	F
a0	mov	mov	mov	mov	mov	mov	mov	vpcmp	vpcmp	vpcmp	vpcmp	nop	nop	nop	nop	nop
b0	nop	nop	nop	nop	nop	nop	nop	nop	nop	nop	nop	nop	nop	nop	nop	nop
c0	vmov	vmov	vmov	vmov	vmov	vmov	vmov	vmov	vmov	vpsub	vpsub	vpsub	vpsub	vmov	vmov	vmov
d0	vmov	vmov	vmov	vmov	vmov	vmov	add	add	add	add	jne	jne	nop	nop	nop	nop
e0	vzero	vzero	vzero	ret												
f0																

### DSB layout

comments

```
4046a0:
                        rax,0xffffffffffff80
way1
                 mov
       4046a7:
                 vpcmpeqd ymm0,ymm0,ymm0
       4046ab:
                 nop WORD PTR cs:[rax+rax*1+0x0]
way2
       4046c0:
                 vmovdqu ymm1,YMMWORD PTR [rdi+rax*1+0x80]
       4046c9:
                 vpsubd ymm1,ymm1,ymm0
       4046cd:
                 vmovdqu YMMWORD PTR [rdi+rax*1+0x80],ymm1
       4046d6:
                 add
                       rax,0x20
       4046da:
                 jne
                       4046c0 <_Z14benchmark_funcPi+0x20>
       4046dc:
                        DWORD PTR [rax+0x0]
                 nop
       4046e0:
way3
                 vzeroupper
       4046e3:
                 ret
```