baseline

Code layout

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
c0	mov	mov	mov	mov	mov	mov	mov	vpcmp	vpcmp	vpcmp	vpcmp	nop	nop	nop	nop	nop
d0	vmov	vmov	vmov	vmov	vmov	vmov	vmov	vmov	vmov	vpsub	vpsub	vpsub	vpsub	vmov	vmov	vmov
e0	vmov	vmov	vmov	vmov	vmov	vmov	add	add	add	add	jne	jne	vzero	vzero	vzero	ret
f0																

DSB layout

		comments
way1	4046c0: mov rax,0xffffffffffffff80	
	4046c7: vpcmpeqd ymm0,ymm0,ymm0	
	4046cb: nop DWORD PTR [rax+rax*1+0x0]	
	4046d0: vmovdqu ymm1,YMMWORD PTR [rdi+rax*1+0x80]	
	4046d9: vpsubd ymm1,ymm1,ymm0	
way2	4046dd: vmovdqu YMMWORD PTR [rdi+rax*1+0x80],ymm1	this instruction is not in the 32B aligned window that starts from 0x4046c0
way3	4046e6: add rax,0x20	
	4046ea: jne 4046d0 <_Z14benchmark_funcPi+0x10>	separate 32B aligned window
	4046ec: vzeroupper	
way4	4046ef: ret	vzeroupper takes 4 uops, so ret can't fit in way3

no_foo

Code layout

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
80																
90	mov	mov	mov	mov	mov	mov	mov	vpcmp	vpcmp	vpcmp	vpcmp	nop	nop	nop	nop	nop
a0	vmov	vmov	vmov	vmov	vmov	vmov	vmov	vmov	vmov	vpsub	vpsub	vpsub	vpsub	vmov	vmov	vmov
b0	vmov	vmov	vmov	vmov	vmov	vmov	add	add	add	add	jne	jne	vzero	vzero	vzero	ret
c0																
d0																

DSB layout

		comments
way1	404690: mov rax,0xffffffffffffff80 404697: vpcmpeqd ymm0,ymm0,ymm0 40469b: nop DWORD PTR [rax+rax*1+0x0]	
way2	4046a0: vmovdqu ymm1,YMMWORD PTR [rdi+rax*1+0x80] 4046a9: vpsubd ymm1,ymm1,ymm0 4046ad: vmovdqu YMMWORD PTR [rdi+rax*1+0x80],ymm1 4046b6: add rax,0x20 4046ba: jne 4046d0 <_Z14benchmark_funcPi+0x10>	new 32B aligned window
way3	4046bc: vzeroupper 4046bf: ret	can't fit in the previous way due to the limit in 6 uops per way

aligned_functions

Code layout

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
a0	mov	mov	mov	mov	mov	mov	mov	vpcmp	vpcmp	vpcmp	vpcmp	nop	nop	nop	nop	nop
b0	vmov	vmov	vmov	vmov	vmov	vmov	vmov	vmov	vmov	vpsub	vpsub	vpsub	vpsub	vmov	vmov	vmov
c0	vmov	vmov	vmov	vmov	vmov	vmov	add	add	add	add	jne	jne	vzero	vzero	vzero	ret
d0																

DSB layout

		comments
way1	4046a0: mov rax,0xffffffffffffff80	
	4046a7: vpcmpeqd ymm0,ymm0,ymm0	
	4046ab: nop DWORD PTR [rax+rax*1+0x0]	
	4046b0: vmovdqu ymm1,YMMWORD PTR [rdi+rax*1+0x80]	
	4046b9: vpsubd ymm1,ymm1,ymm0	
way2	4046bd: vmovdqu YMMWORD PTR [rdi+rax*1+0x80],ymm1	this instruction is not in the 32B aligned window that starts from 0x4046a0
way3	4046c6: add rax,0x20	
	4046ca: jne 4046b0 <_Z14benchmark_funcPi+0x10>	
	4046cc: vzeroupper	vzeroupper takes 4 uops
way4	4046cf: ret	

aligned_blocks

Code layout

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
a0	mov	mov	mov	mov	mov	mov	mov	vpcmp	vpcmp	vpcmp	vpcmp	nop	nop	nop	nop	nop
b0	nop	nop	nop	nop	nop	nop	nop	nop	nop	nop	nop	nop	nop	nop	nop	nop
c0	vmov	vmov	vmov	vmov	vmov	vmov	vmov	vmov	vmov	vpsub	vpsub	vpsub	vpsub	vmov	vmov	vmov
d0	vmov	vmov	vmov	vmov	vmov	vmov	add	add	add	add	jne	jne	nop	nop	nop	nop
e0	vzero	vzero	vzero	ret												
f0																

DSB layout

		comments
way1	4046a0: mov rax,0xffffffffffffff80	
	4046a7: vpcmpeqd ymm0,ymm0,ymm0	
	4046ab: nop WORD PTR cs:[rax+rax*1+0x0]	
way2	4046c0: vmovdqu ymm1,YMMWORD PTR [rdi+rax*1+0x80]	
	4046c9: vpsubd ymm1,ymm1,ymm0	
	4046cd: vmovdqu YMMWORD PTR [rdi+rax*1+0x80],ymm1	
	4046d6: add rax,0x20	
	4046da: jne 4046c0 <_Z14benchmark_funcPi+0x20>	
	4046dc: nop DWORD PTR [rax+0x0]	
way3	4046e0: vzeroupper	
	4046e3: ret	