

# Oscillatory Neural Networks: A digital implementation

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#### **Abstract**

The traditional Von Neumann computing paradigm struggles to keep pace with the exponential growth of data, leading to the exploration of novel computing paradigms. Oscillatory Neural Networks (ONNs), utilize oscillators for computation, offer a promising alternative by enabling efficient neuromorphic computing. In this work, we present an FPGA-based fully digital implementation of ONNs for pattern recognition.

### Introduction

- Smart edge devices are becoming prevalent across industries, but face constraints in power, memory, and bandwidth. While Al applications using deep neural networks are increasingly effective, they demand significant resources and struggle to run efficiently on small edge devices.
- In addition, privacy and security concerns would recommend the data to be stored locally. This creates a challenge for edge computing.
- This has led to research into alternative computing paradigms like neuromorphic systems.

#### **Biological inspiration**

- ONNs use coupled oscillators to mimic neural oscillations of brain, encoding information in phase relationships between oscillators. This allows for fast, energy-efficient parallel computation, making ONNs promising for AI at the edge.
- Contrarily to the classical computation based on voltage amplitude to determine a logic "1," or "0," in ONN we use the phase relations to determine the logic "1" (out-of-phase 180°) or "0" (in-phase 0°).

#### **Associative memory**

 ONNs exhibit associative memory properties similar to Hopfield Neural Networks. They can store patterns and associate inputs with the closest stored pattern[1]. Stored patterns represent the minima of an energy function toward which the network evolves.

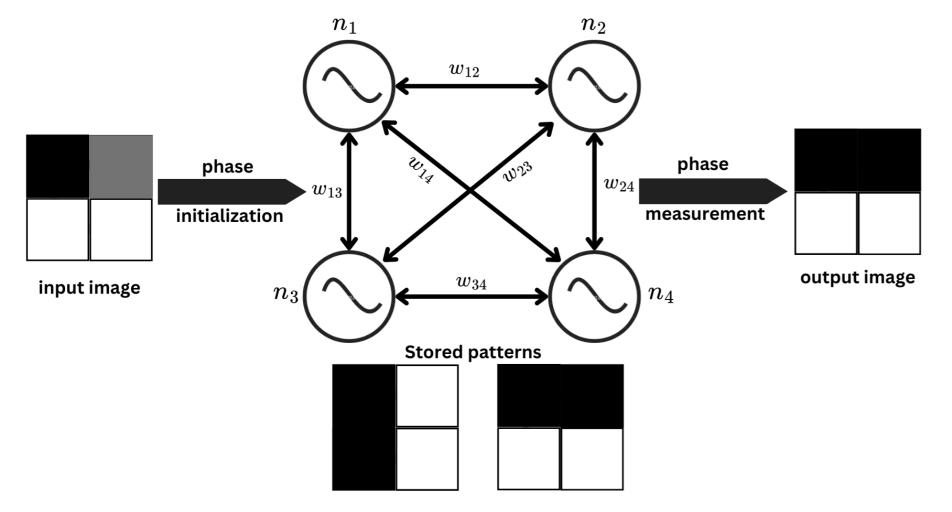


Figure 1. ONN with 4 neurons using associative memory capability to perform image recognition

# **Materials and Methods**

#### **ONN** learning

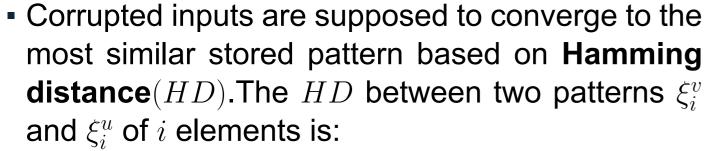
 The Hebbian learning rule is one of the most popular learning algorithm

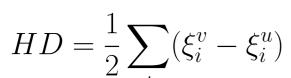
to calculate synaptic weights for bipolar-valued (-1/1) stored patterns[2].

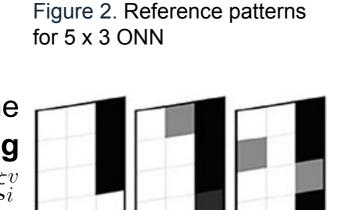
$$w_{ij} = \sum_{k} \xi_i^k \xi_j^{kT} and \quad w_{ij} = 0 \quad \forall \quad i = j$$
 (1)

where  $w_{ij}$  = synaptic weight between neuron  $n_i$  and neuron  $n_j$ .

 $\xi^k$  = vector of k-th stored pattern







(2) Figure 3. Corrupted test patterns of digit 1

#### Phase controlled oscillator

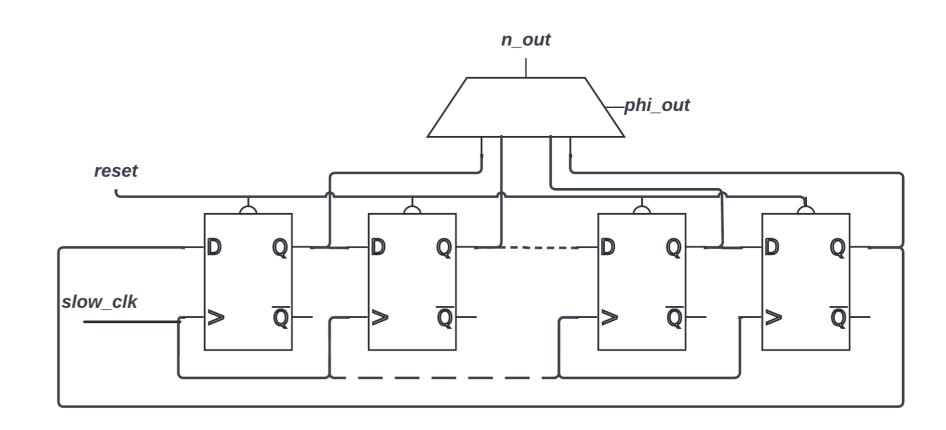


Figure 4. The 16-bit pattern [1111111100000000] cycles continuously in the circular shift register

#### **Digital ONN design**

Arithmetic logic circuit in the synapses block generates the input signal to the *i*-th neuron as:  $n_{in}[i] = sign(\sum_j w_{ij} - \sum_k w_{ik})$ 

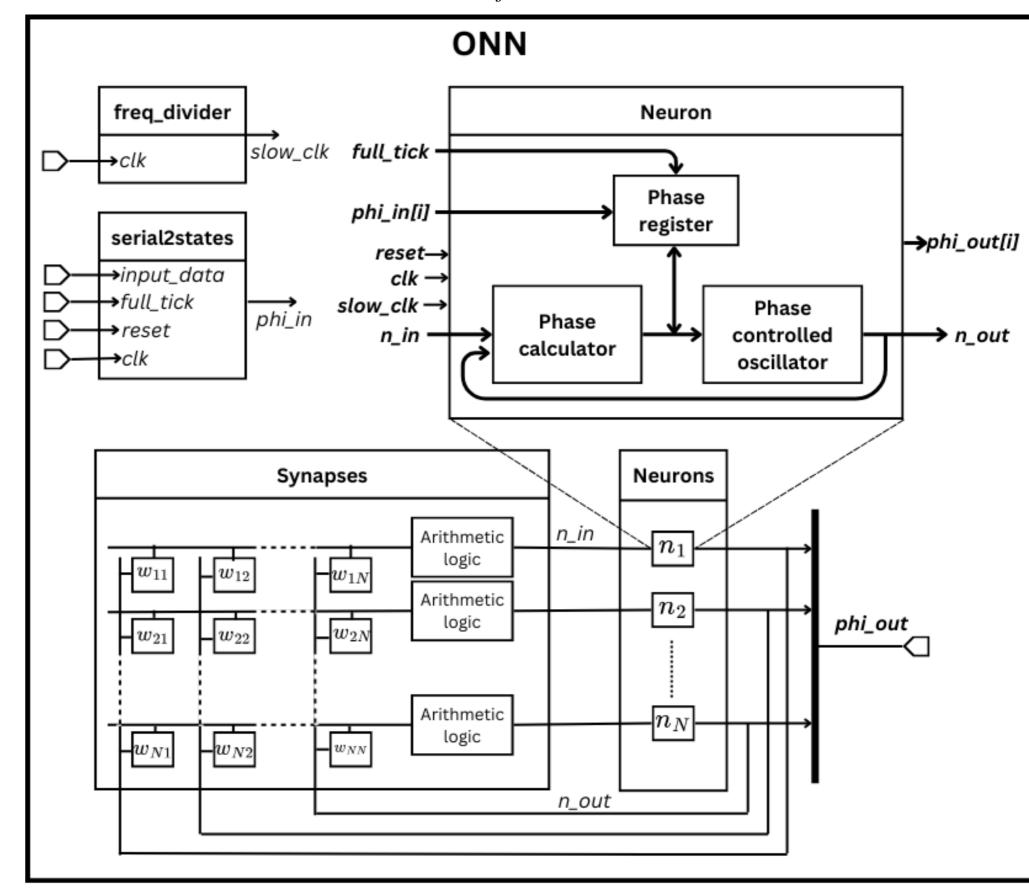


Figure 5. Fully parallel digital ONN architecture

# Results and discussion

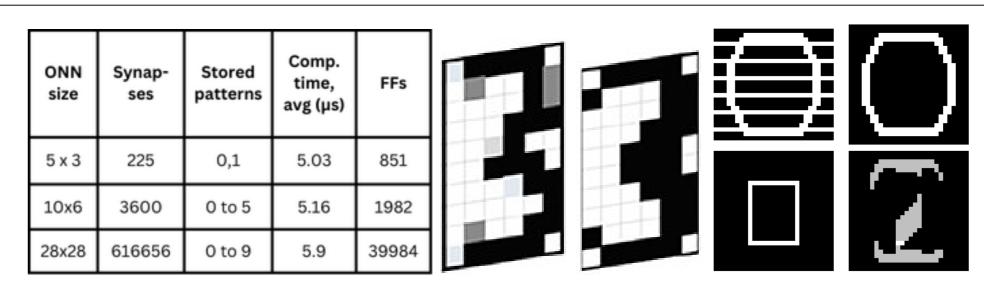


Figure 6. (right)ONN timing performances and resource utilization, (left) Test results

We observe ONN computation time remains nearly constant as network size increases, a **key feature** of the ONN concept.

## **Conclusion and Future directions**

ONNs offer a promising alternative computation paradigm due to their parallel behavior enabling fast computation independent of network size despite limitations in retrieval capacity (can be improved with enhanced learning rules). ONNs are still in their infancy for comparison with benchmarks which is the focus of future works

## References

- [1] Frank C Hoppensteadt and Eugene M Izhikevich.
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