Notes for our Milestone 3 Presentation

Because we simulated in modelsim, our clock could be very tiny. We tried to optimize around this and made sure we used a realistic clock for the FPGA

Make note of how many processing elements we'll have

> Say that we'll max out the board (up to an optimal ammount)

Make sure we have a clear definitino of a processing element

> Have a figure in the report and in the final presentation
> Talk about resources for the processing elements

Explain why we didn't include the waveform

> Do some excessive handwaving

Make sure all group members know wtf is going on

> Define PE inputs and outputs

Talk about NOC Design

> Placement for PEs

Compare to Intel Library

> Talk about optimizations