A 0.6 V, 1.5 GHz 84 Mb SRAM in 14 nm FinFET CMOS Technology With Capacitive Charge-Sharing Write Assist Circuitry

Eric Karl, *Member, IEEE*, Zheng Guo, *Member, IEEE*, James Conary, Jeffrey Miller, Yong-Gee Ng, Satyanand Nalam, *Member, IEEE*, Daeyeon Kim, *Member, IEEE*, John Keane, *Member, IEEE*, Xiaofei Wang, *Member, IEEE*, Uddalak Bhattacharya, and Kevin Zhang, *Fellow, IEEE*

***Abstract*—A 0.6–1.1 V, 84 Mb pipelined SRAM array design implemented in 14 nm FinFET CMOS technology is presented. Two array architectures featuring a high-density 0.0500 μm² 6T SRAM bitcell and a 0.0588 μm² 6T SRAM bitcell targeting low voltage operation are detailed. The high-density array design reaches 2.7 GHz at 1.1 V with 14.5 Mb/mm² bit density, while the low voltage optimized array can operate at 0.6 V, 1.5 GHz under typical process conditions. A capacitive charge-share transient voltage collapse write-assist circuit (CS-TVC) enables a 24% reduction in write energy compared to previous techniques by eliminating bias currents during operation. Technology and assist co-optimization enable >50 mV reduction in V_{MIN} and a 1.81× increase in density over a 22 nm design.**

***Index Terms*—CMOS integrated circuits, semiconductor memory, SRAM.**

I. Introduction

THE growth of battery-powered mobile and wearable devices has increased the importance of low power operation and cost in system-on-a-chip (SoC) design. Supply-voltage scaling remains the predominant approach to active power reduction for SoC integrated circuit design, including voltage scaling for on-die memory given increasing levels of memory integration. High-density SRAM bitcells implemented with minimum-sized transistors can limit the minimum operating voltage (V_{MIN}) of a design, often leading to the introduction of separate voltage supplies for the on-die memory arrays [1] or the use of larger memory cells with increased transistor size. Additional supplies increase platform cost, and operating memory at higher voltage leads to increased power consumption. Using larger transistors in SRAM bitcells often lowers the effective minimum operating voltage, but the larger bitcells increase SoC cost and incur additional leakage currents that can compromise mobile and handheld product battery life.

The introduction of FinFET devices at the 22 nm technology node delivered superior short channel effects and subthreshold slope relative to existing bulk planar device technology, enabling reduction in threshold voltage within a fixed leakage constraint [2]. Lower transistor Vth, improvements to random device variability, and assist circuits to overcome device sizing quantization enabled a >150 mV reduction in SRAM V_{MIN} [3]. At the 14 nm technology node, FinFET device sizing quantization remains a challenge for compact 6T SRAM bitcells with minimum-size transistors. Careful co-optimization between technology and design of memory assist circuits is required in order to deliver dense, low power memory operation at low voltages. In this paper we present a pair of 84 Mb SRAM array designs with wide-range voltage operation on a 14 nm logic technology featuring 2nd generation FinFET transistors.

The rest of this paper is organized as follows: Section II introduces the key features of a 14 nm FinFET logic technology and the design considerations of the two densest 14 nm bitcells. Section III discusses the design and process considerations driving the selection of V_{MIN} margin-enhancing assist circuits paired with the two dense SRAM cells, and Section IV details the design of a pair of 548 kb array macros and their integrated capacitive charge-share transient voltage collapse assist circuits (CS-TVC). Section V summarizes results collected from a 14 nm technology lead vehicle test chip.

II. 14 nm FinFET CMOS Technology

The 14 nm FinFET logic technology features transistors with a 42 nm fin height, a 42 nm fin pitch and 70 nm contacted gate pitch to deliver 83% greater fins/μm^2 relative to the 22 nm Tri-gate logic technology [2], [4]. Metal interconnect pitch scaling ranges from 0.65–0.78× relative to 22 nm, with a minimum interconnect pitch of 52 nm used at M2. The 13-layer Cu interconnect stack utilizes 8 layers of low-k CDO dielectrics and air gaps at 80 nm and 160 nm pitch layers to provide a 17% reduction in back-end metal capacitance. Advanced 193 nm immersion lithography and self-aligned double patterning (SADP) are used at critical layers to deliver logic and memory area scaling matching the historical rate of density improvement per technology generation. Despite the significant geometric scaling

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E. Karl, Z. Guo, Y.-G. Ng, S. Nalam, D. Kim, J. Keane, X. Wang, U. Bhattacharya, and K. Zhang are with Advanced Design, Logic Technology Development, Intel Corporation, Hillsboro, OR 97124 USA (e-mail: eric.a.karl@intel.com).

J. Conary is with the Compiler Memory Organization, Intel Custom Foundry, Intel Corporation, Hillsboro, OR 97124 USA.

J. Miller is with the Device Development Group, Platform Engineering Group, Intel Corporation, Hillsboro, OR 97124 USA.

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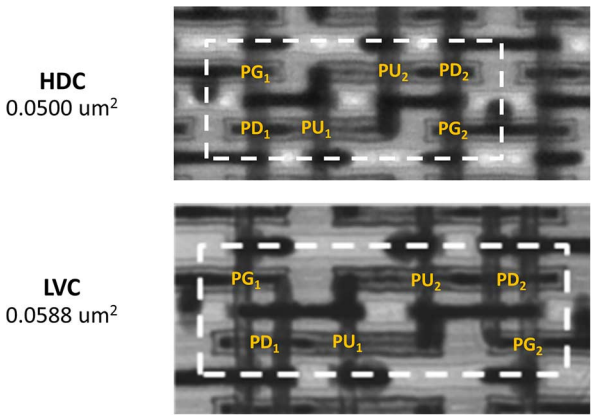

Fig. 1. 14 nm HDC and LVC SRAM bitcell top-down TEM images.

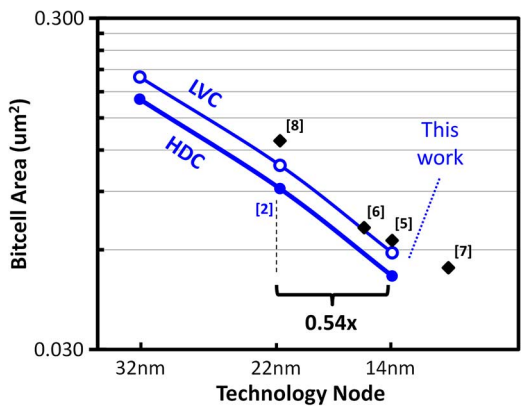

Fig. 2. 14 nm HDC and LVC SRAM bitcell scaling trend vs. recent published 6T SRAM literature. The HDC cell size is reduced to 54% of the comparable SRAM bitcell in 22 nm CMOS technology.

from the 22 nm technology node, optimizations to fin sidewall profiles and subfin doping on the 2nd generation FinFET enable a nearly 2× reduction in device random threshold voltage variation, a critical factor for 6T SRAM V_{MIN}.

Fig. 1 shows a layout diagram of a 0.0500 μm^2 high-density 6T SRAM bitcell (HDC) and a 0.0588 μm^2 low-voltage optimized 6T SRAM bitcell (LVC) in 14 nm FinFET technology. The HDC bitcell features single fins for the passgate (PG), pullup (PU) and pulldown (PD) transistors, providing minimal cell area and leakage with compromises in performance and V_{MIN} due to the single fin PG and PD devices and poor β ratio (PG to PD ratio). The LVC SRAM bitcell features a larger PD device with its 1:1:2 fin ratio (PU:PG:PD), to provide improved read stability and performance at low voltage without adding much area or leakage. Several larger SRAM bitcells featuring higher α ratios (PG to PU size) were developed for very high performance applications, but are not detailed in this work. Fig. 2 highlights recently reported SRAM bitcell designs from 22 nm, 16 nm, 14 nm and 10 nm technologies [3], [5]–[8]. The 0.050 μm^2 HDC cell in this work is the smallest reported production SRAM bitcell to date for any technology node, and is 20–30% smaller than competing solutions in announced 14 nm and 16 nm technologies.

III. SRAM Assist Circuit

Numerous memory assist circuit techniques have been described in literature as a more cost-effective path to increased stability and write margin at low voltages compared to bitcell transistor upsizing or operating the memory array at a higher supply voltage. Fin sizing quantization in FinFET-based logic technology has accelerated the adoption of memory assist circuits for dense bitcells with non-ideal α or β ratios and minimum-sized devices. The HDC SRAM cell has a 1:1 PG to PD ratio, leading to degraded stability from charge injection during read operations. Wordline underdrive (WLUD) is utilized in the HDC arrays as an area efficient approach to enhance read stability margin at the cost of cell performance [3], [9], [10]. Suppressed BL techniques, such as the DNR circuit, also improve read stability but are effective across a limited range of process technology targets, and implementation leads to more area overhead and higher power consumption than WLUD [5], [11]. The LVC SRAM, with a 1:2 PG to PD ratio, has adequate read stability margin and does not require WLUD, enabling both higher performance and increased write margin at low voltage.

The 14 nm HDC and LVC SRAM bitcells both feature an α ratio of 1, motivating a need for write assist circuitry to reduce or overcome PG to PU contention during write operations. The most prevalent approaches to SRAM write assist in recent literature are capacitive coupled negative bitline write assist [6], [9], [11], [12], cell supply voltage collapse write assist [1], [3], [10], [13]–[15] and boosted wordline write assist [16], [17]. Boosted WL write assist is most effective in LP technologies with high Vth targets and improves writability and performance at the same time, but is a poor match to GP/HP device targeted bitcells or low β ratio bitcells, such as HDC, as it can significantly impact read stability on unselected columns. Negative bitline write assist is an area-efficient, relatively low power approach to write margin enhancement, but improvements based upon bitcell passgate V_{GS} enhancement are fundamentally limited when combined with WLUD which is applied during write operations to guarantee read stability on unselected columns in a column-interleaved architecture. Column-based supply voltage collapse write assist (including TVC) is an effective write margin enhancement technique across a range of SRAM device targets. This assist scheme reduces pullup drive strength rather than enhancing passgate V_{GS} so it does not conflict with WLUD, and as a result creates a larger PG:PU drive ratio than can be achieved with the other two popular write assist techniques when combined with WLUD. A column-based TVC circuit is shown in Fig. 3, utilizing an NMOS device to discharge the memory cell supply (VCS) to weaken the PU transistor during writes. Half-selected cells along the written column face an instability risk if VCS is pulled below the minimum retention voltage. This can be mitigated by controlling the amplitude of the supply voltage collapse by enabling keeper devices connected to VCC that will clamp VCS to an intermediate level. The downside in this implementation is the static current flow between VCC and VSS when clamping VCS.

A new charge-share transient voltage collapse write assist circuit (CS-TVC) is introduced in this work. Improved random variation in 14 nm FinFET technology reduces the amplitude of VCS collapse required to achieve low V_{MIN} operation. The conventional TVC circuit topology shown in Fig. 3 requires the

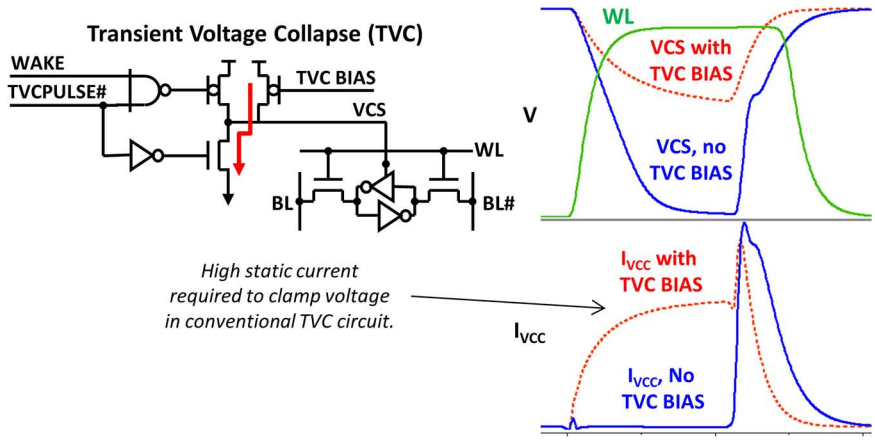

Fig. 3. Conventional transient voltage collapse circuit (TVC) using a simple biasing circuit to clamp the minimum voltage applied to the SRAM cell supply (VCS). This biasing circuit has a significant power overhead in operation when clamping the VCS level.

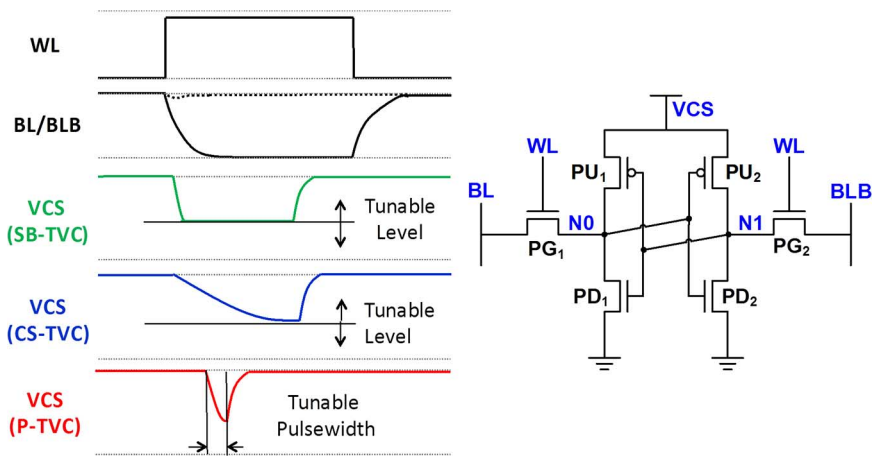

Fig. 4. 6T SRAM Bitcell schematic diagram and write operation waveforms with TVC write assist circuits configured for strong bias transient voltage collapse (SB-TVC), charge-share transient voltage collapse (CS-TVC) and pulse transient voltage collapse (P-TVC).

largest keeper size and hence the highest static current to clamp VCS near VCC, limiting the realizable write energy reduction. The CS-TVC circuit implementation delivers the most consistent margin enhancement across all device targets and addresses the issue of write power consumption by eliminating static bias current during write operations.

Fig. 4 depicts several VCS control options possible with the conventional TVC circuit and the charge-share TVC circuit to mitigate retention risks in bitcells along written columns. The strong-bias (SB-TVC) waveform is achieved using the conventional TVC circuit with a rapid discharge of VCS and a strongly clamped, tunable voltage level with an active bias current. The charge-share (CS-TVC) waveform is produced by the CS-TVC circuit, delivering a slower discharge across a pass transistor configured NMOS device to a tunable capacitor bank that controls the steady-state VCS level by the ratio of node capacitances. It is also possible to limit the amplitude of the VCS collapse by using a tunable pulse generator to control the collapse duration. The final waveform in Fig. 4 illustrates the pulsed TVC (P-TVC) operation, which relies upon tuning the pulse width of the VCS collapse to mitigate retention risks rather than clamping VCS with a keeper, and hence does not incur any static bias current power overhead.

IV. 548 kb Array Design With Charge-Share TVC Circuit

Fig. 5 details a capacitive charge-share transient voltage collapse circuit (CS-TVC) that delivers high performance at low voltage, and is compatible with WLUD across a wide range of technology targets while achieving active power consumption reduction relative to the conventional TVC circuit (Fig. 3) operated in SB-TVC mode. The CS-TVC switch circuits are located at the edges of a 256 row column, breaking the memory cell supply into two distinct 128b regions per column. Multiple switch circuits within a column are connected to a CS-TVC capacitor to reduce area, as only one switch within the column will be active during write. The CS-TVC capacitor contains a primary node and two secondary nodes enabled by CSCAP[1:0] to modulate the effective capacitance. NMOS devices driven by the DISCHARGE signal are used to reset the GCSCAP node to VSS before a write operation. The CS-TVC operation begins with a self-timed pulse (TVC PULSE) aligned to the rising edge of WL that simultaneously disconnects the selected VCS region from VCC, disables the NMOS devices in the CS-TVC capacitor, and connects VCS to the pre-discharged GCSCAP node. Charge is balanced through a PMOS switch between the VCS

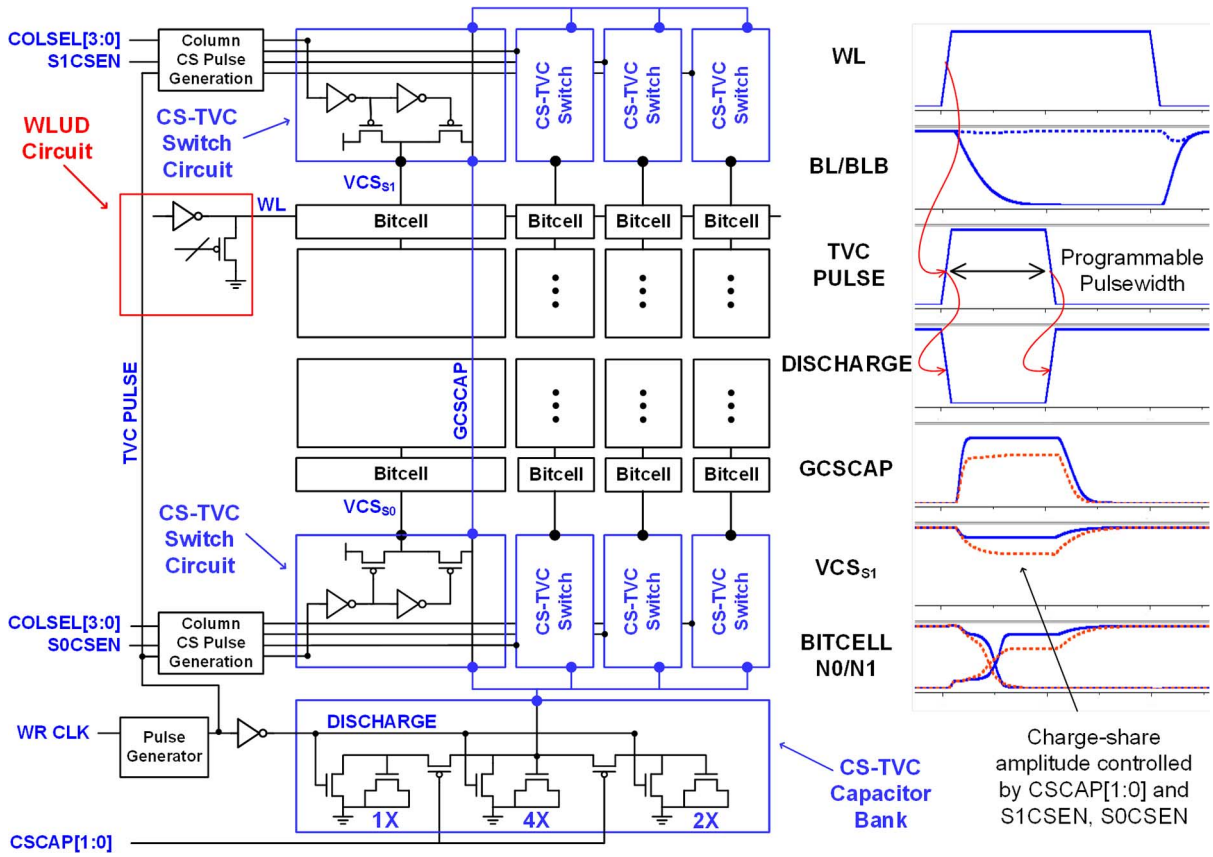

Fig. 5. SRAM array design with integrated capacitive charge-share transient voltage collapse circuit (CS-TVC) and write operation waveforms for selected bitcell columns.

region selected and GCSCAP, resulting in a temporary suppression of the VCS node to improve write margin. The falling edge of the TVC pulse completes the operation, restores the VCS voltage level to VCC, and triggers the rising edge of the DISCHARGE signal to reset the GCSCAP node to VSS in preparation for the next write operation.

Fig. 6 details the architecture of a 548 kb high-performance, pipelined LVC SRAM macro targeting L2/L3 cache applications that is implemented on a 14 nm technology testchip. The 548 kb block is composed of four 137 kb sub-arrays featuring 258 b/BL and 136 b/WL in a butterfly array configuration. In each logical I/O, 4 CS-TVC switch regions share one CS-TVC capacitor bank positioned in the center of the column. The 137 kb LVC sub-arrays with conventional TVC and CS-TVC achieve bit densities of 11.6 and 11.3 Mb/mm^2, respectively. The array efficiency is 71.6% and 69.8%, respectively for conventional TVC and CS-TVC. The TVC circuit is based upon reuse of a large PMOS wake device connected to local VCS nodes and utilized in a sleep circuit implementation that incurs 2% area overhead. In addition to the wake device area overhead, the area costs of the conventional TVC and the CS-TVC circuitry are 3.5% and 4.5%, respectively. A 1% array area reduction is possible by removing biasing transistors from the conventional TVC circuit and controlling the collapse magnitude via self-timed pulse (P-TVC operation). A separate HDC array featuring 2 sub-arrays with a denser 512 b/BL

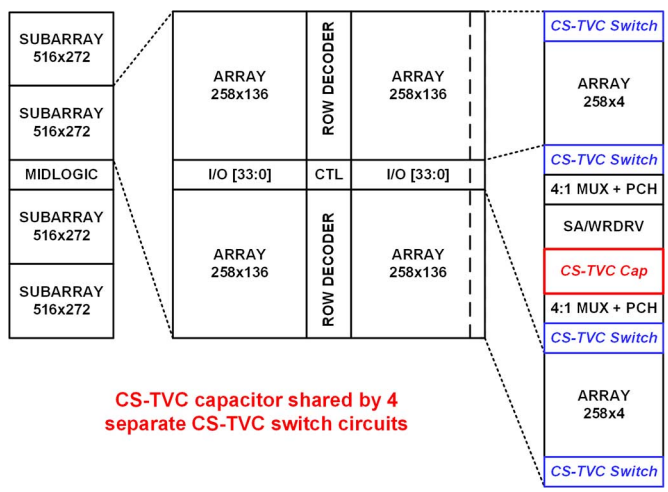

Fig. 6. 548 Kb SRAM sub-array architecture for the 14 nm LVC SRAM design with integrated charge-share transient voltage collapse write assist circuitry (CS-TVC).

column I/O design and conventional TVC write assist circuitry reach a bit density of 14.5 Mb/mm^2 and 76.2% array efficiency.

V. Results

Results are presented from multiple 84 Mb HDC and LVC SRAM arrays implemented on a 14 nm test chip shown in the die

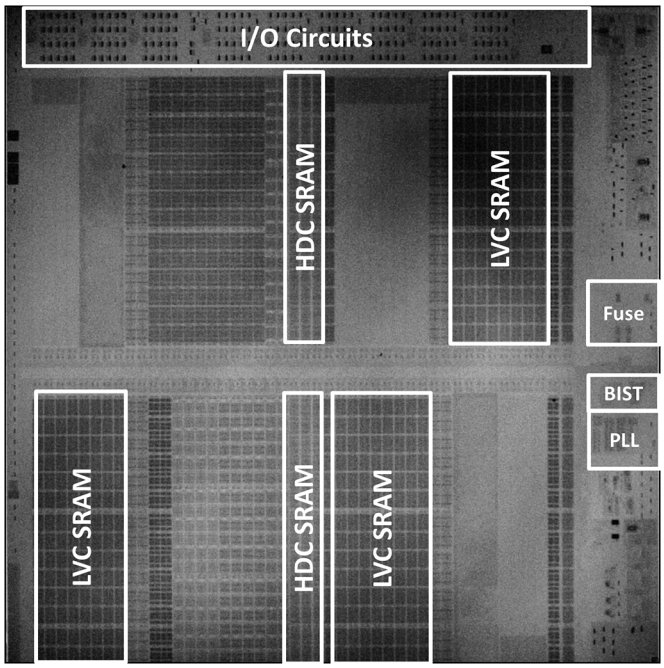

Fig. 7. 14 nm test chip die image with HDC and LVC SRAM arrays, embedded fuse, programmable BIST and high-speed PLLs.

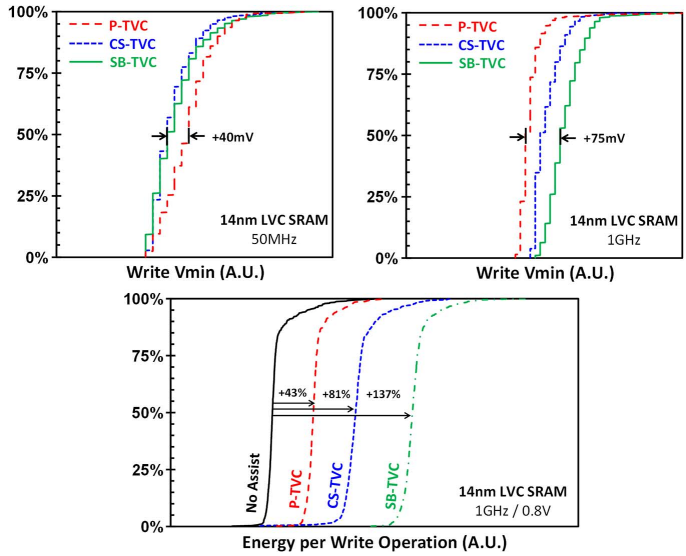

Fig. 8. Measured P-TVC, SB-TVC and CS-TVC 50 MHz and 1 GHz minimum operating voltage (V_{MIN}) and measured 1 GHz write energy comparison.

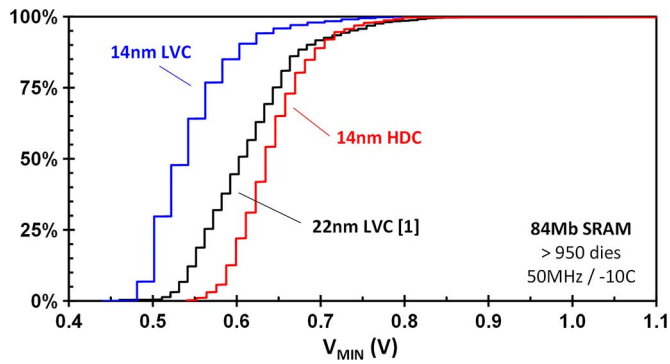

Fig. 9. Measured 84 Mb HDC and LVC SRAM array V_{MIN} distributions on 14 nm FinFET CMOS technology.

micrograph in Fig. 7. The testchip includes the SRAM test array designs described in this work in addition to embedded fuse, programmable BIST, multiple high-speed PLL designs and various I/O circuits. The SRAM testchip is designed for volume yield debug and statistical characterization of SRAM, advanced logic, and other process sensitive circuit and technology collaterals for 14 nm product usage.

Fig. 8 summarizes 50 MHz and 1 GHz LVC SRAM Write V_{MIN} measurements as well as the measured write energy for the different TVC methods. At frequencies significantly above 1 GHz, the voltage collapse magnitude is constrained by the time available to discharge VCS, and the resulting array behavior is similar for each technique. CS-TVC features a charge-share collapse to 48% of VCC and conventional TVC with a strong bias setting (SB-TVC) provides a clamped voltage level at 44% of VCC using the circuit from Fig. 3. The deeper collapse of CS-TVC and SB-TVC, relative to P-TVC, enable 40 mV lower V_{MIN} at 50 MHz. However, at 1 GHz, the deeper collapse and required recovery for these designs increases V_{MIN} by 30 mV for CS-TVC and 75 mV for SB-TVC relative to P-TVC. By eliminating static crowbar current, the CS-TVC circuit reduces active energy by 24% relative to SB-TVC for a comparable low frequency V_{MIN}. A narrow pulse TVC operation (P-TVC) can reduce write energy by 40% relative to SB-TVC while achieving superior high frequency V_{MIN}, but has its own set of challenges and tradeoffs.

The P-TVC approach to voltage collapse delivers good performance and V_{MIN} characteristics, the smallest array area and lowest power overhead compared to the SB-TVC and CS-TVC circuits. However, this technique requires stringent timing across the physical corners of the array design and is difficult to realize in a memory compiler because the collapse depth is a function of the pulse timing, VCS node loading (row count) and device strength. The P-TVC implementation is best suited for a custom memory design with a specific array configuration. SB-TVC offers direct control of VCS through a voltage divider circuit, removing the dependence upon VCS node loading, device strength and pulse timing, greatly simplifying memory compiler development. The CS-TVC implementation delivers comparable V_{MIN} benefits with a clear active power reduction for a small area overhead relative to SB-TVC. The voltage collapse amplitude is controlled by a capacitor that must be adjusted to match the VCS node loading (row count) for best effect, but avoids the device strength and pulse timing design complexities of P-TVC. CS-TVC is an interesting option for compiler-based memory that provides a reduction in active power overhead in exchange for the complexity of tuning the capacitor size to VCS node loading.

Fig. 9 shows the 14 nm LVC V_{MIN} is 0.6 V at the 90th percentile, an 80 mV reduction compared with a comparable LVC array on 22 nm [1]. The 14 nm HDC V_{MIN} is 0.7 V at the 90th percentile, within 15–20 mV of the 22 nm LVC SRAM V_{MIN}. The combination of improved transistor variability and co-optimization of the bitcell design and assist circuits enable a substantial reduction in V_{MIN} despite 0.54× cell

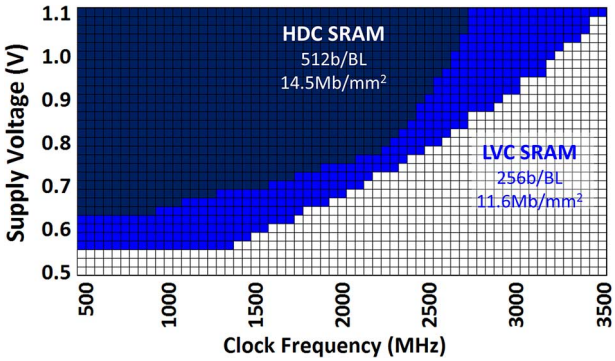

Fig. 10. Measured HDC and LVC SRAM array voltage-frequency shmoo demonstrating 0.6 V, 1.5 GHz LVC operation and 0.7 V, 1.55 GHz HDC operation on typical silicon.

scaling from 22 nm. In Fig. 10, voltage-frequency shmoos for an HDC SRAM array with 512 b/BL and an LVC SRAM array with 256 b/BL at 95°C are presented for typical silicon material. The LVC SRAM array demonstrates 1.5 GHz performance at 0.6 V and wide-range operation to 3.5 GHz at 1.1 V. The denser HDC array demonstrates 1.55 GHz at 0.70 V while achieving 14.5 Mb/mm^2 at the 137 kb sub-array building block.

VI. Conclusion

An 84 Mb high-performance, pipelined array design has been developed in a 14 nm CMOS logic technology with 2nd-generation FinFET and a new, charge-share transient voltage collapse write assist circuit. Aggressive scaling of fin pitch, poly pitch and metal interconnect pitches deliver 0.54× bitcell scaling relative to 22 nm technology, enabling the smallest reported production bitcell area of 0.050 μm^2. Two array designs were described, achieving 11.6 Mb/mm^2 bit density with the LVC SRAM bitcell (0.0588 μm^2) and 14.5 Mb/mm^2 with the HDC SRAM bitcell. A capacitive charge share TVC circuit delivers 24% reduction in write energy compared to strong bias TVC when optimized for low frequency V_{MIN} and pulsed TVC delivers a 40% reduction in write energy compared to strong bias TVC when optimized for 1 GHz operation. The high-performance, pipelined array designs demonstrate 0.6 V/1.5 GHz up to 1.1 V/3.5 GHz operation in a process technology optimized for 3–5 W tablet applications.

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Eric Karl (S'03–M'08) received the B.S.E., M.S.E., and Ph.D. degrees in electrical engineering from the University of Michigan, Ann Arbor, MI, USA, in 2002, 2004, and 2008, respectively.

He held positions at the Intel Circuit Research Lab, IBM T. J. Watson Research Center, and Sun Microsystems prior to 2008. In 2008, he joined Intel Logic Technology Development, where he is a principal engineer engaged in the development of memory circuit technology for low-power and high-performance SoC applications.

Dr. Karl has published more than 18 conference papers and technical journal articles and reviewed for numerous conferences and journals including IEEE Transactions on Very Large Scale Integration Systems and IEEE Journal of Solid-State Circuits.

Zheng Guo (S'03–M'09) received the B.S. degree in computer engineering from the University of Illinois at Urbana-Champaign, IL, USA, in 2003. He received the M.S. and Ph.D. degrees in electrical engineering from the University of California at Berkeley, CA, USA, in 2005 and 2009, respectively.

Since 2010, he has been with the Advanced Design Memory Circuit Technology Group at Intel Corporation, where he works on low-power high-performance high-density SRAM cache design.

Dr. Guo was a recipient of the National Defense Science and Engineering Graduate Fellowship in 2004, and the Best Paper Award at the ACM/IEEE International Symposium of Low-Power Electronics in 2005. In 2009, his research work was recognized as a winner in the 46th DAC/ISSCC Student Design Contest.

James Conary is a 36-year veteran of Intel specializing in memory circuit design.

Jeffrey Miller graduated from the University of Illinois at Urbana-Champaign, IL, USA, in 1986.

He is Principal Design Engineer employed with Intel for 24 years in IA server, desktop, and mobile product developments spanning a dozen process technology generations. He has specialized in cache architecture, specialty memories, low-voltage design, low-power circuits, yield recovery, fault tolerance, and power management.

Yong-Gee Ng was born in Singapore. He received the Bachelor degree and the Master degree in electrical engineering from Arizona State University, Phoenix, AZ, USA, in 1989 and 1991, respectively.

He joined Intel Corporation in September 1991 and is currently a Senior Design Engineer at the Portland Technology Development group. His interests are in low-power high-performance SRAM cache design.

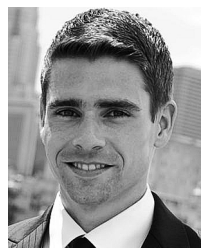
Satyanand Nalam (S'06–M'11) received the B.Tech degree in electrical engineering from the Indian Institute of Technology, Madras, India, in 2004. He received the M.S. and Ph.D. degrees in computer engineering from the University of Virginia, Charlottesville, VA, USA, in 2008 and 2011, respectively.

Since September 2011, he has been working as a Design Engineer in the Advanced Design Memory Circuit Technology group at Intel, Hillsboro, OR, USA, primarily on memory design and validation on test chips at advanced nanometer nodes, simulation methodology and simulation-to-silicon correlation.

Daeyeon Kim (S'08–M'13) received the B.S. degree in electronic and electrical engineering from Pohang University of Science and Technology (POSTECH), Pohang, Korea, in 2006, and the M.S. and Ph.D. degrees in electrical engineering from the University of Michigan, Ann Arbor, MI, USA, in 2008 and 2012, respectively.

He was a graduate research intern at ARM, Inc. in 2010 and 2011. After finishing his Ph.D. in 2012, he joined Advanced Design Group, Logic Technology Development, Intel Corporation, where he works on low-power high-performance SRAM design, statistical yield analysis, and process variation mitigation techniques.

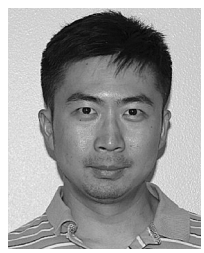
Dr. Kim received the Best Paper Award at the International Symposium on Low Power Electronics and Design in 2009.



John Keane (S'06–M'11) received the B.S. degree in computer engineering from the University of Notre Dame, Notre Dame, IN, USA, in 2003, and the Ph.D. degree in electrical engineering from the University of Minnesota, Minneapolis, MN, USA, in 2010.

He is currently with Advanced Design in the Portland Technology Development group of Intel Corporation, where he is working on memory test circuits. He has co-authored over 20 peer-reviewed publications and is a co-inventor on five US patents.

Dr. Keane won the University of Minnesota Graduate School Fellowship for the 2003-2005 academic years, along with IBM Ph.D. Fellowships in 2008 and 2009. In 2009, he was selected as an award winner in the DAC/ISSCC Student Design Contest, and won Best Paper in Session at the 2009 SRC TECHCON. He served on the technical program committee for the 2011 International Symposium on Low Power Electronics and Design.

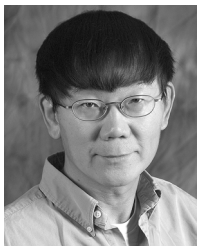


Xiaofei Wang (M'10) received the B.S. degree in physics from the University of Science and Technology of China (USTC), Hefei, China, in 2007, and the M.S. degree in physics and the Ph.D. degree in electrical and computer engineering from the University of Minnesota, Minneapolis, MN, USA, in 2014.

He has completed three internships with Broadcom Corporation in Edina, MN, USA, Texas Instruments in Dallas, TX, USA, and Cisco Systems in San Jose, CA, USA. During these internship periods, he performed research on on-chip aging and yield monitor design, and reliability and variation analysis. He is currently with Advanced Design in the Portland Technology Development group of Intel Corporation, Hillsboro, OR, USA. His research interests include circuit reliability and memory circuit design in advanced technologies. He has authored/coauthored more than 15 publications.

Uddalak Bhattacharya received the B.Tech. degree in electronics and electrical communication engineering from the Indian Institute of Technology, Kharagpur, India, in 1991, and the M.S. and Ph.D. degrees in electrical engineering from the University of California at Santa Barbara, CA, USA, in 1993 and 1996, respectively.

He is a principal engineer in the Logic Technology Development Organization at Intel Corporation. His interests are in high performance and low power memory design, test, measurement, and yield analysis.



Kevin Zhang (F'11) received the Bachelor degree from Tsinghua University, Beijing, China, in 1987 and the Ph.D. degree from Duke University, Durham, NC, USA, in 1994, both in electrical engineering.

He is a Vice President of Technology and Manufacturing Group and an Intel Fellow at Intel Corporation. He is responsible for advanced circuit technology development for the company's future products. He oversees the development of process design rules, circuit and device modeling, digital circuit libraries, key analog and mixed-signal circuits, high-speed I/O and embedded memories. He is also responsible for delivering the first technology vehicles for each new logic technology development at Intel. He has published more than 60 papers at international conferences and in technical journals. He is the editor of *Embedded Memory for Nano-Scale VLSIs* (Springer, 2009). He holds more than 50 U.S. patents in the field of integrated circuit technology. He is the 2016 ISSCC Program chair and also serves on IEEE VLSI Executive Committee.