

UNIT 6

FIELD EFFECT TRANSISTOR

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UNIT 6

FIELD EFFECT TRANSISTOR

6.1 INTRODUCTION

1. The Field effect transistor is abbreviated as FET , it is an another semiconductor device like a BJT which can be used as an amplifier or switch.
2. The Field effect transistor is a voltage operated device. Whereas Bipolar junction transistor is a current controlled device. Unlike BJT a FET requires virtually no input current.
3. This gives it an extremely high input resistance , which is its most important advantage over a bipolar transistor.
4. FET is also a three terminal device, labeled as source, drain and gate.
5. The source can be viewed as BJT's emitter, the drain as collector, and the gate as the counter part of the base.
6. The material that connects the source to drain is referred to as the channel.
7. FET operation depends only on the flow of majority carriers ,therefore they are called uni polar devices. BJT operation depends on both minority and majority carriers.
8. As FET has conduction through only majority carriers it is less noisy than BJT.
9. FETs are much easier to fabricate and are particularly suitable for ICs because they occupy less space than BJTs.
10. FET amplifiers have low gain bandwidth product due to the junction capacitive effects and produce more signal distortion except for small signal operation.
11. The performance of FET is relatively unaffected by ambient temperature changes. As it has a negative temperature coefficient at high current levels, it prevents the FET from thermal breakdown. The BJT has a positive temperature coefficient at high current levels which leads to thermal breakdown.

6.2 CLASSIFICATION OF FET:

There are two major categories of field effect transistors:

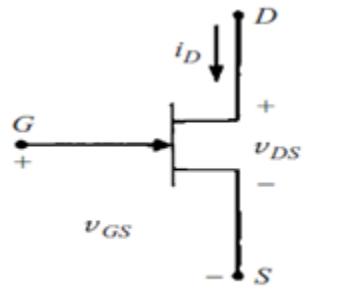
1. Junction Field Effect Transistors
2. MOSFETs

These are further sub divided in to P- channel and N-channel devices.

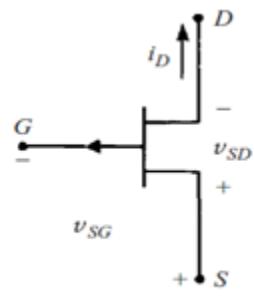
MOSFETs are further classified in to two types Depletion MOSFETs and Enhancement . MOSFETs

When the channel is of N-type the JFET is referred to as an N-channel JFET ,when the channel is of P-type the JFET is referred to as P-channel JFET.

The schematic symbols for the P-channel and N-channel JFETs are shown in the figure.



N-channel FET

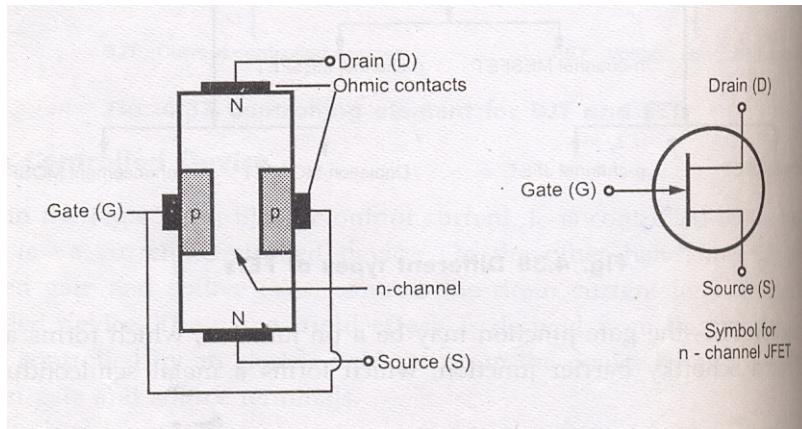


P-channel FET

6.3 CONSTRUCTION AND OPERATION OF N- CHANNEL FET

If the gate is an N-type material, the channel must be a P-type material.

CONSTRUCTION OF N-CHANNEL JFET



A piece of N- type material, referred to as channel has two smaller pieces of P-type material attached to its sides, forming PN junctions. The channel ends are designated as the drain and source . And the two pieces of P-type material are connected together and their terminal is called the gate. Since this channel is in the N-type bar, the FET is known as N-channel JFET.

OPERATION OF N-CHANNEL JFET:-

The overall operation of the JFET is based on varying the width of the channel to control the drain current.

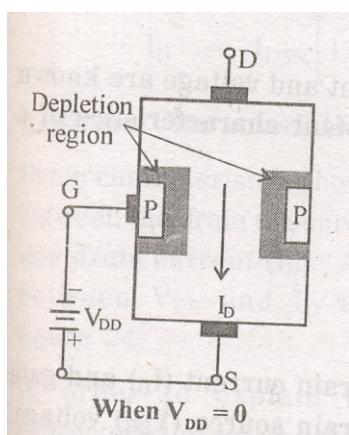
A piece of N type material referred to as the channel, has two smaller pieces of P type material attached to its sites, forming PN –Junctions. The channel's ends are designated the drain and the source. And the two pieces of P type material are connected together and their terminal is called the gate. With the gate terminal not connected and the potential applied positive at the drain negative at the source a drain current I_D flows. When the gate is biased negative with respect to the source the PN junctions are reverse biased and depletion regions are formed. The channel is more lightly doped than the P type gate blocks, so the depletion regions penetrate deeply into the channel. Since depletion region is a region depleted of charge carriers it behaves as an insulator. The result is that the channel is narrowed. Its resistance is increased and I_D is reduced. When the negative gate bias voltage is further increased, the depletion regions meet at the center and I_D is cut off completely.

There are two ways to control the channel width

1. By varying the value of V_{GS}
2. And by Varying the value of V_{DS} holding V_{GS} constant

1 By varying the value of V_{GS} :-

We can vary the width of the channel and in turn vary the amount of drain current. This can be done by varying the value of V_{GS} . This point is illustrated in the fig below. Here we are dealing with N channel FET. So channel is of N type and gate is of P type that constitutes a PN junction. This PN junction is always reverse biased in JFET operation .The reverse bias is applied by a battery voltage V_{GS} connected between the gate and the source terminal i.e positive terminal of the battery is connected to the source and negative terminal to gate.

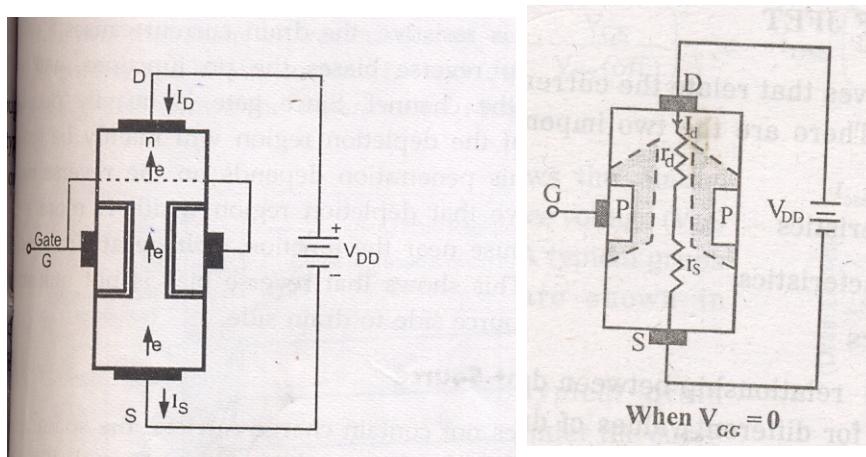


- 1) When a PN junction is reverse biased the electrons and holes diffuse across junction by leaving immobile ions on the N and P sides , the region containing these immobile ions is known as depletion regions.

- 2) If both P and N regions are heavily doped then the depletion region extends symmetrically on both sides.
- 3) But in N channel FET P region is heavily doped than N type thus depletion region extends more in N region than P region.
- 4) So when no V_{ds} is applied the depletion region is symmetrical and the conductivity becomes Zero. Since there are no mobile carriers in the junction.
- 5) As the reverse bias voltage is increases the thickness of the depletion region also increases. i.e. the effective channel width decreases .
- 6) By varying the value of V_{gs} we can vary the width of the channel.

2 Varying the value of V_{ds} holding V_{gs} constant :-

- 1) When no voltage is applied to the gate i.e. $V_{gs}=0$, V_{ds} is applied between source and drain through the channel constituting drain current I_d .
- 2) With $V_{gs}= 0$ for $I_d= 0$ the channel between the gate junctions is entirely open .In response to a small applied voltage V_{ds} , the entire bar acts as a simple semi conductor resistor and the current I_d increases linearly with V_{ds} .
- 3) The channel resistances are represented as r_d and r_s as shown in the fig.



n- channel JFET with gate open and V_{DD} applied between drain and source

- 4) This increasing drain current I_d produces a voltage drop across r_d which reverse biases the gate to source junction, ($r_d > r_s$) .Thus the depletion region is formed which is not symmetrical .
- 5) The depletion region i.e. developed penetrates deeper in to the channel near drain and less towards source because $V_{rd} \gg V_{rs}$. So reverse bias is higher near drain than at source.
 - 6) As a result growing depletion region reduces the effective width of the channel. Eventually a voltage V_{ds} is reached at which the channel is pinched off. This is the voltage where the current I_d begins to level off and approach a constant value.
 - 7) So, by varying the value of V_{ds} we can vary the width of the channel holding V_{gs} constant.

When both V_{gs} and V_{ds} is applied:-

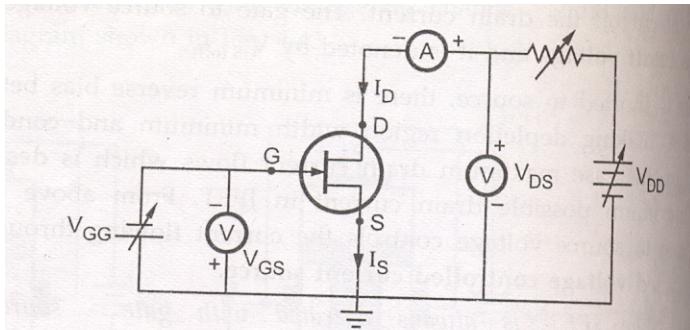
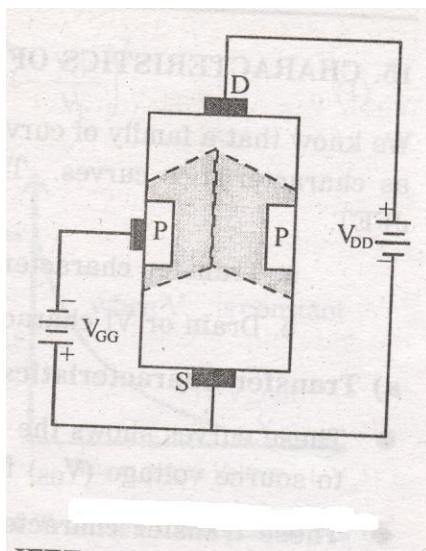


Fig. 4.45 Experimental setup to plot JFET characteristics

It is of course in principle not possible for the channel to close Completely and there by reduce the current I_D to Zero for, if such indeed, could be the case the gate voltage V_{GS} is applied in the direction to provide additional reverse bias

- 1) When voltage is applied between the drain and source with a battery V_{DD} , the electrons flow from source to drain through the narrow channel existing between the depletion regions. This constitutes the drain current I_D , its conventional direction is from drain to source.
- 2) The value of drain current is maximum when no external voltage is applied between gate and source and is designated by I_{DSS} .



- 3) When V_{GS} is increased beyond Zero the depletion regions are widened. This reduces the effective width of the channel and therefore controls the flow of drain current through the channel.

- 4) When V_{GS} is further increased a stage is reached at which two depletion regions touch each other that means the entire channel is closed with depletion region. This reduces the drain current to Zero.

6.4 CHARACTERISTICS OF N-CHANNEL JFET :-

The family of curves that shows the relation between current and voltage are known as characteristic curves.

There are two important characteristics of a JFET.

- 1) Drain or VI Characteristics
- 2) Transfer characteristics

1. Drain Characteristics:-

Drain characteristics shows the relation between the drain to source voltage V_{DS} and drain current I_D . In order to explain typical drain characteristics let us consider the curve with $V_{GS} = 0V$.

- 1) When V_{DS} is applied and it is increasing the drain current I_D also increases linearly up to knee point.
- 2) This shows that FET behaves like an ordinary resistor. This region is called as ohmic region.
- 3) I_D increases with increase in drain to source voltage. Here the drain current is increased slowly as compared to ohmic region.

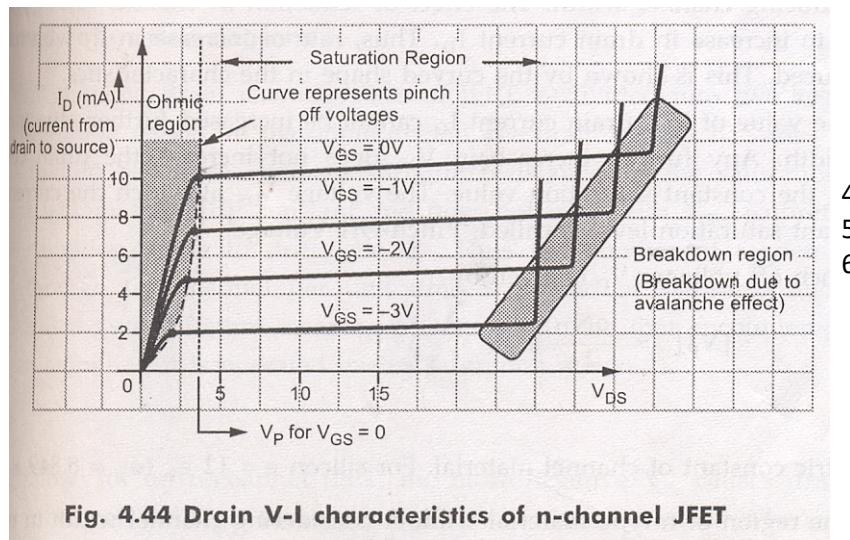


Fig. 4.44 Drain V-I characteristics of n-channel JFET

- 4) It is because of the fact that there is an increase in V_{DS} . This in turn increases the reverse bias voltage across the gate source junction .As a result of this depletion region grows in size thereby reducing the effective width of the channel.

- 5) All the drain to source voltage corresponding to point the channel width is reduced to a minimum value and is known as pinch off.
- 6) The drain to source voltage at which channel pinch off occurs is called pinch off voltage(V_p).

PINCH OFF Region:-

- 1) This is the region shown by the curve as saturation region.
- 2) It is also called as saturation region or constant current region. Because of the channel is occupied with depletion region , the depletion region is more towards the drain and less towards the source, so the channel is limited, with this only limited number of carriers are only allowed to cross this channel from source drain causing a current that is constant in this region. To use FET as an amplifier it is operated in this saturation region.
- 3) In this drain current remains constant at its maximum value I_{DSS} .
- 4) The drain current in the pinch off region depends upon the gate to source voltage and is given by the relation

$$I_d = I_{DSS} [1 - V_{GS}/V_p]^2$$

This is known as shokley's relation.

BREAKDOWN REGION:-

- 1) The region is shown by the curve .In this region, the drain current increases rapidly as the drain to source voltage is increased.
- 2) It is because of the gate to source junction due to avalanche effect.
- 3) The avalanche break down occurs at progressively lower value of V_{DS} because the reverse bias gate voltage adds to the drain voltage thereby increasing effective voltage across the gate junction
This causes
 1. The maximum saturation drain current is smaller
 2. The ohmic region portion decreased.
- 4) It is important to note that the maximum voltage V_{DS} which can be applied to FET is the lowest voltage which causes available break down.

2. TRANSFER CHARACTERISTICS:-

These curves shows the relationship between drain current I_D and gate to source voltage V_{GS} for different values of V_{DS} .

- 1) First adjust the drain to source voltage to some suitable value , then increase the gate to source voltage in small suitable value.

- 2) Plot the graph between gate to source voltage along the horizontal axis and current I_D on the vertical axis. We shall obtain a curve like this.

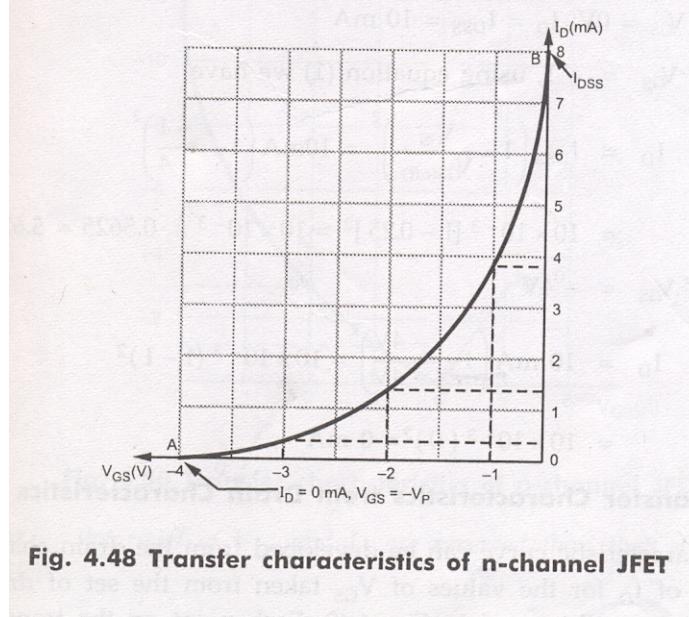


Fig. 4.48 Transfer characteristics of n-channel JFET

- 3) As we know that if V_{GS} is more negative curves drain current to reduce . where V_{GS} is made sufficiently negative, I_d is reduced to zero. This is caused by the widening of the depletion region to a point where it is completely closes the channel. The value of V_{GS} at the cutoff point is designed as V_{GSoff}
- 4) The upper end of the curve as shown by the drain current value is equal to I_{DSS} that is when $V_{GS} = 0$ the drain current is maximum.
- 5) While the lower end is indicated by a voltage equal to V_{GSoff}
- 6) If V_{GS} continuously increasing , the channel width is reduced , then $I_d = 0$
- 7) It may be noted that curve is part of the parabola; it may be expressed as

$$I_d = I_{DSS} [1 - V_{GS}/V_{GSoff}]^2$$

DIFFERENCE BETWEEN V_p AND V_{GSoff} –

V_p is the value of V_{GS} that causes the JFET to become constant current component, It is measured at $V_{GS} = 0V$ and has a constant drain current of $I_d = I_{DSS}$.Where V_{GSoff} is the value of V_{GS} that reduces I_d to approximately zero.

Why the gate to source junction of a JFET be always reverse biased ?

The gate to source junction of a JFET is never allowed to become forward biased because the gate material is not designed to handle any significant amount of current. If the junction is allowed to become forward biased, current is generated through the gate material. This current may destroy the component.

There is one more important characteristic of JFET reverse biasing i.e. J FET's have extremely high characteristic gate input impedance. This impedance is typically in the high mega ohm range. With the advantage of extremely high input impedance it draws no current from the source. The high input impedance of the JFET has led to its extensive use in integrated circuits. The low current requirements of the component makes it perfect for use in ICs. Where thousands of transistors must be etched on to a single piece of silicon. The low current draw helps the IC to remain relatively cool, thus allowing more components to be placed in a smaller physical area.

6.5 JFET PARAMETERS

The electrical behavior of JFET may be described in terms of certain parameters. Such parameters are obtained from the characteristic curves.

A C Drain resistance(r_d):

It is also called dynamic drain resistance and is the a.c.resistance between the drain and source terminal,when the JFET is operating in the pinch off or saturation region. It is given by the ratio of small change in drain to source voltage ΔV_{ds} to the corresponding change in drain current ΔI_d for a constant gate to source voltage V_{gs} .

Mathematically it is expressed as $r_d = \Delta V_{ds} / \Delta I_d$ where V_{gs} is held constant.

TRANSCONDUCTANCE (g_m):

It is also called forward transconductance . It is given by the ratio of small change in drain current (ΔI_d) to the corresponding change in gate to source voltage (ΔV_{ds})

Mathematically the transconductance can be written as

$$g_m = \Delta I_d / \Delta V_{ds}$$

AMPLIFICATION FACTOR (μ)

It is given by the ratio of small change in drain to source voltage (ΔV_{ds}) to the corresponding change in gate to source voltage (ΔV_{gs})for a constant drain current (I_d).

Thus $\mu = \Delta V_{ds} / \Delta V_{gs}$ when I_d held constant

The amplification factor μ may be expressed as a product of transconductance (g_m)and ac drain resistance (r_d)

$$\mu = \Delta V_{ds} / \Delta V_{gs} = g_m r_d$$

6.6 THE FET SMALL SIGNAL MODEL:-

The linear small signal equivalent circuit for the FET can be obtained in a manner similar to that used to derive the corresponding model for a transistor.

We can express the drain current i_d as a function f of the gate voltage and drain voltage V_{ds} .

$$I_d = f(V_{gs}, V_{ds}) \quad \text{---(1)}$$

The transconductance g_m and drain resistance r_d :-

If both gate voltage and drain voltage are varied, the change in the drain current is approximated by using taylor's series considering only the first two terms in the expansion

$$\Delta i_d = \frac{\partial i_d}{\partial V_{gs}} |_{V_{ds}=\text{constant}} \Delta V_{gs} + \frac{\partial i_d}{\partial V_{ds}} |_{V_{gs}=\text{constant}} \Delta V_{ds}$$

we can write $\Delta i_d = i_d$

$$\Delta V_{gs} = V_{gs}$$

$$\Delta V_{ds} = V_{ds}$$

$$I_d = g_m V_{gs} + \frac{1}{r_d} V_{ds} \rightarrow (1)$$

$$\text{Where } g_m = \frac{\partial i_d}{\partial V_{gs}} |_{V_{ds}} \underset{\Delta V_{gs}}{\approx} \frac{\Delta i_d}{\Delta V_{gs}} |_{V_{ds}}$$

$$g_m = \frac{i_d}{V_{gs}} |_{V_{ds}}$$

Is the mutual conductance or transconductance .It is also called as gfs or yfs common source forward conductance .

The second parameter r_d is the drain resistance or output resistance is defined as

$$r_d = \frac{\partial V_{ds}}{\partial i_d} |_{V_{gs}} \underset{\Delta i_d}{\approx} \frac{\Delta V_{ds}}{\Delta i_d} |_{V_{gs}} = \frac{V_{ds}}{i_d} |_{V_{gs}}$$

$$r_d = \frac{V_{ds}}{I_d} \Big|_{V_{gs}}$$

The reciprocal of the r_d is the drain conductance g_d . It is also designated by Yos and Gos and called the common source output conductance. So the small signal equivalent circuit for FET can be drawn in two different ways.

1.small signal current –source model

2.small signal voltage-source model.

A small signal current –source model for FET in common source configuration can be drawn satisfying Eq→(1) as shown in the figure(a)

This low frequency model for FET has a Norton's output circuit with a dependent current generator whose magnitude is proportional to the gate-to –source voltage. The proportionality factor is the transconductance ' g_m '. The output resistance is ' r_d '. The input resistance between the gate and source is infinite, since it is assumed that the reverse biased gate draws no current. For the same reason the resistance between gate and drain is assumed to be infinite.

The small signal voltage-source model is shown in the figure(b).

This can be derived by finding the Thevenin's equivalent for the output part of fig(a) .

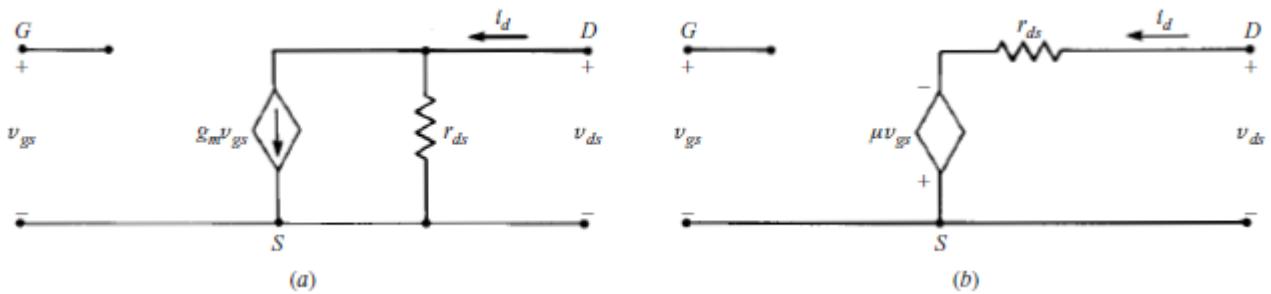
These small signal models for FET can be used for analyzing the three basic FET amplifier configurations:

1.common source (CS) 2.common drain (CD) or source follower

3. common gate(CG).

(a)Small Signal Current source model for FET

(b)Small Signal voltage source model for FET

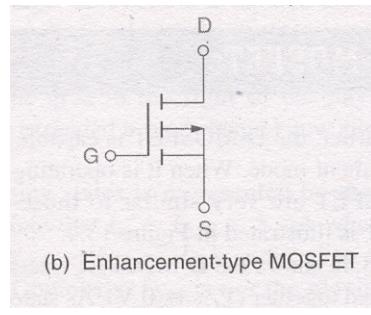
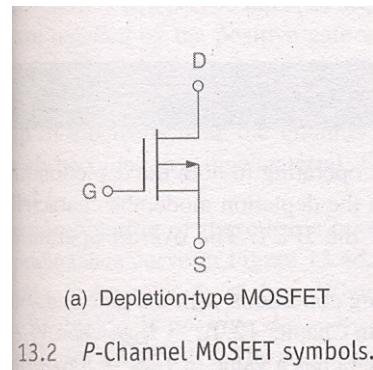


Here the input circuit is kept open because of having high input impedance and the output circuit satisfies the equation for I_D

6.7 MOSFET:-

We now turn our attention to the insulated gate FET or metal oxide semi conductor FET which is having the greater commercial importance than the junction FET.

Most MOSFETS however are triodes, with the substrate internally connected to the source. The circuit symbols used by several manufacturers are indicated in the Fig below.



(a) Depletion type MOSFET

(b) Enhancement type MOSFET

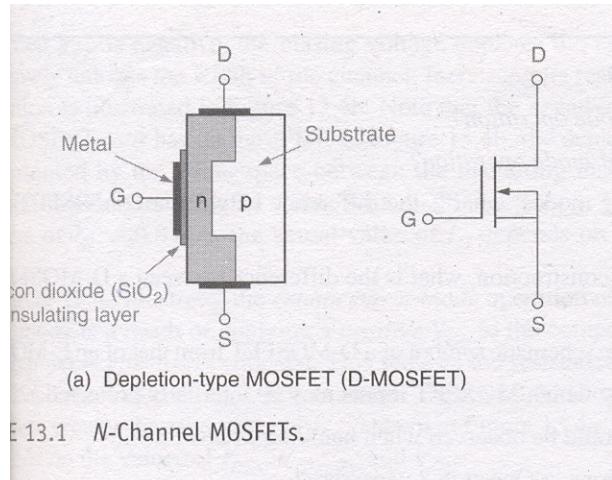
Both of them are P- channel

Here are two basic types of MOSFETS

- (1) Depletion type (2) Enhancement type MOSFET.

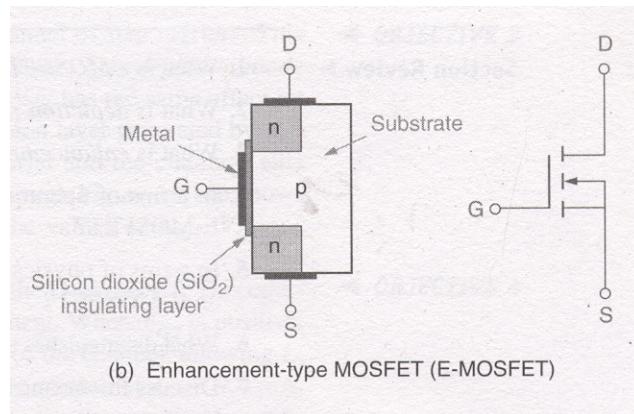
D-MOSFETS can be operated in both the depletion mode and the enhancement mode. E MOSFETS are restricted to operate in enhancement mode. The primary difference between them is their physical construction.

The construction difference between the two is shown in the fig given below.



E 13.1 N-Channel MOSFETs.

As we can see the D MOSFET have physical channel between the source and drain terminals(Shaded area)



The E MOSFET on the other hand has no such channel physically. It depends on the gate voltage to form a channel between the source and the drain terminals.

Both MOSFETs have an insulating layer between the gate and the rest of the component. This insulating layer is made up of SiO_2 a glass like insulating material. The gate material is made up of metal conductor .Thus going from gate to substrate, we can have metal oxide semi conductor which is where the term MOSFET comes from.

Since the gate is insulated from the rest of the component, the MOSFET is sometimes referred to as an insulated gate FET or IGFET.

The foundation of the MOSFET is called the substrate. This material is represented in the schematic symbol by the center line that is connected to the source.

In the symbol for the MOSFET, the arrow is placed on the substrate. As with JFET an arrow pointing in represents an N-channel device, while an arrow pointing out represents p-channel device.

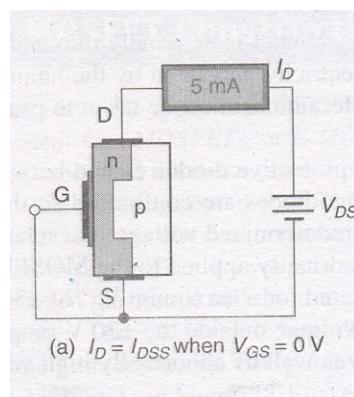
CONSTRUCTION OF AN N-CHANNEL MOSFET:-

The N- channel MOSFET consists of a lightly doped p type substance into which two heavily doped n+ regions are diffused as shown in the Fig. These n+ sections , which will act as source and drain. A thin layer of insulation silicon dioxide (SiO_2) is grown over the surface of the structure, and holes are cut into oxide layer, allowing contact with the source and drain. Then the gate metal area is overlaid on the oxide, covering the entire channel region.Metal contacts are made to drain and source and the contact to the metal over the channel area is the gate terminal.The metal area of the gate, in conjunction with the insulating dielectric oxide layer and the semiconductor channel, forms a parallel plate capacitor. The insulating layer of sio₂

Is the reason why this device is called the insulated gate field effect transistor. This layer results in an extremely high input resistance (10^{10} to 10^{15} ohms) for MOSFET.

6.7.1 DEPLETION MOSFET

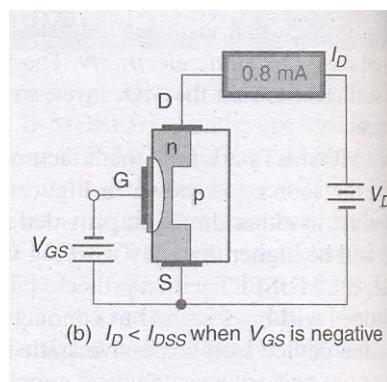
The basic structure of D –MOSFET is shown in the fig. An N-channel is diffused between source and drain with the device an appreciable drain current I_{DSS} flows for zero gate to source voltage, $V_{GS}=0$.



Depletion mode operation:-

- 1) The above fig shows the D-MOSFET operating conditions with gate and source terminals shorted together($V_{GS}=0V$)
- 2) At this stage $I_D=I_{DSS}$ where $V_{GS}=0V$, with this voltage V_{DS} , an appreciable drain current I_{DSS} flows.
- 3) If the gate to source voltage is made negative i.e. V_{GS} is negative .Positive charges are induced in the channel through the SiO_2 of the gate capacitor.

- 4) Since the current in a FET is due to majority carriers(electrons for an N-type material) , the induced positive charges make the channel less conductive and the drain current drops as Vgs is made more negative.
- 5) The re distribution of charge in the channel causes an effective depletion of majority carriers , which accounts for the designation depletion MOSFET.
- 6) That means biasing voltage Vgs depletes the channel of free carriers This effectively reduces the width of the channel , increasing its resistance.
- 7) Note that negative Vgs has the same effect on the MOSFET as it has on the JFET.



- 8) As shown in the fig above, the depletion layer generated by Vgs (represented by the white space between the insulating material and the channel) cuts into the channel, reducing its width. As a result , $I_D < I_{DSS}$.The actual value of ID depends on the value of I_{DSS} , $V_{GS}(\text{off})$ and V_{GS} .

Enhancement mode operation of the D-MOSFET:-

- 1) This operating mode is a result of applying a positive gate to source voltage Vgs to the device.
- 2) When Vgs is positive the channel is effectively widened. This reduces the resistance of the channel allowing ID to exceed the value of I_{DSS}
- 3) When Vgs is given positive the majority carriers in the p-type are holes. The holes in the p type substrate are repelled by the +ve gate voltage.
- 4) At the same time, the conduction band electrons (minority carriers) in the p type material are attracted towards the channel by the +gate voltage.
- 5) With the build up of electrons near the channel , the area to the right of the physical channel effectively becomes an N type material.
- 6) The extended n type channel now allows more current, $I_D > I_{DSS}$

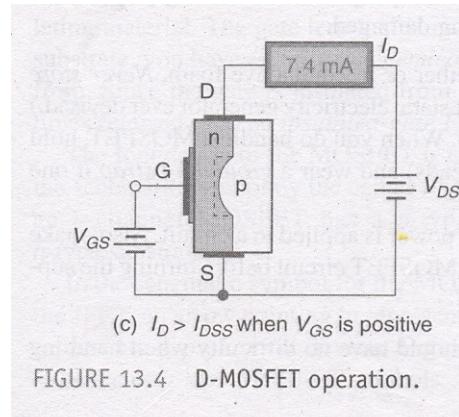
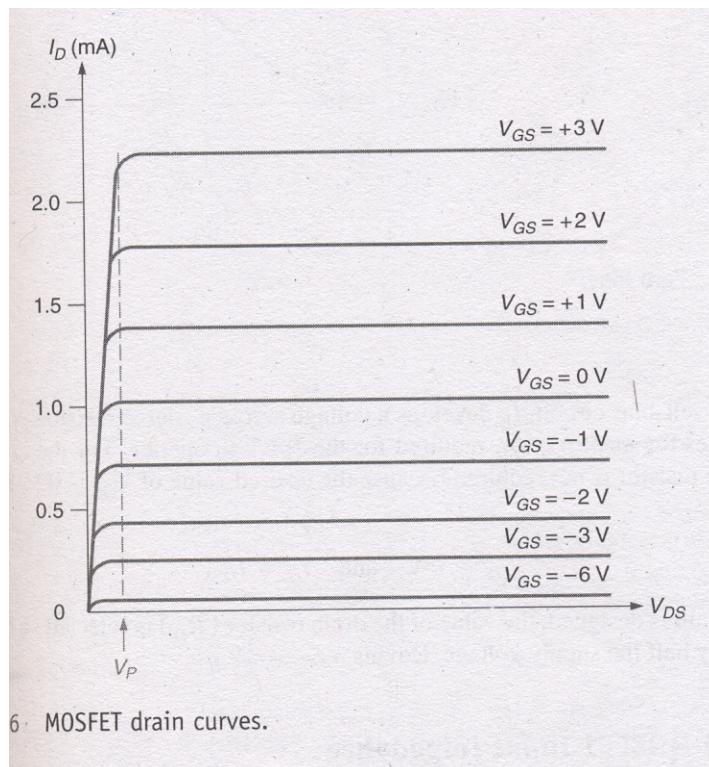


FIGURE 13.4 D-MOSFET operation.

Characteristics of Depletion MOSFET:-

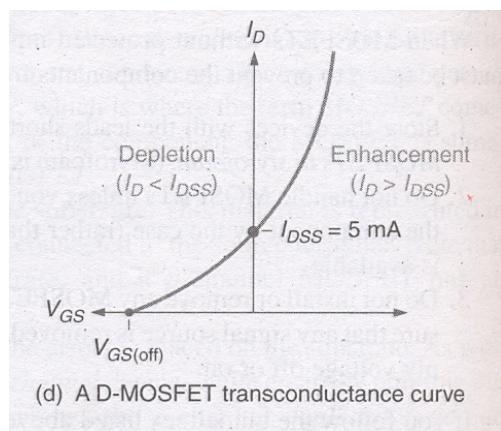
The fig. shows the drain characteristics for the N channel depletion type MOSFET

- 1) The curves are plotted for both V_{GS} positive and V_{GS} negative voltages
- 2) When $V_{GS}=0$ and negative the MOSFET operates in depletion mode when V_{GS} is positive ,the MOSFET operates in the enhancement mode.
- 3) The difference between JFET and D MOSFET is that JFET does not operate for positive values of V_{GS} .
- 4) When $V_{DS}=0$, there is no conduction takes place between source to drain, if $V_{GS}<0$ and $V_{DS}>0$ then I_D increases linearly.
- 5) But as $V_{GS},0$ induces positive charges holes in the channel, and controls the channel width. Thus the conduction between source to drain is maintained as constant, i.e. I_D is constant.
- 6) If $V_{GS}>0$ the gate induces more electrons in channel side, it is added with the free electrons generated by source. again the potential applied to gate determines the channel width and maintains constant current flow through it as shown in Fig



TRANSFER CHARACTERISTICS:-

The combination of 3 operating states i.e. $V_{GS}=0V$, $V_{GS}<0V$, $V_{GS}>0V$ is represented by the D MOSFET transconductance curve shown in Fig.

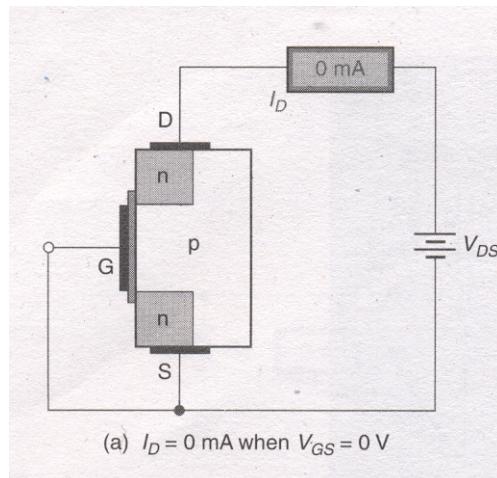


- 1) Here in this curve it may be noted that the region AB of the characteristics similar to that of JFET.
- 2) This curve extends for the positive values of Vgs

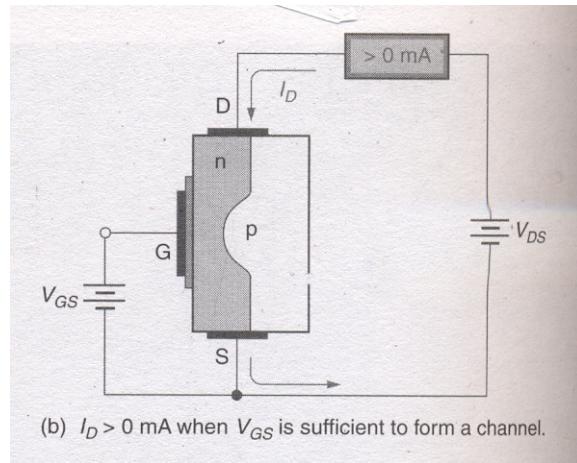
- 3) Note that $I_d = I_{dss}$ for $V_{gs} = 0V$ when V_{gs} is negative, $I_d < I_{dss}$ when $V_{gs} = V_{gs(\text{off})}$, I_d is reduced to approximately 0mA . Where V_{gs} is positive $I_d > I_{dss}$. So obviously I_{dss} is not the maximum possible value of I_d for a MOSFET.
- 4) The curves are similar to JFET so that the D MOSFET have the same transconductance equation.

6.7.2 E-MOSFETS

The E MOSFET is capable of operating only in the enhancement mode. The gate potential must be positive w.r.t to source.



- 1) when the value of $V_{gs}=0V$, there is no channel connecting the source and drain materials.
- 2) As a result, there can be no significant amount of drain current.
- 3) When $V_{gs}=0$, the V_{dd} supply tries to force free electrons from source to drain but the presence of p-region does not permit the electrons to pass through it. Thus there is no drain current at $V_{gs}=0$,
- 4) If V_{gs} is positive, it induces a negative charge in the p type substrate just adjacent to the SiO_2 layer.
- 5) As the holes are repelled by the positive gate voltage, the minority carrier electrons attracted toward this voltage. This forms an effective N type bridge between source and drain providing a path for drain current.
- 6) This +ve gate voltage forms a channel between the source and drain.
- 7) This produces a thin layer of N type channel in the P type substrate. This layer of free electrons is called N type inversion layer.

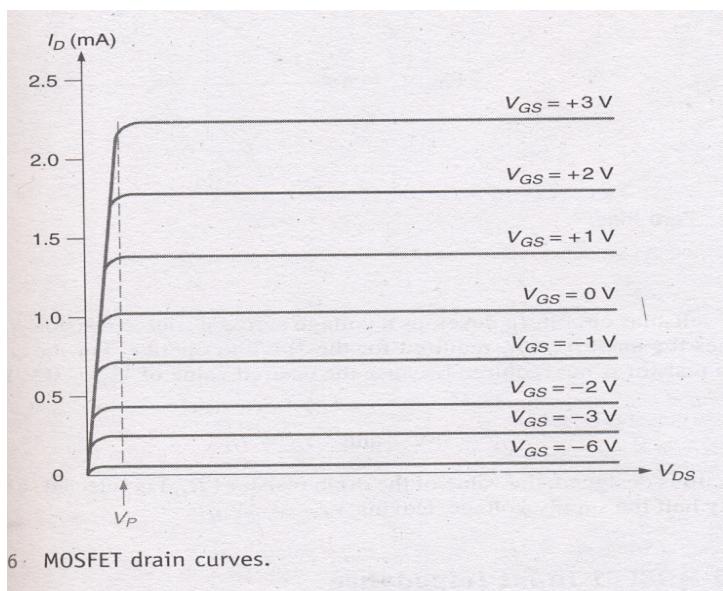


- 8) The minimum V_{GS} which produces this inversion layer is called threshold voltage and is designated by $V_{GS(th)}$. This is the point at which the device turns on is called the threshold voltage $V_{GS(th)}$
- 9) When the voltage V_{GS} is $< V_{GS(th)}$ no current flows from drain to source.
- 10) However when the voltage $V_{GS} > V_{GS(th)}$ the inversion layer connects the drain to source and we get significant values of current.

CHARACTERISTICS OF E MOSFET:-

1. DRAIN CHARACTERISTICS

The volt ampere drain characteristics of an N-channel enhancement mode MOSFET are given in the



2. TRANSFER CHARACTERISTICS:-

- 1) The current I_{DSS} at $V_{GS} \leq 0$ is very small being of the order of a few nano amps.
- 2) As V_{GS} is made +ve , the current I_D increases slowly at first, and then much more rapidly with an increase in V_{GS} .
- 3) The standard transconductance formula will not work for the E MOSFET.
- 4) To determine the value of I_D at a given value of V_{GS} we must use the following relation

$$I_D = K[V_{GS} - V_{GS(Th)}]^2$$

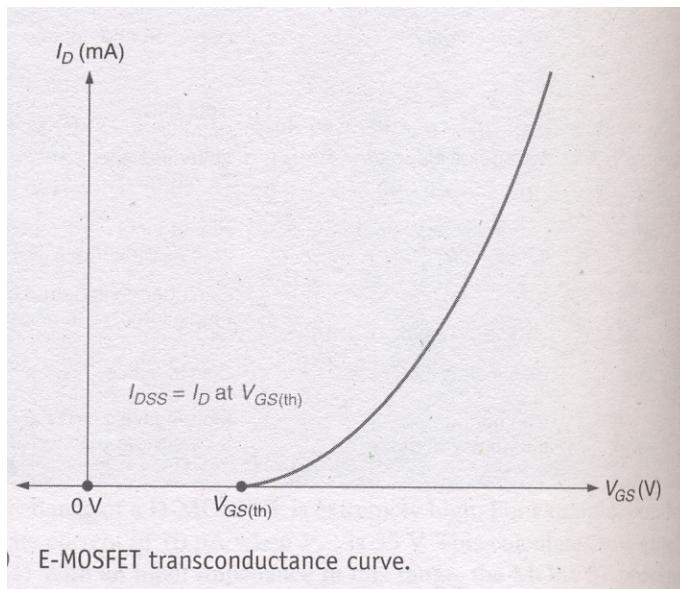
Where K is constant for the MOSFET . found as

$$K = \frac{I_D(\text{on})}{[V_{GS(\text{on})} - V_{GS(\text{Th})}]^2}$$

From the data specification sheets, the 2N7000 has the following ratings.

$I_D(\text{on})= 75\text{mA}(\text{minimum})$.

And $V_{GS(\text{th})}=0.8\text{(minimum)}$



6.8 APPLICATION OF MOSFET

One of the primary contributions to electronics made by MOSFETs can be found in the area of digital (computer electronics). The signals in digital circuits are made up of rapidly switching dc levels. This signal is called as a rectangular wave ,made up of two dc levels (or logic levels). These logic levels are 0V and +5V.

A group of circuits with similar circuitry and operating characteristics is referred to as a logic family. All the circuits in a given logic family respond to the same logic levels, have similar speed and power-handling capabilities , and can be directly connected together. One such logic family is complementary MOS (or CMOS) logic. This logic family is made up entirely of MOSFETs.

6.9 BIASING FET:-

For the proper functioning of a linear FET amplifier, it is necessary to maintain the operating point Q stable in the central portion of the pinch off region The Q point should be independent of device parameter variations and ambient temperature variations

This can be achieved by suitably selecting the gate to source voltage V_{GS} and drain current I_D which is referred to as biasing

JFET biasing circuits are very similar to BJT biasing circuitsThe main difference between JFET circuits and BJT circuits is the operation of the active components themselves

There are mainly two types of Biasing circuits

- 1) Self bias
- 2) Voltage divider bias.

6.9.1 SELF BIAS

Self bias is a JFET biasing circuit that uses a source resistor to help reverse bias the JFET gate. A self bias circuit is shown in the fig. Self bias is the most common type of JFET bias. This JFET must be operated such that gate source junction is always reverse biased. This condition requires a negative V_{GS} for an N channel JFET and a positive V_{GS} for P channel JFET. This can be achieved using the self bias arrangement as shown in Fig. The gate resistor R_G doesn't affect the bias because it has essentially no voltage drop across it, and : the gate remains at 0V . R_S is necessary only to isolate an ac signal from ground in amplifier applications. The voltage drop across resistor R_S makes gate source junction reverse biased.

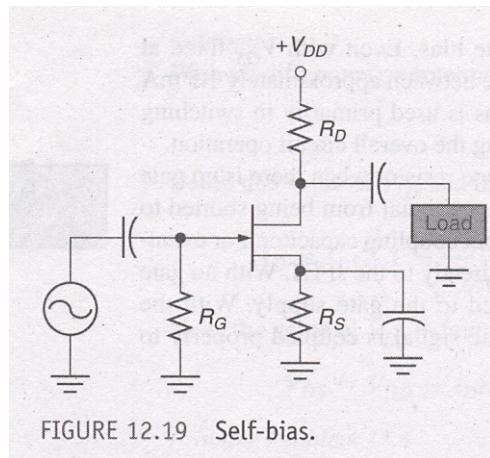


FIGURE 12.19 Self-bias.

For the dc analysis coupling capacitors are open circuits.

For the N channel FET in Fig (a)

Is produces a voltage drop across R_s and makes the source positive w.r.t ground. In any JFET circuit all the source current passes through the device to the drain circuit .This is due to the fact that there is no significant gate current.

We can define source current as $I_s = I_d$

($V_G = 0$ because there is no gate current flowing in R_G So V_G across R_G is zero)

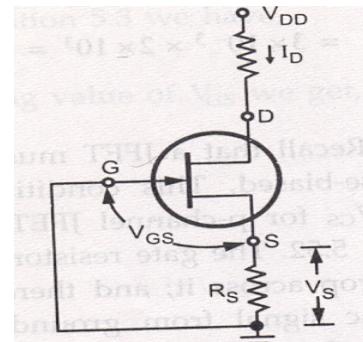
$$V_G = 0 \text{ then } V_s = I_s R_s = I_d R_s$$

$$V_{GS} = V_G - V_s = 0 - I_d R_s = -I_d R_s$$

DC analysis of self Bias:-

In the following DC analysis, the N channel J FET shown in the fig. is used for illustration.

For DC analysis we can replace coupling capacitors by open circuits and we can also replace the resistor R_G by a short circuit equivalent.: $I_G = 0$.The relation between I_d and V_{GS} is given by



$$I_d = I_{dss} \left[1 - \frac{V_{gs}}{V_p} \right]^2$$

V_{GS} for N channel JFET is $= -I_d R_s$

Substituting this value in the above equation

$$I_d = I_{dss} \left[1 - \frac{(-I_d R_s)}{V_p} \right]^2$$

$$I_d = I_{dss} \left[1 + \frac{(I_d R_s)}{V_p} \right]^2$$

For the N-channel FET in the above figure

I_S produces a voltage drop across R_S and makes the source positive w.r.t ground in any JFET circuit all the source current passes through the device to drain circuit this is due to the fact that there is no significant gate current. Therefore we can define source current as $I_S = I_D$ and $V_G = 0$ then

$$V_S = I_S R_S = I_D R_S$$

$$V_{GS} = V_G - V_S = 0 - I_D R_S = -I_D R_S$$

Drawing the self bias line:-

Typical transfer characteristics for a self biased JFET are shown in the fig.

The maximum drain current is 6mA and the gate source cut off voltage is -3V. This means the gate voltage has to be between 0 and -3V.

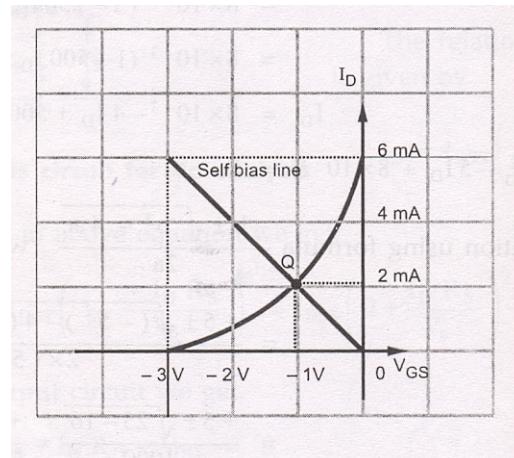


Fig. 5.55 Transfer characteristics

Now using the equation $V_{GS} = -I_D R_S$ and assuming R_S of any suitable value we can draw the self bias line.

Let us assume $R_S = 500\Omega$

With this R_S , we can plot two points corresponding to $I_D = 0$ and $I_D = I_{DSS}$

for $I_D = 0$

$$V_{GS} = -I_D R_S$$

$$V_{GS} = 0 \times (500\Omega) = 0V$$

So the first point is $(0, 0)$

$$(I_D, V_{GS})$$

For $I_D = I_{DSS} = 6\text{mA}$

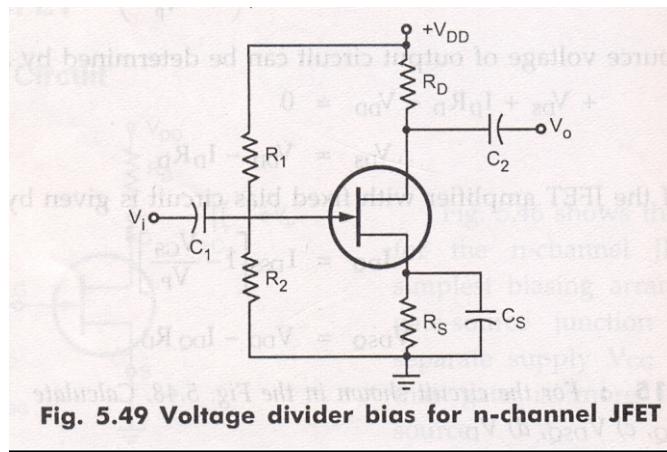
$$V_{GS} = (-6\text{mA}) (500 \Omega) = -3\text{V}$$

So the 2nd Point will be (6mA, -3V)

By plotting these two points, we can draw the straight line through the points. This line will intersect the transconductance curve and it is known as self bias line. The intersection point gives the operating point of the self bias JFET for the circuit.

At Q point, the I_D is slightly $>$ than 2mA and V_{GS} is slightly $>$ -1V. The Q point for the self bias JFET depends on the value of R_S . If R_S is large, Q point far down on the transconductance curve, I_D is small, when R_S is small Q point is far up on the curve, I_D is large.

6.9.2 VOLTAGE DIVIDER BIAS:-



The fig. shows N channel JFET with voltage divider bias. The voltage at the source of JFET must be more positive than the voltage at the gate in order to keep the gate to source junction reverse biased. The source voltage is

$$V_S = I_D R_S$$

The gate voltage is set by resistors R_1 and R_2 as expressed by the following equation using the voltage divider formula.

$$V_G = \left(\frac{R_2}{R_1 + R_2} \right) V_{DD}$$

For dc analysis

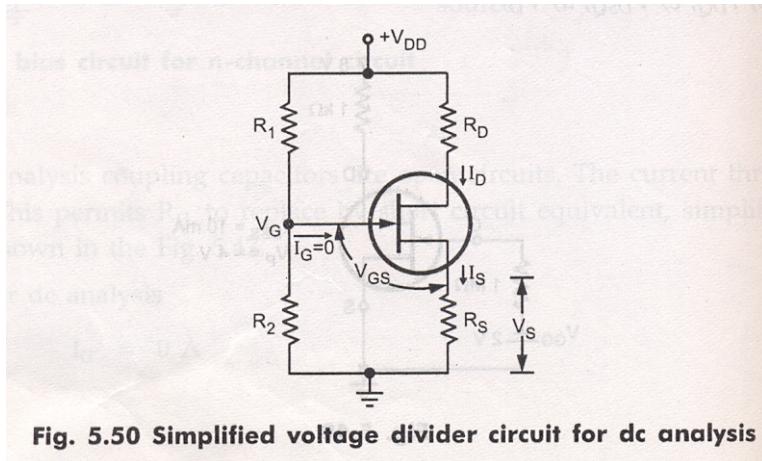


Fig. 5.50 Simplified voltage divider circuit for dc analysis

Applying KVL to the input circuit

$$V_G - V_{GS} - V_S = 0$$

$$\therefore V_{GS} = V_G - V_S = V_G - I_S R_S$$

$$V_{GS} = V_G - I_D R_S \quad \therefore I_S = I_D$$

Applying KVL to the input circuit we get

$$V_{DS} + I_D R_D + V_S - V_{DD} = 0$$

$$\therefore V_{DS} = V_{DD} - I_D R_D - I_S R_S$$

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

The Q point of a JFET amplifier, using the voltage divider bias is

$$I_{DQ} = I_{DSS} [1 - V_{GS}/V_P]^{1/2}$$

$$V_{DSQ} = V_{DD} - I_D (R_D + R_S)$$

COMPARISON OF MOSFET WITH JFET

- In enhancement and depletion types of MOSFET, the transverse electric field induced across an insulating layer deposited on the semiconductor material controls the conductivity of the channel.
- In the JFET the transverse electric field across the reverse biased PN junction controls the conductivity of the channel.
- The gate leakage current in a MOSFET is of the order of $10^{-12} A$. Hence the input resistance of a MOSFET is very high in the order of 10^{10} to $10^{15} \Omega$. The gate

leakage current of a JFET is of the order of 10^{-9} A., and its input resistance is of the order of 10^8 Ω .

- d. The output characteristics of the JFET are flatter than those of the MOSFET, and hence the drain resistance of a JFET (0.1 to $1M\Omega$) is much higher than that of a MOSFET (1 to $50k\Omega$).
- e. JFETs are operated only in the depletion mode. The depletion type MOSFET may be operated in both depletion and enhancement mode.
- f. Comparing to JFET, MOSFETs are easier to fabricate.
- g. Special digital CMOS circuits are available which involve near zero power dissipation and very low voltage and current requirements. This makes them suitable for portable systems.