

27 TRIBHUVAN UNIVERSITY
 INSTITUTE OF ENGINEERING
Examination Control Division
 2074 Ashwin

Exam.	Back		
Level	BE	Full Marks	80
Programme	BEL, BEX, BCT	Pass Marks	32
Year / Part	II / I	Time	3 hrs.

Subject: - Digital Logic (EX502)

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ Attempt All questions.
- ✓ The figures in the margin indicate Full Marks.
- ✓ Assume suitable data if necessary.

1. a) Explain digital wave form based on TTL compatible logic. (Both for input and output) [3]
- b) What is the importance of De-morgan's laws? Show how a two-input NOR gate can be constructed from a two-input NAND gate. [4]
2. Convert decimal 39 into binary and hexadecimal. Use 2'S complement method to perform the following addition (-28+17) [2+3]
3. Simplify the function using K-map $F = \sum(0,1,4,8,10,11,12)$ and $D = \sum(2,3,6,9,15)$. Also realize the simplified logic circuit. [6]
4. a) What is an encoder? Draw the logic circuit of an encoder that converts Octal number into binary. [1+4]
- b) What is a multiplexer tree? Design the 16 to 1 multiplexer using 4 to 1 multiplexer. [1+4]
5. What is the Setup time and hold time of a flip-flop? With the help of excitation table and K-map, convert R-S flip flop into D and J-K flip flops. [2+6]
6. Describe the operation of 4 bit serial in Serial Out shift register, with timing diagram. Consider the input 1011 to be entered into the register. [6]
7. List the advantages and disadvantages of a synchronous counter over asynchronous counter. Design a 3 bit synchronous counter which follow gray code sequence. [2+6]
8. Design a sequential machine that produces output $Y = 1$ when it detects the serial input $X = 100$. [10]
9. Define fan-in and fan-out with reference to TTL. With a circuit diagram explain the operation of 2-bit TTL NAND gate. [2+6]
10. Draw the block diagram with decoders to show hour, minute and second. [6]
11. Write short notes on: (any two) [2×3]
 - i) Static and dynamic hazzard
 - ii) ROM
 - iii) DE-MUX tree

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1. a) Define TTL IC Signal levels for Input and Output logic with example. [3]
- b) Convert 37.432 decimal number to binary. [3]
2. a) State and prove De-Morgan's theorems with necessary diagrams. Prove that negative logic OR Gate is equivalent to positive logic AND Gate. [4+2]
- b) What is Gray code? Explain with example. [2]
3. a) Minize the expression and implement the reduced expression by using NAND gates.

$$F = \overline{ABCD} + \overline{ABC}\overline{D} + \overline{ABC}\overline{D} + \overline{AB}\overline{C}\overline{D} + \overline{AB}\overline{C}\overline{D} + \overline{A}\overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}\overline{C}\overline{D} + \overline{ABC}\overline{D}$$
 [4+2]
 b) What do you mean by Max term? Explain with example. [3]
4. Design the 32:1 Multiplexer using 4:1 multiplexers tree concept and implement the function $F = \sum(0,1,3,8,9,13)$ using suitable Multiplexer. [4+2]
5. a) Explain the operation of 3 bit magnitude comparator with truth table and draw the circuit. [5]

S O L U T I O N S

 b) Draw the circuit to add following bits 1011 and 1100. [3]
6. a) Write down the drawback of SR Flip-Flop. Explain the operation of edge triggered JK Flip-Flop with timing diagram and truth table. [2+4]
 b) Explain the operation of 4 bit serial in serial out (SISO) register with timing diagram. [5]
7. Explain the operation of 3 bit Asynchronous up/down counter with timing diagram. [6]
8. Design a synchronous sequential machine such that it gives output $Z = 1$ if input contains the message 110 and it retains in its own state for other condition giving output zero. Use J-K Flip-Flop. [10]
9. What do you mean by static and dynamic hazards? Give example of static hazards and explain how do you eliminate such hazards? [4+2]
10. With the help of block diagram explain the operation of frequency counter. [4]
11. Draw the schematic diagram of TTL NOR gate and explain about totem pole. [6]

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2073 Shrawan

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1. a) Perform the following code conversions. [3+2]
 - i) $(1110)_{\text{gray}} = (?)_{\text{BCD}}$
 - ii) $(1430)_{10} = (?)_{\text{Excess-3}}$
- b) Construct two input XOR gate using minimum number of 2-input NAND gates only. [5]
2. Implement a full adder circuit using 4:1 Multiplexers. [5]
3. Draw the circuit diagram and explain the working principle of 4-bit parallel in serial out (PISO) shift register. [7]
4. Simplify $\sum 1,2,3,8,10,13 + d(0,4,5,6,7,9,12)$ by using K-Map and write its standard SOP expression. [6]
5. Design 1:32 demultiplexer tree using 1:8 DEMUXS and 1:2 DEMUXS only. [6]
6. Draw the schematic diagram of TTL Inverter. Explain the working principle of circuit. [3+4]
7. Derive characteristic equation of a JK flip flop. How do you make it a toggle flip flop? Draw the input and output wave form of JK flip flop. [3+2+2]
8. Differentiate between combinational and sequential circuits. Explain BCD-to-Decimal decoder circuit with suitable diagram. [2+6]
9. Design a synchronous MOD-5 counter along with block diagram and timing diagrams. Also write the applications of counters and shift registers. [6]
10. Sketch block diagram of digital frequency counter and describe its operation. [8]
11. A sequential machine has to detect serial input sequence of 101, the machine output will be high. The machine contains two JK flip flops, A and B. Assume: single input, x and single output Y. [12]

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 2072 Kartik

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Subject: - Digital Logic (EX502)

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1. What are the major difference between Binary code and BCD code? [2]
2. Explain the operation of gated D flip-flop with timing diagram and truth table. [4]
3. What are the major differences between asynchronous and synchronous counter? Design a Mod-6 synchronous up binary counter using S-R flip flops and draw its timing diagram. [2+6]
4. What are the applications of shift registers? Explain any one of the application with working circuit diagram. [6]
5. Construct MOD-12 asynchronous up-counter with negative edge triggering system in clock. [5]
6. Draw the circuit diagram for 2-input CMOS NAND gate. What is Totem pole output? Explain. [3+3]
7. Convert the decimal number 168 into hexadecimal and gray code by first converting it into binary and perform the following addition using 2's complement 11+15 [2+2+3]
8. Write the minterms of ACD+AB and simplify $\sum 1,2,3,8,9,10,11,13,14+d(0,4,12)$ by using K-Map and write its standard product of sum (POS) expression. [4+6]
9. Differentiate between synchronous and asynchronous inputs of a flip flop with suitable diagram. Derive characteristic equation of a JK flip flop. How do you make it a toggle flip flop? Explain with diagram. [3+5]
10. Draw the schematic diagram of TTL NOR gate. Explain the operation of CMOS to TTL interface. [2+2]
11. Explain with block diagram to build the digital watch from a power supply system. Show second, minute and hour display using decoder. [8]
12. Suppose you have given the following word specification describing the sequential operation of some machine. This machine has a control input X and the clock and two state variables A and B and one output. If the input, is high the machine will change state otherwise this machine is supposed to hold its present state. It also gives output when the sequence is 101. Derive state table and state diagram. Use only T flip-flops and necessary logic gates. [4+8]

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1. Perform the following as indicated in the brackets: [2×4]
 - a. $(10.0101)_2 = (?)_{16}$
 - b. $(101001001)_{\text{binary}} = (?)_{\text{Gray}}$
 - c. $(93)_{10} = (?)_{\text{Excess-3}}$
 - d. $(10.001)_2 - (11.101)_2$ using 2's complement method.
2. a) Describe commutative and associative laws of Boolean algebra with examples and simplify $A+A'B=A+B$. [2+2]
- b) Implement Exclusive OR gate by using NAND gates only. [4]
3. Simplify $\sum 1,2,3,8,9,10,11,13,14 + d(0,4,7,12)$ by using K-Map and write its standard product of sum (POS) expression. [4+3]
4. How do you design 32:1 Mux by using multiplexer tree? Implement logic function $Y = \sum m(0,1,3,8,9,13,15)$ by using suitable multiplexer. [4+3]
5. Realize a full-subtractor using suitable demultiplexer and standard gates. [6]
6. Design a simplest logic circuit for 'b' segment of the BCD to 7 segment decoder. [7]
7. Design and draw the circuit diagram of a 3 bit gray code synchronous counter. [7]
8. Draw ripple decade counter and sketch its timing diagram. [5+2]
9. Draw 2-input TTL NAND gate and explain its working principle. [5]
10. How does second section of a digital clock work? Explain its working principle using block diagram. [6]
11. Design a sequential machine that has a single input 'x' and single output 'z'. The machine is required to give high output when it detects the serial sequence of 011 message. Use JK flip-flops only. [12]

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1. Define digital operations. What is Excess-3 Code explain with example. [2+4]
2. Define universal Gate with example. Realise Ex-OR Gate using NAND gate only. [1+4]
3. Simplify the following using K-map and realize the simplified result with NAND gates only. [3+3]

$$\sum_m(2,5,7,8,10,13) + d(0,6,14,15)$$
4. Implement following combinational circuit with multiplexer. [4]

$$F(A,B,C,D) = \sum_m(1,3,4,11,12,13,14,15)$$
5. Using seven segment display decoder realize the logic circuit for segment 'b', 'c' and 'd'. [5]
6. With neat and clean diagram explain the operation of adder-subtractor circuit. [4]
7. Explain the operation of positive edge triggered RS flip-flop with circuit diagram, truth table and excitation table. [2+8]
8. With clear circuit and timing diagram, explain the operation of parallel in Serial out shift register. [8]
9. Design Synchronous MOD-12 counter using T-flip-flop. [8]
10. Design a sequential machine that can go through 2-bit gray code combination of states. The machine changes its state when serial input is one and remains in same state when input is zero. The machine produces output one when it passes through all states and finally goes back to initial state. (use JK flip flop) [10]
11. What are the characteristics of TTL circuit for logic high and low level? Explain the operation of TTL NAND gate. [2+6]
12. Describe the operation of Digital Clock with block diagram. [6]

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1. What is weighted code and non-weighted code? What will be the BCD, Excess-3 and Gray code for the decimal number 15? [2+3]

2. Perform the following addition using 2's complement -5+12 [4]

3. Implement Exclusive OR gate by using NAND gates only. [3]

4. Simplify the following function using K-map and implement the result using only NOR gates. [4+3]

$$F(A, B, C, D) = \sum m(0, 2, 3, 5, 6, 8, 9) + d(10, 11, 12, 13, 14, 15)$$

5. Design a 32:1 MUX using only 8:1 MUX. Use block diagrams. [5]

6. Design a combinational logic circuit with 3 input variables that will produce logic high output when more than one input variables are logic low. [4]

7. Show with design that a full-adder can be implemented using two half-adders. Subtract $(16)_{10}$ from $(14)_{10}$ using 2's complement method. [6+2]

8. Derive characteristic equation of a JK flip flop. How do you make it a toggle flip flop? Draw the input and output wave form of JK flip flop. [3+2+2]

9. What is a Shift Register? What are its various types? List out some applications of Shift Register. [5]

10. Differentiate between synchronous and asynchronous counters. Describe the operation of asynchronous 3-bit binary down counter. [2+6]

11. Design a sequential circuit with two D flip flops and two inputs, P and Q. If P = 0, the circuit remains in the same state regardless of the value of Q. When P = 1 and Q = 1, the circuit goes through the state transitions from 00 to 01 to 10 back to 00, and repeats. When P = 1 and Q = 0, the circuit goes through the state transitions from 00 to 10 to 01 back to 00, and repeats. The circuit is to be designed by treating the unused state (s) as don't care condition(s). [12]

12. Discuss the following TTL parameters: [2×4]

- Propagation delay
- Worst-Case input voltages
- Fan-out
- Power dissipation

13. Explain clearly the operation of frequency counter with necessary block diagram and timing diagrams. [4]

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1. a) What are the different logical operations? Explain. [3]
- b) Explain different coding system used to represent data. [3]
2. Explain the operation of NAND, NOR, XOR and NOT gates with Boolean expression and truth table. [4]
3. Simplify the Boolean function in both SOP and POS and the implement using basic gates only: $F(A, B, C, D) = \sum (0, 1, 3, 4, 8, 9, 15)$ [8]
4. a) Design 8- to -3 line priority encoder. [4]
- b) Design a combinational logic that produces square of 3 bit number using ROM. [6]
5. a) Implement the full adder using two half adders. [3]
- b) Explain the working principle of binary multiplication. [5]
6. Explain the operation of RS flip flop showing its logic diagram, characteristic table and then derive its characteristics equation and excitation table. [8]
7. With clear circuit diagram, explain the operation of parallel in-Serial out shift register. [4]
8. What do you mean by Presettable Counter? Design a modulo - 12 counter using T-Flip flop. [1+7]
9. Design a sequential machine that takes the one bit of serial data x as input and gives the one bit of data as output z . The machine gives an output $z = 1$ when the input sequence of x contains the message 0100. [12]
10. What are the parameters of TTL? Explain the operation of 74C00 CMOS. [2+6]
11. Explain the operation of digital clock with neat and clean diagram. [4]

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1. Define digital signal and explain Gray code with example. [1+5]
2. Prove that positive X-OR is equivalent to negative X-NOR. [5]
3. a) Convert the following term into standard min term. $A+B'C$. [3]
 - b) Use K-map method to implement the following function and also draw the reduced circuit using NOR gate. [5]
$$F(A, B, C, D) = \Sigma_m(0, 2, 4, 6, 8, 10, 15) \text{ and}$$

$$d = \Sigma_m(3, 11, 14)$$
4. a) Realize the logic circuit of the following using 8:1 MUX. [4]

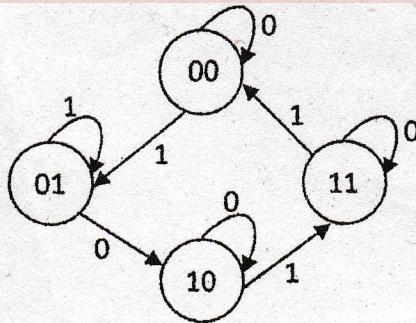
$$F(W, X, Y, Z) = \Sigma_m(1, 2, 5, 7, 8, 10, 12, 13, 15)$$
 - b) When FF_H is ANDed with CO_H what will be the resulting number? Subtract (26) 10 from (16) 10 using 2's complement binary method. [2+2]
5. a) Differentiate between level and Edge triggering? [3]
 - b) Explain the operation of two bit magnitude comparator with truth table and circuit diagram. [5]
6. a) Describe different types of registers with diagram. [8]
 - b) Illustrate how 1011 data can be stored and retrieve in parallel in serial out shift register with neat timing diagram and truth table. [8]
7. Differentiate synchronous and asynchronous sequential circuits. Explain the operation of mod-12 synchronous counter with timing diagram. [2+6]
8. a) Define state diagram and state table with example. [2]
 - b) Design a sequential machine that has one serial input and one output z. The machine is required to give an output $z = 1$ when the input X contains the message 110. [8]
9. Draw the schematic diagram of TTL two input NOR Gate. [6]
10. Explain briefly the block diagram of an instrument to measure frequency. [5]

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1. Describe in your own words the characteristics of an analog signal and a digital signal. [3]
2. Define positive and negative logic with examples. [3]
3. Construct the basic gates using only universal gates. [4]
4. Simplify the following using K-map. $\sum_m(3,4,6,8,10,15) + d(0,2,7,14)$. [3]
5. What are the static hazards in combinational circuit? Also explain how these hazards can be covered. [5]
6. Explain the operation of BCD to decimal decoder with truth table and circuit diagram. Implement 1:4 demux using VHDL. [6+4]
7. Design a full adder circuit using HDL. [4]
8. What is a Fast Adder? Explain with examples. [4]
9. Draw the circuit diagram and explain the operation of edge triggered RS flip-flop. Convert RS flip-flop to JK flip-flop. **SOLUTIONS**— [5+3]
10. Explain the working of serial in -serial out register clearly. [4]
11. Differentiate between the synchronous and Asynchronous counter. Draw and explain the operation of Asynchronous Decade counter with clear timing diagram. [2+6]
12. Design Synchronous sequential circuit for the given state diagram using JK flip flop. [12]



13. Draw the schematic diagram of TTL NAND gate and explain about the CMOS characteristics. [2+6]
14. With the help of block diagram explain the operation of frequency counter. [4]

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1. Define digital IC signal levels. What is Gray Code? Explain with example. [3+3]
2. Construct the given Boolean function: $F = (A+B)(C+D)E$ using NOR gates only. [4]
3. Simplify $F(A,B,C,D) = \pi(0,2,5,8,10) + d(7,15)$. Write its standard SOP and implement the simplified circuit using NOR gates only. [4+4]
4. a) What is priority Encoder? Design octal to binary priority encoder. [2+4]
 - b) Design a 2 bit magnitude comparator. [4]
5. Design a combinational logic that performs multiplication between two 4 bit numbers using binary parallel adder and other gates. [8]
6. Draw the circuit diagram and explain the operation of positive edge triggered JK flip-flop. What are the drawbacks of JK flip-flop? [7+1]
7. Explain the Serial in Serial out (SISO) shift register with timing diagram. [4]
8. Design the synchronous decade counter and also show the timing diagram. [8]
9. Design a sequential machine that detects three consecutive zeros from an input data stream X by making output, Y = 1. [12]
10. Draw the schematic circuit for CMOS NAND gates. What do you mean by totem-pole output? [4+4]
11. Describe the operation of a frequency counter. [4]

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Subject: - Digital Logic

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1. Design a 3-bit even parity generator and parity checker. What do you mean by BCD code? [4+2]
2. Why NAND and NOR gates are called universal gates? Illustrate with examples. [4]
3. Simplify $F = \sum(0, 2, 4, 6, 8, 9, 13, 14)$ by using K-Map. Implement the same given circuit using decoder (Use only the block diagram of decoder). Define Pairs, Quads and Octets in K-Map. [3+3+2]
4. What do you mean by HDL? Design a full adder circuit using HDL. [4]
5. Describe the occurrence of hazards in a combinational circuit. What are the possible solutions to avoid hazards? [4+4]
6. Describe the operation of addition process by Fast adder and the importance of fast adder. [8]
7. Explain the use of BJT as a switch. Draw the schematic diagram of TTL NAND gate. [2+4]
8. What is contact switch bouncing? Describe how it can be eliminated. [6]
9. Describe briefly the operation of a 4 bit Serial-in Serial-out (SISO) shift register with a clear circuit diagram. [4]
10. What do you mean by decoding gates? Design a MOD = 5 synchronous counter showing diagram and output waveforms. [2+6]
11. Define the problems Oscillation and Critical race in asynchronous sequential circuit. [6]
12. A synchronous state machine has one bit serial input x . The output z of machine is to be set high when the input contains the message 011. Draw the state diagram for this machine and design the circuit (Use T flip flop). [12]

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2068 Chaitra

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1. List out the name of universal gates and why they are called universal gate? Relise Ex- OR Gate using only NAND gates. [2+2]
2. Explain Excess 3 code with suitable examples. [6]
3. Simplify the function using K-map $F = \Sigma(0,1,4,8,10,11,12)$ and $D = \Sigma(2,3,6,9,15)$. Also convert the result into standard minterm. [3+5]
4. Design a 32 to 1 multiplexer using 16 to 1 and 2 to 1 multiplexers. [5]
5. Design a 3-bit even parity generator and 4-bit even parity checker circuit. [5]
6. Draw the block diagram of n-bit full adder and explain its operation. [8]
7. Write down the drawbacks of SR flip flop. Explain the operation of data flip flop with timing diagram and truth table. [1+7]
8. With clear circuit and timing diagram, explain the operation of Serial in - Serial out shift register. [4]
9. Define ripple counter. Explain the operation of mode-10 ripple counter with timing diagram. [1+7]
10. Design a sequential machine that has one serial input and one output z. The machine is required to give an output $z = 1$ when the input x contains the message 1010. [12]
11. Describe the voltage profile of TTL. Explain the operation of TTL to CMOS interface. [2+6]
12. What is frequency counter? Explain with block diagram. [4]
