Notes Date ___/___/___

Operational Amplifier Circuits

Bias Circuits Suitable for IC Design

→ Bias circuit used to bias discrete BJTs are not suitable. They require large numbers of resistors as well as large coupling and bypass capacitors.

→ With present IC technology, impossible to fabricate large capacitors, uneconomical to manufacture large resistances.

→ Basically, biasing in IC design is based on use of constant current sources.

→ On an IC chip with number of amplifier stages, a constant dc current is generated at one location and is then reproduced at various other locations of biasing various amplifier stages.

Diode- Connected Transistor

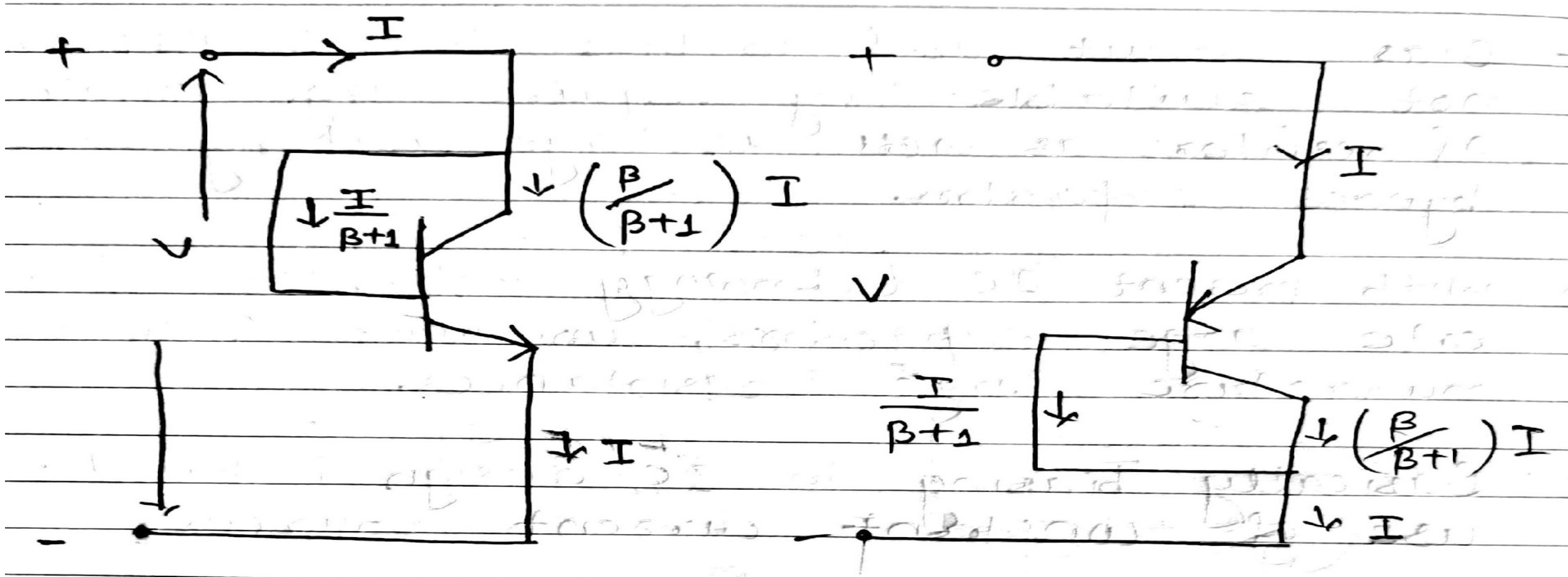


Fig. Diode connected BJTs.

→ Shorting the base and collector of BJT together result in a two terminal device having I-V characteristics identical to $I_E - V_{BE}$ characteristics of BJT.

→ Since, BJT is operated in active-mode, the current I divides between base and collector according to the value of 'β' of the BJT.

Simple Current mirror :

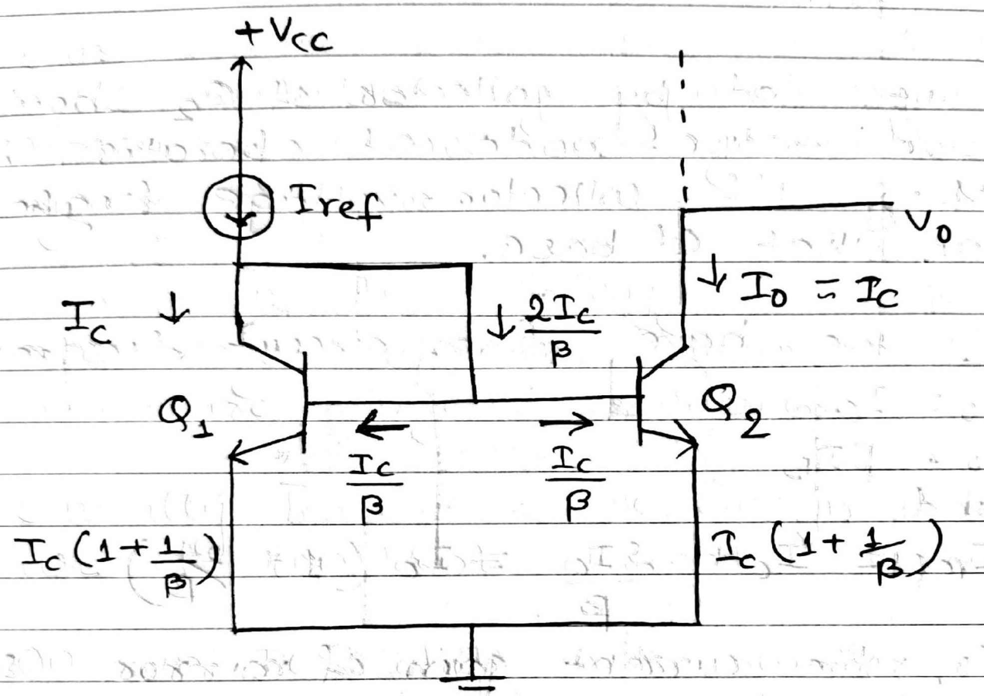


Fig. simple current mirror

circuits in which the output current is forced to be equal to the input current is called current mirror circuit.

it consists of two matched transistors Q_1 and Q_2 and connected as shown in figure. Q_1 is connected as diode.

current mirror is fed with a constant current source Iref and output is taken from collector of Q_2 as shown in figure.

- Circuit fed by collector of Q_2 should ensure active mode of operation by keeping its collector-voltage higher than that of base.

we have from circuit diagram

$I_0 = I_C$

$I_0 = \beta I_B$

and,

$$I_{ref} = I_C + \frac{2I_C}{\beta} = I_C\left(1 + \frac{2}{\beta}\right)$$

So, the current gain of mirror is

$$\frac{I_0}{I_{ref}} = \frac{I_C}{I_C(1+2/\beta)} = \frac{1}{1+2/\beta}$$

If $\beta >> 1$, then $(1 + \frac{2}{\beta}) \simeq 1$

$$\therefore \frac{I_0}{I_{ref}} = 1$$

$$\boxed{\therefore I_0 = I_{ref}}$$

Assumptions:

→ Q_1 and Q_2 conduct equal collector currents.

Widlar Current Source: [6+8]

- Differ from basic current mirror in an important way i.e. resistor R_E is included in emitter load of Q_2.

- Assumption: Q_1 and Q_2 are perfectly matched.

- Neglecting base currents, we have

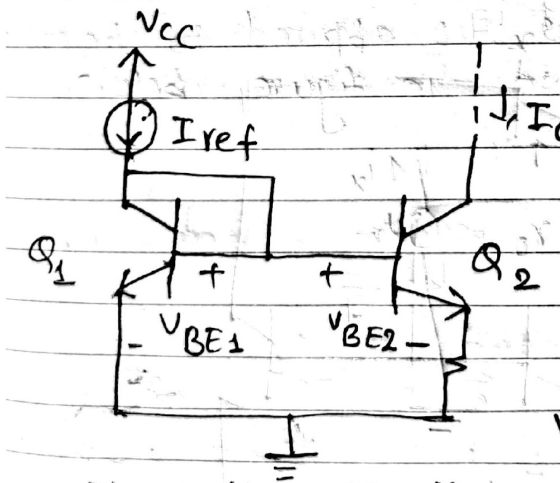


Fig. Widlar Circuit

$$V_{BE1} = V_T \ln\left(\frac{I_{ref}}{I_S}\right)$$

$$V_{BE2} = V_T \ln\left(\frac{I_O}{I_S}\right)$$

$$V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_{ref}}{I_O}\right)$$

From figure,

$$V_{BE1} - V_{BE2} = I_O R_E$$

$$\therefore I_O R_E = V_T \ln\left(\frac{I_{ref}}{I_O}\right)$$

→ Widlar circuit allows generation of small constant current using relatively small resistors. This is an important advantage that results in considerable saving in chip area.

→ Output resistance is high.

→ Increase in output resistance is due to emitter degeneration resistance R_E.

Calculation of output resistance (R_{out}):

→ To determine the output resistance of Q_2 we replace Q_2 with its π-model and a test voltage v_x is applied to the collector as shown in figure below

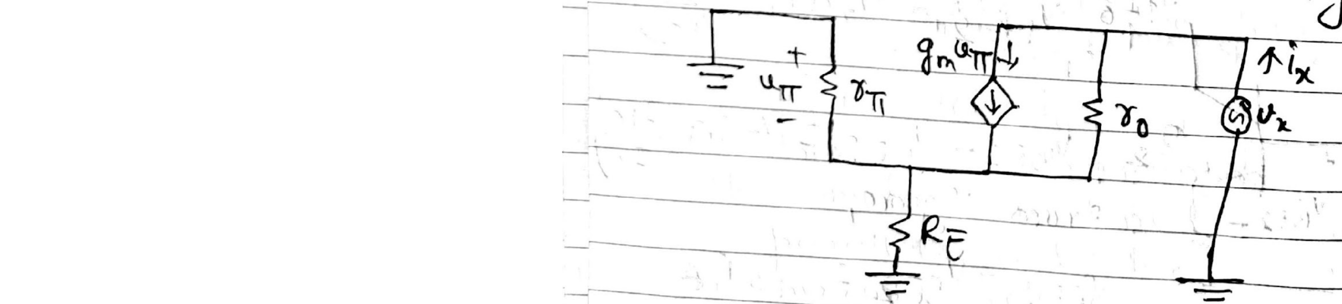
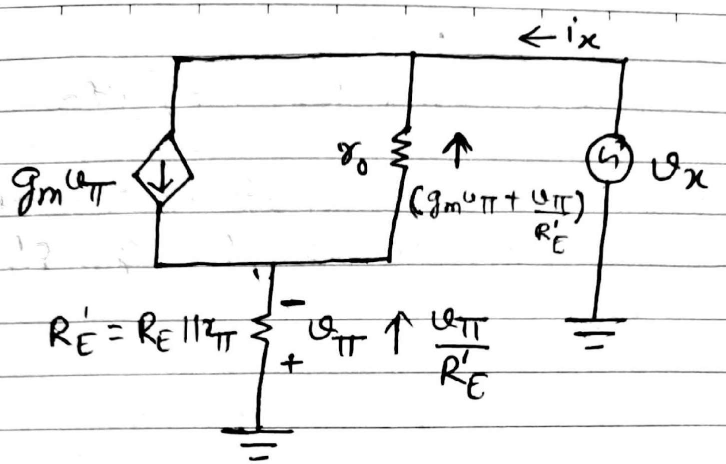


Fig. Equivalent π-model of BJT (Q_2)



From figure, we have

$$v_x = -v_\pi - \left(g_m + \frac{1}{R_E'}\right) v_\pi r_o$$

and,

$$i_x = g_m v_\pi - \left(g_m + \frac{1}{R_E'}\right) v_\pi$$

$\therefore$ The output resistance is

$$R_o = \frac{v_x}{i_x} = \frac{-v_\pi - \left(g_m + \frac{1}{R_E'}\right) v_\pi r_o}{g_m v_\pi - \left(g_m + \frac{1}{R_E'}\right) v_\pi}$$

$$= \frac{-1 - \left(g_m + \frac{1}{R_E'}\right) r_o}{g_m - g_m - 1/R_E'}$$

$$R_o = R_E' + (1 + g_m R_E') r_o$$

$$R_o = (1+g_m R_E')r_o$$
$$= [1 + g_m(R_E \| r_\pi)]r_o$$

which shows that output resistance is increased by factor of $(1+g_m R_E')$.

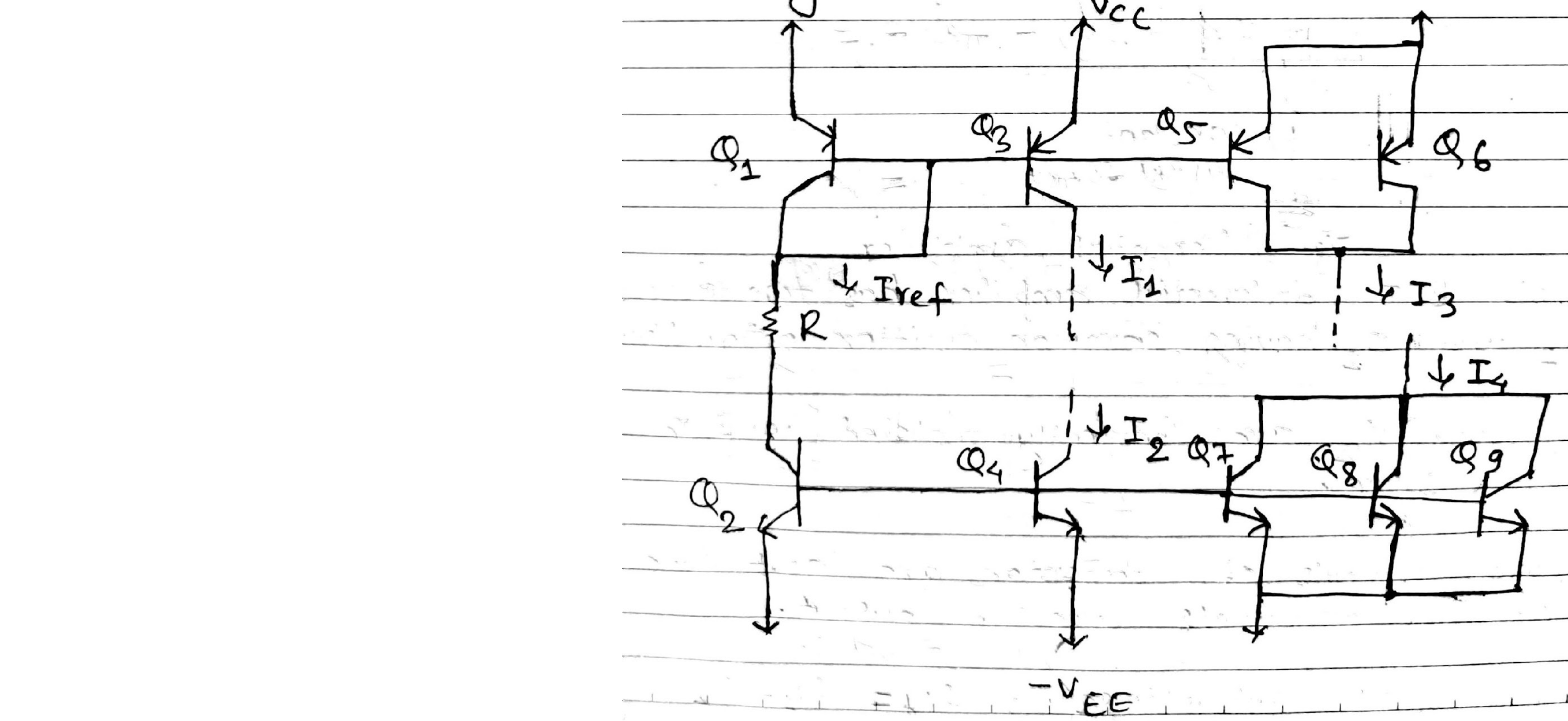
Q. Figure s

Current Steering Circuits [595]

- Utilizes two power supplies V_{CC} and $-V_{EE}$
- Assuming high β, $I_{ref} = I_1$
- Transistor Q_3 supplies current to any load as long as voltage at collector doesn't exceeds that at the base $(V_{CC} - V_{BE3})$
- To generate dc current twice the value of I_{ref}, two transistors Q_5 and Q_6, each of which is matched to Q_1 are connected in parallel and the combination forms a mirror with Q_1. Thus $I_3 = 2I_{ref}$.

→ Parallel combination of Q_5 and Q_6 is equivalent to transistor with EBJ area double that of Q_1.

→ Similarly, to generate current three times I_{ref}, three transistors: Q_7, Q_8 and Q_9, each of which is matched to Q_2, are connected in parallel and the combination is placed in a mirror configuration with Q_2.



The Differential Amplifier [808]

Ideal Differential Amplifier :

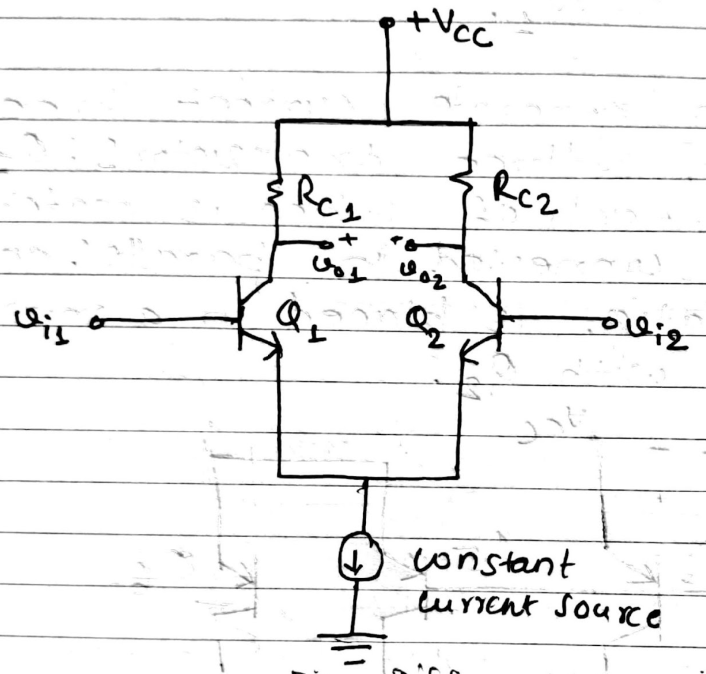


Fig. Differential amplifier

- Basic BJT differential amplifier has two transistors Q_1 and Q_2 having common emitter configuration.
- Q_1 and Q_2 are perfectly matched i.e. β, r_e are same.
- Base terminals of transistors are input while collector terminals are the output.
- Differential input voltage is $v_{id} = v_{i1} - v_{i2}$

• Differential output voltage is $v_{od} = v_{o1} - v_{o2}$

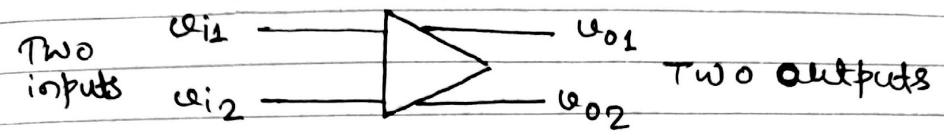


Fig. schematic symbol for differential amplifier.

• Since there are two inputs and two outputs, amplifier is said to has double ended (double sided) input and double ended output.

Single ended Voltage gain
The voltage is applied at both the inputs whereas output is taken from one end only i.e.

$$A_v = \frac{v_{o1}}{v_{i1} - v_{i2}} \quad \text{or} \quad A_v = \frac{v_{o2}}{v_{i1} - v_{i2}}$$

Double ended Voltage gain

$$A_v = \frac{v_{o1} - v_{o2}}{v_{i1} - v_{i2}}$$

Q. Show that the output of differential amplifier is proportional to difference between two input voltages.

To show: $v_o \propto v_{i_1} - v_{i_2}$

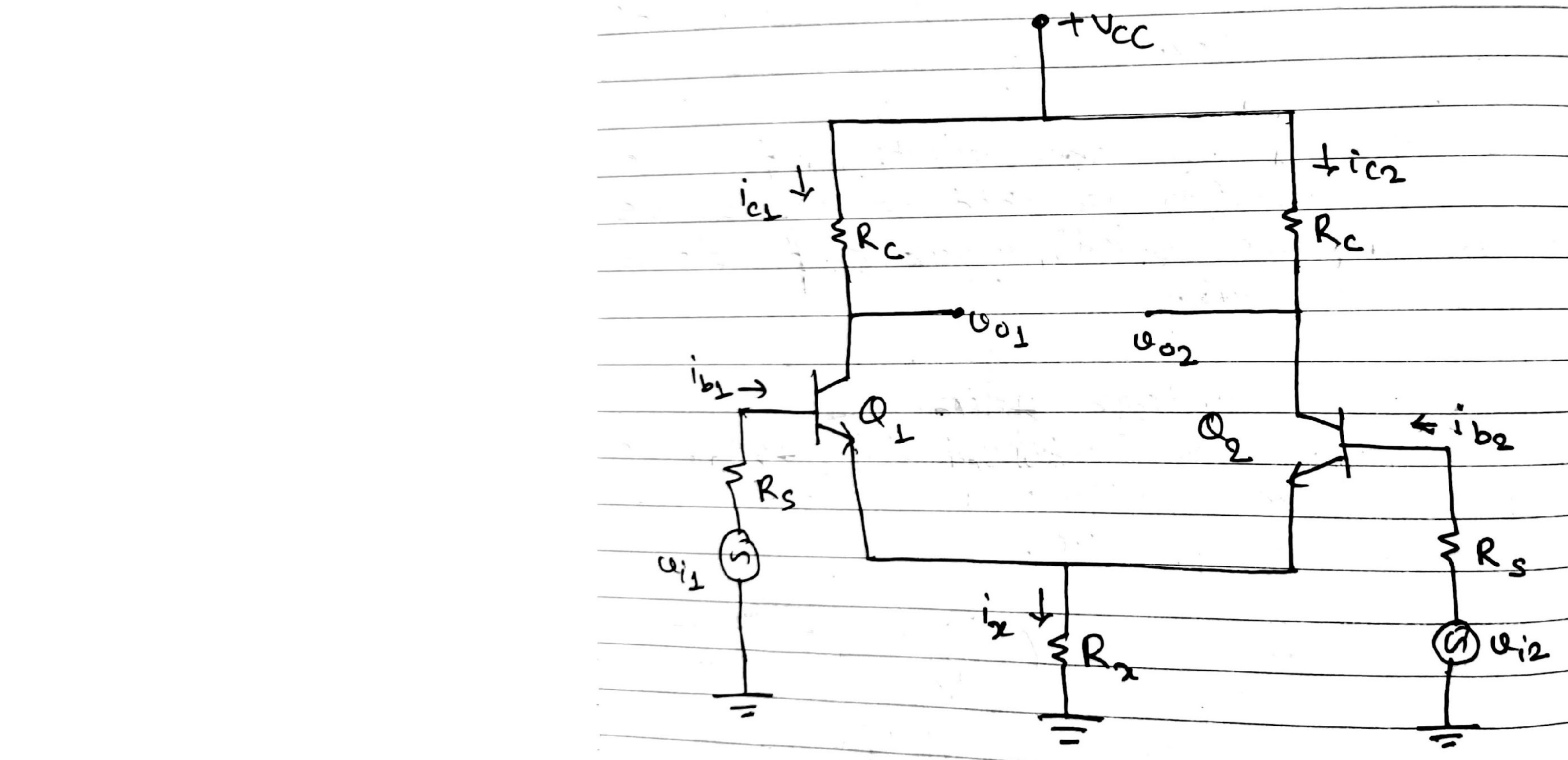


Fig. Differential amplifier

From, the circuit, we have

$$v_{i1} = i_{b1} R_S + i_{e1} r_e + i_x R_x \longrightarrow i)$$

$$v_{i2} = i_{b2} R_S + i_{e2} r_e + i_x R_x \longrightarrow ii)$$

now,

$$v_{i1} - v_{i2} = (i_{b1} - i_{b2}) R_S + (i_{e1} - i_{e2}) r_e$$

we also have,

$$i_{e1} = (\beta+1) i_{b1} \quad \text{and} \quad i_{e2} = (\beta+1) i_{b2}$$

$$\therefore v_{i1} - v_{i2} = (i_{b1} - i_{b2}) R_S + (\beta+1)(i_{b1} - i_{b2}) r_e$$

$$= (i_{b1} - i_{b2}) [R_S + (\beta+1) r_e]$$

$$\therefore i_{b1} - i_{b2} = \frac{v_{i1} - v_{i2}}{R_S + (\beta+1) r_e} \longrightarrow (iii)$$

Again, $v_o = v_{o1} - v_{o2}$

$$= i_{c1} R_C - i_{c2} R_C$$

$$= \beta i_{b1} R_C - \beta i_{b2} R_C$$

$$= \beta R_C (i_{b1} - i_{b2}) \longrightarrow iv)$$

From (iii) and (iv) we get

$$v_o = \beta R_c \left[\frac{v_{i1} - v_{i2}}{R_s + (\beta+1) r_e} \right]$$

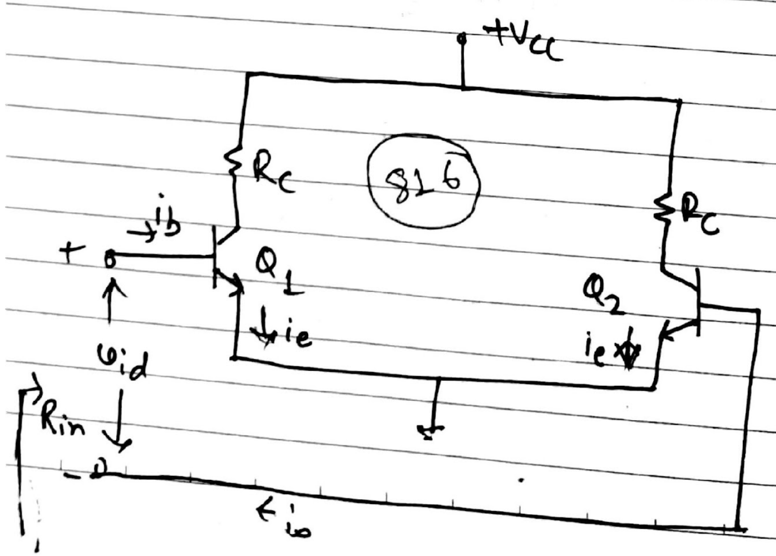
$$v_o = K (v_{i1} - v_{i2})$$

where,

$$K = \frac{\beta R_c}{R_s + (\beta+1) r_e}$$

$$\boxed{v_o \propto (v_{i1} - v_{i2})}$$ Proved

Differential input resistance in terms of circuit parameter :



$$i_e' = \frac{v_{id}}{2r_e} \Rightarrow i_b' = \frac{i_e'}{\beta+1}$$

$$R_{in} = \frac{v_{id}}{i_b'} = 2(\beta+1)\,r_e.$$

DC Analysis of Differential Amplifier

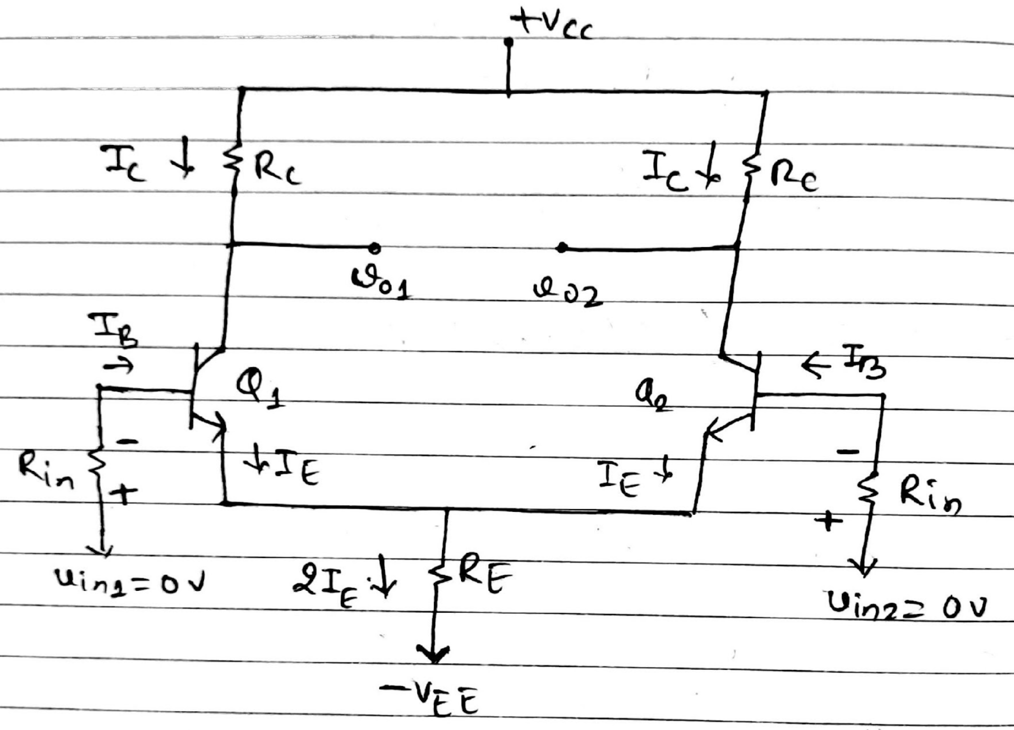


Fig: Dual input balanced output differential amplifier.

- DC Analysis of differential amplifier circuit is done for determination of operating points (I_{CQ} and V_{CEQ}) when no signal is applied.

- For dc analysis, we set $v_{in1} = v_{in2} = 0$ (i.e. ground)

- Since, both transistors Q_1 and Q_2 are identical we calculate Q-point for transistor Q_1 only. The same Q-point can be used for transistor Q_2 also.

Applying KVL to base-emitter loop of transistor Q_1, we get

$$-I_B R_{in} - V_{BE} - 2I_E R_E + V_{EE} = 0$$

since $I_C \simeq I_E$ and $I_B = \dfrac{I_E}{\beta+1}$, we have

$$-\frac{I_E}{\beta+1} R_{in} - V_{BE} - 2I_E R_E + V_{EE} = 0$$

$$I_E = \frac{V_{EE} - V_{BE}}{R_E + \dfrac{R_{in}}{\beta+1}}$$

since $\dfrac{R_{in}}{\beta+1} << R_E$, so

$$I_E = \frac{V_{EE} - V_{BE}}{R_E}$$

$$\boxed{I_C = \frac{V_{EE} - V_{BE}}{R_E}}$$

The above expression shows that emitter current can be set by varying R_E only. Also, it is noticeable that emitter current in transistor Q_1 and Q_2 is independent of collector resistance R_C.

To find V_{CE}, we have

$$V_C = V_{CC} - I_C R_C$$

and, $V_{CE} = V_C - V_E$

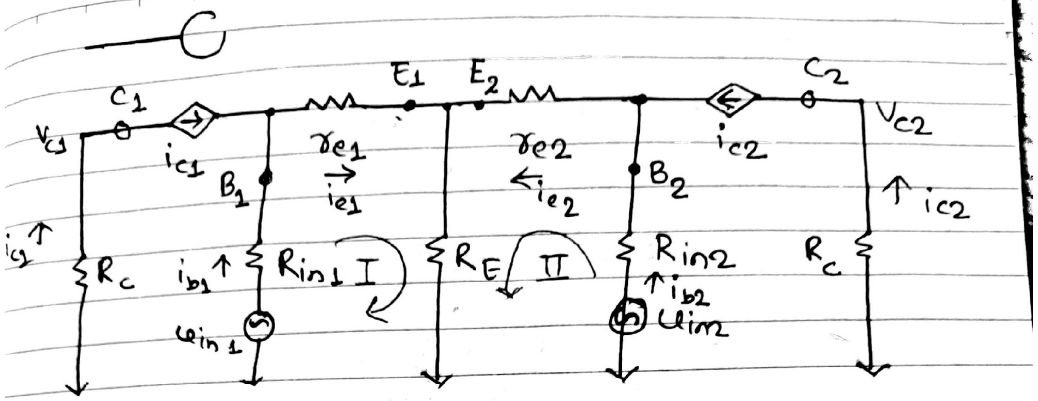
$$= V_{CC} - I_C R_C - (-V_{BE})$$

$$\boxed{V_{CE} = V_{CC} + V_{BE} - I_C R_C}$$

Hence, for both transistors I_{CQ} and V_{CEQ} can be determined by using above expressions.

AC Analysis

For ac analysis, the dc voltages $+V_{CC}$ and $-V_{EE}$ are set at zero and small signal T- equivalent models are substituted for transistors Q_1 and Q_2.



Since the transistors Q_1 and Q_2 are matched so that $r_{e1} = r_{e2} = r_e$ and $R_{in1} = R_{in2} = R_{in}$

Now, applying KVL in loop I and loop II, we get

$$v_{in_1} = i_{b1} R_{in1} + i_{e1} r_{e1} + (i_{e1} + i_{e2}) R_E$$

$$v_{in2} = i_{b2} R_{in2} + i_{e2} r_{e2} + (i_{e1} + i_{e2}) R_E$$

So, $v_{in_1} - v_{in_2} = (i_{b1} - i_{b2}) R_{in} + (i_{e1} - i_{e2}) r_e$

$$= (i_{b1} - i_{b2}) R_{in} + (\beta+1)(i_{b1} - i_{b2}) r_e$$

$$= (i_{b1} - i_{b2}) [R_{in} + (\beta+1) r_e]$$

$$i_{b1} - i_{b2} = \frac{v_{in_1} - v_{in2}}{R_{in} + (\beta+1) r_e}$$

Now, we have.

$$v_o = v_{c2} - v_{c1}$$

$$= -i_{c2}R_c - (-i_{c1}R_c)$$

$$= (i_{c1} - i_{c2}) R_c$$

$$= \beta (i_{b1} - i_{b2}) R_c$$

$$\Rightarrow \quad v_o = \beta R_c \frac{(v_{in1} - v_{in2})}{R_{in} + (\beta+1)r_e}$$

$$\Rightarrow \quad \frac{v_o}{v_{in1} - v_{in2}} = \frac{\beta R_c}{R_{in} + (\beta+1)r_e}$$

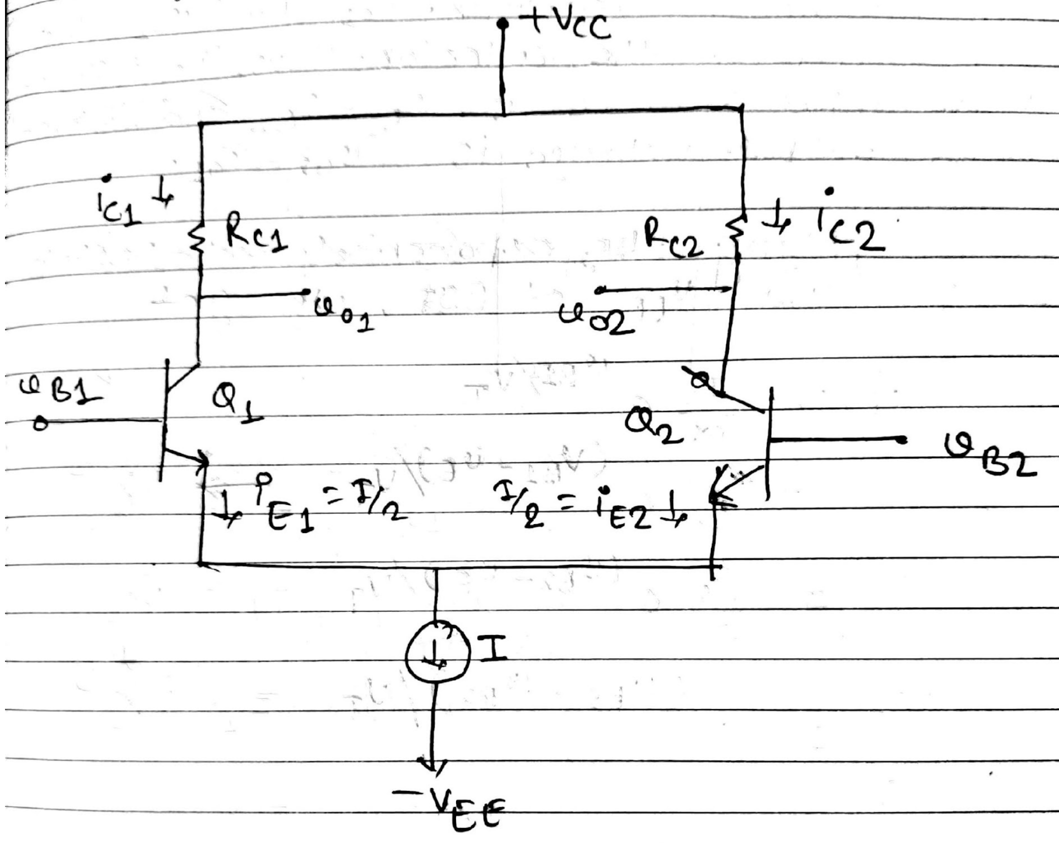
since $(\beta+1)r_e >> R_{in}$, we have

$$\Rightarrow \quad \frac{v_o}{v_{in1} - v_{in2}} = \frac{R_c}{r_e}$$

$$\boxed{\therefore \; A_d \text{ (differential gain)} = \frac{v_o}{v_{id}} = \frac{R_c}{r_e}}$$

The expression shows that A_d is directly proportional to the collector resistance R_c i.e. load.

Cumplete analysis of Differential Amplifier



Let v_{B1} and v_{B2} be two input signals to the differential amplifier. v_{o1} and v_{o2} be the outputs at the collector. Thus, the differential Input voltage is $v_{B1} - v_{B2}$ and differential output voltage is $v_{o2} - v_{o1}$.

Now, applying the exponential relationship of i_E and v_{BE} of BJT, we get

$$i_{E1} = \frac{I_s}{\alpha} e^{v_{BE1}/V_T}$$

$$= \frac{I_s}{\alpha} e^{(v_{B1} - v_E)/V_T} \longrightarrow \text{i)}$$

$$i_{E2} = \frac{I_s}{\alpha} e^{(v_{B2} - v_E)/V_T} \longrightarrow \text{ii)}$$

$$\frac{i_{E1}}{i_{E2}} = e^{(v_{B1} - v_{B2})/V_T} \longrightarrow \text{iii)}$$

Thus, we get

$$\frac{i_{E1}}{i_{E1} + i_{E2}} = \frac{1}{1 + e^{-(v_{B1} - v_{B2})/V_T}} \longrightarrow \text{iv)}$$

$$\frac{i_{E2}}{i_{E1} + i_{E2}} = \frac{1}{1 + e^{(v_{B1} - v_{B2})/V_T}} \longrightarrow \text{v)}$$

we have,

$$i_{E1} + i_{E2} = I$$

$$\therefore \quad i_{E1} = \frac{I}{1 + e^{-v_{id}/V_T}} \qquad \left[\cancel{v_{id} = v_{B1} - v_{B2}}\right]$$

$$\left[v_{id} = v_{B1} - v_{B2}\right]$$

and, $$i_{E2} = \frac{I}{1 + e^{v_{id}/V_T}}$$

So, $$i_{C1} = \frac{\alpha I}{1 + e^{-v_{id}/V_T}}$$

$$i_{C2} = \frac{\alpha I}{1 + e^{v_{id}/V_T}}$$

Now, multiplying numerator and denominator by $e^{v_{id}/2V_T}$, we get

$$i_{C1} = \frac{\alpha I \, e^{v_{id}/2V_T}}{e^{v_{id}/2V_T} + e^{-v_{id}/2V_T}}$$

$$= \frac{\alpha I \left(1 + \frac{v_{id}}{2V_T} + \cdots\cdots\right)}{\left(1 + \frac{v_{id}}{2V_T} + \cdots\cdots\right) + \left(1 - \frac{v_{id}}{2V_T} + \cdots\right)}$$

$$= \frac{\alpha I}{2} + \frac{\alpha I}{2V_T} \cdot \left(\frac{v_{id}}{2}\right)$$

$$= \underset{(dc)}{I_{C1}} + \underset{(ac)}{i_{c1}}$$

Similarly,

$$i_{c2} = \frac{\alpha I}{2} - \frac{\alpha I}{2V_T} \cdot \frac{v_{id}}{2}$$

So,

(ac) $$i_{c1} = \frac{\alpha I}{2V_T} \cdot \frac{v_{id}}{2} = \frac{I_c}{V_T} \cdot \frac{v_{id}}{2} = \frac{g_m v_{id}}{2}$$

(ac) $$i_{c2} = -\frac{\alpha I}{2V_T} \cdot \frac{v_{id}}{2} = \frac{-I_c}{V_T} \cdot \frac{v_{id}}{2} = \frac{-g_m v_{id}}{2}$$

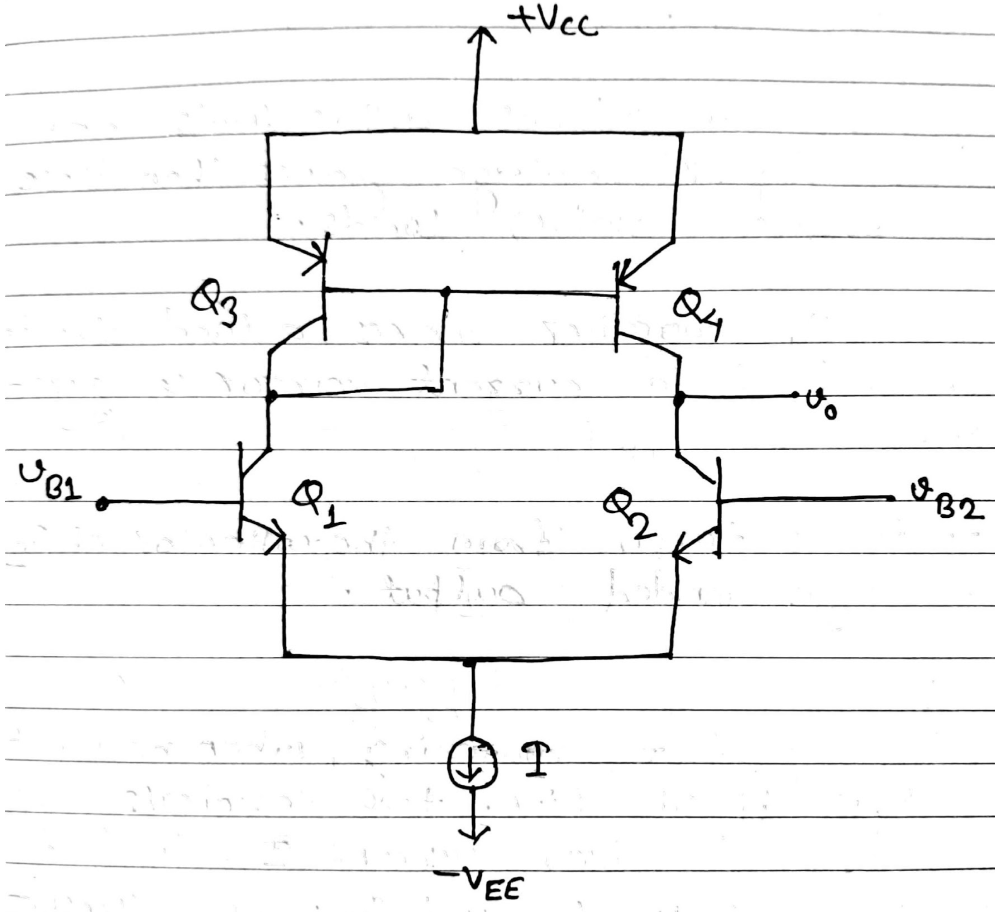
Thus, $$v_{o1} = V_{CC} - i_{c1} R_C$$
$$v_{o2} = V_{CC} - i_{c2} R_C$$

∴ output voltage is given by

$$v_o = v_{o2} - v_{o1}$$
$$= -\frac{g_m v_{id}}{2} R_C - \frac{g_m v_{id}}{2} R_C$$

$$v_o = g_m v_{id} R_C$$

BJT Amplifier with active load



→ Active devices (transistors) occupy much less silicon area than medium and large sized resiotors.

→ BJT load transistor is usually connected as a current source.

→ The output resistance of current source is very high.

→ Amplifier that utilizes active loads can achieve higher voltage gains than those with passive (resistive) loads.

→ Q_3 and Q_4 together makes a load circuit connected in a current mirror configuration.

→ Output is taken from the collector of Q_2 i.e. single ended output.

Case I :

Assuming perfect matching, when no input signal is applied (i.e. two terminals are grounded), the bias current I divided equally between Q_1 and Q_2. The current of Q_1 is fed to the input transistor of the mirror Q_3. Thus, the replica of this current is provided by the output transistor of mirror Q_4. The output node of the two current $I/2$ balance each other out leaving a zero current to the load.

Case II :

consider, differential signal $v_{id} = (v_{B1} - v_{B2})$ is applied at the input. Then the current signals $\frac{g_m v_{id}}{2}$ will result in the collector of Q_1 and Q_2 with polarities indicated. Also, due to current mirror configuration, the current signal $g_m\left(\frac{v_{id}}{2}\right)$ flows through collector of Q_4. Now, if resistance between output terminal and ground is R_o, then

$$v_o = g_m v_{id} R_o$$