UNIT VII

FET AMPLIFIERS

7.0 INTRODUCTION

Field Effect Transistor (FET) amplifiers provide an excellent voltage gain and high input impedence. Because of high input impedence and other characteristics of JFETs they are preferred over BJTs for certain types of applications.

There are 3 basic FET circuit configurations:

i)Common Source

ii)Common Drain

iii)Common Gain

Similar to BJT CE,CC and CB circuits, only difference is in BJT large output collector current is controlled by small input base current whereas FET controls output current by means of small input voltage. In both the cases output current is controlled variable.

FET amplifier circuits use voltage controlled nature of the JFET. In Pinch off region, I_D depends only on V_{GS}.

7.1 Common Source (CS) Amplifier

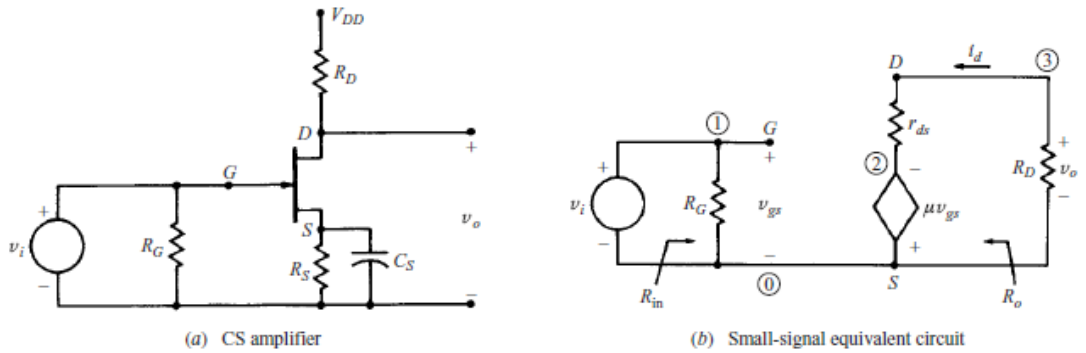


Fig. 7.1 (a) CS Amplifier (b) Small-signal equivalent circuit

A simple Common Source amplifier is shown in Fig. 7.1(a) and associated small signal equivalent circuit using voltage-source model of FET is shown in Fig. 7.1(b)

Voltage Gain

Source resistance (R_S) is used to set the Q-Point but is bypassed by C_S for mid-frequency operation. From the small signal equivalent circuit ,the output voltage

$$V_O = -R_D \mu V_{gs}(R_D + r_d)$$

Where $V_{gs} = V_i$, the input voltage,

Hence, the voltage gain,

$$A_V = V_O / V_i = -R_D \mu (R_D + r_d)$$

Input Impedence

From Fig. 7.1(b) Input Impedence is

$$Z_i = R_G$$

For voltage divider bias as in CE Amplifiers of BJT

$$R_G = R_1 \parallel R_2$$

Output Impedance

Output impedance is the impedance measured at the output terminals with the input voltage $V_I = 0$

From the Fig. 7.1(b) when the input voltage $V_i = 0$, $V_{gs} = 0$ and hence

$$\mu V_{gs} = 0$$

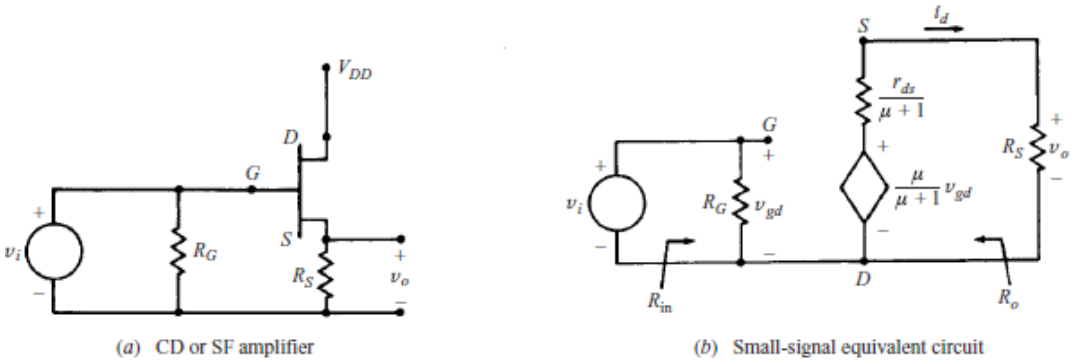
The equivalent circuit for calculating output impedence is given in Fig. 7.2.

Output impedence $Z_o = r_d \parallel R_D$

Normally r_d will be far greater than R_D . Hence $Z_o \approx R_D$

7.2 Common Drain Amplifier

A simple common drain amplifier is shown in Fig. 7.2(a) and associated small signal equivalent circuit using the voltage source model of FET is shown in Fig. 7.2(b).Since voltage V_{gd} is more easily determined than $V_{gs,}$ the voltage source in the output circuit is expressed in terms of V_{gs} and Thevenin's theorem.



(a) CD or SF amplifier (b) Small-signal equivalent circuit

Fig. 7.2 (a)CD Amplifier (b)Small-signal equivalent circuit

Voltage Gain

The output voltage,

$$V_O = R_S \mu V_{gd} / (\mu + 1) R_S + r_d$$

Where $V_{gd} = V_i$ the input voltage.

Hence, the voltage gain,

$$A_v = V_O / V_i = R_S \mu / (\mu + 1) R_S + r_d$$

Input Impedence

From Fig. 7.2(b), Input Impedence $Z_i = R_G$

Output Impedence

From Fig. 7.2(b), Output impedence measured at the output terminals with input voltage $V_i = 0$ can be calculated from the following equivalent circuit.

As $V_i = 0$: $V_{gd} = 0$: $\mu v_{gd} / (\mu + 1) = 0$

Output Impedence

$$Z_O = r_d / (\mu + 1) \parallel R_S$$

When $\mu \gg 1$

$$Z_O = (r_d / \mu) \parallel R_S = (1/g_m) \parallel R_S$$

7.3 BIASING FET:-

For the proper functioning of a linear FET amplifier, it is necessary to maintain the operating point Q stable in the central portion of the pinch off region The Q point should be independent of device parameter variations and ambient temperature variations

This can be achieved by suitably selecting the gate to source voltage V_{GS} and drain current I_D which is referred to as biasing

JFET biasing circuits are very similar to BJT biasing circuitsThe main difference between JFET circuits and BJT circuits is the operation of the active components themselves

There are mainly two types of Biasing circuits

1. Self bias
2. Voltage divider bias.

7.3.1. SELF BIAS:-

Self bias is a JFET biasing circuit that uses a source resistor to help reverse bias the JFET gate.

A self bias circuit is shown in the fig 7.3

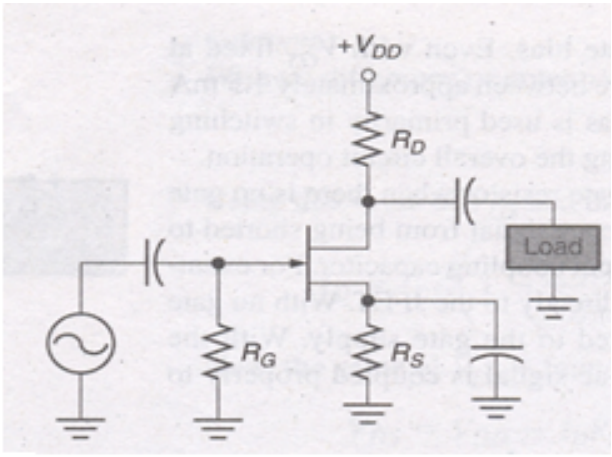


fig 7.3

Self bias is the most common type of JFET bias. This JFET must be operated such that gate source junction is always reverse biased. This condition requires a negative V_{GS} for an N channel JFET and a positive V_{GS} for P channel JFET. This can be achieved using the self bias arrangement as shown in Fig 7.3. The gate resistor R_G doesn't affect the bias because it has essentially no voltage drop across it, and : the gate remains at 0V .R_G is necessary only to isolate an ac signal from ground in amplifier applications. The voltage drop across resistor R_S makes gate source junction reverse biased.

DC analysis of self Bias:-

In the following DC analysis , the N channel J FET shown in the fig7.4. is used for illustration.

For DC analysis we can replace coupling capacitors by open circuits and we can also replace the resistor R_G by a short circuit equivalent.

:. $I_G = 0$

The relation between I_D and V_{GS} is given by

$$Id=Idss[1-\frac{Vgs}{Vp}]^2$$

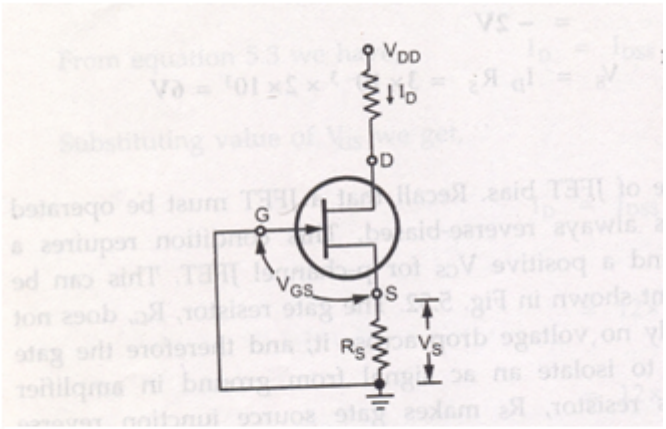


fig 7.4

V_{GS} for N channel JFET is =-id Rs

Substuting this value in the above equation

$$Id=Idss[1-\frac{(-IdRs)}{Vp}]^2$$

$$Id=Idss[1+\frac{(IdRs)}{Vp}]^2$$

For the N-chanel FET in the above figure

Is produces a voltage drop across Rs and makes the source positive w.r.t ground

in any JFET circuit all the source current passes through the device to drain circuit this is due to the fact that there is no significant gate current

therefore we can define source current as Is=Id and Vg=0 then

Vs= Is Rs =IdRs

Vgs=Vg-Vs=0-IdRs=-IdRs

Drawing the self bias line:-

Typical transfer characteristics for a self biased JFET are shown in the fig7.5.

The maximum drain current is 6mA and the gate source cut off voltage is -3V. This means the gate voltage has to be between 0 and -3V.

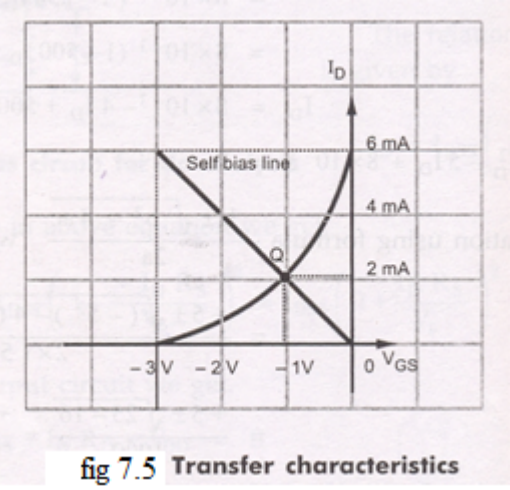


fig 7.5 Transfer characteristics

Now using the equation $V_{GS} = -I_D R_S$ and assuming R_S of any suitable value we can draw the self bias line.

Let us assume RS = 500Ω

With this Rs , we can plot two points corresponding to $I_D = 0$ and Id = I_{DSS}

for $I_D = 0$

$V_{GS} = -I_D R_S$

$V_{GS} = 0X (500.Ω) = 0V$

So the first point is (0 ,0)

(I_d, V_{GS})

For $I_D = I_{DSS} = 6mA$

$V_{GS} = (-6mA) (500 Ω) = -3V$

So the 2nd Point will be (6mA,-3V)

By plotting these two points, we can draw the straight line through the points. This line will intersect the transconductance curve and it is known as self bias line. The intersection point gives the operating point of the self bias JFET for the circuit.

At Q point , the I_D is slightly > than 2mA and V_{GS} is slightly > -1V. The Q point for the self bias JFET depends on the value of Rs.If Rs is large, Q point far down on the transconductance curve ,I_D is small, when Rs is small Q point is far up on the curve , I_D is large.

7.3.2 VOLTAGE DIVIDER BIAS:-

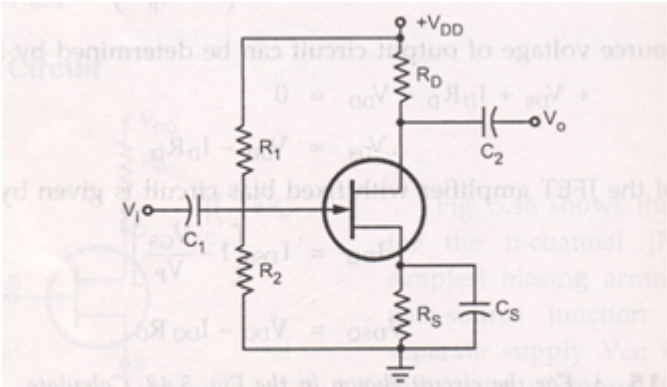


fig 7.6 **Voltage divider bias for n-channel JFET**

The fig7.6 shows N channel JFET with voltage divider bias. The voltage at the source of JFET must be more positive than the voltage at the gate in order to keep the gate to source junction reverse biased. The source voltage is

$V_S = I_D R_S$

The gate voltage is set by resistors R1 and R2 as expressed by the following equation using the voltage divider formula.

$$V_g = \left(\frac{R2}{(R1+R2)}\right) Vdd$$

For dc analysis fig 7.7

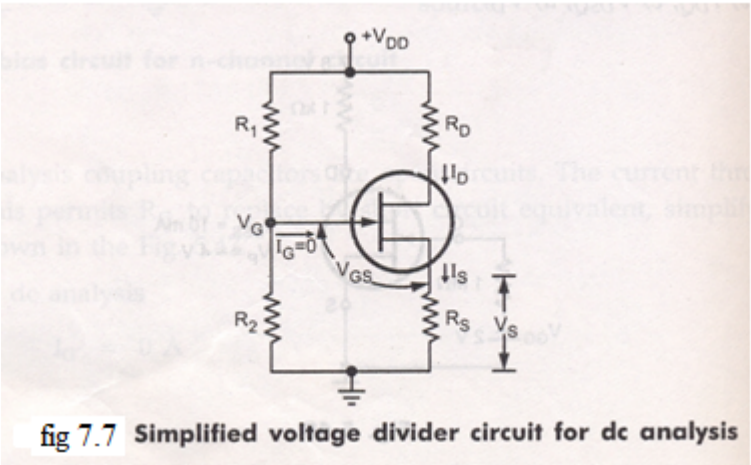


fig 7.7 **Simplified voltage divider circuit for dc analysis**

Applying KVL to the input circuit

$V_G - V_{GS} - V_S = 0$

:: $V_{GS} = V_G - V_S = V_G - I_S R_S$

$V_{GS} = V_G - I_D R_S$ :: $I_S = I_D$

Applying KVL to the input circuit we get

$V_{DS} + I_D R_D + V_S - V_{DD} = 0$

$::V_{DS} = V_{DD} - I_D R_D - I_D R_S$

$V_{DS} = V_{DD} - I_D (R_D + R_S)$

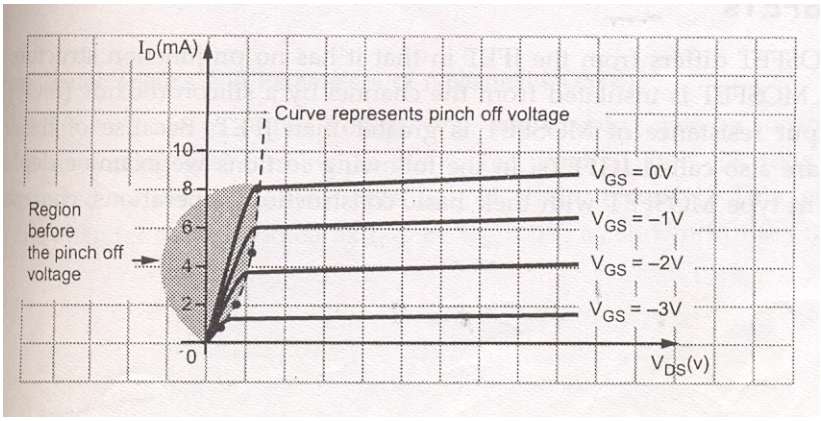
The Q point of a JFET amplifier , using the voltage divider bias is

$I_{DQ} = I_{DSS} [1 - V_{GS}/V_P]2$

$V_{DSQ} = V_{DD} - I_D (R_D + R_S)$

7.4 JFET AS A VVR OR VDR:-

Let us consider the drain characteristics of FET as shown in the fig.



In this characteristics we can see that in the region before pinch off voltage, drain characteristics are linear, i.e. FET operation is linear. In this region the FET is useful as a voltage controlled resistor,i.e. the drain to source resistance is controlled by the bias voltage V_{GS}.(In this region only FET behaves like an ordinary resistor This resistances can be varied by V_{GS}) .The operation of FET in the region is useful in most linear applications of FET.In such an application the FET is also referred to as a voltage variable resistor (VVR) or voltage dependent resistor (VDR).

The drain to source conductance (rd)

$g_d = \frac{Id}{Vds}$ for small values of V_{DS} which may also be expressed as

$$g_d = g_{d0}\left(1 - \left(\frac{Vgs}{Vp}\right)^{1/2}\right)$$

Where g_{d0} is the value of drain conductance

When the variation of the rd with VGS can be closely approximated by the expression

rd= $\left(\frac{r0}{1-KVgs}\right)$ Where ro = drain resistance at zero gate bias.K = a constant, dependent upon FET type.

7.4.1 APPLICATION OF VVR

The VVR property of FET can be used to vary the voltage gain of a multistage amplifier A, as the signal level is increased. This action is called AGC automatic gain control. A typical arrangement is shown in the fig.

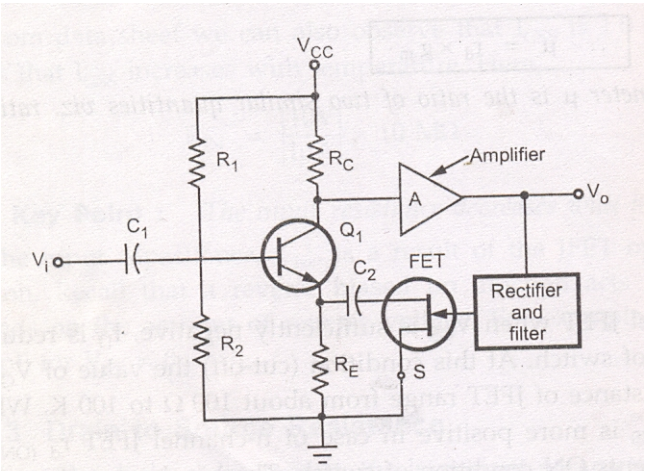


Fig. 4.54 AGC amplifier using FET as a voltage variable resistor

Here maximum value of signal is taken rectified; filter to produce a DC voltage proportional to the output signal level. This voltage is applied to the gate of JFET, this causing the resistance between drain and source to change. As this resistance is connected across RE, so effective RE also changes according to change in the drain to source resistance. When output signal level increases, the drain to source resistance rd increases, increasing effective RE. Increase in RE causes the gain of transistor Q1 to decrease, reducing the output signal. Exactly reverse process takes place when output signal level decreased.

:: The output signal level is maintained constant. It is to be noted that the DC bias conditions of Q1 are not affected by JFET since FET is isolated from Q1 by capacitor C2

7.5 UNI JUNCTION TRANSISTOR (UJT)

Another device whose construction is similar to that of the FET is shown in the figure.

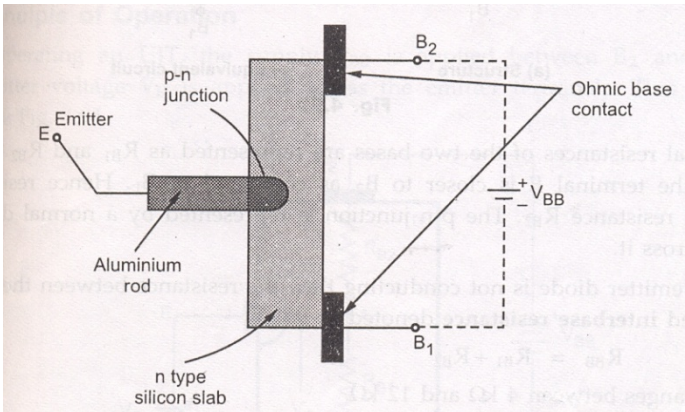


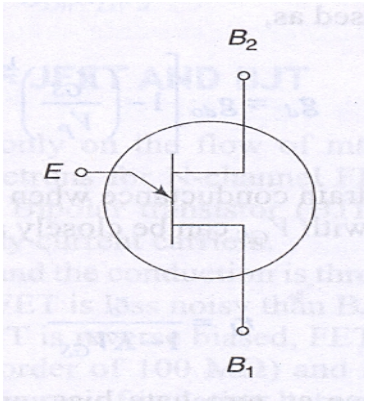
Fig. 4.91 Construction of UJT

It is a three terminal device, having two layers.It consists of a slab of lightly doped N-type silicon material. The two base contacts are attached to both ends of this N-type surface. These are denoted as B1 and B2 respectively.

A P-type material is used to form a pn junction at the boundary of the aluminium rod and N-type slab. The N-type is lightly doped while P-type is heavily doped. That is N-type provides high resistivity and P-type provides low resistivity.

This device was originally described in the literature as the double-base diode, but is now commercially available under the designation Uni Junction transistor (UJT).

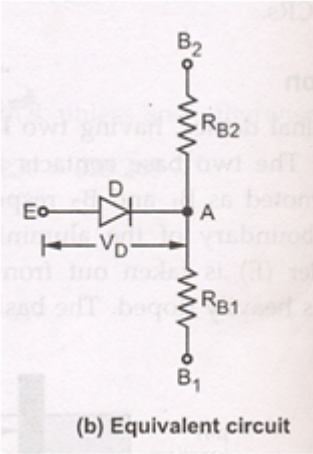
The standard symbol for this device is shown in the fig.



Here the emitter arrow is inclined and points toward B1 and This emitter arrow which is at an angle to the vertical line representing N-type material. This arrow indicates the direction of flow of conventional current when UJT is forward biased.

EQUIVALENT CIRCUIT OF UJT

The circuit of UJT is shown in the fig.



(b) Equivalent circuit

In the construction ,the terminal emitter is closer to B_2 as compared to B_1.

If we see the equivalent circuit of UJT, The internal resistances of the two bases are represented as $R_{b1}$and R_{b2}. Hence R_{b1} is greater than R_{b2}. The pn junction is represented by a normal diode with V_d as the drop across it. When the emitter diode is not conducting then the resistance between the two bases B_1 and B_2 is called interbase resistance denotes R_{bb}

$$R_{bb}=R_{b1}+R_{b2}$$

Its value ranges from 4kΩ to 12kΩ

Intrinsic stand off ratio (η)

Consider UJT as shown in the fig. to which supply V_{bb} is connected. With I_e=0, That is emitter diode is not conducting ,

$$R_{bb}=R_{b1}+R_{b2}$$

Then the voltage drop across R_{b1} can be obtained by using potential divider rule.

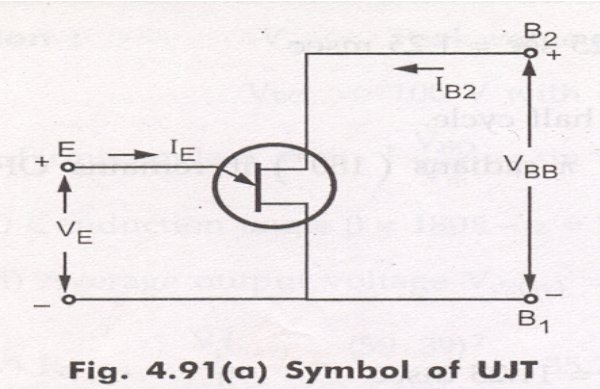
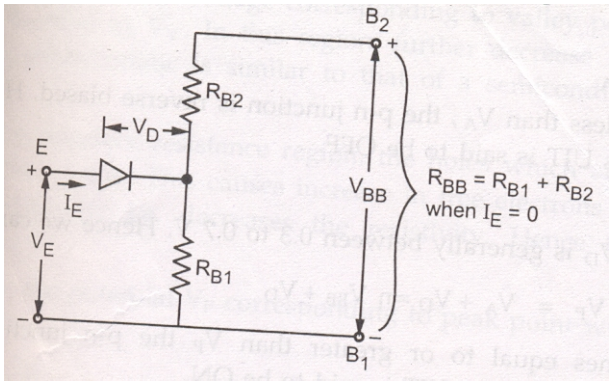


Fig. 4.91(a) Symbol of UJT

Replacing with its equivalent circuit



$R_{bb}=R_{b1}+R_{b2}$

When I_e =0

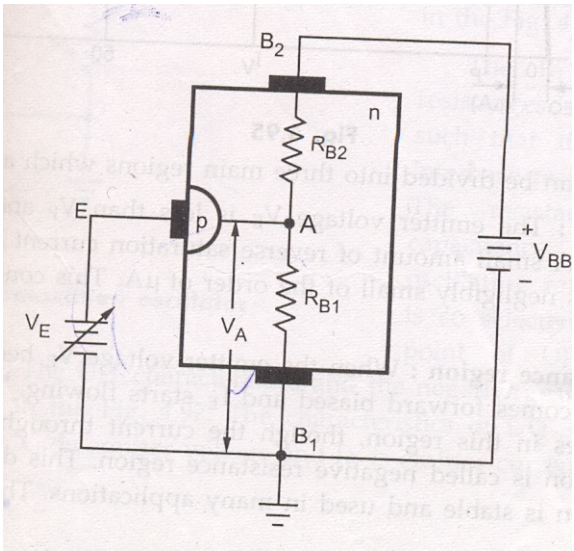
$V_{RB1}=\left(\frac{RB1}{RB1+RB2}\right) V_{BB} = \eta.V_{BB}$ When I_e=0

η = Intrinsic stand off ratio = $\left(\frac{RB1}{RB1+RB2}\right)$ when Ie=0

$\eta = \left(\frac{RB1}{RBB}\right)$ when I_e=0

The value of η is from 0.5 to 0.8 the voltage V_{rb1} is called intrinsic stand off voltage, because it keeps the emitter diode reverse biased for all emitter voltages less than V_{rb1}.

Operation



1.The supply V_{bb} is applied between B_2 and B_1 .

2. Variable emitter voltage V_e is applied across the emitter terminals.

3. If V_e is varied , potential of A is decided by η and is equal to ηV_{bb}

$$V_a = V_{rb1} = \eta V_{bb}$$

Case 1: If $V_e < V_a$

As long as $V_e < V_a$, the pn junction is reverse biased. Hence emitter current I_e will not flow. Thus UJT is said to be off.

Case 2: if $V_e > V_p$

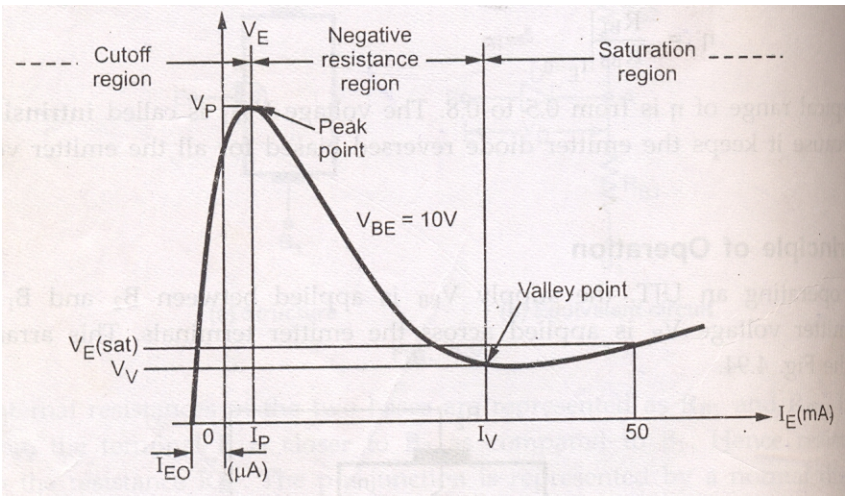
The diode drop V_d is generally between 0.3 to 0.7v.

We can write $V_p = V_a + V_d = \eta V_{bb} + V_d$

When V_e becomes equal to or greater than V_p the pn junction becomes forward biased and current I_e flows. Thus UJT is said to be ON.

VI Characteristics

1.The graph of I_e against emitter voltage plotted for a particular value of V_{bb} is called the characteristics of UJT.



The characteristics can be divided in to three main regions.

1.cut off 2. Negative resistance region 3. Saturation region.

1.cut off: The $V_e < V_p$ and the pn junction is reverse biased . A small amount of reverse saturation current I_{e0} flows through the device which is negligibly small of the order of micro amps. This condition remains till the peak point.

2. Negative resistance region: When emitter voltage V_e becomes equal to V_p then p n junction becomes forward biased and I_e starts flowing. The voltage across the device decreases in this region though the current through the device increases. Hence the region is called negative resistance region. This decreases the resistance R_{b1}. This region is stable and used in many applications. This region continues till valley point.

3. Saturation region: The region to the right of the valley point is called saturation region. In the valley point, the resistance changes from negative to positive. The resistance remains positive in the saturation region.

As V_{bb} increases , the potential V_p corresponding to peak point will increase.

Applications of UJT

The UJT is mainly used in the triggering of other devices such as SCR. It is also used in the sawtooth wave generators and some timing circuits. The most popular application of UJT is as a relaxation oscillator to obtain short pulses for triggering of SCRs.

The relaxation oscillator using UJT which is ment for generating sawtooth waveform. It consists of a UJT and a capacitor , which is charged through emitter resistor as the supply voltage V_{bb} is switched 0N.