Politecnico di Torino

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Prof. G. Masera

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4 - "HELLO" FSM

In this section a circuit that scrolls the word "HELLO" over the display has been implemented. The image below shows the architecture of the circuit generated using a VHDL description:

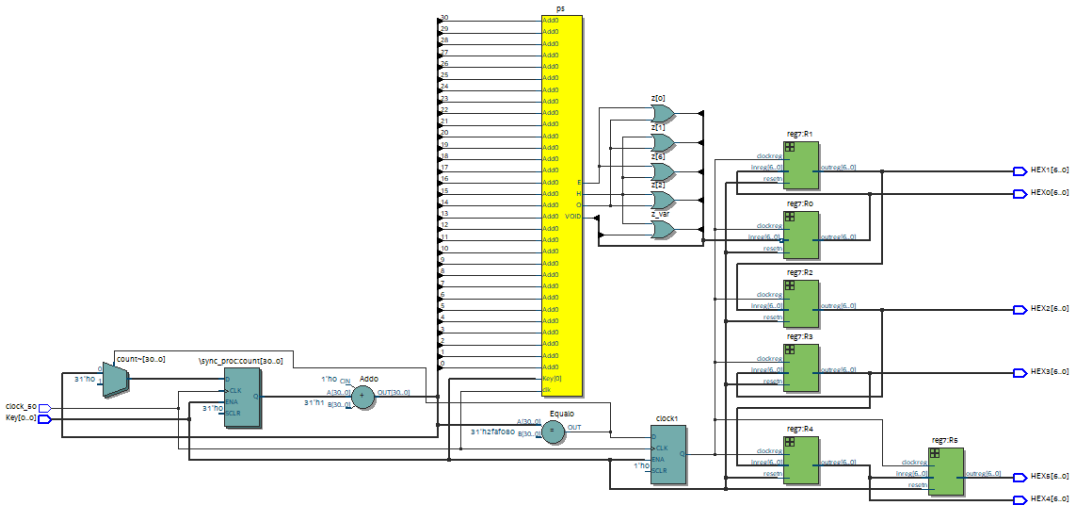

Figure 1: Implemented architecture

The circuit uses six 7-bit registers connected in a pipeline fashion. Each of them directly drives a 7-segment display.

The FSM controls the pipeline by inserting the characters (H,E,L,L,O) into the first 7-bit register. Every second the letters scroll from right to left, once the cycle is completed (i.e. The 'O' letter reach the leftmost display) the FSM starts the process again in an infinite loop. The state diagram of the implemented FSM is shown below:

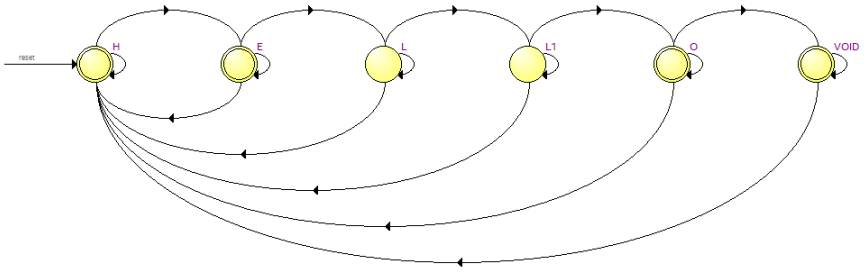

Figure 2: State Diagram

The 6 7-bit resisters have been implemented using a behavioral approach. The testbench shown below has been performed to check their functionalities:

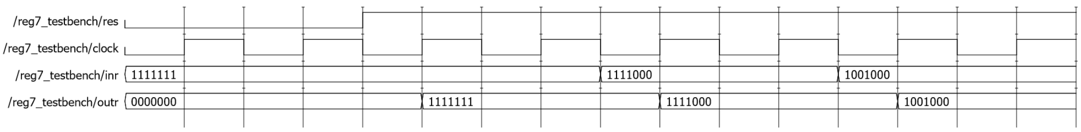

Figure 3: 7-bit register testbench

Finally a testbench for the entire design has also been implemented, showing the correct behavior of the circuit.

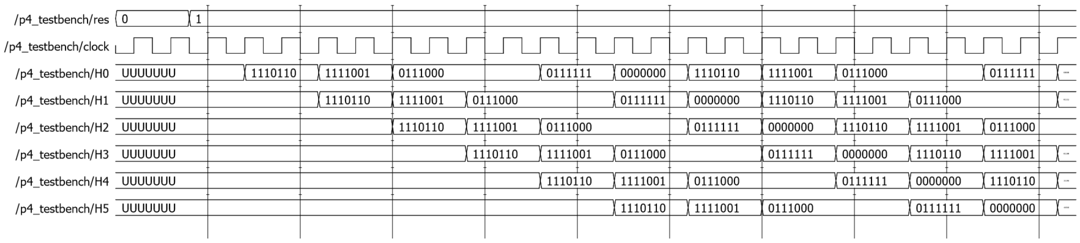

Figure 4: "HELLO" FSM testbench

Note that to keep the simulation fast enough the letter scrolls every 2 clock cycles.