Politecnico di Torino

Digital systems electronics
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Lab 04

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1 Gated SR latch

The circuit shown in *figure* 1 implements a gated SR latch. Once coded into VHDL the Quartus Prime compiler uses separate memory components as shown in *figure* 2 to depict the electric circuit.

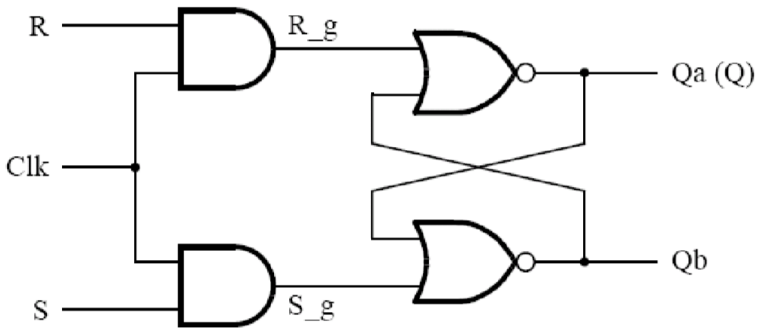

Figure 1: A gated SR latch circuit

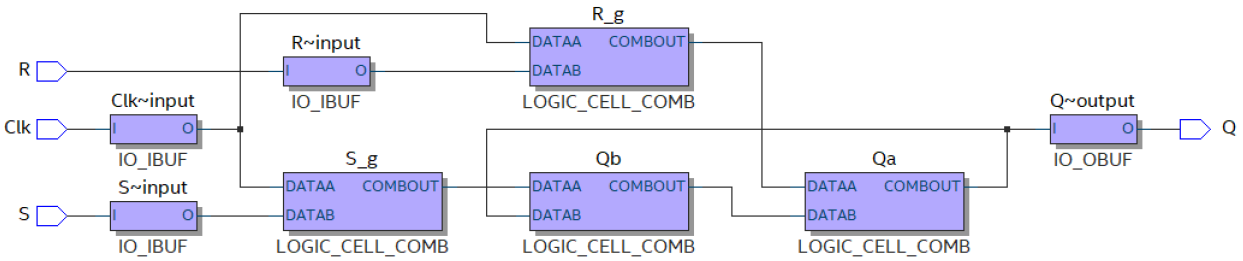

Figure 2: Quartus circuit implementation

Finally, a testbench has been written to test the behavior of the circuit, according to the table shown below:

Clk	S	R	Q(*t* + 1)
0	x	x	Q(*t*) (no change)
1	0	0	Q(*t*) (no change)
1	0	1	0
1	1	0	1
1	1	1	x

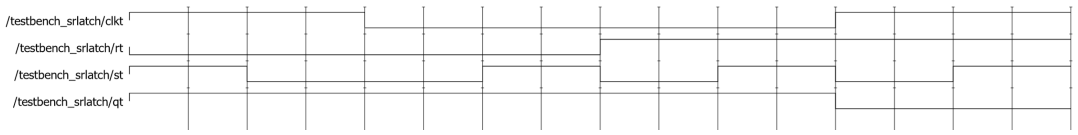

Figure 3: Modelsim Testbench waves

The testbench results are shown by means of the simulated waves shown in *figure* 3. Initially $CLK = 1$, the lath is enabled. For $S = 1$, $R = 0$ the set condition is triggered and $Q = 1$. Viceversa $Q = 0$ when $S = 0$, $R = 1$, in reset condition. Once $CLK = 0$ the latch is disabled entering in the memory condition as $S = 0$, $R = 0$. In the other hand for $S = 1$, $R = 1$ the latch behavior becomes unpredictable.

2 16-bit synchronous counter

The circuit in *figure* 4 implements a 4-bit counter using T flip flops. A 16-bit version has been implemented using the same structure. Using the Quartus tools the maximum working frequency has been identified to be equal to $F = 374.53MHz$ as reported in *figure* 5 using a total of 31 LEs.

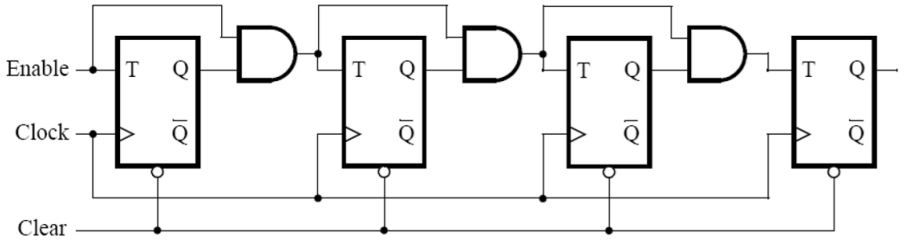

Figure 4: 4-bit counter

Fmax	Restricted Fmax	Clock Name
374.53 MHz	374.53 MHz	KEY0

Figure 5: Maximum working frequency

Finally a testbench had been designed to check the functionality of the circuit, the results are shown in *figure* 6 where the counting process is shown using the HEX display. Notice that the circuit is firstly initialized resetting the current state of every FF. Then the counting process has been started enabling the circuit and applying a clock to every FF.

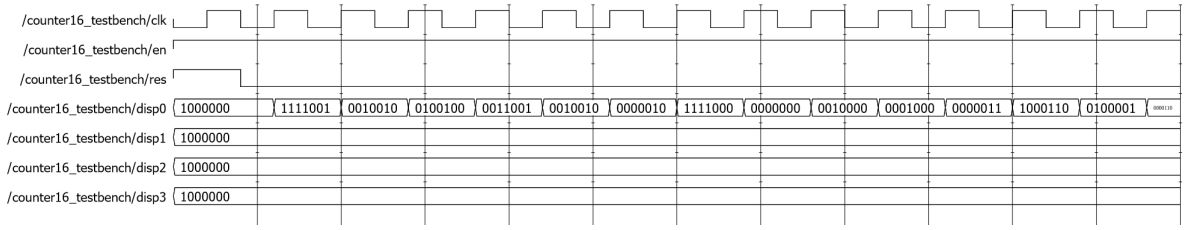

Figure 6: Modelsim Testbench waves