Politecnico di Torino

Digital systems electronics
A.A. 2018/2019

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Lab 06

14 may 2019

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Introduction to the assigned problem

This relation deals with the design of a simple digital filter. From the given functional specifications, a final digital circuit has been implemented in VHDL including memories, control unit and data-path.
The design process will be analyzed using a bottom-up approach, starting from the individual components and their interconnections to the final custom designed FSM.

Overall specs description

As already mentioned, the final purpose of this activity is to implement a digital filter following the relation:

$$Y(n) = -0.5X(n) - 2X(n-1) + 4X(n-2) + 0.25X(n-3)$$

where $X(n)$ are the input stream data and $Y(n)$ the corresponding filtered data generated by the top equation.

The circuit starts by means of a $START$ signal which enable a loading process of the input data into a 1 kByte memory. Then, the circuit automatically filters the data stream exploiting the equation already provided and loads the output filtered data into a second memory. Finally, the circuit reports end of process asserting an $HIGH$ logical value to the $DONE$ signal and awaits until the next $START$.

Shift registers

Memories

Adder

Counter