



POLITECNICO DI TORINO

DIGITAL SYSTEMS ELECTRONICS
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PROF. G. MASERA

Lab 05

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1 One-Hot Finite state machine

The FSM from the STG diagram given in *figure 1* was implemented using a One-Hot state assignment shown in *figure 2* with the circuit shown in *figure 3*.

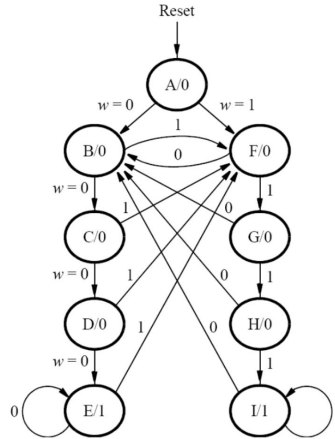


Figure 1: State diagram of the FSM

Name	State Code
	$y_8y_7y_6y_5y_4y_3y_2y_1y_0$
A	000000001
B	000000010
C	000000100
D	000001000
E	000010000
F	000100000
G	001000000
H	010000000
I	100000000

Figure 2: One-Hot code

The correct behavior of the circuit has been verified by means of a testbench. The result of the simulation are shown in *figure 4*.

2 Modified One-Hot FSM

In this section we had to implement the same FSM of the previous section, but with another One-Hot code shown in *figure 5*. The value of this state encoding is that the reset state is coded as 000000000. This excludes the need of a set port for the

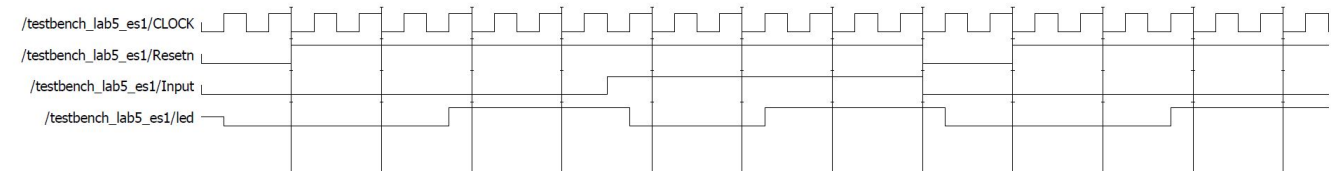


Figure 3: One-Hot code

Flip Flops in the circuit that now have only a reset port.
The Circuit that implements this FSM with this state encoding is shown in *figure 6* and is very similar to the one of the previous section. An inverter at the output of the y_0 Flip Flop was added while all the other connections are unchanged.

Name	State Code
	$y_8y_7y_6y_5y_4y_3y_2y_1y_0$
A	000000000
B	000000011
C	000000101
D	000001001
E	000010001
F	000100001
G	001000001
H	010000001
I	100000001

Figure 4: Modified One-Hot code

4 - “HELLO” FSM

In this section a circuit that scrolls the word "HELLO" over the display has been implemented. The image below shows the architecture of the circuit generated using a VHDL description:

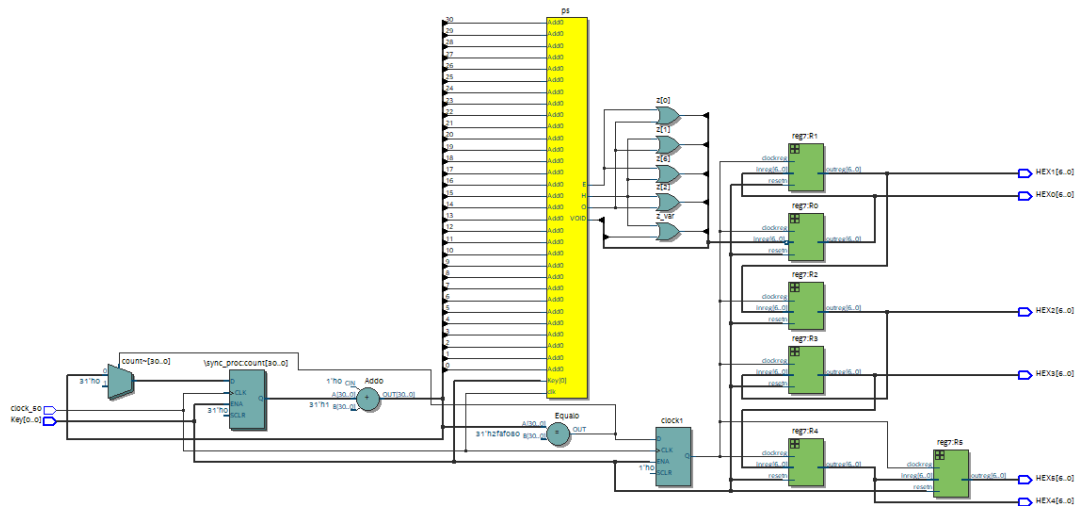


Figure 5: Implemented architecture

The circuit uses six 7-bit registers connected in a pipeline fashion. Each of them directly drives a 7-segment display.

The FSM controls the pipeline by inserting the characters (H,E,L,L,O) into the first 7-bit register. Every second the letters scroll from right to left, once the cycle is completed (i.e. The 'O' letter reach the leftmost display) the FSM starts the process again in an infinite loop. The state diagram of the implemented FSM is shown below:

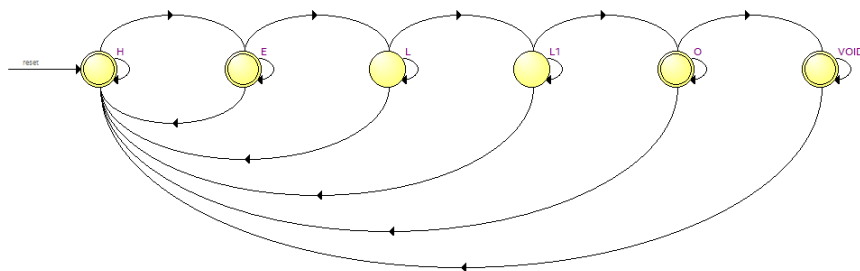


Figure 6: State Diagram

The 6 7-bit registers have been implemented using a behavioral approach. The testbench shown below has been performed to check their functionalities:

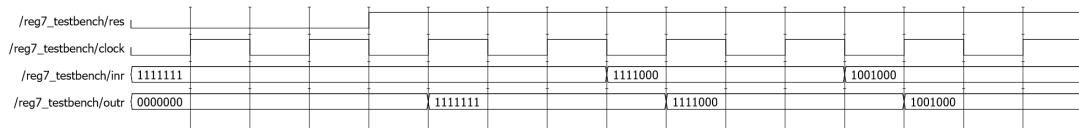


Figure 7: 7-bit register testbench

Finally a testbench for the entire design has also been implemented, showing the correct behavior of the circuit.

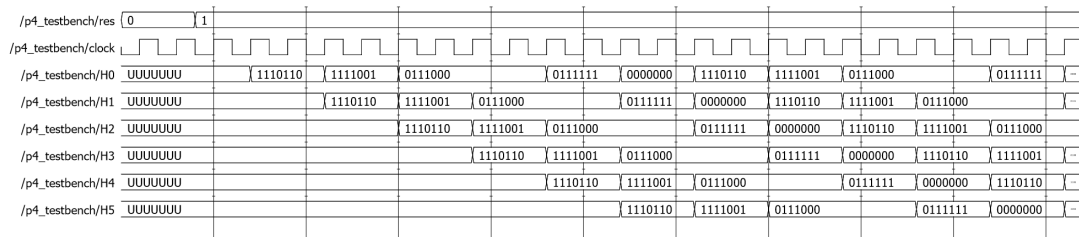


Figure 8: "HELLO" FSM testbench

Note that to keep the simulation fast enough the letter scrolls every 2 clock cycles.