Politecnico di Torino

Digital systems electronics
A.A. 2018/2019

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Lab 02

24 Mar 2019

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1 Controlling a 7-segments display

Figure 1 shows a 7-segment decoder module whose input bits $C2C1C0$ drive a 7 segment display through the bits $HEX0_0 -> HEX0_6$

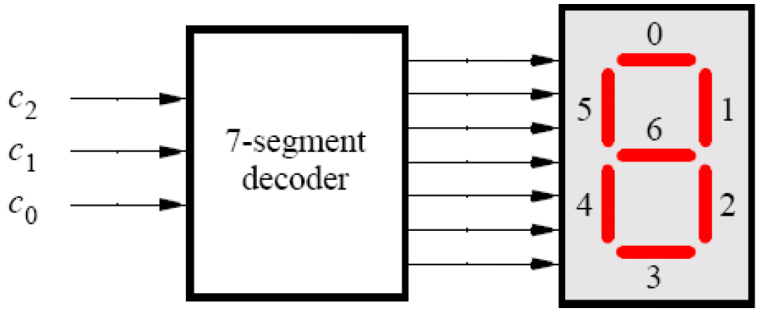

Figure 1: 7-segment decoder + display

Figure 2 shows the truth table to be implemented for the 7-segment decoder. As shown just the characters $HELO$ will be implemented. The sequent logical states can be easily derived from the table:

$$HEX6 = \overline{C2} \cdot \overline{C1}$$
$$HEX5 = \overline{C2}$$
$$HEX4 = \overline{C2}$$
$$HEX3 = \overline{C2} \cdot (C0 + C1)$$
$$HEX2 = \overline{C2} \cdot \overline{C1} \cdot \overline{C0} + \cdot\overline{C2} \cdot C1 \cdot C0$$
$$HEX1 = \overline{C2} \cdot \overline{C1} \cdot \overline{C0} + \cdot\overline{C2} \cdot C1 \cdot C0$$
$$HEX0 = \overline{C2} \cdot C0$$

C2	C1	C0	HEX6	HEX5	HEX4	HEX3	HEX2	HEX1	HEX0
0	0	0	1	1	1	0	1	1	0
0	0	1	1	1	1	1	0	0	1
0	1	0	0	1	1	1	0	0	0
0	1	1	0	1	1	1	1	1	1
1	X	X	0	0	0	0	0	0	0

Figure 2: decoder truth table

Finally the logic states are implemented using gates as shown in $figure3$.
The circuit is then described into VHDL using a dataflow style approach, the VHDL file is called *puntoA.vhd*.

The VHDL entry has been finally simulated via *testbenchapproach* where every possible input combination has been considered validating the output. The testbench results are shown below in figure 4.

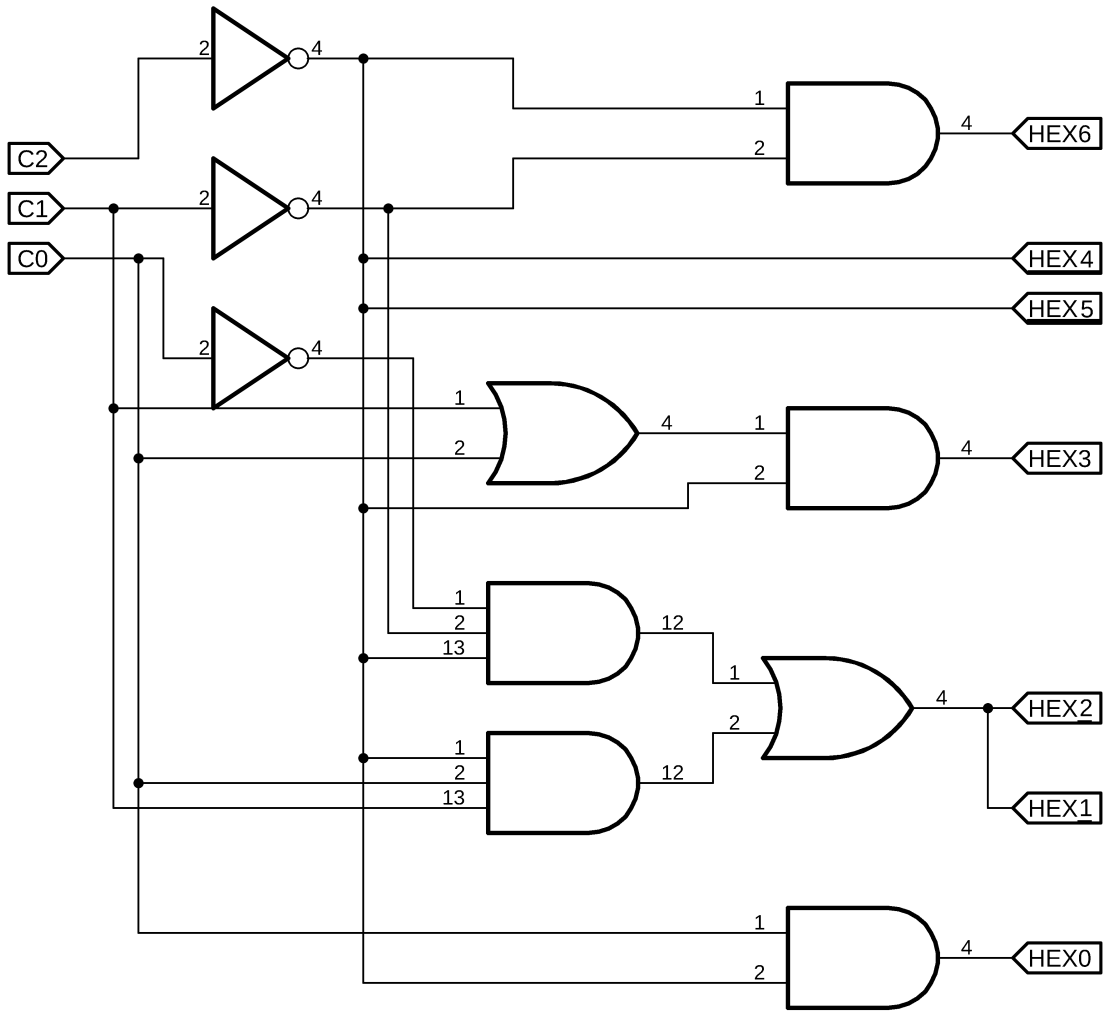

Figure 3: decoder gates implementation

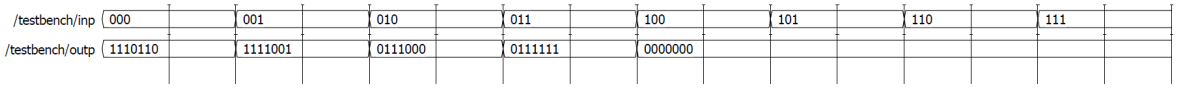

Figure 4: Testbench results

2 Multiplexing the 7-segments display output

Figure 5 shows.....

explanation

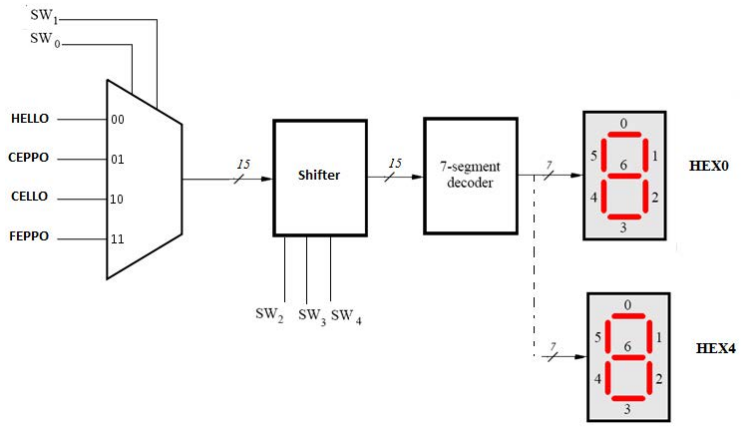

Figure 5: multiplexer + shifter + 7-segment decoder + display

3 Binary to Decimal converter

punto 3

4 Binary-to-BCD Converter

punto 4