



POLITECNICO DI TORINO

DIGITAL SYSTEMS ELECTRONICS  
A.A. 2018/2019

PROF. G. MASERA

---

## Lab 09

04 june 2019

---

Berchialla Luca	236032
Laurasi Gjergji	238259
Mattei Andrea	233755
Lombardo Domenico Maria	233959
Wylezek Karolina	267219

## Output compare VS Reload

In the following report the Output Compare register and/or auto-reload register can be calculated from the desired asserted flag frequency using the following formula:

$$F_X = \frac{F_{CLK}}{(OC + 1) \cdot (ARR + 1)} \quad (1)$$

Notice that to correctly generate a square wave with a desired frequency  $F_X$  exploiting the OC or ARR approach, the formula 1 should also be divided by a 2 factor.

### 1 - Interrupt-based variable frequency square wave-form generator

In the following section a variable frequency square wave has been implemented exploiting the interrupt approach.

$$\text{delta1} = (OC_{max1} - OC_{min1}) * \text{lettura}/ADC_{max} + OC_{min1};$$

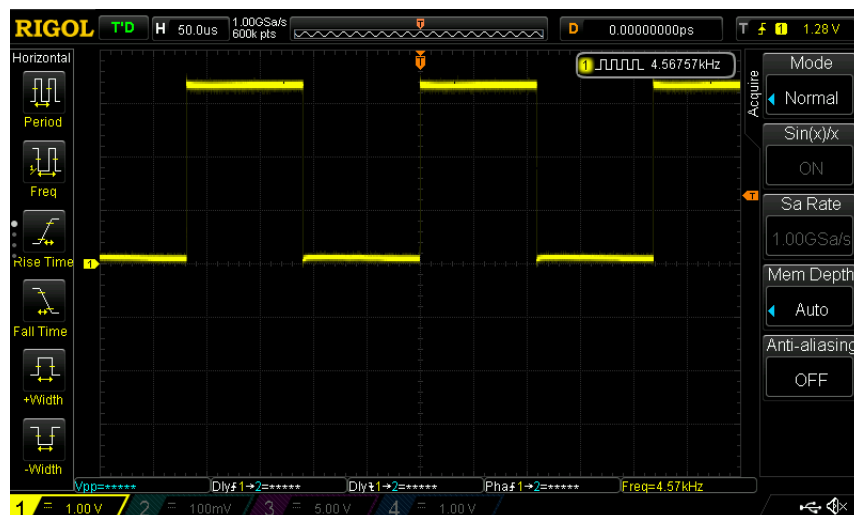


Figure 1:

sono molto più stabili no jitter senza systick, piccolo jitter con systick

## 2.1

image 12 -13 -11

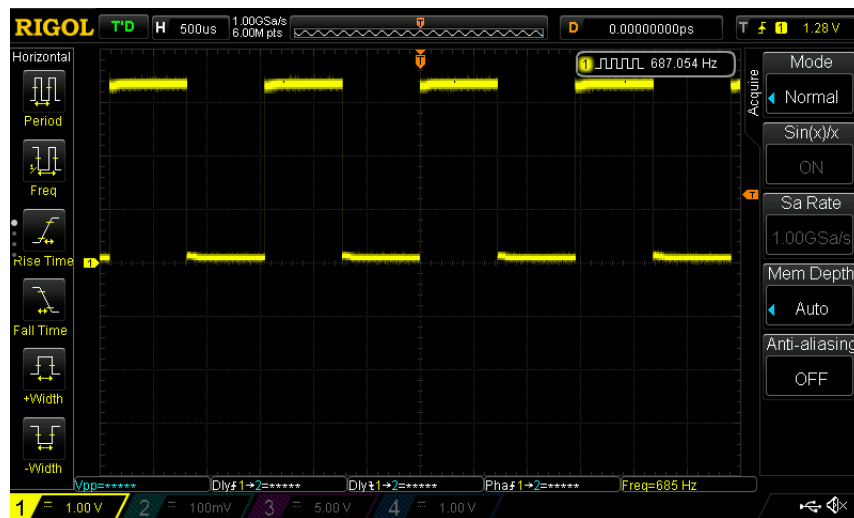


Figure 2:

## 2.2

il jitter non è apprezzabile perche l'isr è corta???

## 2.3

image 14 min image 15 max