Nikhil N. Gohil

Contact Information

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Education

University of Cincinnati, Cincinnati, Ohio USA — Advisor: Dr. Ranga Vemuri
***M.S.**, Electrical Engineering(GPA: 3.83)* — Graduated: November 2017

Priyadarshini Institute of Engineering and Technology, Nagpur, Maharashtra India
***B.E.**, Electronics and Communication Engineering* — June 2010

Professional Experience

Intel Corporation, Folsom, California USA
***Design Automation Intern** - Power Estimation and Optimization* — Nov 2015 - Apr 2016

- ➔ Improved deployment time of the tool PowerArtist across the design team by validating new versions and maintaining the perl wrapper
- ➔ Improved design flow by writing scripts to mine relevant data from tool logs
- ➔ Helped front-end design team by analyzing power differences between front-end and back-end power numbers

Relevant Coursework

- Physical VLSI Design
- VLSI Design Automation
- Low Power VLSI Design
- Computer Architecture
- VLSI Testing and Validation
- Digital Circuits (*Undergraduate Course*)

Research Topic

Design of DPA-Resistant Integrated Circuits

- ➔ Tested resistance of different flip-flop configurations to differential power analysis (DPA) attacks
- ➔ Created a design flow to implement DPA-resistant circuits using a custom combinational cell library and different flip-flop configurations.

Skills

- **Languages:** Perl, Verilog, Unix shell scripts, C++.
- **Tools:** Synopsys Design Tools (*Design Compiler, IC Compiler, Custom Designer, Nanosim, HSPICE, Hercules*), Magic Layout Editor, IRSIM, Modelsim, Matlab.

Projects Undertaken

Implementation of a Channel Routing Algorithm
A C++ Implementation of the Left-Edge algorithm (with dogleg-routing) for channel routing given a netlist of connections.

Implementation of Graph Partitioning Heuristic
A C++ Implementation of the Kernighan-Lin Heuristic to partition a graph with minimum cost (interconnections between the split partitions), given a netlist of connections.

Power analysis using Synopsys utilities
Used Design Compiler and Power Compiler to analyze circuit power consumption. Further, used clock gating and Multi-voltage Design (Static Voltage Scaling) for power reduction.

Scan Chain Insertion
Inserted an internal scan chain into a given design(*booth multiplier*). Used Synopsys DFT compiler for scan chain insertion and generated test patterns using Tetramax ATPG.

Design of a 10x10 interconnect network IC
Used the layout tool MAGIC to design a custom bit-sliced 10x10 interconnect network inside a padframe. The IC was fabricated.