EE1 Project 2021 – Circuit Simulator File Format

Your circuit simulator should read an input file that defines the circuit and the simulation. The format of the input file is compatible with SPICE, but you only need to support a subset of the features of SPICE, which are described in this document.

Components

The netlist is described by lines defining the type, designator (name), nodes and value of each component

Designator letter	Component	Node order	Value
V	Independent Voltage source	+, -	Voltage (V) or function
I	Current source	In, out	Current (A) or function
R	Resistor	Doesn't matter	Resistance (Ω)
C	Capacitor	Doesn't matter	Capacitance (F)
L	Inductor	Doesn't matter	Inductance (H)
D	Diode	Anode, Cathode	Model name
Q	BJT	Collector, Base, Emitter	Model name
M	MOSFET	Drain, Gate, Source	Model name
G	Voltage-controlled Current Source	+, -, Control +, Control -	Transconductance (S)

The format of each line is:

```
<designator> <node0> <node1> [<node 2> [<node 3>]] <value>
```

Designator

The designator field contains a letter and a number. The letter specifies the type of component (see table above) and the number is added to make a unique identifier for each component

Node list

A list of two to four node names occurs after the designator. Node names have the format `N123`. The component is connected to these nodes in the order given in the table above. The reference (ground) node is named `0`

Value

The value is the component value in the units given in the table above. Numbers can be followed by a multiplier:

Multiplier	Value
p	$\times 10^{-12}$
n	$\times 10^{-9}$
u	$\times 10^{-6}$
m	$\times 10^{-3}$
k	$\times 10^{3}$
Meg	$\times 10^{6}$
G	$\times 10^{9}$

Independent voltage and current sources can have a DC value, or a function. The only function required is an AC source written in the form:

```
AC <amplitude> <phase>
```

AC amplitude has units of Volts or Amps. Phase has units of degrees. Frequency isn't specified because the AC analysis will sweep through a range of frequencies.

Diodes and transistors are given a model name instead of a value. The following models should be defined internally in your software:

Model name	Type
D	Silicon diode
NPN	NPN BJT
PNP	PNP BJT
NMOS	N-channel MOSFET
PMOS	P-channel MOSFET

Simulation settings

The AC analysis simulation is described with a line of the form:

```
.ac dec <points per decade> <start frequency> <stop frequency>
```

The frequency sweep is evaluated between the start frequency and the stop frequency. The interval between frequencies specified in frequencies per decade. That means the frequency of step n is given by: $f_n = 10^{n/n_p} f_s$, where n_p is the number of points per decade and f_s is the start frequency

End of file

The file ends with the line:

```
.end
```

Comments

The input file may contain comments on lines beginning with *

These lines should be ignored.

Extensions to the specification

You can extend the file format if necessary to support any additional features you have added. Maintain compatibility with SPICE if possible.

Example

```
* A test circuit to demonstrate SPICE syntax
V1 N003 0 AC(1 0)
R1 N001 N003 1k
C1 N001 0 1µ
I1 0 N004 0.1
D1 N004 N002 D
L1 N002 N001 1m
R2 N002 N001 1Meg
Q1 N003 N001 0 NPN
.ac dec 10 10 100k
.end
```

You can generate your own examples by drawing a circuit in the LTspice software and choosing the option View → SPICE Netlist. LTspice includes some additional lines which aren't required for your

simulator. You may wish to configure your simulator to ignore these lines so you can produce test circuits directly from LTspice.