ISTE NITK

1) **Name of Project-**
Design and Implementation of 64-point Fast Fourier Transform Chip for OFDM

2) **Tags Related to Project**- VLSI, FPGA FFT, Verilog, VHDL

3) **Members of the Project**- Rahul , Madhunala Nikhil

4) Project Summary(50 words)-

Our aim is to build a 64-point FFT architecture using two 8-point FFT blocks that can fulfill the requirement for Wireless LAN 802.11a where each FFT/IFFT operation must be completed under 4-80µs. In this the chip is manufactured using 0.25µm BiCMOS technology and has area of 6.8mm2 and average dynamic power consumption of 41mW at 20MHz operating frequency at 1.8V supply voltage. It would be interesting to see how the performance, power, and area of this design when it is implemented using 45nm CMOS technology as we will do in our project.

5) **Project Description(200 words)-**

Fourth generation wireless and mobile systems are currently the focus of research and development. Broadband wireless systems based on orthogonal frequency division multiplexing (OFDM) will allow packet-based high-data-rate communication suitable for video transmission and mobile Internet applications. The IEEE 802.11a standard defines the principal functions and architecture of such a high-data-rate communication system. Apart from the high speed of operation, the system demands low power consumption since it is primarily aimed at portable and mobile applications. A general purpose DSP with associated software is not beneficial for this application since on average, the power consumption of a software solution is an order of magnitude higher compared to a functionally equivalent dedicated hardware solution. Considering this fact we proposed a datapath architecture

using dedicated hardware for the baseband processor of the above-mentioned standard. We also showed through extensive simulation that the most computationally intensive parts of such a high-data-rate system are the 64-point inverse fast Fourier transform (IFFT) in the transmit direction and the Viterbi decoder in the receive direction. Accordingly, an appropriate design methodology for constructing them has to be chosen. For a given functional specification, the main design concerns are:
1) how much silicon area is needed;
2) how easily the particular architecture can be made flat for implementation in VLSI (routability);
3) in actual implementation how many wire crossings and how many long wires carrying signals to remote parts of the design are necessary (interconnect delay)
4) how small the power consumption can be Extensive simulation of different algorithms and algorithmto-architecture mapping quality exploration is necessary to choose the best algorithm for a given specification.

Image related to the Project-