# ISTE NITK

# Design and Implementation of 64-point Fast Fourier Transform Chip for OFDM


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**Tags Related to Project**- FFT, Verilog, Modelsim

## 1) Project Summary(50 words)-


Our aim is to build a 64-point FFT (Fast Fourier Transform) architecture using two 8-point FFT blocks that can fulfill the requirement for Wireless LAN where each FFT/IFFT operation must be completed under less time.
This architecture consumes less silicon area and results in considerable reduction in cost. For computation of IFFT/FFT full parallel scheme is adopted there by making it very fast. Complex multiplication constant are calculated using shift and add operation there by reducing area and power consumption as compared to multiplier.


## 2) Project Description(200 words)-

Fast Fourier Transform (FFT) is an algorithm used to quickly calculate the Discrete Fourier Transform (DFT) of a sequence of digital samples. The DFT is a mathematical transformation that converts a sequence of time-domain samples into its frequency-domain representation.

In Digital communication, FFT is used in many applications such as modulation, demodulation, channel equalization, and spectrum analysis. One of the most important applications of FFT in digital communication is in Orthogonal Frequency Division Multiplexing (OFDM) systems.

Fourth and fifth generation wireless and mobile systems are currently the focus of research and development. Broadband wireless systems based on orthogonal frequency division multiplexing (OFDM) will allow packet- based high-data-rate communication suitable for video transmission and mobile Internet applications. The IEEE standard defines the principal functions and architecture of such a high-data-rate communication system. Apart from the high speed of operation, the system demands low power consumption since it is primarily aimed at portable and mobile applications. A general purpose DSP with associated software is not beneficial for this application since on average, the power consumption of a software solution is an order of magnitude higher compared to a functionally equivalent dedicated hardware solution.

## 3) Method For Fast Fourier Transform computation:

$$X(k)=\sum_{n=0}^{N-1}x(n)W_N^{nk},\ k=0,1,...,N-1$$

$$W_N=e^{-i2\pi/N}$$

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DFT with N point changes into the DFT with N/2.

$$X(k)=DFT_{N/2}\left\{x_{even}(m),k\right\}+W_N^{\,k}.DFT_{N/2}\left\{x_{odd}(m),k\right\}$$

$$W_N^{\,x+N/2}=W_N^{\,x}W_N^{\,N/2}$$

$$=W_N^{\,x}e^{-i\pi}=-W_N^{\,x}$$

DFT with N point changes into the DFT with N/2.

$$X(k)=DFT_{N/2}\left\{x_{even}(m),k\right\}+W_N^{\,k}.DFT_{N/2}\left\{x_{odd}(m),k\right\}$$

| | | |
|---|---|---|
| $W_N^0$ | 1 | $W_N^0$ |
| $W_N^1$ | $\frac{\sqrt{2}}{2}-j\frac{\sqrt{2}}{2}$ | $W_N^1$ |
| $W_N^2$ | $-j1$ | $W_N^2$ |
| $W_N^3$ | $-\frac{\sqrt{2}}{2}-j\frac{\sqrt{2}}{2}$ | $W_N^3$ |
| $W_N^4$ | $-1$ | $-W_N^0$ |
| $W_N^5$ | $-\frac{\sqrt{2}}{2}+j\frac{\sqrt{2}}{2}$ | $-W_N^1$ |
| $W_N^6$ | $j1$ | $-W_N^2$ |
| $W_N^7$ | $\frac{\sqrt{2}}{2}+j\frac{\sqrt{2}}{2}$ | $-W_N^3$ |

Fig1. Twiddle factor for 8 point FFT

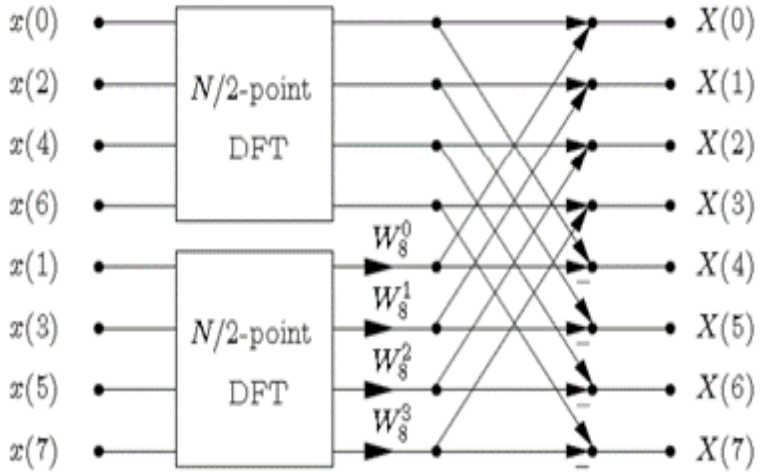



Fig2. 8-point DFT graph for calculation of two DFT with N/2 points.

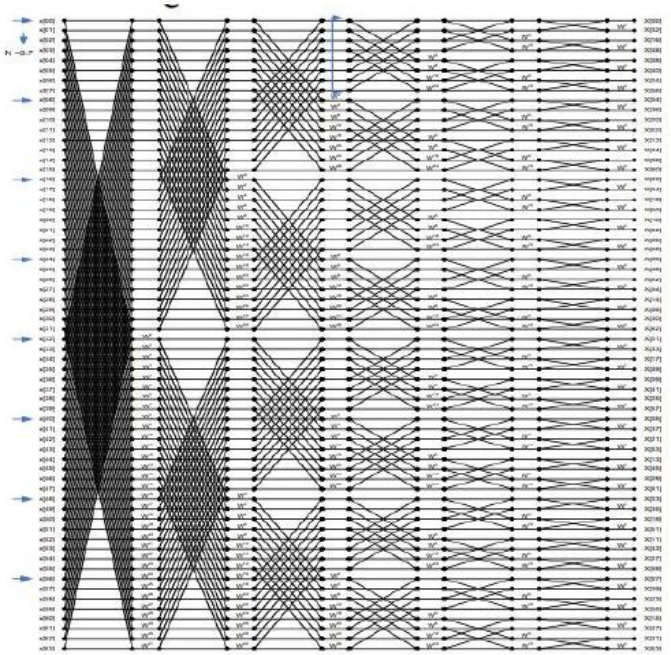
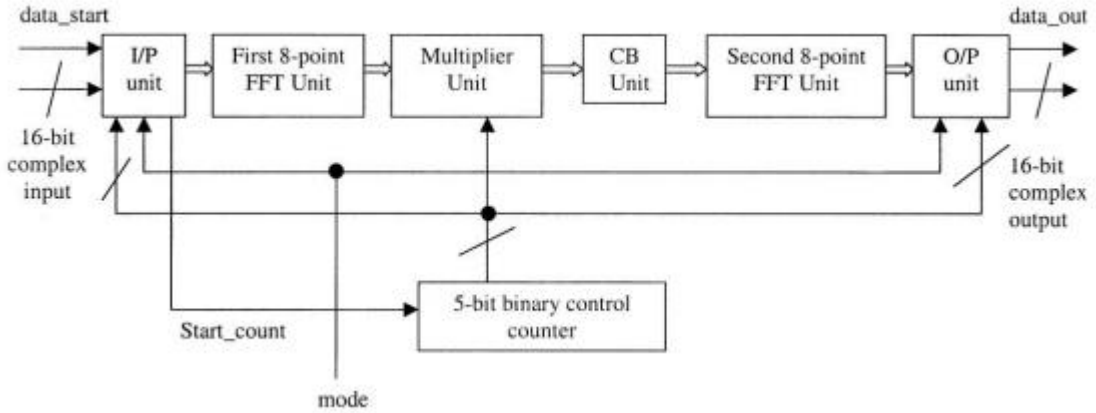


Fig3. The completely decomposed 64-point DFT graph

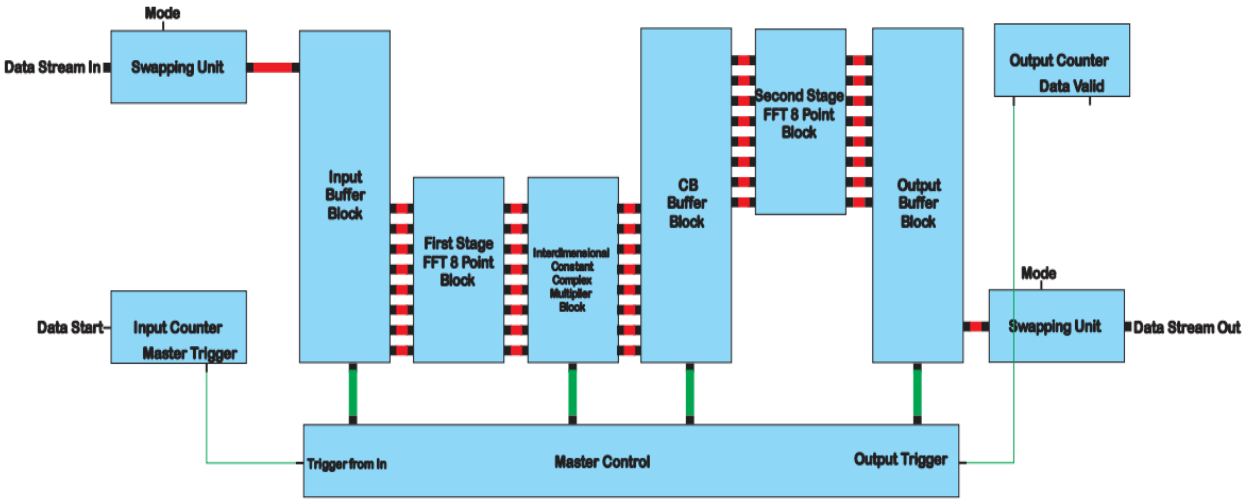
## Circuit Architecture:

It consists of an input unit (I/P unit), two 8-point FFT units, a multiplier unit, an internal storage register bank (CB unit), an output unit (O/P unit), and a 5-bit binary counter that acts as the master controller for the entire architecture.

## Block Diagram:

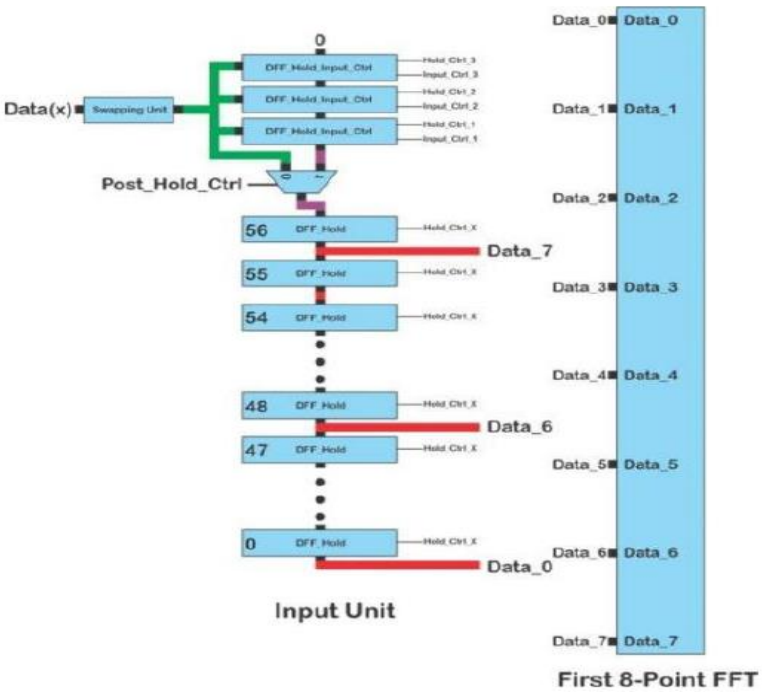


## Chip Architecture:

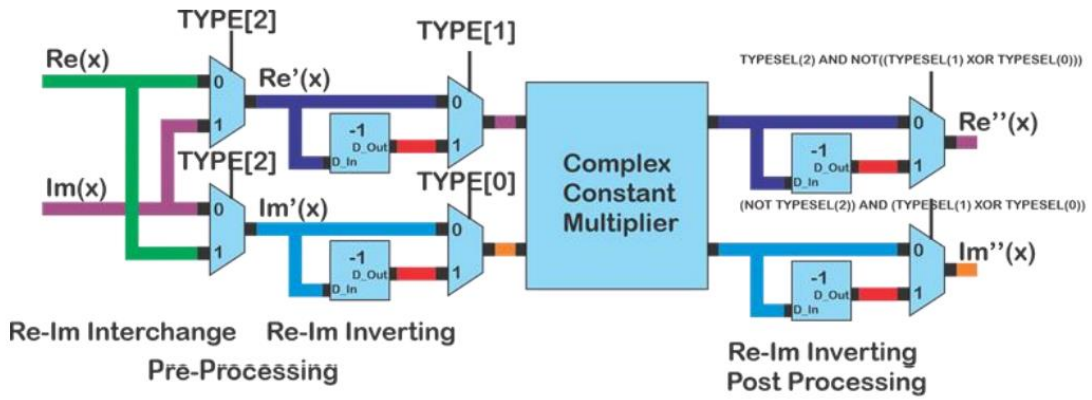



## Block diagram of each module :

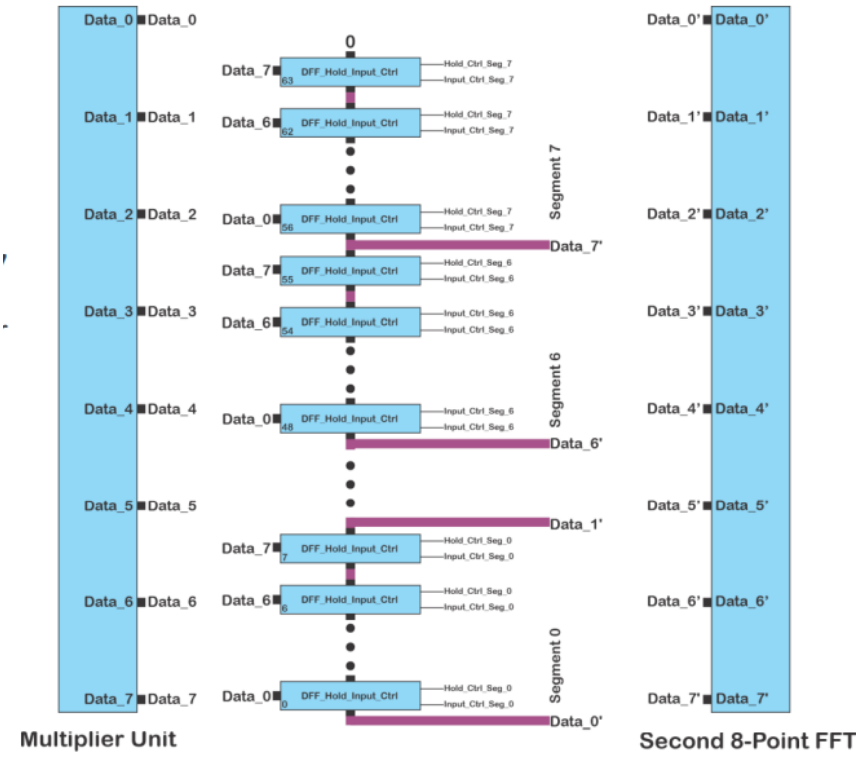
## 1. Input circuit:



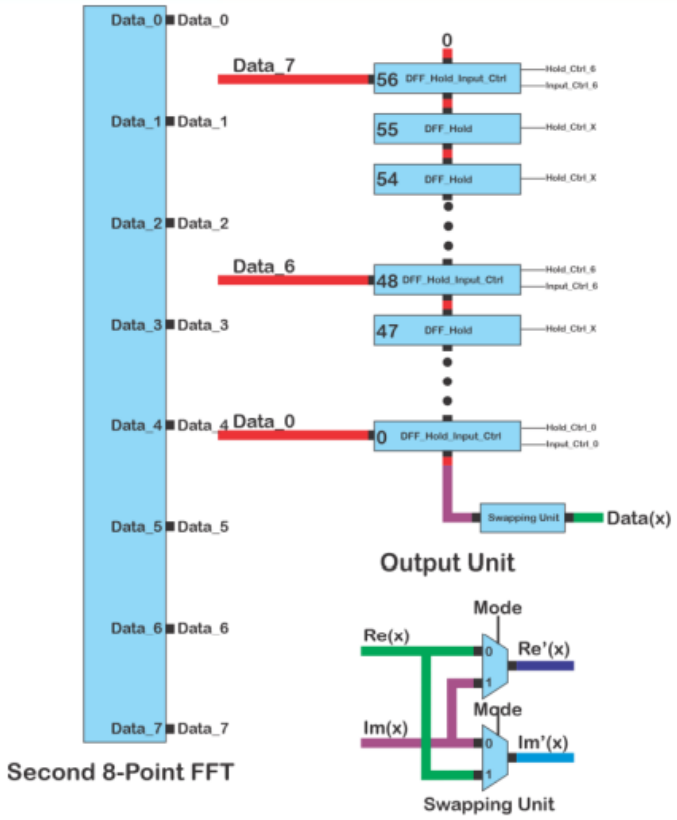

## 2. Multiplier Unit



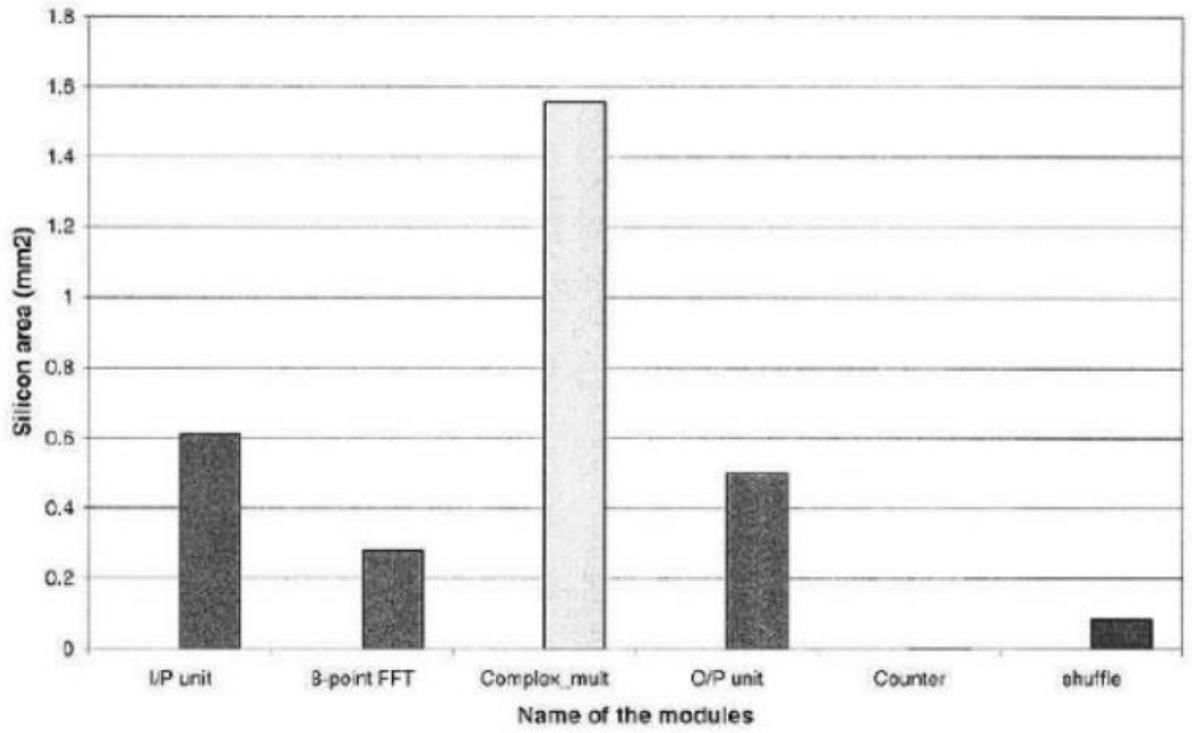
## 3. Storage Registers (CB)




## 4. Output unit:



**Silicon area consumption for each above modules.**




## Simulation results:


Fig11. Matlab Simulation: 8 point FFT output

| | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| 1 | '20612061' | 'FFCD0031' | 'FF4BFFAF' | 'FEC7FF2B' |
| 2 | '09200A8B' | 'FF1F00D5' | 'FEA2005A' | 'FE16FFD4' |
| 3 | '042C063C' | 'FF7A01A5' | 'FF02012E' | 'FE7200A2' |
| 4 | '03550491' | '005C018F' | 'FFEC011D' | 'FF560082' |
| 5 | '02D102E0' | '00A700A5' | '00380035' | 'FF9DFF8D' |
| 6 | '01A801B7' | 'FFEFFFFB' | 'FF7CFF89' | 'FEC7FECD' |
| 7 | '007401B4' | 'FF0A0055' | 'FE9DFFEA' | 'FDCDFF1F' |
| 8 | '003C0263' | 'FF0D013E' | 'FEA200D3' | 'FDBDFFF8' |
| 9 | '00E50287' | 'FFE9018C' | 'FF81011F' | 'FE810022' |
| 10 | '016301B7' | '008100D0' | '001A0063' | 'FEF6FF34' |
| 11 | '00E000BE' | '0016FFF0' | 'FFAAFF82' | 'FE55FE20' |
| 12 | 'FFDA00AB' | 'FF20FFF3' | 'FEADFF84' | 'FCF2FDC9' |
| 13 | 'FF710174' | 'FEC500CE' | 'FE550061' | 'FC19FE36' |
| 14 | '000A0202' | 'FF70016B' | 'FF0000F8' | 'FC01FE05' |
| 15 | '00D2018F' | '00460101' | 'FFD60089' | 'FB39FBD4' |
| 16 | '00BD0094' | '00320007' | 'FFBAFF88' | 'F603F588' |

Fig12. Matlab Simulation: 64 point FFT output

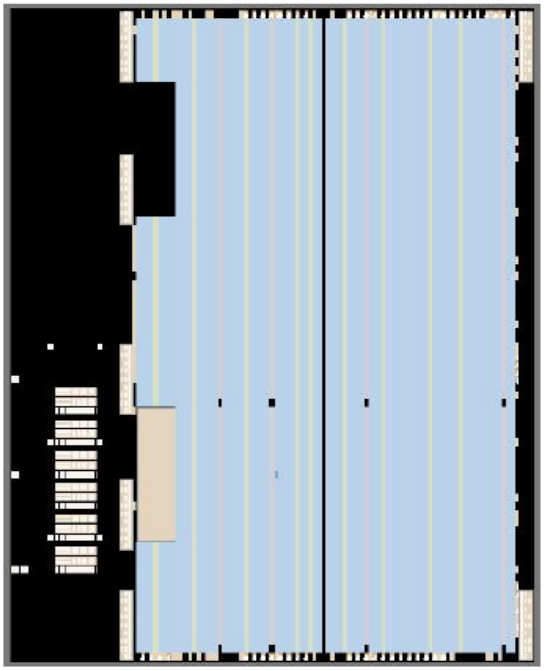


Fig13. Die photograph of the fabricated 64-point FFT/IFFT processor

**Pin Diagram of Cyclone V – 5CGXFC7C7F23C8 :**

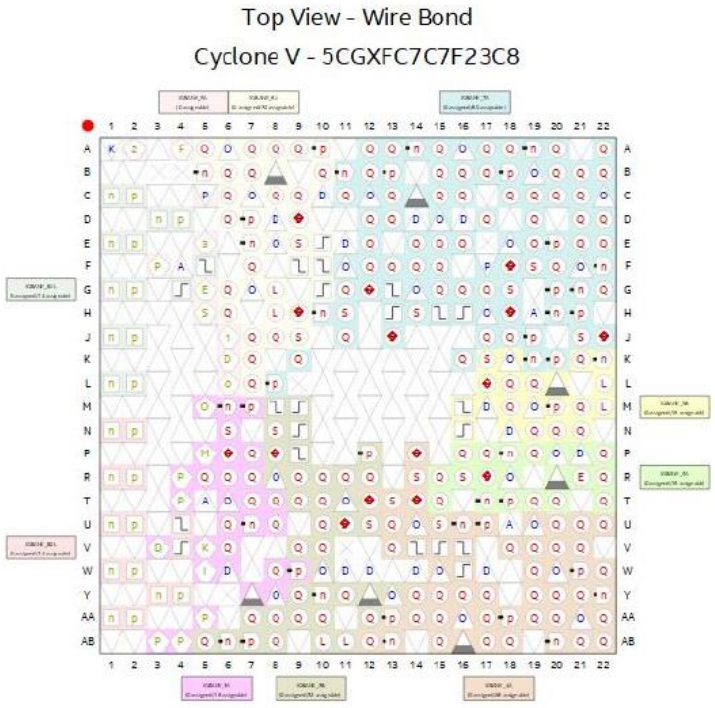
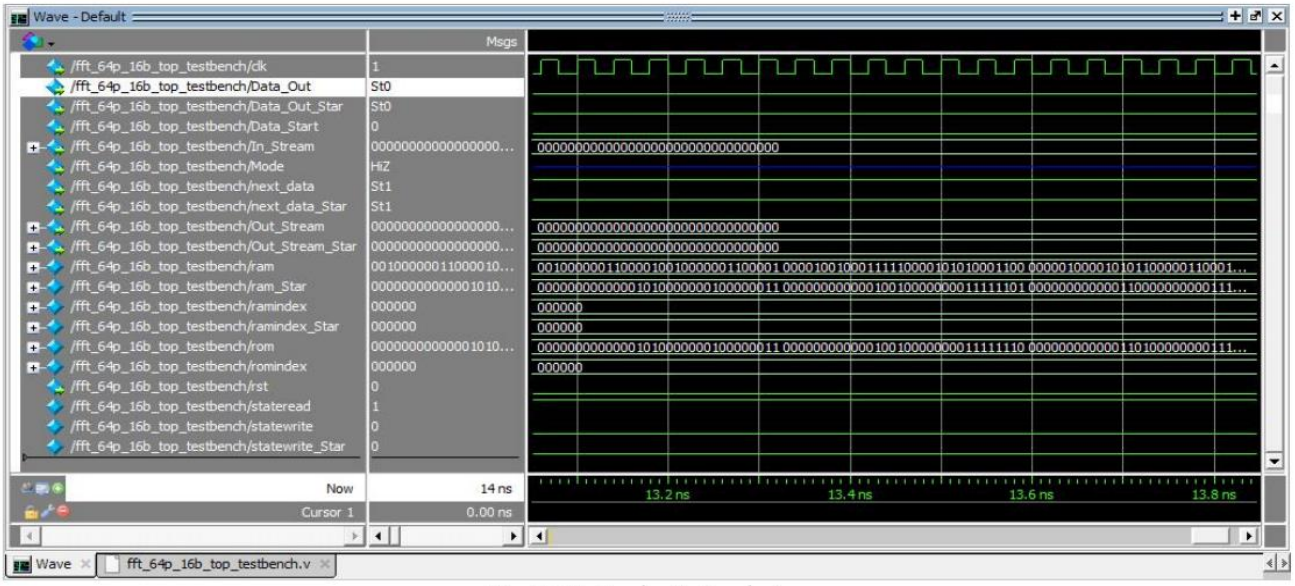



Fig14. 77 I/O pins where 8 pins are power supply pins

## RTL Synthesis Simulation:




## Conclusion:

Proposed method describes a novel 64-point IFFT/FFT architecture to be used in high speed WLAN system based on OFDM transmission.
This architecture consumes less silicon area and results in considerable reduction in cost. Number of non-trivial complex multiplication are 49 that is 26% less than required by radix-2 64 point FFT.
For computation of IFFT/FFT full parallel scheme is adopted there by making it very fast.