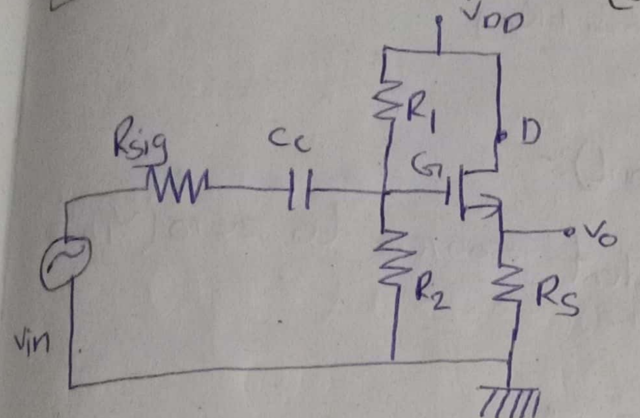
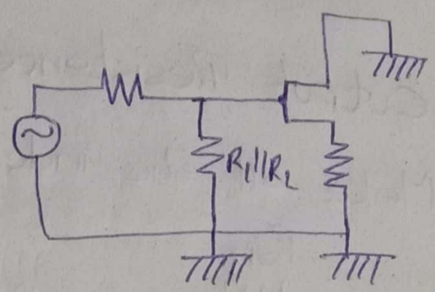
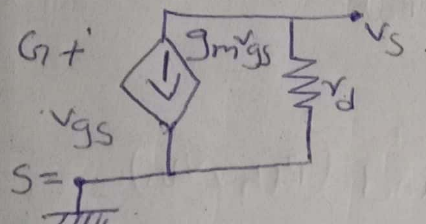
Common Drain Amplifier (Source Follower)

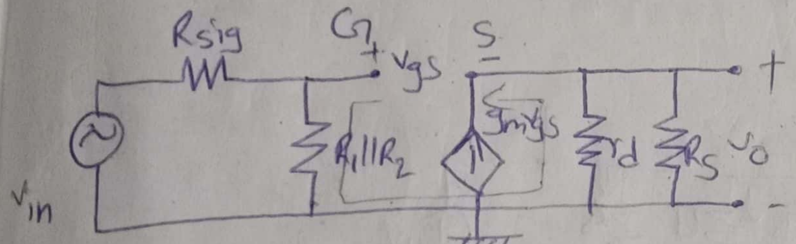


$\Rightarrow$

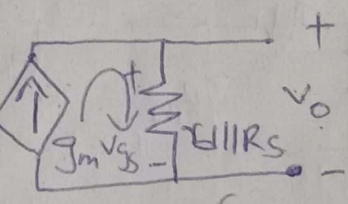




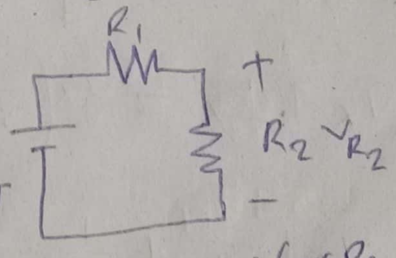
$$A_v = \frac{v_o}{v_{in}}$$



Small signal equivalent circuit



$$v_o = g_m v_{gs} (r_d || R_S)$$



$$v_{gs} = v_{Rin} + (-v_o)$$

$$v_{gs} = v_{Rin} - g_m v_{gs} (r_d || R_S)$$

$$v_{R_2} = \frac{V_T \times R_2}{R_1 + R_2}$$

$$v_{gs}(1 + g_m (r_d || R_S)) = v_{Rin}$$

$$v_{Rin} = \frac{v_{in} \times (R_{in})}{R_{in} + R_{sig}}$$

$$v_{gs} = \frac{v_{Rin}}{1 + g_m (r_d || R_S)}$$

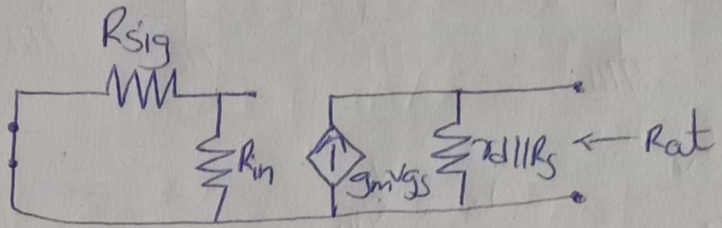
$$v_{gs} = \frac{1}{1 + g_m (r_d || R_S)} \times \left(\frac{R_{in}}{R_{in} + R_{sig}}\right) \times v_{in}$$

$$v_o = g_m v_{gs} \cdot (r_d || R_S)$$

$$V_o = \frac{g_m(r_d \| R_S)}{1+g_m(r_d \| R_S)} \times \left(\frac{R_{in}}{R_{in}+R_{sig}}\right) V_{in}$$

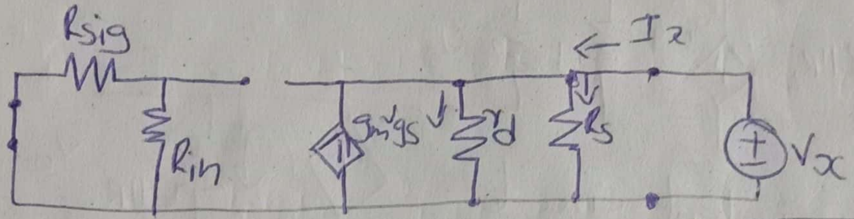
Output Resistance (R_{out}):-

(i) Make all the independent source to zero ($V_{in} \to 0$)



② Ind + Dep $R_{th} = \frac{V_{th}}{I_N}$ ① independ (R_{th}, V_{th})

③ Depen $\to R_{th}$



$$\boxed{R_{out} = \frac{V_x}{I_x}}$$

$$g_m V_{gs} + I_x = \frac{V_x}{r_d} + \frac{V_x}{R_S}$$

$$-g_m V_x + I_x = V_x\left(\frac{1}{r_d} + \frac{1}{R_S}\right)$$

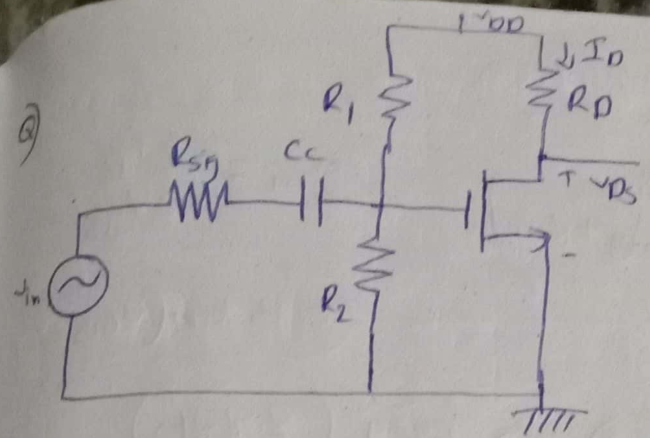
$$V_x\left(g_m + \frac{1}{r_d} + \frac{1}{R_S}\right) = I_x$$

$$A_v = \frac{V_o}{V_{in}} = \frac{g_m(r_d \| R_S)}{1+g_m(r_d \| R_S)} \cdot \frac{R_{in}}{(R_{in}+R_{sig})} \quad \left[\because R_{sig} << R_{in}\right]$$

$$R_{in} = R_1 \| R_2$$

$$R_{out} = \frac{1}{g_m + \frac{1}{r_d} + \frac{1}{R_S}}$$

Q)



Find out the A_V of a common source circuit.

$V_{DD} = 10V$, $R_1 = 70.9k\Omega$, $R_2 = 29.1k\Omega$, $R_D = 5k\Omega$, $V_{TN} = 1.5V$,

$K_n = 0.5mA/V^2$ $\lambda = 0.01V^{-1}$ $R_{sig} = 4k\Omega$

$$I_D = K_n (V_{GS} - V_{TN})^2$$

$$I_{DQ} = K_n (V_{GSQ} - V_{TN})^2$$

$$I_D = \frac{V_{DD} - V_{DS}}{R_D} \Rightarrow V_{DS} = V_{DD} - I_D R_D$$

$$V_{GSQ} = \frac{V_{DD} \times R_2}{R_1 + R_2} \Rightarrow \frac{10 \times 29.1}{70.9 + 29.1} = \frac{291}{100} = 2.91V$$

$$I_{DQ} = K_n (V_{GSQ} - V_{TN})^2 = I_{DQ} = 1mA$$

$$V_{DSQ} = V_{DD} - I_{DQ} \cdot R_D = 5V$$

$V_{DSQ} > V_{GSQ} - V_{TN}$ $\rightarrow$ Mosfet in saturation region

Small-signal v/g gain:

$$A_v = -g_m(r_d \| R_D)\left(\frac{R_{in}}{R_{sig}+R_{in}}\right)$$

$$g_m = \frac{\partial I_D}{\partial v_{gs}}$$

$$= 2k_n(V_{GS}-V_T)$$

$$2\times 0.5(2.91-1.5) \Rightarrow 1(2.91-1.5)$$

$$g_m = 1.41\,mA/V$$

$$R_{in} = R_1 \| R_2$$

$$r_d = \frac{\partial v_{DS}}{\partial I_D} = [\lambda \cdot I_{DQ}]^{-1}$$

$$= [0.01\times 1]^{-1}$$

$$= 100\,K\Omega$$

$$A_v = -1.41\times 10^{-3}(100\|5)\times 10^3\left(\frac{20.6}{4+20.6}\right)$$

$$= -1.41\times 10^{-3}(4.761)\times 10^3(0.837)$$

$$= -1.41\times 10^{-3}(3.984957)$$

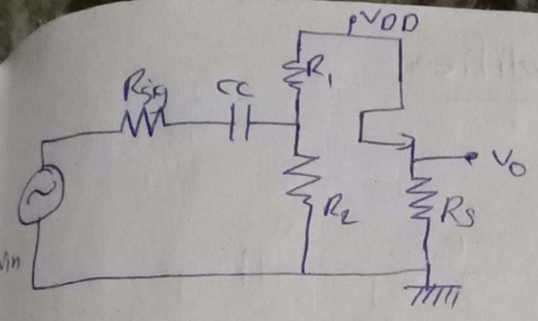
$$= -5.62$$

$$R_o = r_d \| R_D \Rightarrow (100\|5) = 4.761$$

(2) Calculate the small signal v/g gain (A_v) of a source follower $V_{DD} = 12V$, $R_1 = 162K\Omega$, $R_2 = 463K\Omega$

$R_{sig} = 4K\Omega$ $R_S = 0.75K\Omega$ $V_{TN} = 1.5V$, $K_n = 4mA/V^2$

$\lambda = 0.01V^{-1}$



DC calculations:-

$V_{GSQ} = V_{th} = \frac{V_{DD} \times R_2}{R_1 + R_2} = \frac{12 \times 463}{168 + 463} = \frac{5556}{0625} =$

8.8896

$I_{DQ} =$

$g_m = 2k_n(V_{GSQ} - V_{TN}) = 2 \times 4 \times 10^{-3}(\quad \Rightarrow 11.3\,mA/V$

$r_d = [\lambda I_{DQ}]^{-1} \Rightarrow (0.01 \times 7.97)^{-1} \Rightarrow 12.5\,K\Omega$

$A_v = \frac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)} \cdot \left(\frac{R_{in}}{R_{in} + R_{sig}}\right) -$

$= 0.86$

$R_{out} = \frac{1}{g_m + \frac{1}{r_d} + \frac{1}{R_S}} = \frac{1}{11.3 \times 10^{-3} \times \frac{1}{12.5 \times} + \frac{1}{0.75}}$

$\frac{9.375}{13.23} \Rightarrow 0.7\,K\Omega$

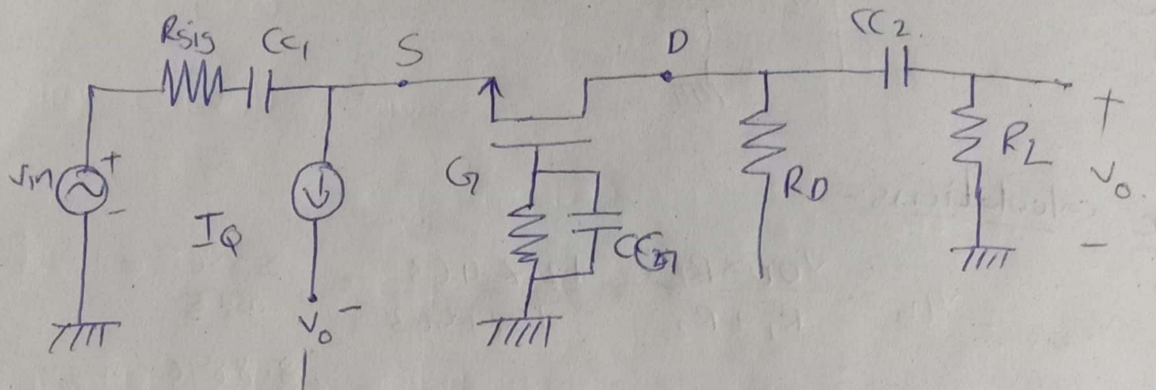
$= \frac{1}{11.3 \times 10^{-3}}$

$= \frac{1}{11.3 \times 0.7}$

$= 0.07$

Scanned with CamScanner

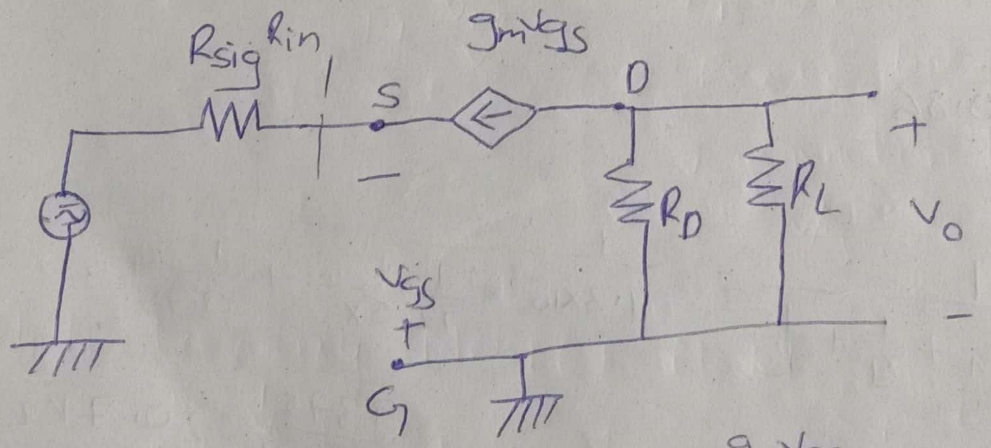
Common Gate Amplifier:-



I/p → source terminal

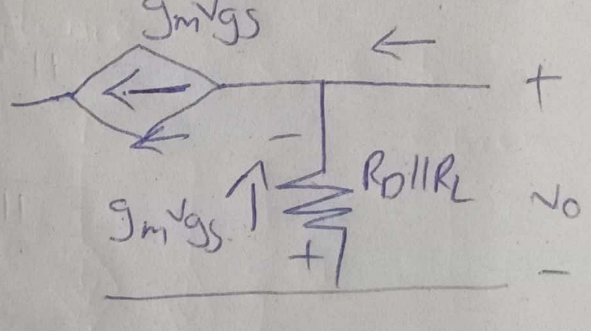
O/p → Drain terminal

Small signal equivalent ckt for CG configuration



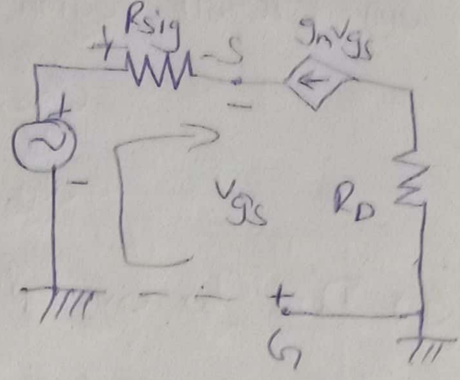
$R_{in} = R_{SG}$

$A_V = \frac{V_o}{V_{in}}$



$$V_o = -\left(g_m v_{gs}(R_D \| R_L)\right)$$

$$v_{gs} = -V_{in} - g_m v_{gs} \cdot R_{sig}$$



$$v_{gs}(1+g_m R_{sig}) = -V_{in}$$

$$v_{gs} = \frac{-V_{in}}{1+g_m R_{sig}}$$

$$V_o = -\left(g_m\left(\frac{-V_{in}}{1+g_m R_{sig}}\right) R_D \| R_L\right)$$

$$\boxed{A_v = \frac{V_o}{V_{in}} = \frac{g_m(R_D \| R_L)}{1+g_m R_{sig}}}$$ ($R_{sig} \to$ neglected)

$$A_v = g_m(R_D \| R_L)$$

$$R_{in} = \frac{1}{g_m}, \quad R_{out} = R_D$$

Mosfet Internal Capacitances:-

① Gate capacitive effect → C_{gs}, C_{gd}, C_{ds}.

② Body " " → S-b capacitance } Depletion
D-b " } layer.

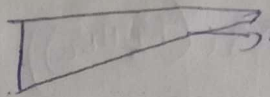
Gate-capacitance effect:-

(i) Triode: WLC_{ox} $C_{gs} = \frac{1}{2} WLC_{ox}$

$C_{gd} = \frac{1}{2} WLC_{ox}$

(ii) Saturation Region

$C_{gs} = \frac{2}{3} WLC_{ox}$



→ channel length modulation

$C_{gd} = 0$

(iii) cut-off region:-

$C_{gs} = C_{gd} = 0$

$C_{gb} = WLC_{ox}$

(iv) Due to overlap:-

$C_{ov} = WL_{ov} \cdot C_{ox}$ (L_{ov} = 5 to 10% of length of channel)

Junction Capacitances:-

(i) $C_{sb} = \dfrac{C_{sbo}}{\sqrt{1 + \frac{V_{SB}}{V_0}}}$

C_{sbo} → capacitance when there is zero body source bias

(ii) $C_{Db} = \dfrac{C_{Dbo}}{\sqrt{1 + \frac{V_{DB}}{V_0}}}$

V_{SB} → Magnitude of Reverse biase v/g

V_0 = junction built in v/g

High Frequency MOSFET Model:-

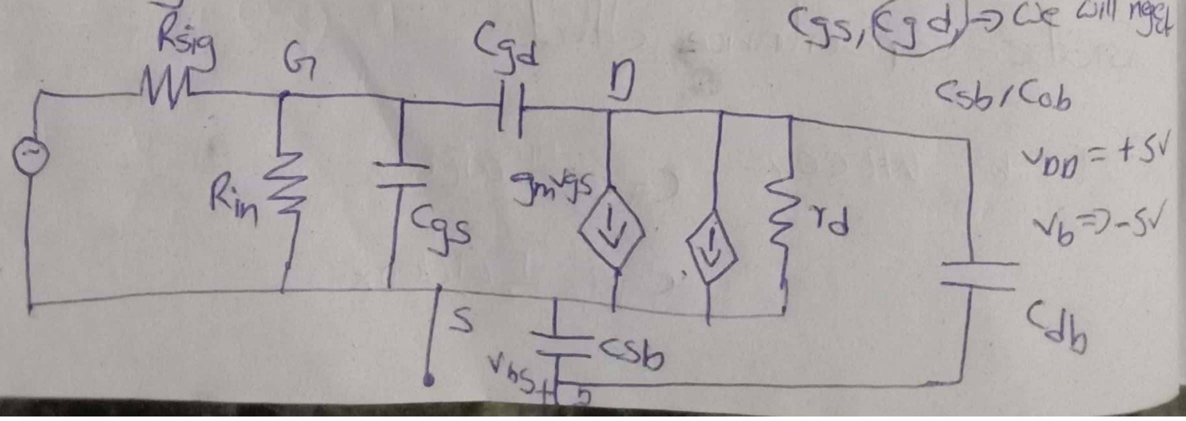
↓

only internal capacitance

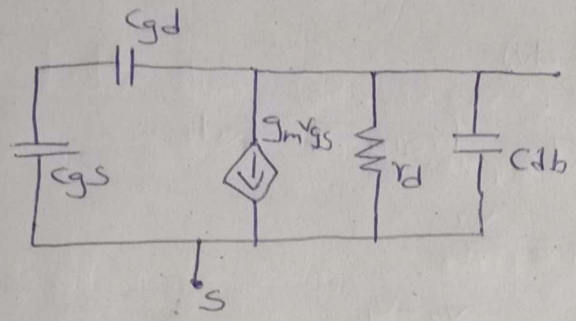
capacitance → ($R_s = 0$)

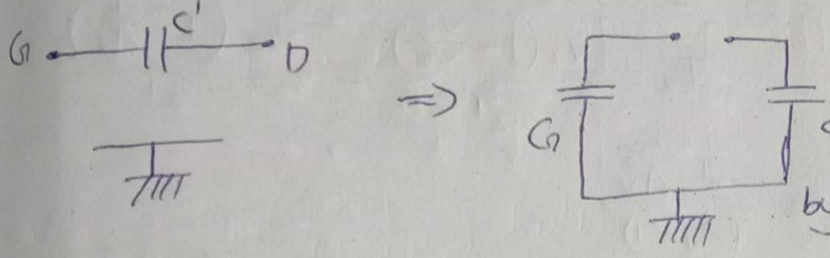
↓

C_{gs}, C_{gd} → we will neglect C_{sb}/C_{db}



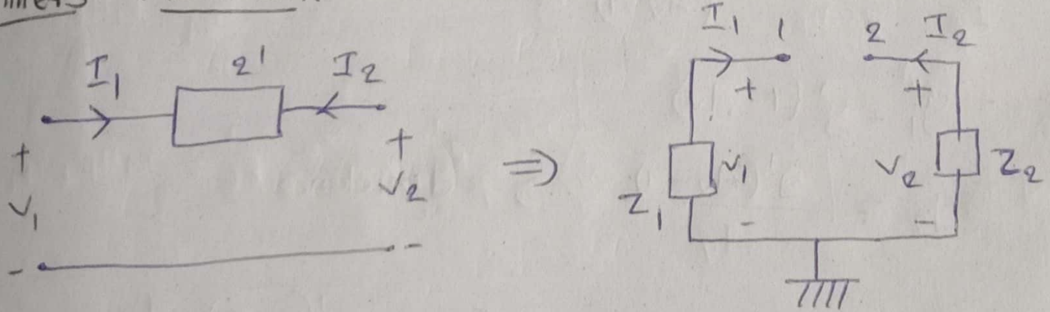
CS amplifier ckt





by Million's theorem

Miller's Theorem:-



If $V_1 > V_2$, I_1 flows from 1 to 2

$$I_1 = \frac{V_1 - V_2}{z'} = \frac{V_1\left(1 - \frac{V_2}{V_1}\right)}{z'} = \frac{V_1(1 - A_v)}{z'}$$

$$I_1 = \frac{V_1}{\left[z'/(1-A_v)\right]} \qquad \left[\because \frac{V_1}{I_1} = Z_1\right]$$

$$\boxed{\frac{V_1}{I_1} = Z_1 = \frac{z'}{1 - Av}}$$ → in b/w 1/2

Incease of impedance

In case of admidence capacitor

$$y = y'(1-A_v)$$

$V_2 > V_1$, I_2 from 2 to 1,

$$Z_2 = \frac{V_2}{I_2}$$

$$I_2 = \frac{V_2 - V_1}{Z'}$$

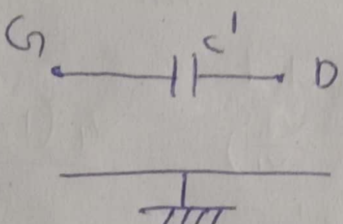
$$I_2 = \frac{V_2\left(1-\frac{V_1}{V_2}\right)}{Z'} = \frac{V_2\left(1-\frac{1}{A_v}\right)}{Z'}$$

$$Z_2 = \frac{Z' A_v}{(A_v - 1)}$$

$$\frac{V_2}{I_2} = Z_2 = \frac{Z' A_v}{(A_v-1)} \rightarrow \text{Impedance}$$

$$y_1 = y'(1-A_v)$$

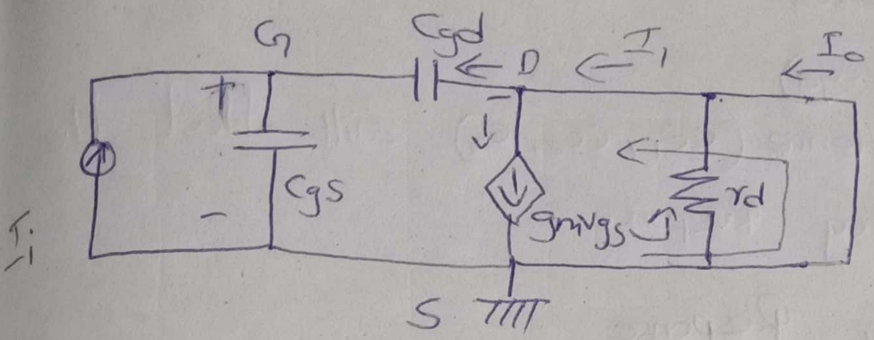
$$y_2 = \frac{y'(A_v-1)}{A_v} \rightarrow \text{admidance}$$



$$\boxed{C_1 = c'(1-A_v) \qquad C_2 = \frac{c'(A_v-1)}{A_v}}$$

MOSFET unity gain frequency (f_T):

$$\frac{I_o}{I_{in}} = A_I(sc) = 1$$



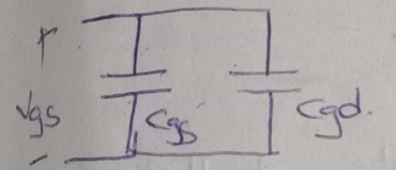
S
C−S
C−D

$$I_o = g_m v_{gs}$$

$$\frac{V}{Z} = I$$

$$I_o = g_m v_{gs} - sC_{gd} \cdot v_{gs}$$

$$V \cdot Y = I$$



$$\frac{v_{gs}}{I_i} = \frac{1}{s(C_{gs}+C_{gd})}$$

$$I_o = g_m \left(\frac{I_{in}}{s(C_{gs}+C_{gd})}\right)$$

$$1 = \frac{g_m}{j\omega_T (C_{gs}+C_{gd})} \Rightarrow 1 = \frac{g_m}{\omega_T (C_{gs}+C_{gd})}$$

$$\omega_T = \frac{g_m}{(C_{gs}+C_{gd})}$$

$$\boxed{f_T = \frac{g_m}{2\pi (C_{gs}+C_{gd})}}$$

$$g_m = \mu_n C_{ox} \frac{W}{L} \cdot V_{ov}$$

$$g_m = \frac{2 I_D}{V_{ov}}$$

Frequency Response of the CS Amplifier:-

For common source 180°

" drain 0°

" gate 0°

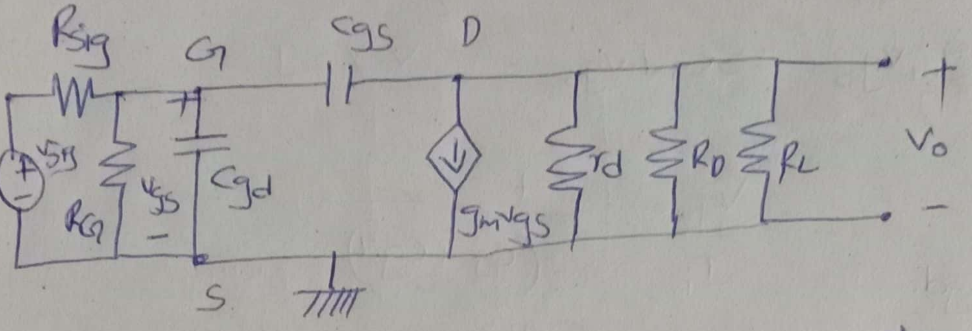
$$A_m = -g_m (r_d \| R_D \| R_L) \left(\frac{R_G}{R_G + R_{sig}}\right)$$

Scanned with CamScanner

Internal capacitances will affect the high frequency Response. (C_{gs}, C_{gd})

External capacitance (C_{C1}, C_{C2}, C_s) will affect the lower frequency Response.

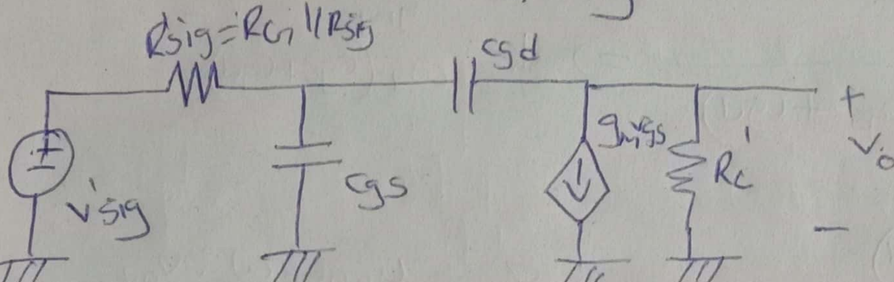
High Frequency Response



$$V'_{sig} = V_{gs} = \frac{V_{sig} \times R_G}{R_G + R_{sig}}$$

$R'_{sig} = R_G \| R_{sig}$

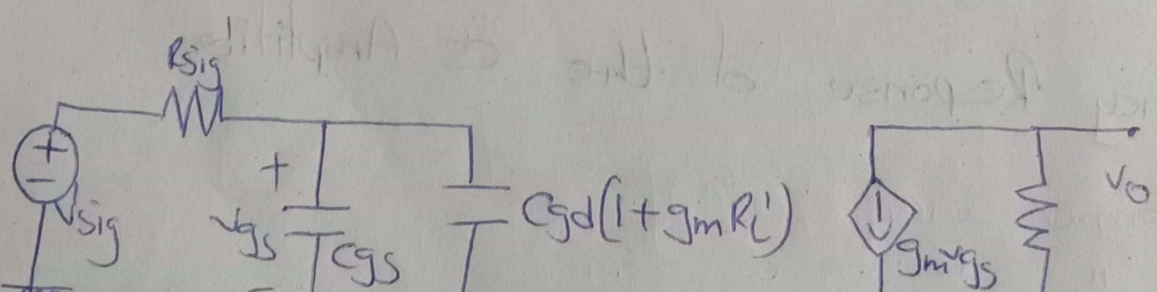
$R_{sig} = R_1 \| R_2$



$R'_L = r_d \| R_D \| R_L$

$$\boxed{V_o = -g_m V_{gs} \cdot R'_L}$$

$A_v = -g_m R'_L$



Upper 3dB $\quad \frac{V_o}{V_{sig}} = \frac{A_m}{\left(1 + \frac{s}{\omega_H}\right)}$

$\omega_H = \omega_0 = \frac{1}{C_{in} \cdot R'_{sig}}$

$$f_H = \frac{1}{2\pi C_{in} \cdot R_{sig}'}$$

Observations:-

(i) $R_{sig}' = R_{sig} \| R_G$, $C_{in} = C_{gs} + C_{gd}(1 + g_m R_L')$

$R_{sig}' = R_{sig}$ ($\because R_G >> R_{sig}$)

(ii) All the C_{gd} is usually very small capacitience it effects on the freq amplifier frequency response can be which is approx midband gain of the amplifier.

(iii) The multiplication effect the C_{gd} undergoes comes about because it is connected b/w two nodes whose v/g are related by a large -ve gain. $(-g_m R_L')$ This effect is known as Miller effect and $(1+g_m R_L')$ is known as Miller multiplier. It is the Miller effect that causes common source amplifies to have a large total input capacitance and hence low upper 3dB frequency (f_H)

(iv) To extend the high frequency response of a MOSFET amplifier, we have to find configuration in which the Miller effect is absent (or) reduced.

Basic FET Amplifiers

5.1 Introduction

In this chapter, we emphasize on the use of FETs in linear amplifier applications. Linear amplifiers imply that, we are dealing with analog signals mostly. The magnitude of an analog signal may have any value, within limits, and may vary continuously with respect to time. Although a major use of MOSFETs is in digital applications, they are also used in linear amplifier circuits.

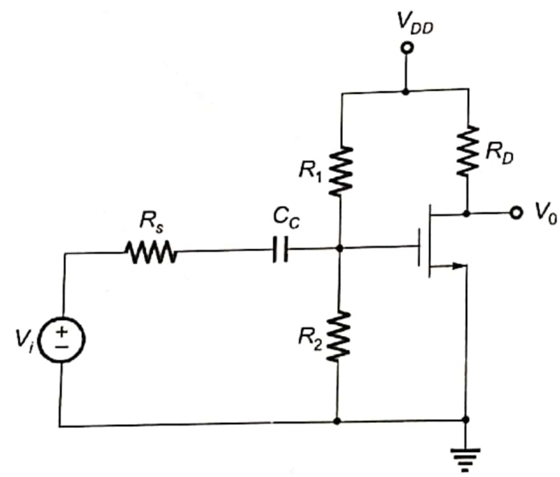


Figure-5.1 *Common-source circuit with voltage divider biasing and coupling capacitor*

5.2 The Common-Source Amplifier

Fig. (5.1) shows a basic common-source circuit with voltage-divider biasing. We see that the source is at ground potential hence the name common source. The signal from signal source is coupled into the gate of transistor through coupling capacitor C_C, which provides DC isolation between amplifier and signal source. The DC transistor biasing is established by R_1 and R_2 and is not disturbed when the signal source is capacitively coupled to the amplifier. Fig. (5.2) shows the resulting small-signal equivalent circuit. Since the source is at ground potential, so there is no body-effect.

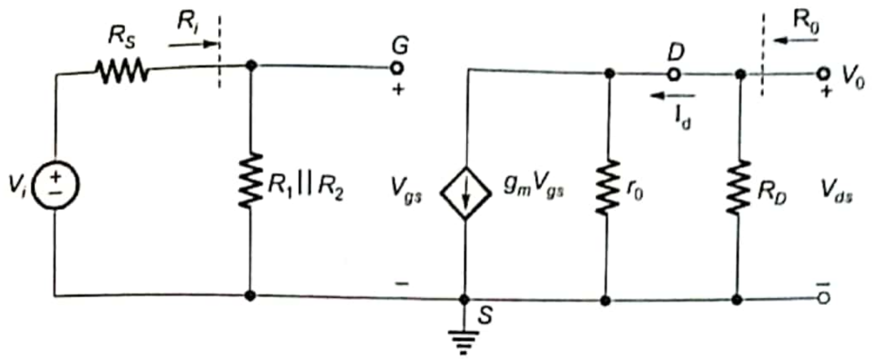


***Figure-5.2:** Small-signal equivalent circuit, assuming coupling capacitor acts as a short-circuit*

The output voltage is

$$\boxed{V_0 = -g_m V_{gs} (r_o \| R_D)} \quad ...(5.1)$$

The input gate-to-source voltage is

$$V_{gs} = \left(\frac{R_i}{R_i + R_s}\right) \cdot V_i$$

so the small-signal voltage gain is

$$\boxed{A_V = \frac{V_0}{V_i} = -g_m (r_0 || R_D) \cdot \frac{R_i}{R_i + R_s}} \quad ...(5.2)$$

We can also relate the AC drain current to AC drain-to-source voltage as $V_{ds} = I_d(R_D)$.

Example-5.1 **Determine the small-signal voltage gain and input and output resistances of a common-source amplifier. For the circuit in Fig. (5.1), the parameters are:**
V_{DD} = 10 V, R_1 = 70.9 kΩ, R_2 = 29.1 kΩ and R_D = 5 kΩ. The transistor parameters are: V_{TN} = 1.5 V, K_n = 0.5 mA/V² and λ = 0.01 V⁻¹. Assume R_s = 4 kΩ.

Solution:

DC Calculations:

The dc or quiescent gate-to-source voltage is

$$V_{GSQ} = \left(\frac{R_2}{R_1 + R_2}\right)(V_{DD}) = \left(\frac{29.1}{70.9 + 29.1}\right)(10) = 2.91\,\text{V}$$

The quiescent drain current is

$$I_{DQ} = K_n (V_{GSQ} - V_{TN})^2 = (0.5)(2.91 - 1.5)^2 \simeq 1\text{ mA}$$

and the quiescent drain-to-source voltage is

$$V_{DSQ} = V_{DD} - I_{DQ} R_D = 10 - (1)(5) = 5\text{ V}$$

Since $V_{DSQ} > V_{GSQ} - V_{TN}$, the transistor is biased in saturation region.

Small-signal Voltage gain:

The small-signal transconductance g_m is then

$$\begin{aligned} g_m &= 2K_n (V_{GSQ} - V_{TN}) \\ &= 2(0.5)(2.91 - 1.5) \\ &= 1.41\text{ mA/V} \end{aligned}$$

and the small-signal output resistance r_0 is

$$r_o \cong [\lambda I_{DQ}]^{-1} = [(0.01)(1)]^{-1}$$
$$= 100 \text{ k}\Omega$$

The amplifier input resistance is

$$R_i = R_1 || R_2 = 70.9 || 29.1$$
$$= 20.6 \text{ k}\Omega$$

Hence, the small-signal voltage gain is

$$A_v = -g_m(r_o || R_D) \frac{R_i}{R_i + R_s}$$

$$= -(1.41)(100||5)\left(\frac{20.6}{20.6+4}\right)$$

$\Rightarrow$ $$A_v = -5.62$$

Input and Output Resistance:

The amplifier input resistance is

$$R_i = R_1 || R_2 = 70.9 || 29.1$$
$$= 20.6 \text{ k}\Omega$$

and the amplifier output resistance is

$$R_o = R_D || r_o = 5 || 100$$
$$= 4.76 \text{ k}\Omega$$

5.2.1 Common Source Amplifier with Source Resistor

A source resistor R_s tends to stabilize the Q-point against variations in transistor parameters [Fig. (5.3)]. However, a source resistor also reduces the signal gain.

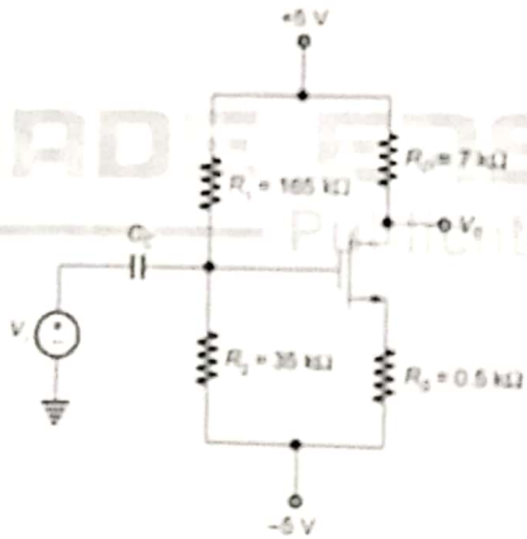


Figure-5.3 : Common-source circuit with source resistor and positive and negative supply voltages

The circuit in Fig. (5.3) is an example of a situation in which the body effect should be taken into account. The substrate (not shown) would normally be connected to –5 V supply, so that the body and substrate terminals are not at same potential. However, in the following example, we will neglect this effect.

Example-5.2 Determine the small-signal voltage gain of a common-source circuit containing a source resistor. Consider the circuit in Fig. (5.3). The transistor parameters are: $V_{TN} = 0.8$ V, $K_n = 1$ mA/V^2 and $\lambda = 0$.

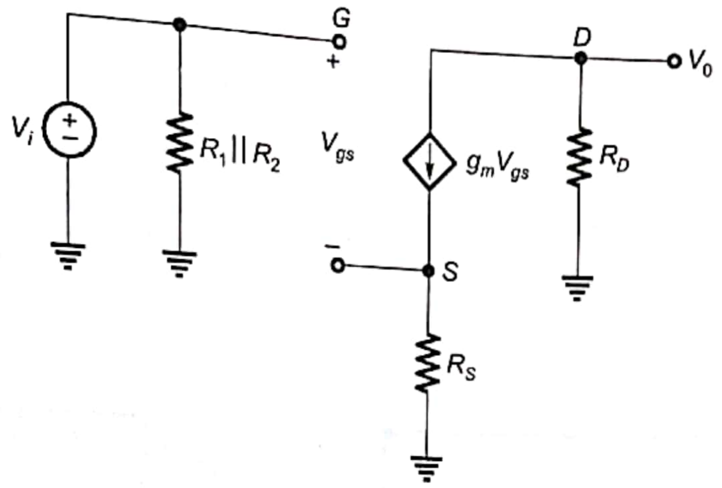


***Figure-5.4:** Small-signal equivalent circuit of NMOS common-source amplifier with source resistor*

Solution:

From DC analysis of the circuit, we find that $V_{GSQ} = 1.50$ V, $I_{DQ} = 0.50$ mA and $V_{DSQ} = 6.25$ V. The small-signal transconductance is

$$g_m = 2K_n(V_{GS} - V_{TN}) = 2(1)(1.50 - 0.8) = 1.40 \text{ mA/V}$$

and small-signal resistance is

$$r_0 \cong [\lambda I_{DQ}]^{-1} = \infty$$

Fig. (5.4) shows the resulting small-signal equivalent circuit. To sketch the small-signal equivalent circuit, let's start with three terminals of the transistor, draw the transistor equivalent circuit between three terminals, and then sketch other circuit elements around the transistor.

The output voltage is

$$V_0 = -g_m V_{gs} R_D$$

Writing KVL equation from the input around the gate-source loop, we find

$$V_i = V_{gs} + (g_m V_{gs})R_s = V_{gs}(1 + g_m R_s)$$

or

$$V_{gs} = \frac{V_i}{1 + g_m R_s}$$

The small-signal voltage gain is

$$A_v = \frac{V_0}{V_i} = \frac{-g_m R_D}{1 + g_m R_s}$$

We may note that if g_m is large, then the small-signal voltage gain would be approximately

$$A_v \cong \frac{-R_D}{R_s}$$

Substituting the approximate parameters into the actual voltage gain expression, we find

$$A_v = \frac{-(1.4)(7)}{1 + (1.4)(0.5)} = \mathbf{-5.76}$$

5.2.2. Common-source Circuit with Source Bypass Capacitor

A bypass capacitor added to the common-source circuit with a source resistor will minimize the loss in small-signal voltage gain, while maintaining the Q-point stability.

The Q-point stability can be further increased by replacing the source resistor with a constant-current source. The resulting circuit is shown in Fig. (5.5), assuming an ideal signal source. If the signal frequency is sufficiently large so that the bypass capacitor acts essentially as an ac short-circuit, the source will be held at signal ground.

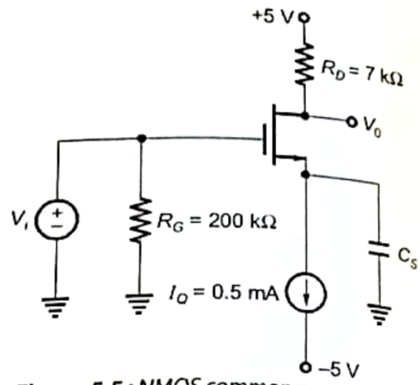


Figure-5.5 : *NMOS common-source circuit with source bypass capacitor*

Example-5.3 Determine the small-signal voltage gain of a circuit biased with a constant-current source and incorporating a source bypass capacitor. For the circuit shown in Fig. (5.5), the transistor parameters are: $V_{TN} = 0.8$ V, $K_n = 1$ mA/V², and $\lambda = 0$.

Solution:

Since the dc gate current is zero, the DC voltage at source terminal is $V_s = -V_{GSQ}$, and gate-to-source voltage is determined from

$$I_{DQ} = I_Q = K_n(V_{GSQ} - V_{TN})^2$$

or

$$0.5 = (1)(V_{GSQ} - 0.8)^2$$

which yields,

$$V_{GSQ} = -V_s = 1.51 \text{ V}$$

The quiescent drain-to-source voltage is

$$V_{DSQ} = V_{DD} - I_{DQ}R_D - V_s$$
$$= 5 - (0.5)(7) - (-1.51)$$
$$= 3.01 \text{ V}$$

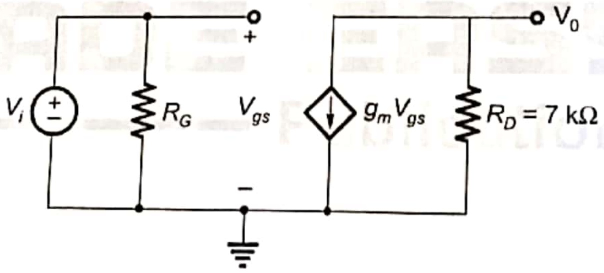


Figure-5.6 : *Small-signal equivalent circuit, assuming the source bypass capacitor acts as a short-circuit*

The transistor is therefore biased in saturation region.

The small-signal equivalent circuit is shown in Fig. (5.6). The output voltage is

$$V_0 = -g_m V_{gs} R_D$$

Since $V_{gs} = V_i$, the small-signal voltage gain is

$$A_v = \frac{V_0}{V_i} = -g_m R_D$$

$$= -(1.414)(7) = \mathbf{-9.9}$$

NOTE

Comparing the small-signal voltage gain of 9.9 in this example to 5.76 calculated in the previous example, we see that the magnitude of gain increases when a source bypass capacitor is included.

5.3 Common-Drain (Source Follower) Amplifier

The circuit configuration of common-drain amplifier is shown in Fig. (5.7). The small-signal equivalent circuit, assuming the coupling capacitor acts as a short-circuit, is shown in Fig. 5.8 (a) and (b). We are again neglecting the body effect.

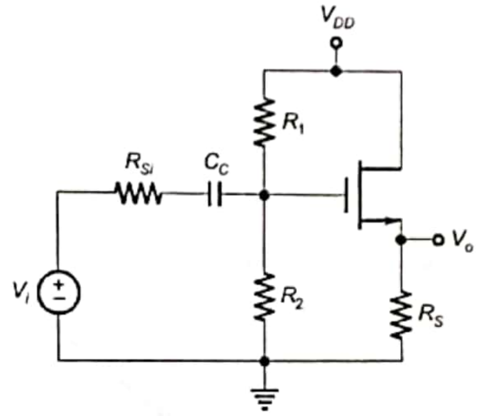


Figure-5.7 : *NMOS source-follower or common-drain amplifier*

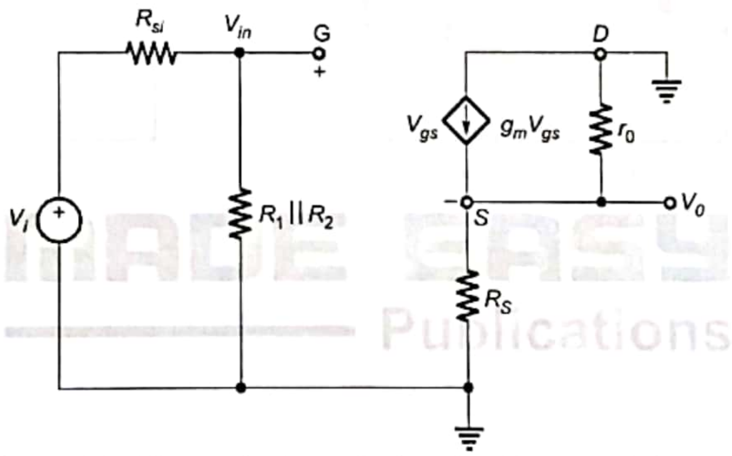


Figure-5.8 : *(a) Small-signal equivalent circuit of NMOS source follower*

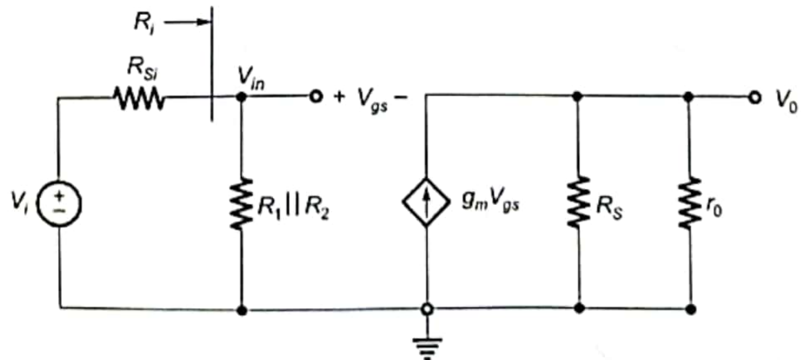


Figure- 5.8 : *(b) Small-signal equivalent circuit of NMOS source follower with all signal grounds at a common point)*

The output voltage is

$$V_0 = (g_m V_{gs})(R_s || r_0) \quad ...(5.3)$$

Writing a KVL equation from input to output results in the following:

$$V_{in} = V_{gs} + V_0 = V_{gs} + g_m V_{gs}(R_s || r_0)$$

Therefore, the gate-to-source voltage is

$$V_{gs} = \frac{V_{in}}{1+g_m(R_s || r_0)} = \left[\frac{1/g_m}{\frac{1}{g_m} + (R_s || r_0)}\right] \cdot V_{in} \quad ...(5.4)$$

The V_{in} is related to source input voltage V_i by

$$V_{in} = \left(\frac{R_i}{R_i + R_{si}}\right) \cdot V_i \quad ...(5.5)$$

where $R_i = R_1 || R_2$ is input resistance to the amplifier. So, we have the small-signal voltage gain,

$$A_v = \frac{V_0}{V_i} = \frac{g_m(R_s || r_0)}{1+g_m(R_s || r_0)} \cdot \left(\frac{R_i}{R_i + R_{si}}\right)$$

or

$$\boxed{A_v = \frac{R_s || r_0}{\frac{1}{g_m} + R_s || r_0} \cdot \left(\frac{R_i}{R_i + R_{si}}\right)} \quad ...(5.6)$$

5.3.1 Input and Output Impedance

The small-signal input resistance R_i is defined in Fig. 5.8 (b) which is the Thevenin equivalent of bias resistors. Even though the input resistance to the gate of MOSFET is essentially infinite, the input bias resistances do provide a loading effect.

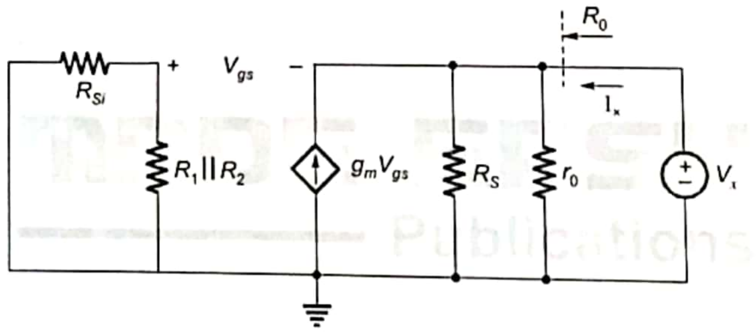


Figure-5.9: *Equivalent circuit of NMOS source follower, for determining output resistance*

To calculate the small-signal output resistance, we set all independent small-signal sources equal to zero, apply a test voltage to the output terminals, and measure a test current.

Since there are no capacitors in the circuit, the output impedance is simply an output resistance, which is defined by

$$R_0 = \frac{V_x}{I_x} \quad ...(5.7)$$

Writing a KCL equation at output source terminal produces

$$I_x + g_m V_{gs} = \frac{V_x}{R_s} + \frac{V_x}{r_0} \quad ...(5.8)$$

Since there is no current in input portion of the circuit, we see that $V_{gs} = -V_x$. Therefore,

$$I_x = V_x\left(g_m + \frac{1}{R_s} + \frac{1}{r_0}\right)$$

or

$$\frac{I_x}{V_x} = \frac{1}{R_0} = g_m + \frac{1}{R_s} + \frac{1}{r_0} \qquad \text{...(5.9)}$$

The output resistance is then

$$\boxed{R_0 = \frac{1}{g_m} \| R_s \| r_0} \qquad \text{...(5.10)}$$

Example-5.4 Calculate the small-signal voltage gain of a source-follower circuit in Fig. (5.7). Assume that the circuit parameters are $V_{DD} = 12\ V$, $R_1 = 162\ k\Omega$, $R_2 = 463\ k\Omega$ and $R_s = 0.75\ k\Omega$ and the transistor parameters are $V_{TN} = 1.5\ V$, $K_n = 4\ mA/V^2$ and $\lambda = 0.01\ V^{-1}$. Also assume $R_{si} = 4\ k\Omega$.

Solution:

The dc analysis results are $I_{DQ} = 7.97$ mA and $V_{GSQ} = 2.91$ V. The small-signal transconductance is therefore,

$$g_m = 2K_n(V_{GSQ} - V_{TN}) = 2(4)(2.91 - 1.5) = 11.3\ mA/V$$

and the small-signal transistor resistance is

$$r_0 \cong [\lambda I_{DQ}]^{-1} = [(0.01)(7.97)]^{-1} = 12.5\ k\Omega$$

The amplifier input resistance is

$$R_i = R_1 \| R_2 = 162 \| 463 = 120\ k\Omega$$

The small-signal voltage gain then becomes

$$A_v = \frac{g_m(R_s \| r_0)}{1 + g_m(R_s \| r_0)} \cdot \frac{R_i}{R_i + R_{si}}$$

$$\Rightarrow \qquad A_v = \frac{(11.3)(0.75 \| 12.5)}{1 + (11.3)(0.75 \| 12.5)} \cdot \frac{120}{120 + 4} = 0.860$$

NOTE The magnitude of the small-signal voltage gain is less than 1 and positive, which means that the output singal voltage is in phase with the input signal voltage.

5.4 The Common-Gate Configuration

The common-gate configuration shown in Fig. 5.10 (a) is biased with a constant current source I_Q. The small-signal equivalent circuit is shown in Fig. 5.10 (b).

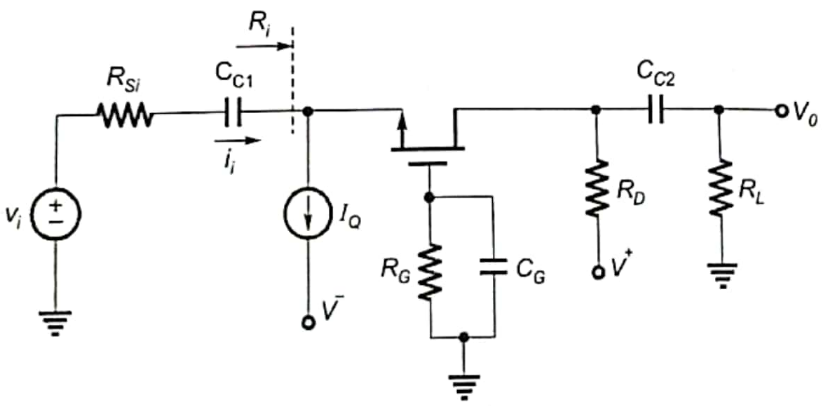


Figure-5.10: *(a) Common-gate circuit*

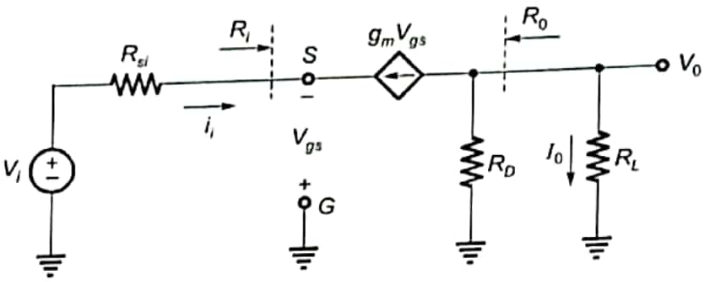


Figure-5.10: *(b) Small-signal equivalent circuit of common-gate amplifier*

The output voltage is

$$V_0 = -(g_m V_{gs})\,(R_D || R_L) \qquad ...(5.11)$$

Writing KVL equation around the input, we get

$$V_i = I_i R_{si} - V_{gs} \qquad ...(5.12)$$

where $I_i = -g_m V_{gs}$. The gate-to-source voltage can now be written as

$$V_{gs} = \frac{-V_i}{1 + g_m R_{si}} \qquad ...(5.13)$$

The small-signal voltage gain is found to be

$$A_v = \frac{V_0}{V_i} = \frac{g_m (R_D || R_L)}{1 + g_m R_{si}} \qquad ...(5.14)$$

Also, since the voltage gain is positive, hence the output and input signals are in phase.

The small-signal current gain is given by

$$\boxed{A_i = \frac{I_0}{I_i} = \left(\frac{R_D}{R_D + R_L}\right) \cdot \left(\frac{g_m R_{si}}{1 + g_m R_{si}}\right)} \qquad ...(5.15)$$

We may note that if $R_D >> R_L$ and $g_m R_{si} >> 1$, then the current gain is essentially unity.

5.4.1 Input and Output Impedance

The input resistance is defined as

$$R_i = \frac{-V_{gs}}{I_i} \qquad ...(5.16)$$

Since, $I_i = -g_m V_{gs}$, the input resistance is

$$\boxed{R_i = \frac{1}{g_m}} \qquad ...(5.17)$$

We can find the output resistance by setting input signal voltage equal to zero. From Fig. 5.10 (b) we see that $V_{gs} = -g_m V_{gs} R_{si}$, which means that $V_{gs} = 0$. Consequently, $g_m V_{gs} = 0$. The ouput resistance looking back from the load resistance, is therefore

$$\boxed{R_o = R_D} \qquad ...(5.18)$$