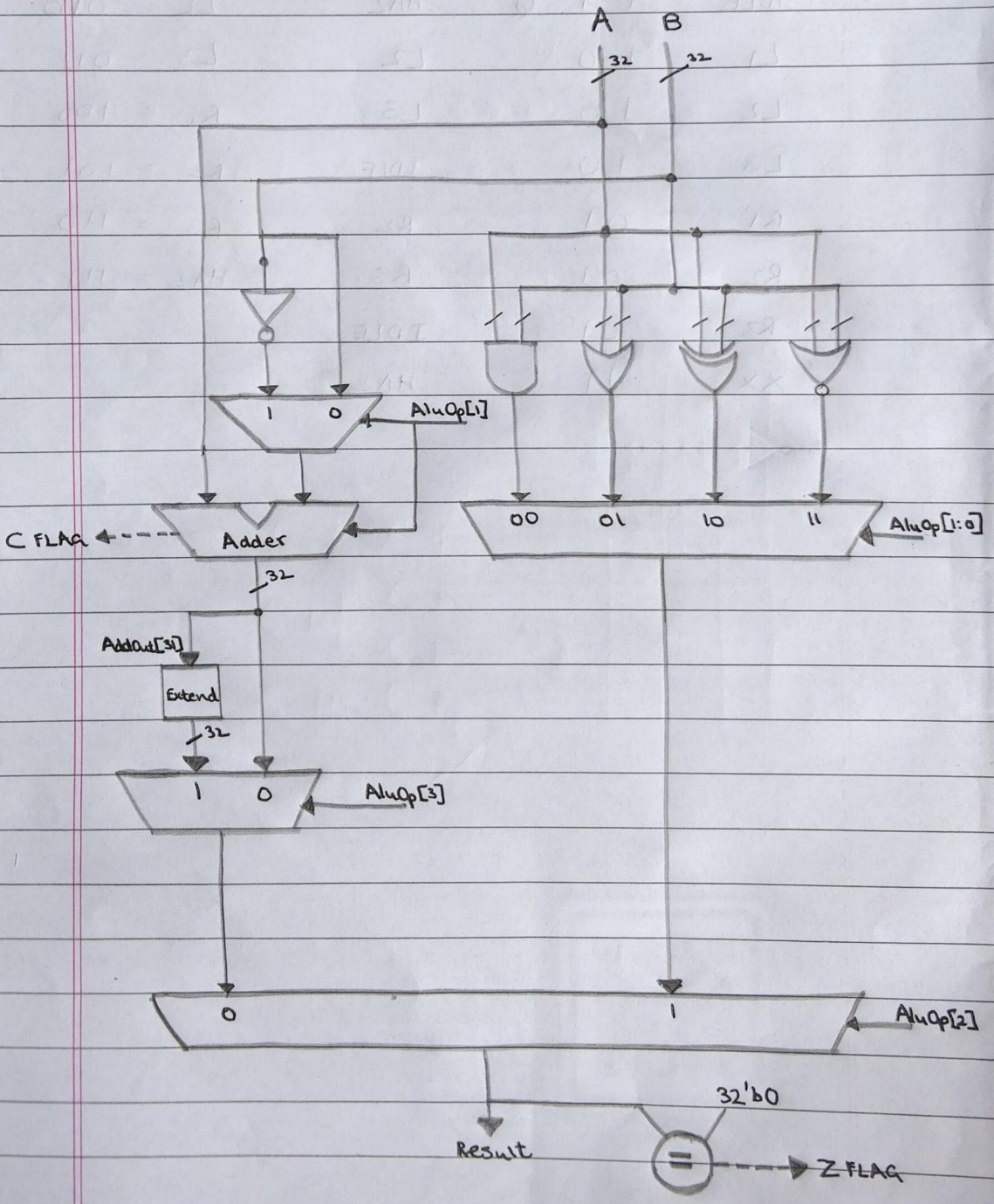
LAB 5 – IMPLEMENTING AN ALU

Designing an ALU that performs a subset of the ALU operations of a full MIPS ALU

add, sub, slt, and, or, xor, nor

ALU ARCHITECTURE BLOCK DIAGRAM:

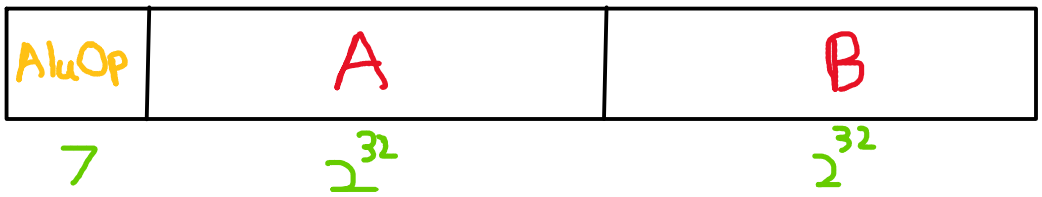


Lab5 - MIPS ALU

21 September 2024 22:06

Part 2

Until now, we have always verified our circuits by exhaustively testing them. Assume that we can test 1 input every second, how long would it take us to test our ALU by trying each and every possible input combination. Please consider only the 7 valid combinations for the AluOp in Table 1. Provide the calculations.



$$7 + 2^{32+32} = 1.8446 * 10^{19} \text{ sec}$$

Part 3

Investigate the different reports to find the answers to the questions below. Show the assistants your result in this part.

Number of LUTs	79
Number of bonded IOBs	102
Which pin of the FPGA is the output 'zero' connected? (pin name)	IO_L3P_T0_DQS_AD5P_35
Where does the longest path start from	IBUF/AluOp[1]
Where does the longest path end	OBUF /C
How long is the longest path	
How much of the longest path is routing	
How many levels of logic is in the longest path	10