DDCA Lab 3 - 7 Seg Verilog

08 September 2024 12:54

Display	S3	S2	S1	S0	a	b	c	d	e	f	g
0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	1	1			1	1	1	1
2	0	0	1	0			1			1	
3	0	0	1	1					1	1	
4	0	1	0	0	1			1	1		
5	0	1	0	1		1			1		
6	0	1	1	0		1					
7	0	1	1	1				1	1	1	1
8	1	0	0	0							
9	1	0	0	1					1		
A	1	0	1	0				1			
B	1	0	1	1	1	1					
C	1	1	0	0		1	1				1
D	1	1	0	1	1					1	
E	1	1	1	0		1	1				
F	1	1	1	1		1	1	1			

D[6] . . . . . D[0]

7'h01
7'h4F
7'h12
7'h06
7'h4C
7'h24
7'h20
7'h0F
7'h00
7'h04
7'h08
7'h60
7'h31
7'h42
7'h30
7'h38