1. The figure below shows the i^{th} full-adder block of a binary adder circuit. C_i is the input carry and C_{i+1} is the output carry of the circuit. Assume that each logic gate has a delay of 2 nanosecond, with no additional time delay due to the interconnecting wires. If the inputs A_i ,B_i, are available and stable throughout the carry propagation, the maximum time taken for an input C_i to produce a steady-state output C_{i+1}is_____nanosecond