

A 5-V Switch for Analog Multiplexers With 2.5-V Transistors in 28-nm CMOS Technology

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Abstract—Despite the scaling of the supply voltage of deep-submicrometer CMOS technologies, many applications still require to deal with off-chip signals in high-voltage domains (e.g., 3.3 and 5 V). Hence, foundries offer fabrication processes with voltage-tolerant transistors, which are inherently protected from the electrical stress, at the expenses of compromising their performances, reducing the design portability, and augmenting the production costs in case of the customization of the process. As an alternative, circuit techniques, such as cascoding, adaptive biasing, and voltage shifting, result effective in designing analog circuits, such as amplifiers and voltage drivers at high supply voltage with voltage-scaled transistors. This article presents the architecture of a switch for analog multiplexers (MUXs) able to handle signals up to twice the nominal supply voltage of the employed transistors. To validate the circuit choice, a switch for a 5-V MUX has been designed with 2.5-V transistors in 28-nm CMOS technology. The comparison with a benchmark architecture with tailored 5-V devices shows that an about three times larger area and 4- μ A static current demand have to be considered. Moreover, an accelerated degradation test (ADT) showed a similar decay of the features of both types of switches.

Index Terms—Adaptive biasing, CMOS switch, electrical stress, input multiplexer (MUX), voltage tolerant circuit.

I. INTRODUCTION

THE shrinking of transistor size, which characterizes CMOS technology scaling, enables the implementation of system-on-chip (SoC) of increasing complexity. The related decrease of the nominal supply voltage is appetible in the perspective of reducing the power consumption, but it also determines a lower maximum tolerable voltage drop across the transistor terminals. Transistors with minimum channel length below 65 nm have a nominal supply voltage lower than 1.2 V. Hence, deep-submicrometer CMOS technologies are not straightforward to be employed in circuit blocks, which have to be compliant with 5-V off-chip signals, as required, for example, by the universal serial bus (USB). In order to overcome this issue, fabrication processes also include voltage-resistant transistors, meant to be employed in the

Manuscript received 7 October 2022; revised 2 January 2023; accepted 21 January 2023. (*Corresponding author: Stefano D’Amico*)

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Color versions of one or more figures in this article are available at <https://doi.org/10.1109/TVLSI.2023.3240002>.

Digital Object Identifier 10.1109/TVLSI.2023.3240002

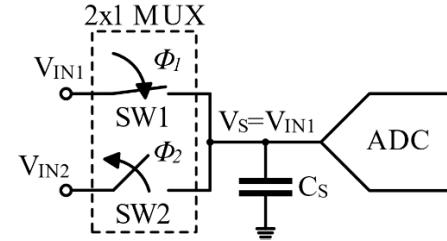


Fig. 1. Scheme including a 2×1 MUX at the input of a two-channel ADC.

input–output (I/O) interfaces in order to allow the handling of high-voltage signals. Nevertheless, a given process flavor does only include a limited set of I/O transistors. For example, standard processes of 28-nm CMOS technology include 2.5-V I/O transistors, but it does not include 5-V-tolerant transistors. As it is required to handle voltages higher than the maximum one for the available I/O transistors, two solutions are possible. The first one is to require the foundry to customize the I/O transistors in order to achieve a greater tolerable voltage. The drawbacks are the increase of the fabrication cost and the impairment of transistor performances, as unity gain frequency, flicker noise, and power consumption. Hence, extending the use of the available transistors to the implementation of blocks with supply voltage larger than the nominal one is attractive in the perspective of overcoming these limits. Thus, the second solution relies on a careful circuit design, which guarantees that none of the transistors experiences electric stress exceeding the maximum tolerable one [1]. In particular, this approach employs specific circuit schemes, such as transistor cascoding, voltage-shifting, and adaptive biasing, which keep the voltage difference between the transistor terminals for each transistor below the maximum tolerable one [2].

Even if these solutions have been demonstrated to be effective for implementing many circuit blocks, such as high-voltage driver [3], voltage regulator [4], and digital-to-analog converter (DAC) [2], the design of analog multiplexers (MUXs) in voltage-scaled technology remains challenging. In fact, the bias voltage of the switches included in a MUX dramatically depends on the input voltage. Fig. 1 shows the scenario where a 2×1 MUX is adopted for the selection of the input of a two-channel analog-to-digital converter (ADC).

In the proposed case of study, the two input voltages, V_{IN1} and V_{IN2} , range up to a maximum signal voltage, V_{SUP} . Since V_{IN1} and V_{IN2} are, in general, independent, the SW2 switch

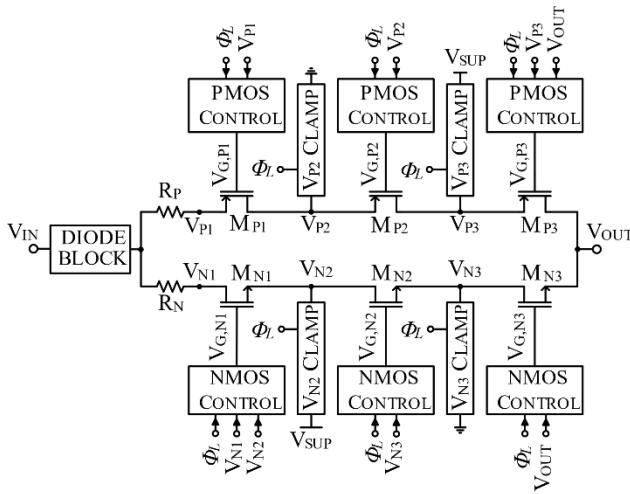


Fig. 2. Architecture of the switch described in [5].

in the open state sees a voltage drop up to the maximum signal voltage at its terminals, as V_{IN1} is at V_{SUP} and V_{IN2} is at ground or vice versa. Assuming V_{SUP} larger than the maximum tolerable voltage, V_{MAX} , the open-switch SW2 is exposed to an overvoltage stress.

This article demonstrates that circuit techniques can be used for implementing a switch able to operate with signals varying over a range up to twice the maximum tolerable voltage, which in general corresponds to the nominal supply voltage of the employed transistor. A switch for a 5-V MUX in 28-nm CMOS technology has been implemented as case of study. The proposed solution relies on the 2.5-V transistors made available by the fabrication process. The values of the conduction resistance in the closed state and the leakage current in the open state have been chosen as target specifications. The latter have also been used for the design of a further switch with the customized 5-V transistors, which has been used as a benchmark for the area occupation and current consumption. Moreover, an accelerated degradation test (ADT) showed that the proposed solution exhibits a comparable reliability.

This article is structured as follows: Section II compares the proposed switch architecture with a previous work presented in [5]; Section III describes the control and the clamping circuits; Section IV introduces the proposed case of study of a 5-V switch in 28-nm CMOS technology; Section V presents the measurements results; in Section VI, conclusions are drawn.

II. COMPARISON TO THE PREVIOUS SWITCH ARCHITECTURE

Bicciro et al. [5] presented a switch for input MUX able to handle voltages up to twice the maximum tolerable one by the adopted transistors, V_{max} (see Fig. 2).

This architecture is based on two parallel complementary signal paths, which consist of three series transistors each. Cascading is fundamental for distributing the voltage drop between the input and the output nodes when the switch is in the open state. In the same manner, it is important to set the intermediate nodes to fixed voltage by means of clamping circuits, in order not to leave them floating. The two R_P and

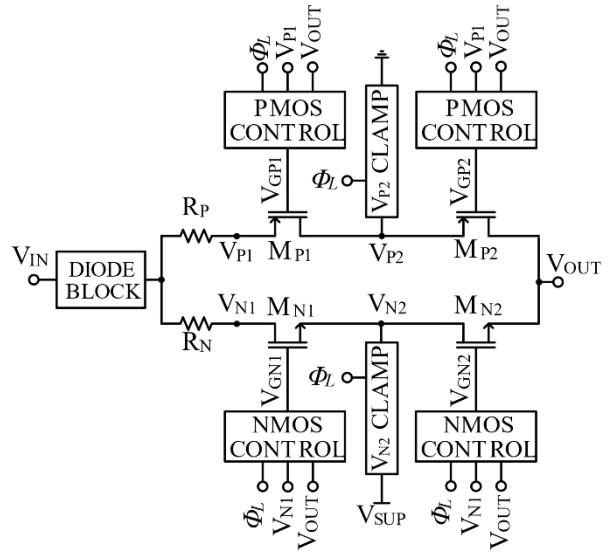


Fig. 3. Block scheme of the proposed switch with voltage scaled devices.

R_N series resistors further help in reducing the leakage current in off state, but they increase the closed state resistance value. The gate voltage of each transistor is opportunely generated by a control circuit in order to keep the voltages at the transistor terminals (the gate-drain, V_{GD} , the gate-source, V_{GS} , and the drain-source, V_{DS} , voltages) under the tolerable limit for any values of V_{IN} and V_{OUT} voltages.

The proposed switch architecture is shown in Fig. 3. It has been simplified with respect to the one presented in [5]. In fact, only two pass transistors are cascaded. Each of them sustains at least V_{max} , when the $|V_{IN} - V_{OUT}|$ voltage drop becomes equal to twice V_{max} . Moreover, the number of nodes to be monitored is reduced from 4 to 2. As a consequence, the number of clamping circuits is reduced by the same quantity, while the number of control circuits that drive the gate terminals of the switch transistors drops from 6 to 4. Therefore, a significant amount of current consumption is saved.

Finally, the control circuitry has been further optimized in order to save current.

III. CONTROL AND CLAMPING CIRCUITS

Both the previous and the proposed switches employ transistors able to withstand up to the half of the maximum signal V_{SUP} . Therefore, driving the gate terminals of the switch transistors with a signal reaching V_{SUP} exposes the transistors to dangerous electrical stress.

In order to avoid overvoltages, specific control blocks have been implemented for producing the gate voltages of the M_{N1} , M_{N2} , M_{P1} , and M_{P2} transistors (i.e., V_{GN1} , V_{GN2} , V_{GP1} , and V_{GP2} , voltages, respectively). Indeed, these gate voltages must be adapted to the actual values of V_{IN} and V_{OUT} voltages according to the value of the enabling signal, Φ_L ranging between 0 V and at least $V_{SUP}/2$. Thus, Φ_L and its complementary Φ_L^* signals are obtained by using standard logic gates supplied by a voltage equal to $V_{SUP}/2$. Similarly, the gate terminals of the pMOS transistors in the control circuit

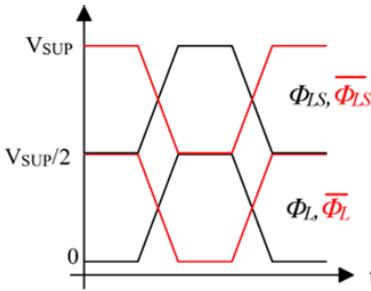


Fig. 4. Qualitative behavior of the enabling signals employed in the switch control blocks driving the gates of the nMOS (Φ_L) and the pMOS (Φ_{LS} and $\bar{\Phi}_{LS}$) switch transistors.

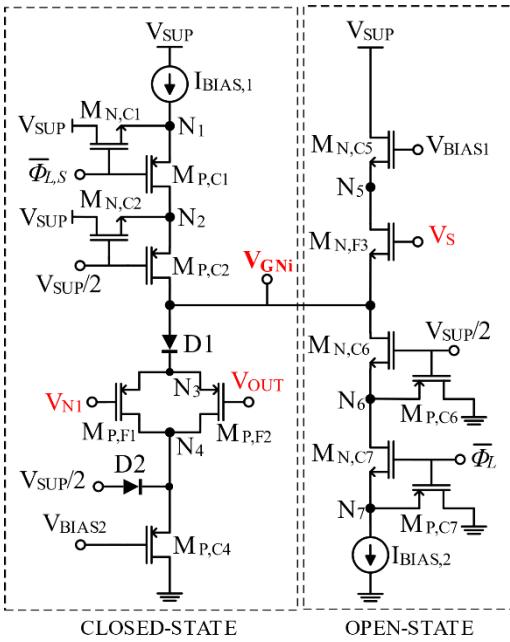


Fig. 5. Scheme of the i th nMOS transistor control block in Fig. 3.

blocks are driven by Φ_{LS} and its complementary $\bar{\Phi}_{LS}$ signals. The Φ_{LS} signal is obtained by shifting $\bar{\Phi}_L$ by means of a voltage shifter [6] that moves up it by $V_{SUP}/2$.

Fig. 4 shows the qualitative behavior of Φ_L and $\bar{\Phi}_L$ and Φ_{LS} and $\bar{\Phi}_{LS}$.

The scheme of each nMOS control block is shown in Fig. 5. For the pMOS control, a dual solution has been implemented.

The circuit consists of two branches, which operate alternatively for determining the gate voltage V_{GNi} of the i th nMOS transistor, M_{Ni} .

A. Closed-State Behavior

In closed state ($\Phi_L = V_{SUP}/2$), the branch on the right in Fig. 5 is switched off, while the one on the left is switched on. In fact, it results $\bar{\Phi}_L = 0$ and $\Phi_{LS} = V_{SUP}/2$, so that $I_{BIAS,1}$ is turned on, while $I_{BIAS,2}$ is turned off.

The gate voltage of each switch transistor has to be set to obtain the wanted conductivity. In order to guarantee safe operations, it is fundamental to keep the $|V_{GS}|$ voltage of each switch transistor below V_{MAX} . This implies that the V_{GNi} and V_{GPi} gate voltages of the switch transistors in Fig. 3 have to

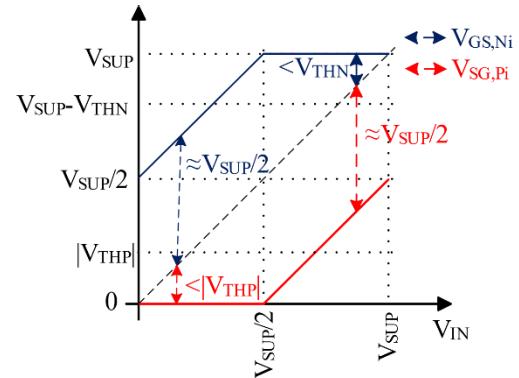


Fig. 6. Qualitative behaviors of the V_{GNI} and V_{GPi} gate voltages produced by the control blocks in Fig. 3.

be tailored according to the actual values of V_{IN} and V_{OUT} voltages.

Thus, V_{N1} and V_{OUT} voltages are tracked by $M_{P,F1}$ and $M_{P,F2}$ transistors, respectively, which operate as voltage followers (see Fig. 5). The lowest between V_{N1} and V_{OUT} voltages determines the V_{GNI} voltage. In other terms, the control block sets a control voltage, $V_{G,Ni,on}$, equal to a shifted copy of the actual source of the nMOS transistor as follows:

$$V_{G,Ni,on} = \min\{V_{N1}; V_{OUT}\} + V_{SG,MPF1,2} + V_D \quad (1)$$

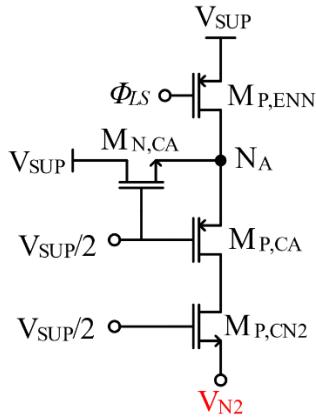
where $V_{SG,MPF1,2}$ is the source-gate voltage of $M_{P,F1}$ and $M_{P,F2}$ transistors, and V_D is the voltage drop across the D_1 diode.

The $V_{SG,MPF1,2} + V_D$ voltage is the overall gate-source voltage applied to the i th nMOS switch transistor. Thus, it has been set close to $V_{SUP}/2$ in order to achieve the minimum resistance, while not incurring in an excessive voltage drop across the transistor terminals. Observe that as V_{N1} ($= V_{IN}$) and V_{OUT} voltages exceed $V_{SUP}/2$, no headroom is available for the maximum overdrive. For V_{IN} and V_{OUT} voltages approaching V_{SUP} voltage, the complementary pMOS path takes care of limiting the overall switch resistance within the targeted value. Fig. 6 depicts the behaviors of both $V_{G,Ni,on}$ and $V_{G,Pi,on}$ voltages versus the input signal, V_{IN} ranging from 0 V up to V_{SUP} . Since $V_{G,Ni,on}$ assumes values between $V_{SUP}/2$ and V_{SUP} as V_{IN} and V_{OUT} vary, the transistors composing the control block circuit in Fig. 5 must be protected from incurring into not tolerable voltage drops at their terminals. Hence, the voltages of all nodes (N_1, N_2, \dots, N_7) of the control block reported in Fig. 5 must be prevented from assuming values that make transistors to experience excessive voltage drops at their ends. In detail, N_1 and N_2 node voltages assume values larger than $V_{SUP}/2$. In fact, as their voltages fall below $V_{SUP}/2$, $M_{N,C1}$ and $M_{N,C2}$ transistors start conducting opposing further voltage drops. Then, the $I_{BIAS,1}$ current generator and the $M_{N,C1}$ transistor are not exposed to voltage drops exceeding $V_{SUP}/2$. The $V_{SUP}/2$ voltage reference applied to the drain of $M_{N,C2}$ transistor and to the anode of the D_2 diode is generated by a resistor divider applied to the supply voltage, V_{SUP} . The N_3 node voltage follows the minimum voltage between gate voltages of $M_{P,F1}$ and $M_{P,F2}$ transistors. The drain voltage of these transistors, corresponding to the N_4 node, is kept around

TABLE I

VALUES OF V_S VOLTAGE IN THE nMOS AND pMOS CONTROL BLOCKS

	M_{N1}	M_{N2}	M_{P1}	M_{P2}
V_S	V_{N1}	V_{OUT}	V_{P1}	V_{OUT}

Fig. 7. Scheme of the clamping circuit employed for controlling the V_{N2} voltage in nMOS path in the open state of the switch.

$V_{SUP}/2$ by the $M_{P,C4}$ transistor, as long as it is on, i.e., for high values of V_{N1} and V_{OUT} voltages. In fact, the gate of the $M_{P,C4}$ transistor is set to V_{BIAS2} , which is about $V_{SUP}/3$.

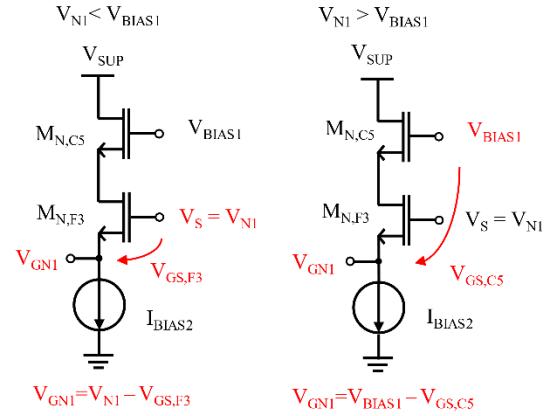
As V_{N1} and V_{OUT} voltages move to the ground, the D_2 diode keeps N_4 node voltage around its anode voltage, i.e., $V_{SUP}/2$.

N_5 , N_6 , and N_7 nodes belong to the right branch which is open state; then, it is not passed by a bias current. The $M_{N,F3}$ transistor is off as its gate voltage is set at V_S , corresponding to one between V_{N1} and V_{OUT} voltages according to Table I, while its source voltage corresponds to $V_{G,Ni}$. According to (1), we can say that the $V_{G,Ni}$ voltage is equal to the lowest between V_{N1} and V_{out} voltages, plus the V_{SG} of M_{P1} and M_{P2} transistors, and a voltage drop on the D_1 diode. Therefore, the $V_{G,Ni}$ voltage is certainly larger than V_S . In these conditions, the V_{GS} voltage of $M_{N,F3}$ transistor is below the threshold voltage.

N_6 node voltage is kept tied to $V_{SUP}/2$ by the $M_{N,C6}$ and $M_{P,C6}$ transistor couple, even if $V_{G,Ni}$ is varying. N_7 node voltage is close to N_6 node voltage since the $M_{P,C7}$ transistor is off.

B. Open-State Behavior

In the open state ($\Phi_L = 0$), the $V_{IN} - V_{OUT}$ voltage difference is carefully distributed across the switch transistors of each pMOS and nMOS path, so that none of them is exposed to an excessive drain-source voltage, in case of $|V_{IN} - V_{OUT}| > V_{MAX}$. For this purpose, the V_{N2} and V_{P2} voltages in Fig. 3 are clamped to the intermediate value, $V_{SUP}/2$, by a dedicated circuit. The circuit employed for controlling the potential of V_{N2} in the open state is shown in Fig. 7 and described in [5]. To control the V_{P2} voltage, a dual circuit architecture has been designed. This circuit is also fundamental for providing a low-resistive path for currents

Fig. 8. Simplified schemes of the open-state branch of the control circuit in Fig. 5 in the two possible cases $V_S < V_{BIAS1}$ (left) and $V_S > V_{BIAS1}$ (right).

leaking through M_{N1} , which would otherwise affect V_{OUT} voltage.

As concern the control circuit of the nMOS transistor in Fig. 5, in open state, the right branch is enabled, while the left branch is switched off. In fact, it results that $\Phi_{LS} = V_{SUP}$ and $\Phi_L = V_{SUP}/2$, so that $I_{BIAS,1}$ is disabled, while $I_{BIAS,2}$ is enabled.

To turn off the switch transistor, the $V_{G,Ni}$ voltage must be kept close to the actual source voltage, so that the V_{GSi} voltage does not exceed the threshold voltage value. For the M_{N1} transistor, the source node is given by the node at the lowest voltage between V_{N1} , which can assume any value in the range $[0, V_{SUP}]$ and V_{N2} , which is clamped at $V_{SUP}/2$ by the clamping circuit shown in Fig. 7. Instead, for the M_{N2} transistor, the source node is given by the node at the lowest voltage between V_{OUT} , which can assume any value in the range $[0, V_{SUP}]$ and V_{N2} . Hence, the biasing of the two switch transistors must be adapted to the values of V_{IN} and V_{OUT} , respectively. Two possible cases can occur depending on whether V_S voltage is higher or lower with respect to V_{BIAS1} , which is set to $2/3 V_{SUP}$. V_S voltage is equal to V_{N1} for M_{N1} and equal to V_{OUT} for M_{N2} (see Table I), as schematically reported in Fig. 8. The two cases are discussed in the following.

Case 1 ($V_S < V_{BIAS1}$): The $M_{N,F3}$ transistor is in saturation region. Its source voltage tracks V_S , so that $V_{G,Ni} = V_S - V_{GS,F3}$, where $V_{GS,F3}$ is the gate-source voltage of $M_{N,F3}$ transistor.

Case 2 ($V_S > V_{BIAS1}$): $M_{N,F3}$ transistor is pushed in triode region. Therefore, its source voltage cannot track V_S . $V_{G,Ni}$ voltage is clamped by source voltage of the $M_{N,C5}$ transistor, so that $V_{G,Ni} \cong V_{BIAS1} - V_{GS,C5} \cong V_{SUP}/2$ where $V_{GS,C5}$ is the gate-source voltage of $M_{N,C5}$ transistor.

In other terms, $M_{N,F3}$ and $M_{N,C5}$ transistors allow setting V_{GN1} , i.e., the gate voltage of the M_{N1} switch transistor, to the lowest value between $V_{IN} \cong V_{N1} = V_S$ and $V_{N2} \cong V_{BIAS1} - V_{GS,C5} \cong V_{SUP}/2$. For the M_{N2} transistor, similar consideration can be done by replacing V_{IN} with V_{OUT} .

Even in the open state, all the devices in Fig. 5 are protected from excessive voltage drops. Indeed, N_1 node voltage is set

at V_{SUP} by $M_{N,C1}$ and $M_{P,C1}$ transistors, so that $I_{\text{BIAS}1}$ is protected. The voltage of the N_2 node, corresponding to the drain of the $M_{P,C1}$ transistor, is clamped to about $V_{\text{SUP}}/2$ by the $M_{P,C2}$ and the $M_{N,C2}$ transistors. The N_3 and N_4 node voltages are clamped to about $V_{\text{SUP}}/2$ due to D_1 and D_2 , respectively. The N_5 node voltage is set to $V_{\text{BIAS}1} - V_{GS,C5} \cong V_{\text{SUP}}/2$; thus, both $M_{N,C5}$ and $M_{N,F3}$ transistors do not incur in excessive voltage drops between their own drain-source and gate-source nodes. N_6 node voltage is set to $V_{\text{SUP}}/2 - V_{GS,C6}$, where $V_{GS,C6}$ is the gate-source voltage of the $M_{N,C6}$ transistor designed to be less than $V_{\text{SUP}}/2$. Since the drain of $M_{N,C6}$ transistor, corresponding to $V_{G,Ni}$, is at least, $V_{\text{SUP}}/2$, the V_{DS} voltage does not exceed $V_{\text{SUP}}/2$.

N_7 node voltage is close to the N_6 node voltage, as the $M_{N,C7}$ transistor operates in the triode region. Therefore, the $I_{BIAS,2}$ current generator is biased with a voltage close to $V_{SUP}/2 - V_{GSC6}$ (i.e., less than $V_{SUP}/2$), keeping it in safe conditions.

Analogous considerations can be done for M_{P1} and M_{P2} transistors.

C. Comparison to the Control Circuit Reported in [5]

Fig. 9 shows the control circuit adopted in [5]. It includes only one bias current source, I_{BIAS} , whose current is deviated on the closed-state or in the open-state branch, according to the state of the switch.

The proposed control circuit includes two current sources, $I_{BIAS,1}$ and $I_{BIAS,2}$, one for each branch of the control circuit. These current generators are enabled according to the state of the circuit. They allow to separately optimize the current consumption for each state, enabling further current consumption reduction.

IV. PROPOSED CASE OF STUDY AND BENCHMARK SWITCH

The following specifications have been chosen as target for the design of the proposed switch, which safely handles signals varying over a range up to twice the nominal supply voltage of the employed transistors.

- Overall resistance R_{ON} between V_{IN} and V_{OUT} in the closed state lower than $2\text{ k}\Omega$.
 - Leakage current I_{LKG} lower than 90 nA when a maximum input current I_{IN} equal to 3 mA is provided in the open state [5]. Both cases of a drained (negative) and sourced (positive) I_{IN} have been considered. In other terms, the I_{LKG}/I_{IN} ratio must be less than 30 ppm .
 - Input signal range between 0 and 5 V ($=V_{SUP}$).

The adopted technology is a CMOS 28-nm technology with 2.5-V I/O transistors option. The same features have been targeted for the design of a 5-V switch with customized 5-V tolerant transistors: the aim is to use the latter as benchmark for a comparison in terms of area occupation, current demand, and aging speed.

The architecture employed for the switch based on voltage-resistant transistors is shown in Fig. 10 and it is described in [5]. The enabling signal Φ assumes the value 0 V (switch off) and 5 V, corresponding to V_{SUP} (switch on).

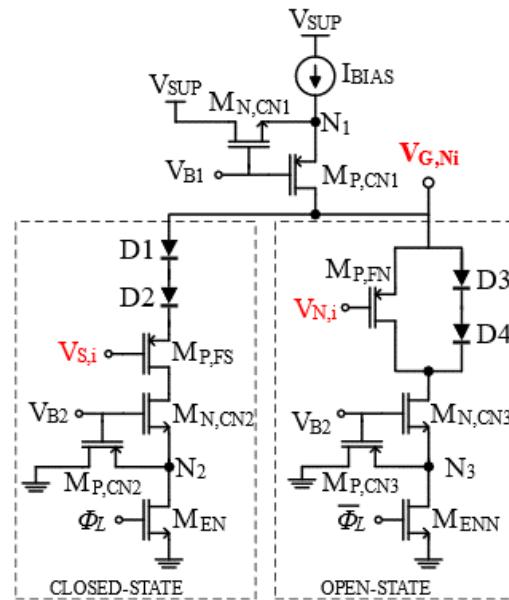


Fig. 9. Simplified scheme of the control block of the i th nMOS transistor of the switch proposed in [5].

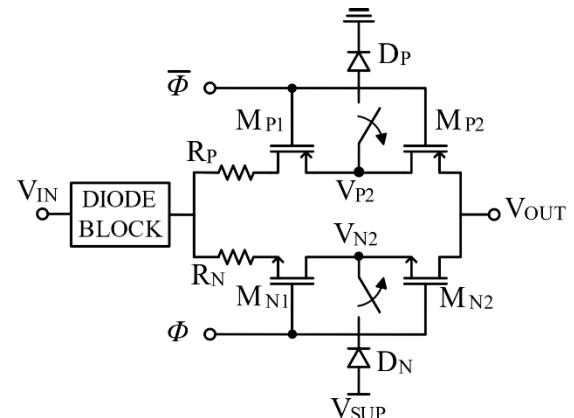


Fig. 10. Scheme of the switch made by high-voltage transistors.

V. CHARACTERIZATION OF THE CHIP WITH 5-V SWITCHES

The proposed and the benchmark switches with 5-V supply voltage have been fabricated in a 28-nm CMOS technology. Fig. 11 shows the layout of the chip and the package that contains it. Despite the inherent lower size of the 2.5-V devices, the proposed architecture required an area of about $7000 \mu\text{m}^2$ with respect to the $2500 \mu\text{m}^2$ of the benchmark architecture with 5-V transistors. This is due to the higher complexity of the circuitry for the generation of the enabling signals. Moreover, a cost in terms of current consumption of about $4 \mu\text{A}$ has to be paid for keeping operative the control blocks.

A. Closed-State Resistance

The conduction resistance, R_{ON} , of both types of switches has been evaluated according to the scheme in Fig. 12.

The switch-under-test (SUT) is biased with the V_{BIAS} voltage, while a test current, I_{TEST} , equal to 10 μ A is sourced.

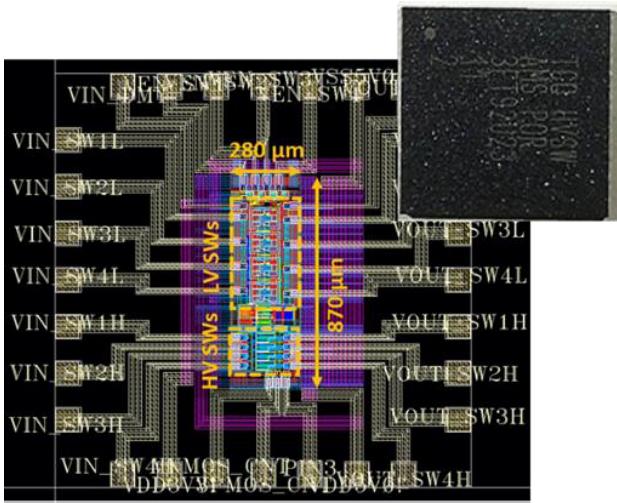


Fig. 11. Test-chip and layout.

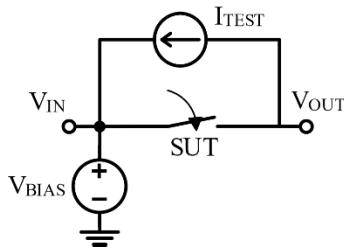


Fig. 12. Scheme for the evaluation of the conduction resistance of the SUT.

The V_{BIAS} voltage has been swept from 0 to V_{SUP} to characterize the R_{ON} over the whole signal range. The R_{ON} resistance for a given V_{BIAS} is

$$R_{ON}|_{V_{BIAS}} = \frac{V_{BIAS} - V_{OUT}|_{V_{BIAS}}}{I_{TEST}}. \quad (2)$$

Specifically, the 10-A I_{TEST} generator has been implemented with a commercial component (Texas Instruments LM334). The V_{BIAS} voltage has been varied in the range [0 V; V_{SUP}] with a function generator.

The characterization has been carried out over 15 chips obtained by different fabrication processes, which is given in detail as follows.

- 1) Five chips by the namely typical NMOS, typical PMOS (TT) process.
- 2) Five chips by the namely fast NMOS, fast PMOS (FF) process.
- 3) Five chips by the namely slow NMOS, slow PMOS (SS).

Moreover, measurements have been repeated with different supply voltages: 3, 5, and 5.5 V.

The resulting curves of the R_{ON} resistance versus V_{BIAS} voltage are plotted in Fig. 13. Values do not include the contribution of the current limiting resistor in the diode-protecting block. Hence, its value can be chosen, so that the maximum overall resistance of 2 kΩ is never reached. It is worth to notice that the proposed solution not only achieves the required R_{ON} but also the different curves show an analogous behavior with respect to the input voltage variations, even in case of supply and process variations.

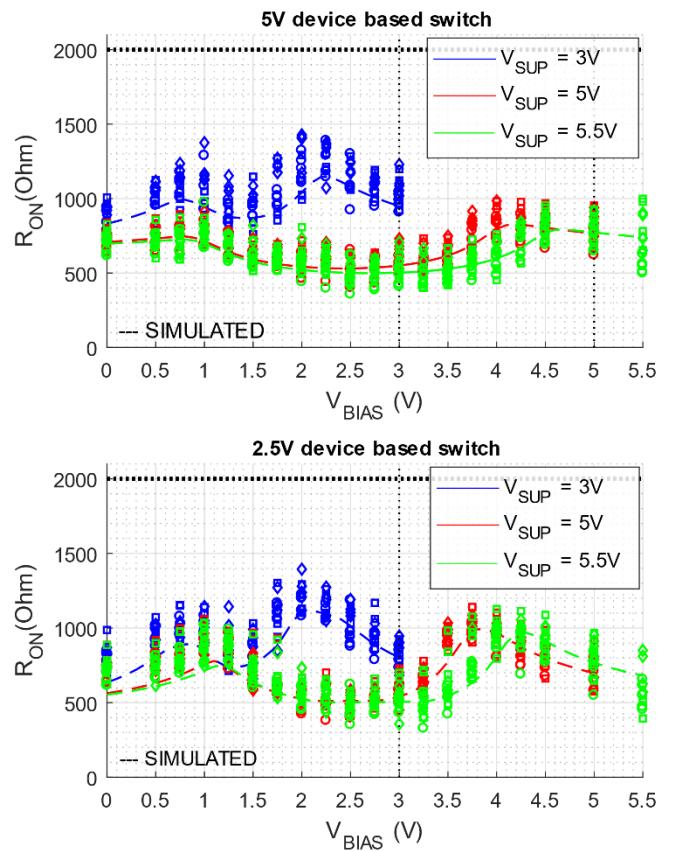


Fig. 13. Measured closed-state resistance R_{ON} versus biasing voltage V_{BIAS} of the switch with voltage-resistant (above) and voltage-scaled (below) devices when supply voltage V_{SUP} is 3, 5, and 5.5 V. A 15 samples (five in typical, five in fast, and five in slow fabrication process) have been measured. Measurements are compared to simulation results.

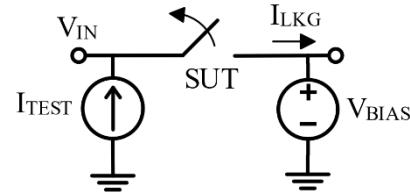


Fig. 14. Scheme for the evaluation of the leakage current of the SUT.

B. Leakage Current in the Open State

The scheme in Fig. 14 has been employed for the evaluation of the leakage current I_{LKG} when an input current I_{TEST} is applied to the SUT in the open state. Both cases of a sourced (positive) and drained (negative) current have been considered. The V_{BIAS} voltage has been chosen equal to 0 V or V_{SUP} .

In practical, V_{BIAS} generator is replaced by source meter, and the V_{TEST} current is provided by a power supply generator employed as a current source (Keithley 2400).

Moreover, measurements have been repeated with supply voltage V_{SUP} equal to 3, 5, and 5.5 V.

Table II reports the maximum values of the I_{LKG}/I_{TEST} current ratio: for the proposed architecture with 2.5-V devices, the current ratios are well below (more than one order of magnitude) the required 10 ppm, while for that with 5 V, they result close to the specification.

TABLE II

MAXIMUM RATIOS BETWEEN THE LEAKAGE CURRENT I_{LKG} AND THE TEST CURRENT I_{TEST} IN THE OPEN STATE FOR SWITCHES WITH 2.5- AND 5-V DEVICES WHEN V_{SUP} IS EQUAL TO 3, 5, AND 5.5 V

	I_{LKG}/I_{TEST} (ppm)	
	$I_{TEST} = +3\text{ mA}$	$I_{TEST} = -3\text{ mA}$
2.5 V devices		
3 V	0.03	0.055
5 V	0.16	0.5
5.5 V	0.39	2.3
5 V devices		
3 V	10	13
5 V	4.8	20
5.5 V	4.3	23

The proposed solution exhibits better values of leakage current with respect to the benchmark one for all the considered test conditions.

C. Accelerated Degradation Test

Even if the solution with voltage-scaled devices has been proven to achieve performances analogous to those of a switch with voltage-resistant devices, it is fundamental to guarantee a comparable lifetime. In other terms, the proposed architecture is feasible to replace the standard one only if it exhibits an adequate reliability toward the operating conditions. For this purpose, an ADT has been carried out: rather than estimating the expected lifetime with an accelerated lifetime testing (ALT), an ADT returns information on the decay process experienced by the device under examination [7]. In particular, the value of the conduction resistance R_{ON} has been chosen as the indicator of the correct operation of the switch. Then, a variation of 10% from the starting value has been set as the maximum tolerable for assuming a correct behavior of the switch.

Eight switches with 2.5-V devices and eight switches with 5-V devices fabricated using the TT process have been tested according to the scheme in Fig. 12. A slowly varying (0.1 Hz) full-scale sine has been applied to the input of each SUT, while a test current, I_{TEST} , is sourced in the closed state. The decay of the SUT is accelerated by employing a supply voltage, V_{SUP} , equal to 7 V, while V_{BIAS} is kept at 2.5 V, and I_{TEST} is set to $10\ \mu\text{A}$.

The R_{ON} resistance has been monitored once per day for seven days. Fig. 15 shows the variations of the R_{ON} resistance due to the ADT and the dashed curves have been obtained from the interpolation of the mean values at the end points. Average reductions of 16% and 22% have been experienced from the switches with voltage-resistant devices (SWH) and voltage-scaled devices (SWL), respectively. At the end of the ADT, no “hard” failure occurs in both types of switches, but the proposed solution shows a slightly less robust behavior with respect to the benchmark one. However, referring to the

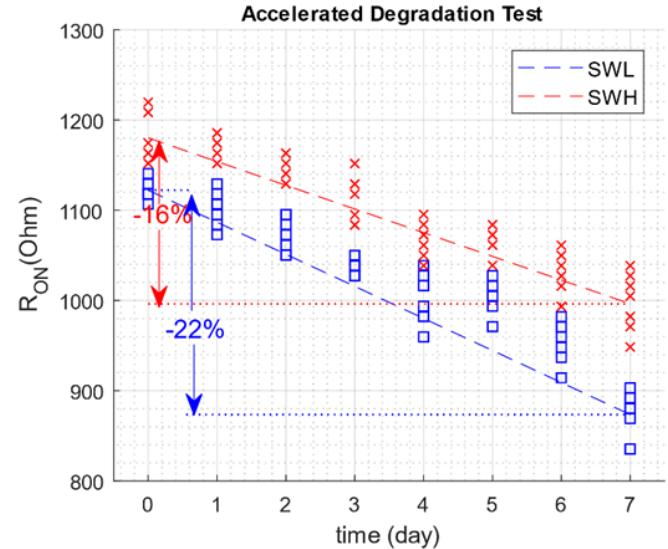


Fig. 15. Variations of the conduction resistance, R_{ON} , for both the switches with 2.5-V devices (SWL) and 5-V devices (SWH) during the ADT test. Dashed curves are the interpolations of the endpoint mean values.

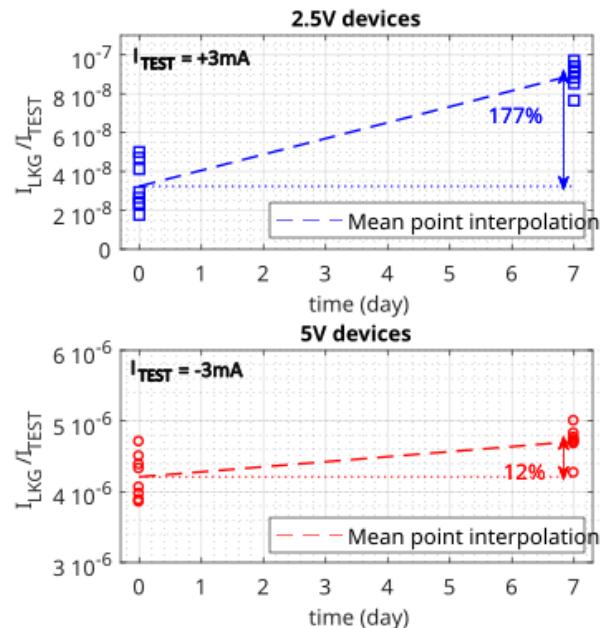


Fig. 16. Variations of the ratio between the leakage current, I_{LKG} , and the test current, I_{TEST} , for both switches with 2.5- and 5-V devices in the open state after the ADT. I_{TEST} is equal to $+3\text{ mA}$.

10% variation assumed as the maximum tolerable, the two architectures operate correctly for the same period, which is about four days. Thus, it represents a positive feedback on the reliability of the proposed solution.

The reduction of the conduction resistance can be reasonably ascribed to the reduction of the threshold voltage of the MOS transistors.

A further proof in favor of the speculation about the cause of the actual degradation of the switch is obtained from the evaluation of the leakage current, I_{LKG} , at the end of the ADT by means of the test scheme in Fig. 14: considering a positive

TABLE III
COMPARISON OF THE PROPOSED LV SWITCH WITH
OTHER STATE-OF-THE-ART WORKS

Parameter	This Work	[2]	[5]	[9]	[10]	[11]
Power Consumption [μW]	20	$6 \cdot 10^4$	38.4	---	$7 \cdot 10^4$	92
Current Consumption [μA]	4	200	40	90	$5.8 \cdot 10^3$	15
Area [mm 2]	0.007	0.267	0.0021	0.26	---	0.67
Conduction resistance [k Ω]	0.7	---	1.4	0.7	0.018	0.0039
I_{LKG} [nA]	6.9	0.030	24.6	60	---	12
V_{DD} [V]	2.5	5	0.96	3.3	12	2.7-5
V_{MAX} [V]	5	300	1.76	120	200	5
Technology node	28nm	65nm	28nm	HV 0.35 μm	SOI	BCD 0.18 μm
ADT	yes	yes	none	none	none	none

test current I_{TEST} of 3 mA, the ratios $I_{\text{LKG}}/I_{\text{TEST}}$ of both types of switches underwent a sensible variation (see Fig. 16). Both dashed curves, obtained from the interpolation of the mean values at the beginning and at the end of the test, show an increase of the leakage of 177% and 12% for the switches with 2.5- and 5-V devices, respectively. This is a further proof that the degradation of the switch is reasonably due to the reduction of the threshold voltage. Observe that the average ratio for the proposed solution is still about two orders of magnitude lower than that of the solution with voltage-tolerant devices.

The ADT demonstrated that the proposed solution is competitive with the standard approach even in terms of reliability.

This finally proved the feasibility of employing voltage-scaled devices in the high-voltage switch implementation, while not incurring in a faster decay due to stressing operating conditions.

D. Comparison to the State of the Art

A comparison between the proposed switch with other works at the state-of-the-art is shown in Table III. The proposed work and that one presented in [2] show the results of reliability test, which is important to validate the design approach as transistors undergo significant voltage stresses. Most of the works from literature do not report data about reliability.

The proposed work is well compared in terms of current consumption.

With respect to the previous design reported in [5], we improved the current consumption of a 10 factor, passing from 40 μA of the old design to 4 μA of the proposed design.

The proposed design occupied more than three times the area of the previous design. Indeed, even if the same technology has been adopted, in this design, we used the 2.5-V MOS transistors, which intrinsically occupy more die area as their minimum length is 60 nm, i.e., more than twice larger than

the minimum one (28 nm) of the core transistors used in the previous design.

VI. CONCLUSION

This work proposed the architecture of a switch for input channel MUXs for signals over a range up to twice the nominal supply voltage of the employed transistors. In particular, due to the use of adaptive biasing, diode protection, and voltage shifting techniques, a 5-V switch has been implemented with the 2.5-V transistors available in the fabrication option of the employed 28-nm CMOS technology rather than recurring to customized and costly 5-V tolerant transistors. The proposed architecture has been demonstrated to achieve the required performances in terms of conduction resistances (lower than 2 k Ω) and current leakage in the open state (lower than 30 ppm of the applied input current). With respect to a standard switch based on the customized 5-V tolerant transistors, a larger area (less than three times) and a current demand of 5 μA are required. However, the proposed approach showed adequate reliability, as demonstrated by the variation of the conduction resistance during an ADT. The proposed solution has been proven effective for replacing the switch designed with the standard approach with customized voltage-tolerant devices in terms of both performance and robustness to prolonged operations.

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