A High-Speed Low-Noise Comparator With Auxiliary-Inverter-Based Common-Mode Self-Regulation for Low-Supply-Voltage SAR ADCs

Lei Qiu, Tianyi Meng, Bingbing Yao, Zihao Du, and Xiaohua Yuan

***Abstract*— A high-speed low-noise comparator with an auxiliary inverter-based (AIB) preamplifier is proposed in this brief. The preamplifier adopts an inverter-based input pair without tail transistors, which is well-suitable for low-supply-voltage applications, especially in deep submicrometer technologies. Moreover, it achieves high bandwidth and low noise with high current efficiency. Dynamic common-mode feedback combined with a secondary inverter-based input pair regulates the output common-mode (CM) voltage of the preamplifier by itself against PVT and input CM voltage sensitivity without complex control logic and quiescent current. Embedded in a 200 MS/s 16-bit successive-approximation-register (SAR) analog-to-digital converter (ADC) in standard 28-nm CMOS technology, the proposed comparator achieves a 68.1-ps delay at a 50-μV differential input voltage and a root-mean-square input-referred noise of 45.6 μV_{rms} under the 1-V power supply.**

***Index Terms*— Analog-to-digital converter (ADC), common-mode feedback (CMFB), inverter amplifier, latch-type comparator, low supply voltage.**

I. Introduction

Technology scaling makes the successive-approximation-register (SAR) analog-to-digital converter (ADC) one of the most promising architectures to be used in high-performance applications owing to its mostly digital architecture. However, without preamplification, the tradeoff between the bandwidth and noise of commonly used comparators limits the performance of ADCs, especially in high-speed and high-resolution scenarios. Meanwhile, the decreasing supply voltage of modern technologies poses great challenges for designing low-noise preamplifiers with high bandwidths.

Efforts have emerged to improve the performance of preamplifiers to realize high-speed and low-noise comparators. Inverter-based preamplifiers [1], [2], [3], [4] have become popular owing to their high current efficiencies (50% better) [3] and good submicrometer CMOS technology adaptability. However, they suffer from PVT and input common-mode (CM) sensitivity. Furthermore, their pseudodifferential features result in no CM rejection. Therefore, CM feedback (CMFB) is required. Fig. 1 shows an inverter-based preamplifier with conventional CMFB using two tail transistors, which controls the pull-up and push-down current to regulate output CM voltage. Several comparator designs are based on this idea [1], [2], [3]. However, with decreasing supply voltage, it is more difficult to guarantee that both the input and tail transistors are in the saturation region. Moreover, some extra circuits are added in critical signal paths to realize high CM rejection, such as operational amplifiers [1], timing-control switches, and capacitors [2], [3], which increase complexity, introduce additional noise, and limit bandwidth. A dynamic inverter-based preamplifier without CMFB circuits for low-speed applications is proposed in [4], which is not suitable for high-speed applications with the presence of complicated timing and large capacitive loading maintaining CMRR.

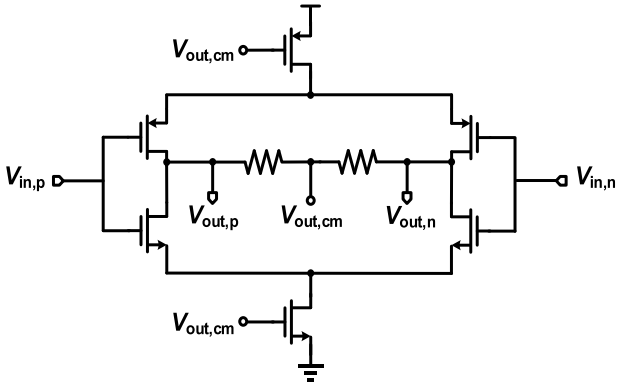

Fig. 1. Inverter-based preamplifier with conventional CMFB.

This brief presents a high-speed and low-noise comparator with an auxiliary inverter-based (AIB) preamplifier (Fig. 2). By employing a self-regulated CMFB, which has a negligible effect on the bandwidth and noise of the signal path, PVT, and input CM insensitivity and high rejection on CM variation are achieved simultaneously. This brief is organized as follows. Section II presents the principle and implementation of the proposed AIB preamplifier. The prototype comparator implementation is described in Section III. Section IV shows the simulation results. Finally, conclusions are drawn in Section V.

II. Proposed Preamplifier in Comparator

A. Auxiliary Inverter-Based (AIB) Preamplifier

The structure of the proposed AIB preamplifier is presented in Fig. 2. M_1–M_4 form a static pseudodifferential inverter amplifier, which not only suits well for low-supply-voltage applications, but also isolates the signal-dependent kickback noise from the dynamic latch. A secondary inverter-based input pair M_5–M_8, which is a quarter of the size of the main inverter amplifier for reducing the impact on the gain and noise of the preamplifier, is introduced to adjust the output CM voltage. In the proposed AIB preamplifier design, all transistors are biased in the saturation region once the CMFB loop converges. With the decrease of V_{gs} during operation, the transistors are further pushed into the vicinity of the week-inversion region. For simplicity of analysis, we assume that all transistors always work in the saturation region. The gain can be expressed as

$$A_V = G_m R_{out} = (g_{m1} + g_{m3}) \cdot (r_{o1} \parallel r_{o3} \parallel r_{o5} \parallel r_{o7}) \quad (1)$$

where $g_{m1,3}$ is the transconductance of $M_{1,3}$ and $r_{o1,3,5,7}$ is the equivalent resistor of $M_{1,3,5,7}$ while considering the channel-length modulation. As $M_{5,7}$ is 4× smaller than $M_{1,3}$ $r_{o1,3}$ can be ignored.

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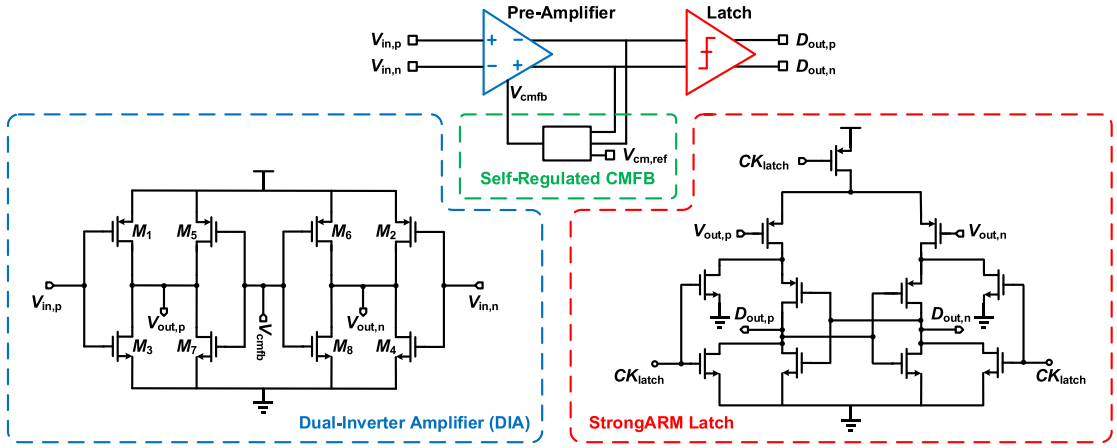

Fig. 2. Schematic of the proposed comparator with the AIB preamplifier and self-regulated CMFB.

Taking output node capacitance C_{out} into consideration, the bandwidth of the AIB preamplifier can be calculated as

$$\text{BW} = \frac{1}{2\pi R_{\text{out}} C_{\text{out}}} = \frac{G_m}{2\pi A_{V,\text{dc}} C_{\text{out}}} = \frac{C_{\text{gs1}}}{A_{V,\text{dc}} C_{\text{out}}} \frac{g_{m1}}{2\pi C_{\text{gs1}}} + \frac{C_{\text{gs3}}}{A_{V,\text{dc}} C_{\text{out}}} \frac{g_{m3}}{2\pi C_{\text{gs3}}}. \tag{2}$$

Therefore

$$\text{BW} = \frac{1}{A_{V,\text{dc}}} \left(\frac{C_{\text{gs1}}}{C_{\text{out}}} f_{\text{T,pMOS}} + \frac{C_{\text{gs3}}}{C_{\text{out}}} f_{\text{T,nMOS}} \right) \tag{3}$$

where f_{T} is the transit frequency, and $C_{\text{gs1,3}}$ is the capacitance between the gate and the source of $M_{1,3}$. $A_{V,\text{dc}}$ represents the dc gain of the AIB preamplifier. Owing to the absence of tail transistors, the AIB preamplifier achieves a larger V_{gs} at the same input CM voltage, and thus, a larger f_{T}. With an input CM voltage of 500 mV, the postlayout simulation results show that $f_{\text{T,pMOS}} = 105.4$ GHz and $f_{\text{T,nMOS}} = 136.6$ GHz. C_{out} mainly comprises junction and parasitic capacitances; C_{out} is $\sim 1.9\times$ larger than $C_{\text{gs1,3}}$. The proposed AIB preamplifier can achieve a higher bandwidth with the same $A_{V,\text{dc}}$ (~ 7) owing to larger overdrive voltage ($V_{\text{ov}} = V_{\text{gs}} - V_{\text{th}}$) and smaller loading capacitances. The junction and parasitic capacitances at nodes $D_{\text{out},p}$ and $D_{\text{out},n}$ are both ~ 13 fF.

The noise of a transistor is modeled using a current source and described as power spectral density The differential input-referred noise voltage $V_{n,\text{in}-\text{diff}}$ can be derived as

$$\overline{V_{n,\text{in-diff}}^2} = \frac{\overline{I_{n,d}^2}}{(g_{m1} + g_{m3})^2} + \frac{\overline{V_{n,\text{latch}}^2}}{(g_{m1} + g_{m3})^2 R_d^2} \tag{4}$$

where $I_{n,d}$ is aggregated noise current of the preamplifier, including channel thermal noise current and flicker noise current. $V_{n,\text{latch}}$ is the noise voltage contributed by the latch seen at the input of the latch. R_d is the equivalent output impedance of the preamplifier. As the transconductances of nMOS and pMOS are combined, approximately $\sqrt{2}\times$ reduction in $V_{n,\text{in-diff}}$ could be achieved. According to (4), the preamplifier would dominate the input-referred noise due to the high gain of $(g_{m1} + g_{m3})R_d$. The simulated integrated (from 1 Hz to 100 GHz) noise contribution of the preamplifier (M_1–M_8) is listed in Table I.

TABLE I
INTEGRATED NOISE CONTRIBUTION SUMMARY

M1(Thermal)	10.5%	M5(Thermal)	4.1%
M2(Thermal)	10.5%	M6(Thermal)	4.1%
M3(Thermal)	11.7%	M7(Thermal)	2.4%
M4(Thermal)	11.7%	M8(Thermal)	2.4%
M3(Flicker)	16.1%	M1(Flicker)	0.7%
M4(Flicker)	16.1%	M2(Flicker)	0.7%
Others (Overall)	8.9%		

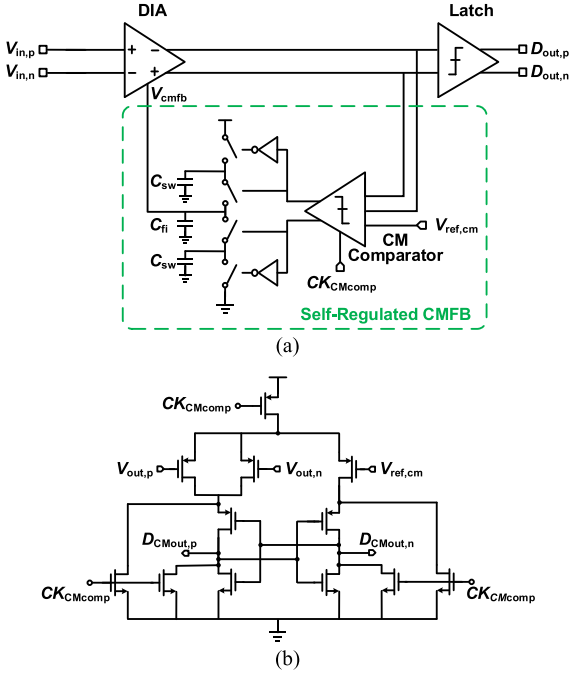

Fig. 3. (a) Schematic of the proposed self-regulated CMFB. (b) CM comparator is based on the StrongARM comparator.

B. Self-Regulated CMFB

To build a robust preamplifier against PVT and input CM voltage variations, a self-regulated CMFB is proposed, which comprises a CM comparator and a low-pass filter, as shown in Fig. 3(a). The implemented CM comparator is used to detect the output CM voltage of the AIB preamplifier ($V_{\text{out, CM}}$), as shown in Fig. 3(b); it judges whether $V_{\text{out,CM}}$ is higher or lower than the reference CM voltage

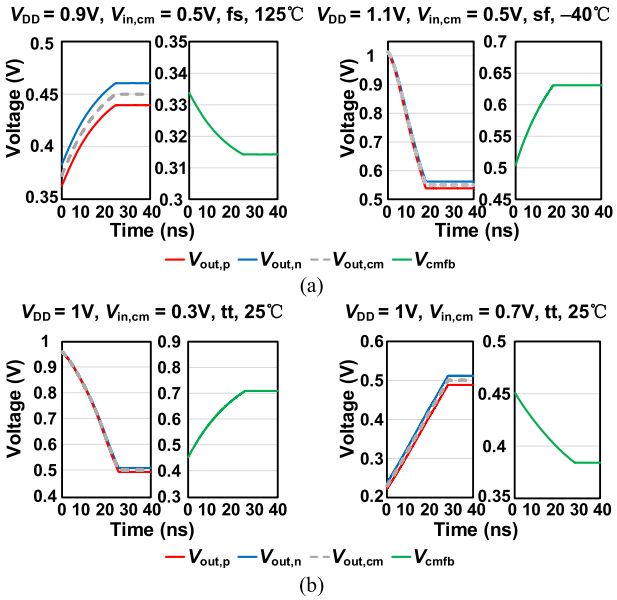

Fig. 4. Preamplifier behavior simulation with (a) PVT variations and (b) input CM voltage variations.

$V_{ref,CM}$, which is set to $V_{DD}/2$ to guarantee that the output CM voltage of the AIB preamplifier is $V_{DD}/2$. If $V_{out,\,CM}$ is higher than $V_{ref,CM}$, the decision of the CM comparator is positive, and then, the charge stored in C_{sw} is added to C_{fi} and V_{CMFB} increases. When V_{CMFB} increases, the strength of nMOS ($M_{7,8}$) becomes higher than that of pMOS ($M_{5,6}$), which makes the push-down current higher than the pull-up current. Consequently, $V_{out,CM}$ decreases and vice versa. Subsequently, $V_{out,CM}$ approaches $V_{ref,CM}$, and V_{CMFB} converges. Additionally, C_{fi} is larger than C_{sw} to guarantee the stability of the loop.

Schematic simulation results under different PVT corners are shown in Fig. 4(a). Taking two extreme cases (V_{DD} = 0.9 V, fs corner, 125 °C and V_{DD} = 1.1 V, and sf corner, −40 °C) as examples, the self-regulated CMFB generates different V_{CMFB}, which are fed to the secondary inverter input pair to regulate the output CM voltage at $V_{DD}/2$. Therefore, with the fixed input CM voltage, the input pair of the AIB preamplifier is always in the saturation region under PVT variations. Similarly, the AIB preamplifier also works well when the input CM voltage varies, as shown in Fig. 4(b). Owing to the parallel feature of the AIB preamplifier, a large input CM range can be allowed. If the input CM voltage is decreased below $V_{th,nMOS}$, $M_{3,4}$ is OFF and $M_{7,8}$ is driven by V_{CMFB} to act as a current source for ensuring that the operation region of $M_{1,2}$ and the output CM voltage is unchanged. The same mechanism works when the input CM voltage is higher than $V_{DD} - |V_{th,pMOS}|$. If sizes of M_{5-8} are too small to provide enough current when M_{5-8} act as current sources, the output CM voltage cannot be regulated at $V_{DD}/2$. Compared with the inverter-based preamplifier with the conventional CMFB (in Fig. 1), the input CM range of the proposed AIB preamplifier with self-regulated CMFB is around $2V_{ov}$.

C. CM Variation Rejection

The proposed preamplifier is followed by a latch. The input CM voltage variation of the latch leads to an offset of the comparator and, thus, to nonlinearity. By employing a self-regulated CMFB, $V_{out,CM}$ is adjusted to the reference CM voltage $V_{ref,CM}$. In this case, high CM variation rejection is guaranteed. Meanwhile, two types of CM variations should be analyzed carefully. Once the CMFB converges, the outputs of the CM comparator toggle between positive and negative, which results in the fluctuation of V_{CMFB} and then engenders output CM variation. For each cycle k, the feedback voltage is given as

$$V_{CMFB}(k+1) = V_{CMFB}(k)\frac{C_{fi}}{C_{sw}+C_{fi}} + V_{sw}\frac{C_{sw}}{C_{sw}+C_{fi}} \tag{5}$$

where V_{sw} is the voltage supplied for charge sharing. In the conventional case, $V_{sw} = V_{DDs}$ (CM comparator outputs are high) or V_{ss} (CM comparator outputs are low). The step of V_{CMFB} can be expressed as

$$\begin{aligned} V_{CMFB,step}(k+1) &= V_{CMFB}(k+1) - V_{CMFB}(k) \\ &= [V_{sw} - V_{CMFB}(k)]\frac{C_{sw}}{C_{sw}+C_{fi}}. \end{aligned} \tag{6}$$

To achieve a small fluctuation of V_{CMFB}, we can make $C_{fi} \gg C_{sw}$ or $V_{sw} = V_{CMFB}(k)$. Accordingly, minimum-sized transistors are used as switches for minimum parasitic capacitances, thus allowing a smaller C_{fi} for area-saving [6]. The systematical offset of the CM comparator contributes to CM variation. Fig. 5 shows the simulated CM offset depending on the differential input voltage of the CM comparator which is input-signal-dependent in SAR ADCs, with 0.5-V CM voltage. As the differential input signal amplitude decreases, the CM offset is reduced. Each SAR step reduces the maximum differential output voltage amplitude

$$V_{out,diff} = \frac{V_{ref}}{2^N}A_{V,dc} \tag{7}$$

where V_{ref} is the reference voltage of the SAR ADC and N is the number of finished SAR steps. Therefore, the CM detection is activated after the sixth step in the proposed SAR ADC, where the signal-dependent CM variation due to the systematical offset of the CM comparator is insignificant. Hence, the random CM variation hardly influences the critical signal path.

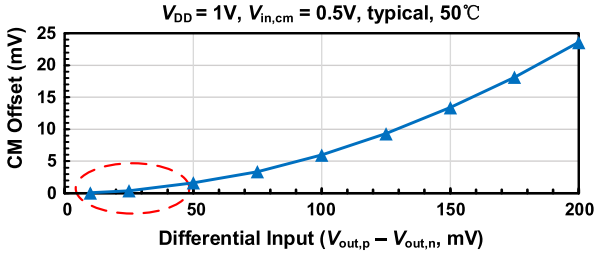

Fig. 5. CM offset of the CM comparator with different differential input voltages.

III. Proposed Comparator Implementation

As shown in Fig. 2, the proposed comparator comprises the AIB preamplifier stage with a CMFB followed by a latch. The latch used here is a dynamic sense-amplifier latch [7], also known as the StrongARM latch [8]. According to the detailed analysis described in [9], all noise contributions in a StrongARM latch have a kT/C form with some additional factors, which can be reduced by scaling the transistor sizes at the expense of longer decision times [10]. However, with the proposed AIB preamplifier, the noise and offset of the latch can be decreased by the gain of the AIB preamplifier when referred to an input of the comparator. In this design, the gain of the AIB preamplifier is above 6 under PVT variations, which is large enough to suppress the latch stage noise and offset. At the same time, the delay of the comparator can be expressed as

$$t_{delay} = t_{DIA} + t_{latch}. \tag{8}$$

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

	This Work *		2020 JSSC [4]		2020 SSC-L [11]	2018 JSSC [3]	2018 JSSC [12]
Featured Architecture	**Proposed AIB +StrongARM**	StrongARM	Dynamic FIA +StrongARM	StrongARM	Cross-coupled pre-amp + latch	Inverter-based pre-amp + latch	Dynamic Bias comparator
Process [nm]	**28**	28	180	180	65	14	65
Supply [V]	**1**	1	1.2	1.2	1	0.85	1.2
Noise [μV_{rms}]	**45.6**	72.2	46	62	220	76	400
Delay [ns] @50μV_{in}	**0.068**	0.083	-	-	13	0.152	0.4
Area [μm^2]	**550**	300	9800	7700	1025	-	125
Input CM Insensitivity	**Yes**	No	Yes	No	No	Yes	No

* *Post layout simulation results*

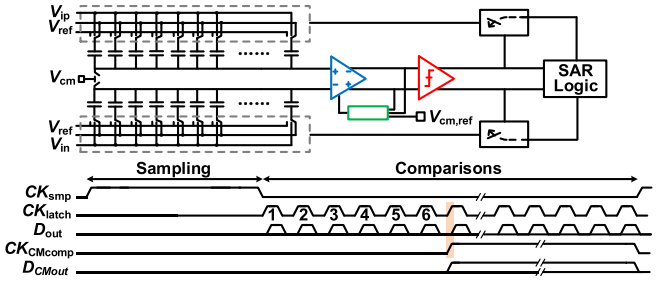

Fig. 6. Architecture and timing diagram of the SAR ADC.

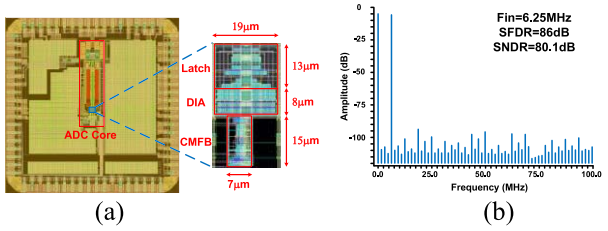

Fig. 7. (a) Layout of the proposed comparator and ADC. (b) Fast Fourier transform (FFT) plot with 6.25-MHz input at 200 MS/s.

Owing to the high bandwidth of the AIB preamplifier, t_{AIB} contributes 10% of t_{delay}. Additionally, the gain of the AIB preamplifier greatly reduces t_{latch} by amplifying the input signal amplitude of the latch. The architecture and timing diagram of an SAR conversion cycle is shown in Fig. 6. The sampling clock CK_{smp} is 1/3 of the total conversion period. The falling edge of CK_{smp} initiates the first comparison by triggering CK_{latch}. The latch resets ($CK_{latch} = 0$) when a completed decision D_{out} is made. As described in Section II-C, the clock of the CM comparator CK_{CMcomp} is triggered at the sixth comparison and resets until the next SAR conversion cycle begins. The output CM voltage converges at $V_{DD}/2$ after several SAR conversion cycles. Thus, only an additional low-frequency clock signal CK_{CMcomp} (200 MHz) is added and the CMFB regulates output CM voltage by itself. Moreover, the operation of SAR conversion will not be disturbed by CMFB, thus guaranteeing high-speed operation of the comparator.

IV. SIMULATION RESULTS

To demonstrate the proposed comparator, a design example of a 200 MS/s 16-bit SAR ADC is verified in 28-nm CMOS technology. Layout photographs of the ADC and the proposed comparator are shown in Fig. 7(a). The unit cap size is 3 fF, and the single-ended DAC is 6 pF. The TRAN noise simulation with setting the noise bandwidth $f_{min} = 10$ kHz and $f_{max} = 100$ GHz, respectively. Based on the postlayout simulation [Fig. 7(b)], the ADC achieves an SNDR of 80.1 and a 86-dB SFDR with 1.8-$V_{pp,diff}$ input amplitude at Nyquist under 1-V supply voltage. The input CM voltage of the ADC is 0.5 V.

Fig. 8 shows the gain, bandwidth, rms input-referred noise, and power of the AIB preamplifier under PVT corners with the output CM setting at $V_{DD}/2$ via CMFB. Fig. 9(a) shows the result of 100 points postlayout Monte Carlo simulation of the proposed comparator, including both the preamplifier and latch. The mean of the offset is 365.1 μV and the standard deviation is 1.15 mV. Fig. 9(b) shows the cumulated density function (CDF) curve plot. To make a fair comparison between the conventional StrongARM and the proposed

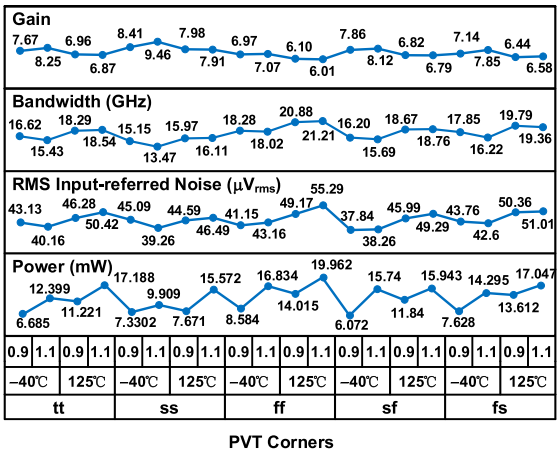

Fig. 8. Simulated gain, bandwidth, rms input-referred noise, and power of the AIB preamplifier under different PVT corners.

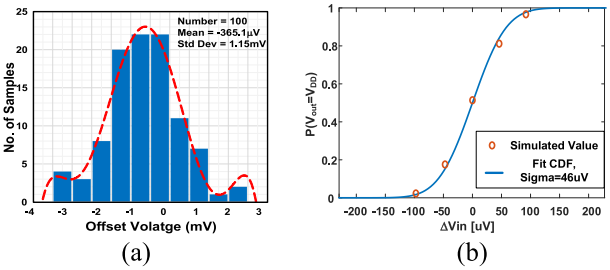

Fig. 9. (a) Postlayout Monte Carlo simulation results of the proposed comparator. (b) Simulated and fit CDF curve plot.

comparator, their input pairs are used with the same size (W/L = 96 μm/30 nm). Fig. 10 shows the simulated delay versus different ial input voltage. The delay is the time between the clock edge and the instance when V_{out} crosses $1/2V_{DD}$. As shown in Fig. 10, the $V_{in,CM}$ insensitivity of the proposed comparator is better than that

TABLE III

COMPARATOR PERFORMANCE IN SAME 28-NM CMOS. (A) SAME INPUT REFERRED NOISE $V_{n,in}$ $V_{DD} = 1$ V, $V_{in,cm} = 0.5$ V, TYPICAL, 50 °C. (B) SAME SPEED f_{clk} & NOISE $V_{n,in}$ $V_{DD} = 1$ V, $V_{in,cm} = 0.5$ V, TYPICAL, 50 °C

(a)

Architecture	$f_{clk,max}$ [Hz]	P [mW]	C_{in} [fF]	$V_{n,in}$ [mV$_{rms}$]
This Work	**8G**	9.86	69.1	0.046
FIA+StrongARM Based on [4]	**750M**	1.01	69.1	0.045
StrongARM	**5G**	11.59	203.0	0.048

(b)

Architecture	C_{in} [fF]	f_{clk} [Hz]	$V_{n,in}$ [mV$_{rms}$]	P [mW]
This Work	**69.1**	5G	0.046	9.83
FIA+StrongARM Based on [4]	**334.2**	5G	0.051	9.94
StrongARM	**203.0**	5G	0.048	11.59

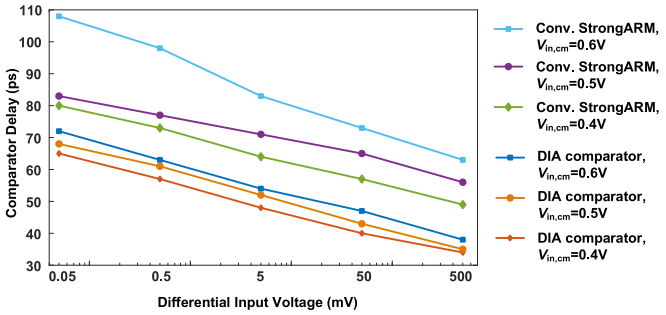

Fig. 10. Simulated comparator delays versus input voltages.

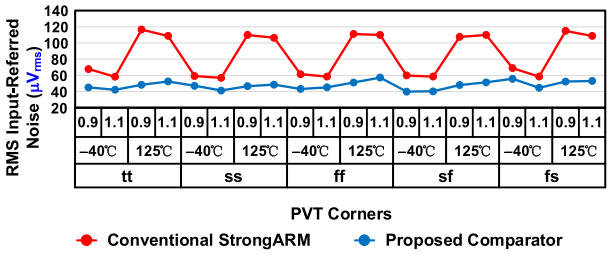

Fig. 11. Simulated comparator rms input-referred noise under different PVT corners.

of the conventional StrongARM (pMOS input-based). A dc input voltage is applied to simulate the rms input-referred noise. By fitting the output of the comparator to a Gaussian cumulative distribution function, the simulation results can be extracted (Fig. 11). Table II summarizes the performance of the prototype design and compares it with other state-of-the-art comparators. To make the comparison reasonable and fair, the work in [4] and conventional StrongARM are both rebuilt in 28-nm CMOS technology. And comparisons are listed in Table III. Table III(a) shows that under the same noise specification, the proposed preamplifier could achieve a better bandwidth (8 GHz). Additionally, under the same noise and speed performance [Table III(b)], the proposed preamplifier exhibits less capacitive loading (69.1 fF), which is critical for the design of high-speed high-resolution SAR ADC.

V. CONCLUSION

The AIB preamplifier achieves high current efficiency, high bandwidth, and low input-referred noise. Meanwhile, this preamplifier is well-suited for low-supply-voltage applications. The dynamic self-regulated CMFB achieves input CM and PVT insensitivity without complex control logic.

REFERENCES

[1] C. C. Lee, C.-Y. Lu, R. Narayanaswamy, and J. B. Rizk, "A 12 b 70 MS/s SAR ADC with digital startup calibration in 14nm CMOS," in *Proc. Symp. VLSI Circuits (VLSI Circuits)*, Jun. 2015, pp. C62–C63.

[2] B. Verbruggen, K. Deguchi, B. Malki, and J. Craninckx, "A 70 dB SNDR 200 MS/s 2.3 mW dynamic pipelined SAR ADC in 28 nm digital CMOS," in *Symp. VLSI Circuits Dig. Tech. Papers*, Honolulu, HI, USA, Jun. 2014, pp. 1–2.

[3] D. Luu et al., "A 12-bit 300-MS/s SAR ADC with inverter-based preamplifier and common-mode-regulation DAC in 14-nm CMOS FinFET," *IEEE J. Solid-State Circuits*, vol. 53, no. 11, pp. 3268–3279, Nov. 2018.

[4] X. Tang et al., "An energy-efficient comparator with dynamic floating inverter amplifier," *IEEE J. Solid-State Circuits*, vol. 55, no. 4, pp. 1011–1022, Apr. 2020.

[5] W. Jiang, Y. Zhu, M. Zhang, C.-H. Chan, and R. P. Martins, "A temperature-stabilized single-channel 1-GS/s 60-dB SNDR SAR-assisted pipelined ADC with dynamic Gm-R-based amplifier," *IEEE J. Solid-State Circuits*, vol. 55, no. 2, pp. 322–332, Feb. 2020.

[6] L. Kull et al., "A 10 b 1.5 GS/s pipelined-SAR ADC with background second-stage common-mode regulation and offset calibration in 14 nm CMOS FinFET," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 474–475.

[7] T. Kobayashi, K. Nogami, T. Shirotori, and Y. Fujimoto, "A current-controlled latch sense amplifier and a static power-saving input buffer for low-power architecture," *IEEE J. Solid-State Circuits*, vol. 28, no. 4, pp. 523–527, Apr. 1993.

[8] B. Razavi, "The StrongARM latch [a circuit for all seasons]," *IEEE Solid-State Circuits Mag.*, vol. 7, no. 2, pp. 12–17, Spring 2015.

[9] P. Nuzzo, F. De Bernardinis, P. Terreni, and G. Van der Plas, "Noise analysis of regenerative comparators for reconfigurable ADC architectures," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 6, pp. 1441–1454, Jul. 2008.

[10] B. Wicht, T. Nirschl, and D. Schmitt-Landsiedel, "Yield and speed optimization of a latch-type voltage sense amplifier," *IEEE J. Solid-State Circuits*, vol. 39, no. 7, pp. 1148–1158, Jul. 2004, doi: 10.1109/JSSC.2004.829399.

[11] S. Chevella, D. O'Hare, and I. O'Connell, "A low-power 1-V supply dynamic comparator," *IEEE Solid-State Circuits Lett.*, vol. 3, pp. 154–157, 2020.

[12] H. S. Bindra, C. E. Lokin, D. Schinkel, A.-J. Annema, and B. Nauta, "A 1.2-V dynamic bias latch-type comparator in 65-nm CMOS with 0.4-mV input noise," *IEEE J. Solid-State Circuits*, vol. 53, no. 7, pp. 1902–1912, Jul. 2018, doi: 10.1109/JSSC.2018.2820147.