

EE 671 VLSI DESIGN

COURSE PROJECT I REPORT

Submitted by:

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Under the supervision of

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- **CIRCUIT DIAGRAM**

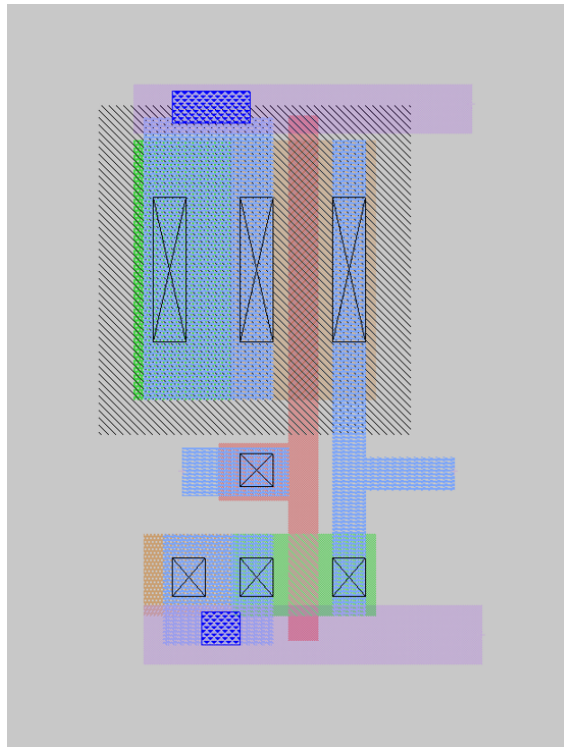


Figure 1: INVERTER

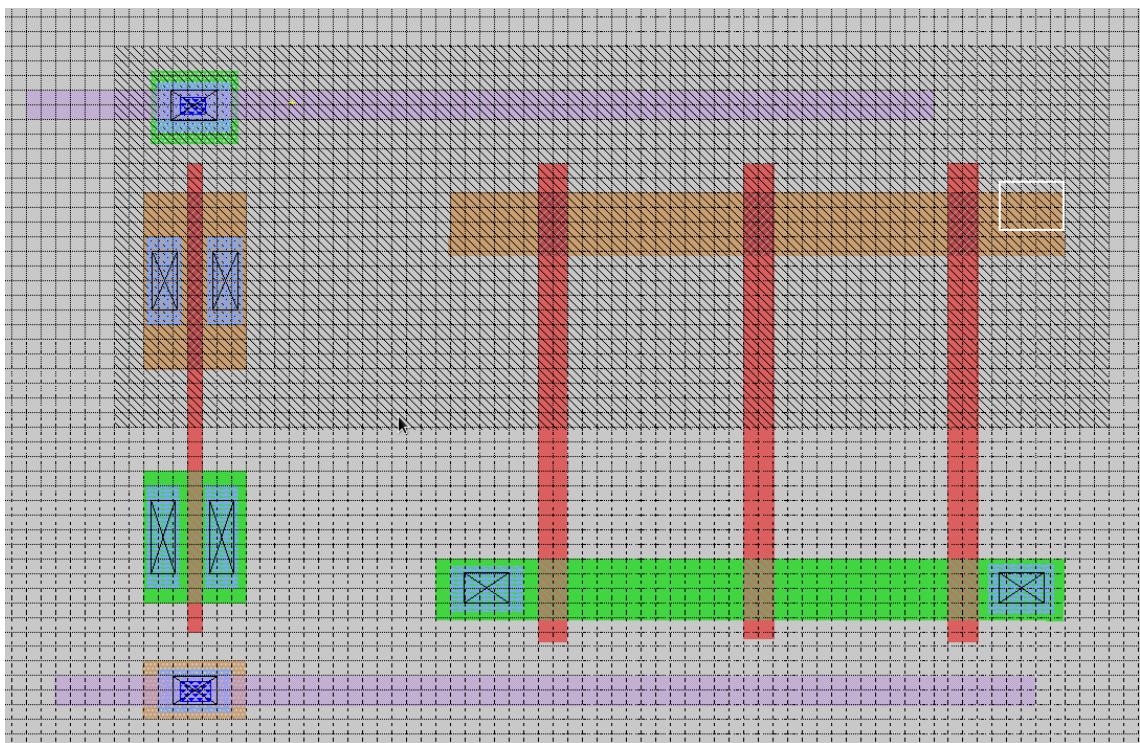


Figure 2: NAND

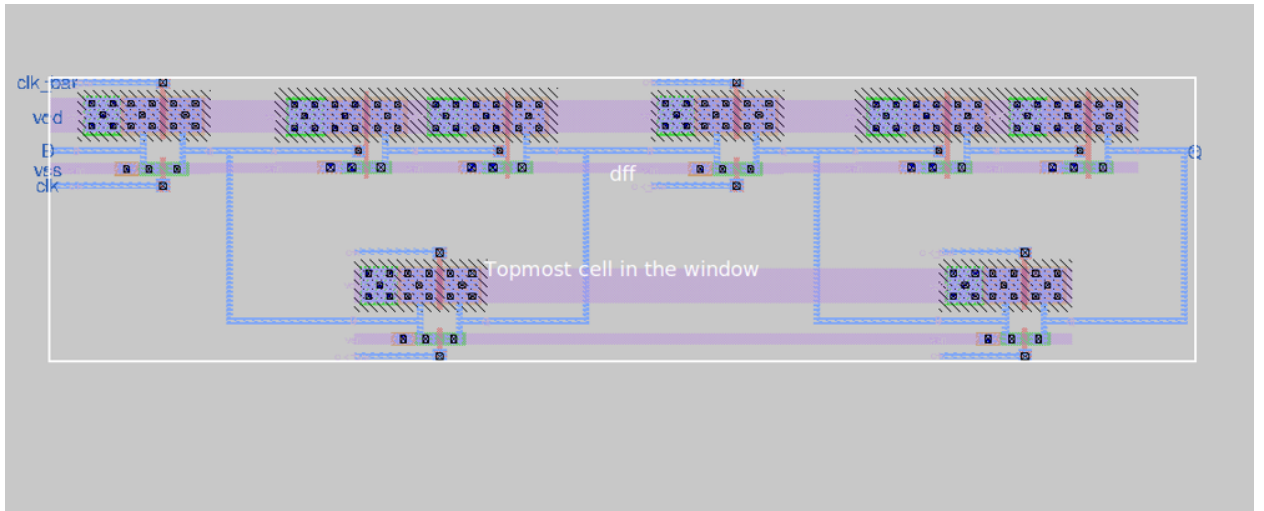


Figure 3: DFF

• **DESIGN PARAMETER TABLE**

NMOS	Width (μm)	Length (μm)
Inverter	0.45	0.15
Nand	0.9	0.15
DFF	0.45	0.15

PMOS	Width (μm)	Length (μm)
Inverter	1.33768	0.15
Nand	0.81	0.15
DFF	1.34	0.15

• PEX

```

1 MACRO INVERTER
2 CLASS BLOCK ;
3 FOREIGN INVERTER ;
4 ORIGIN 0.980 0.250 ;
5 SIZE 1.980 BY 3.000 ;
6 PIN A
7 ANTENNAGATEAREA 0.264000 ;
8 PORT
9 LAYER l11 ;
10 RECT -0.550 0.620 0.000 0.870 ;
11 END
12 END A
13 PIN Y
14 ANTENNADIFFAREA 0.528000 ;
15 PORT
16 LAYER l11 ;
17 RECT 0.230 0.820 0.400 2.460 ;
18 RECT 0.230 0.650 0.860 0.820 ;
19 RECT 0.230 0.000 0.400 0.650 ;
20 END
21 END Y
22 PIN vdd
23 ANTENNADIFFAREA 1.072000 ;
24 PORT
25 LAYER nwell ;
26 RECT -0.980 0.940 0.630 2.640 ;
27 LAYER l11 ;
28 RECT -0.600 2.580 -0.200 2.720 ;
29 RECT -0.750 1.120 -0.080 2.580 ;
30 LAYER met1 ;
31 RECT -0.800 2.500 0.950 2.750 ;
32 END
33 END vdd
34 PIN vss
35 ANTENNADIFFAREA 0.315000 ;
36 PORT
37 LAYER l11 ;
38 RECT -0.650 -0.150 -0.080 0.420 ;
39 LAYER met1 ;
40 RECT -0.750 -0.250 1.000 0.050 ;
41 END
42 END vss
43 END INVERTER
44 END LIBRARY
  
```

Figure 4: INVERTER PEX

```

1 * .subckt nand3
2 **devattc a=4163.227 d=4117.255
3 X1 a_421_389# a_390_n14# a_211_389# VDD aky130_fd_pr__pfet_01v8 ad=0.4002 pd=2.66 aa=0.4117 pa=
4 **devattc a=4117.225 d=4002.266
5 X2 a_n1_389# a_n30_n15# a_n120_389# VDD aky130_fd_pr__pfet_01v8 ad=0.4163 pd=2.27 aa=0.414 pa=2.
6 **devattc a=4140.272 d=4163.227
7 X3 a_n1_14# a_n30_n15# a_n135_14# a_n436_n105# aky130_fd_pr__nfet_01v8 ad=0.4163 pd=2.27 aa=0.41
8 **devattc a=4830.302 d=4163.227
9 X4 a_421_14# a_390_n14# a_211_14# a_n436_n105# aky130_fd_pr__nfet_01v8 ad=0.4048 pd=2.68 aa=0.421
10 **devattc a=4117.225 d=4048.268
11 X5 a_n375_254# a_n390_n15# a_n435_254# VDD aky130_fd_pr__pfet_01v8 ad=0.8145 pd=4.52 aa=0.8145
12 **devattc a=8145.452 d=8145.452
13 X6 a_211_14# a_n30_n15# a_n1_14# a_n436_n105# aky130_fd_pr__nfet_01v8 ad=0.4117 pd=2.25 aa=0.41
14 **devattc a=4163.227 d=4117.255
15 X7 a_n375_15# a_n390_n15# a_n435_15# a_n436_n105# aky130_fd_pr__nfet_01v8 ad=0.6075 pd=3.6 aa=0.
16 **devattc a=6075.360 d=6075.360
17 C0 VDD a_n30_n15# 0.30483#
18 C1 a_n375_15# a_n135_14# 0.001129#
19 C2 a_n375_15# a_n30_n15# 4.96e-19
20 C3 a_n375_254# VDD 0.05193#
21 C4 a_n435_254# a_n30_n15# 1.77e-19
22 C5 a_n390_n15# a_n30_n15# 0.007513#
23 C6 a_n375_254# a_n30_n15# 1.77e-19
24 C7 VDD a_n435_15# 0.00366#
25 C8 a_n1_389# VDD 0.010654#
26 C9 VDD a_211_14# 0.00125#
27 C10 a_421_389# a_n375_254# 1.87e-21
28 C11 a_n375_15# VDD 0.003703#
29 C12 VDD a_n435_254# 0.026529#
30 C13 a_n1_389# a_n375_254# 2.56e-20
31 C14 VDD a_n390_n15# 0.105887#
32 C15 a_n375_15# a_n30_n15# 1.59e-19
33 C16 a_n375_15# a_421_14# 5.09e-20
34 C17 a_n1_14# VDD 0.00138#
35 C18 a_n375_15# a_n375_254# 0.006539#
36 C19 a_n375_254# a_n435_254# 0.05912#
37 C20 VDD a_n120_389# 0.005298#
38 C21 a_n375_254# a_n390_n15# 0.007845#
39 C22 a_n375_15# a_n435_15# 0.068979#
40 C23 VDD a_n390_n14# 0.289297#
41 C24 a_n435_15# a_n435_254# 0.006597#
42 C25 a_n435_15# a_n390_n15# 0.008984#
43 C26 VDD a_n135_14# 8e-19
44 C27 a_n375_254# a_n120_389# 3.12e-20
45 C28 VDD a_n30_n15# 0.309509#
46 C29 a_n375_15# a_n390_n14# 0.034503#
47 C30 a_n375_15# a_211_14# 3.35e-19
48 C31 a_n375_254# a_n390_n14# 8.9e-20
49 C32 VDD a_211_389# 0.009454#
50 C33 a_n375_15# a_n30_n15# 0.03421#
51 C34 a_n375_15# a_n390_n15# 0.009303#
52 C35 a_n375_254# a_n30_n15# 4.9e-19
53 C36 a_n1_14# a_n375_15# 7.55e-19
54 C37 a_n390_n15# a_n435_254# 0.007845#
55 C38 a_n375_254# a_211_389# 1.13e-20
56 C39 a_n435_15# a_n30_n15# 1.4e-19
57 C40 a_n375_15# a_n390_n14# 1.03e-19
58 C41 a_421_14# a_n436_n105# 0.003435#
59 C42 a_211_14# a_n436_n105# 0.010601#
60 C43 a_n1_14# a_n436_n105# 0.010719#
61 C44 a_n135_14# a_n436_n105# 0.006216#
62 C45 a_n375_15# a_n436_n105# 0.058842#
63 C46 a_n435_15# a_n436_n105# 0.064524#
64 C47 a_421_389# a_n436_n105# 4.44e-19
65 C48 a_211_389# a_n436_n105# 0.00137#
66 C49 a_n1_389# a_n436_n105# 0.001385#
67 C50 a_n120_389# a_n436_n105# 6.89e-19
68 C51 a_n375_254# a_n436_n105# 0.009462#
69 C52 a_n435_254# a_n436_n105# 0.036074#
70 C53 a_n390_n14# a_n436_n105# 0.342216#
71 C54 a_n180_n15# a_n436_n105# 0.302592#
72 C55 a_n30_n15# a_n436_n105# 0.309052#
73 C56 a_n390_n15# a_n436_n105# 0.161333#
74 C57 VDD a_n436_n105# 5.31442#
75 .ends
  
```

Figure 5: NAND PEX

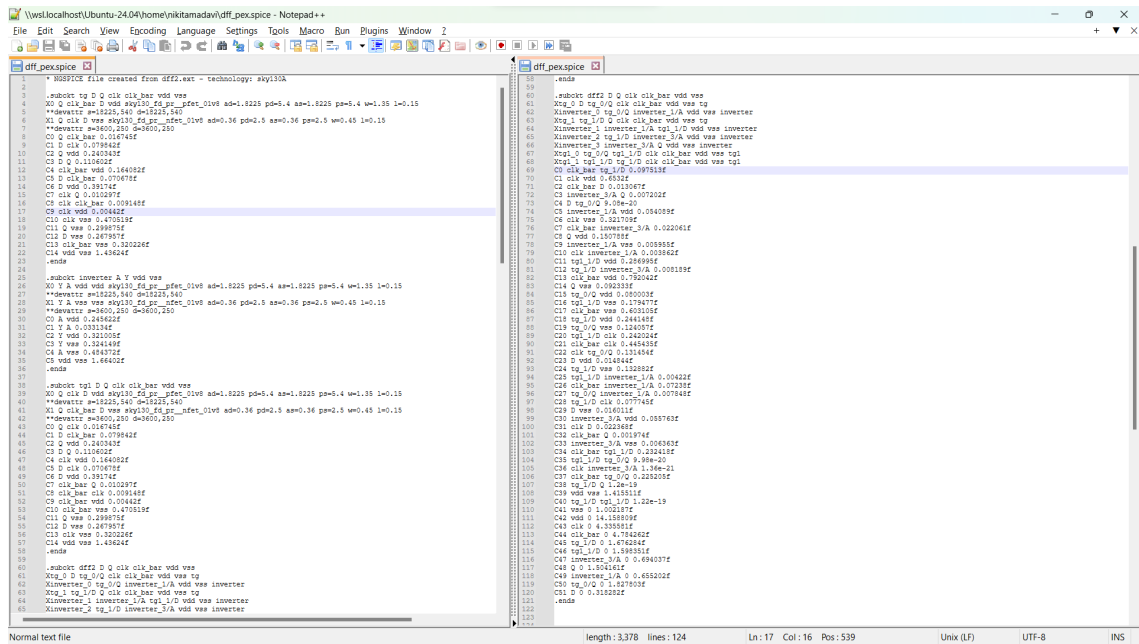


Figure 6: DFF PEX

• DRC

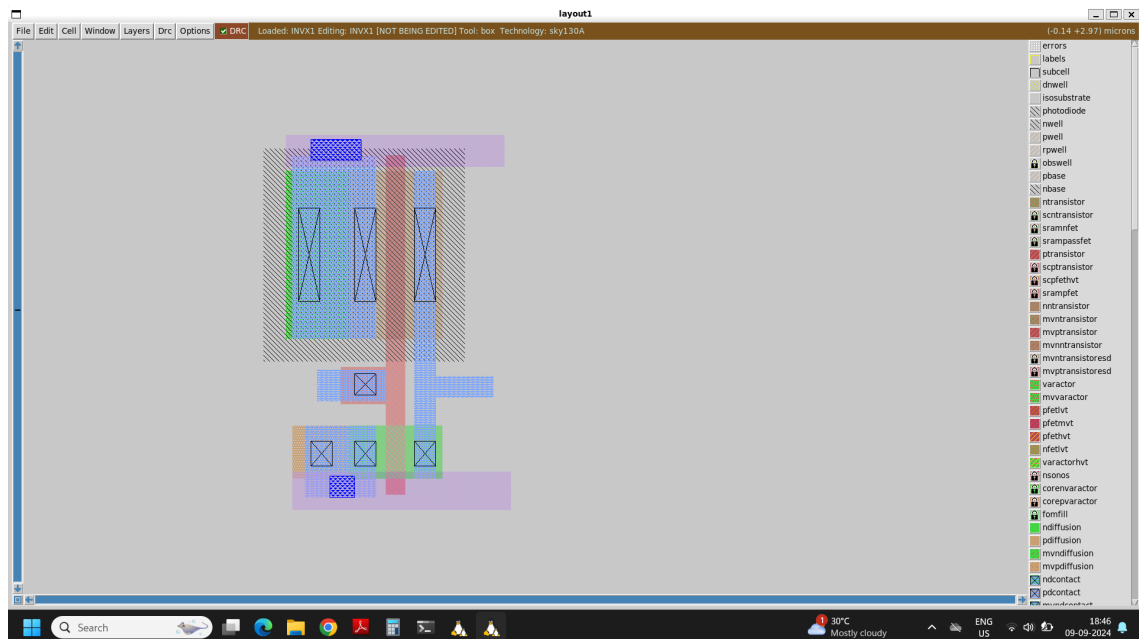


Figure 7: INVERTER DRC

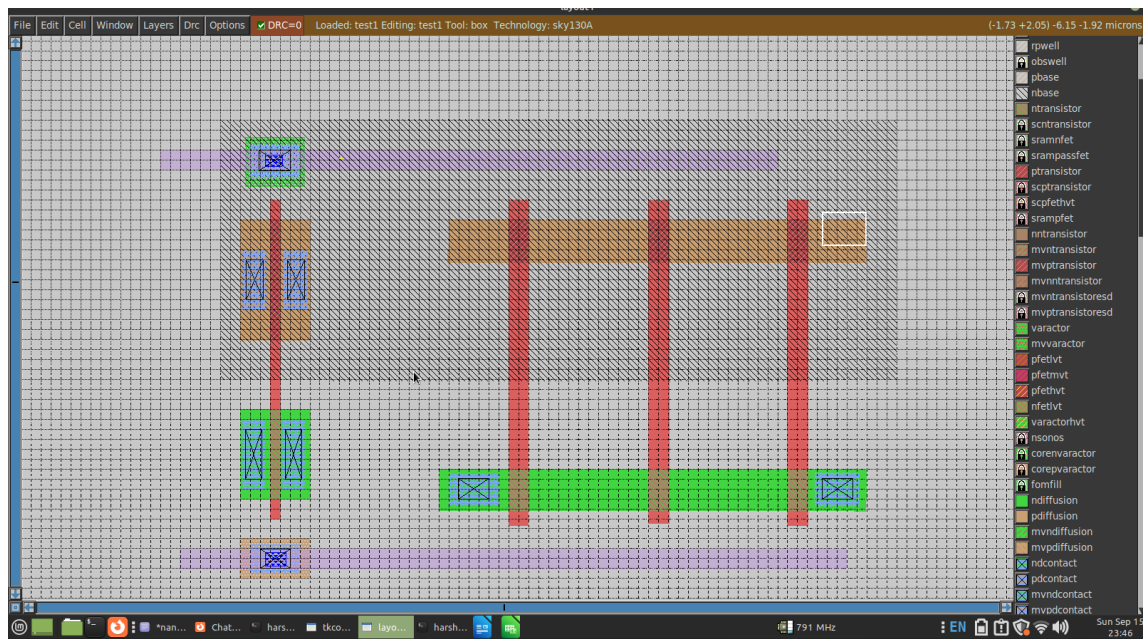


Figure 8: NAND DRC

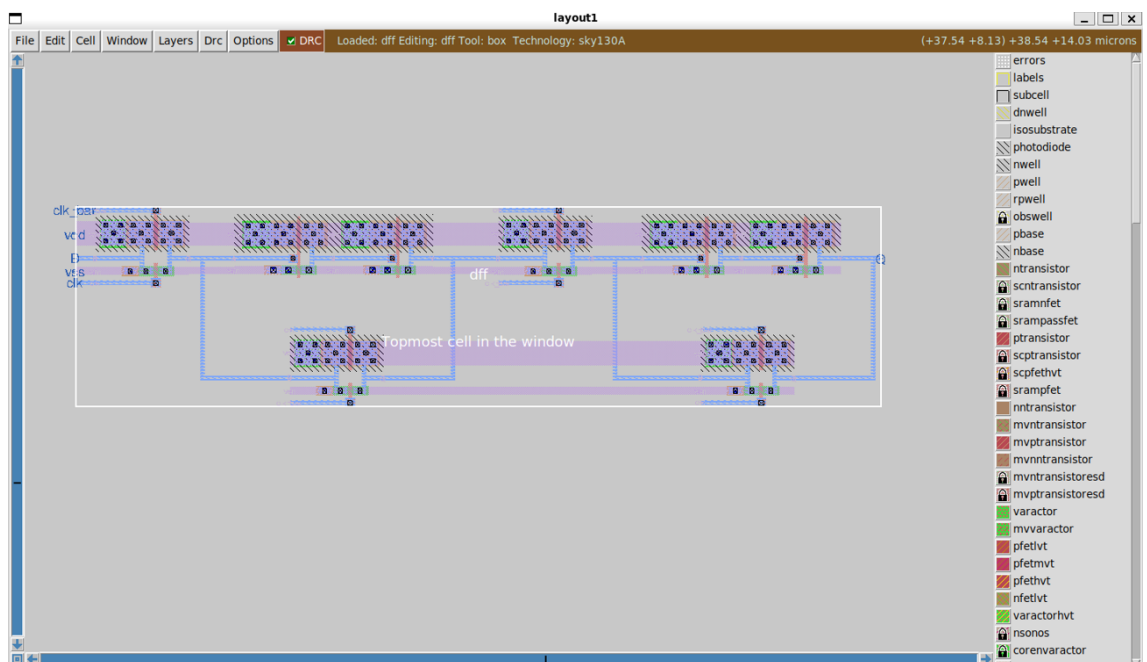


Figure 9: DFF DRC

- LVS

```

root@LAPTOP-M216N101: ~/fr
Model sky130_fd_pr__pfet_01v8 pin 1 == 3
No property mult found for device sky130_fd_pr__pfet_01v8
No property sa found for device sky130_fd_pr__pfet_01v8
No property sb found for device sky130_fd_pr__pfet_01v8
No property sd found for device sky130_fd_pr__pfet_01v8
No property nf found for device sky130_fd_pr__pfet_01v8
No property nrd found for device sky130_fd_pr__pfet_01v8
No property nrs found for device sky130_fd_pr__pfet_01v8
No property area found for device sky130_fd_pr__pfet_01v8
No property perim found for device sky130_fd_pr__pfet_01v8
No property topography found for device sky130_fd_pr__pfet_01v8
Comparison output logged to file comp.out
Logging to file "comp.out" enabled
Circuit sky130_fd_pr__pfet_01v8 contains no devices.
Circuit sky130_fd_pr__nfet_01v8 contains no devices.

Contents of circuit 1: Circuit: 'INVX1'
Circuit INVX1 contains 2 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances: 1
  Class: sky130_fd_pr__pfet_01v8 instances: 1
Circuit contains 4 nets.
Contents of circuit 2: Circuit: 'invertor'
Circuit invertor contains 2 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances: 1
  Class: sky130_fd_pr__pfet_01v8 instances: 1
Circuit contains 4 nets.

Circuit 1 contains 2 devices, Circuit 2 contains 2 devices.
Circuit 1 contains 4 nets, Circuit 2 contains 4 nets.

Final result:
Circuits match uniquely.
.
Logging to file "comp.out" disabled
LVS Done.
root@LAPTOP-M216N101: ~/new_pdk_sky/ngspice_simulations#

```

Figure 10: INVERTER LVS

```

Circuit 1 contains 2 devices, Circuit 2 contains 2 devices.
Circuit 1 contains 4 nets, Circuit 2 contains 4 nets.

Final result:
Circuits match uniquely.
.
Logging to file "comp.out" disabled
LVS Done.

```

Figure 11: NAND LVS

```

nikitamadavi@NIKITA: ~
Class: skyl30_fd_pr__pfet_0lv8 instances: 1
Circuit contains 6 nets.

Circuit 1 contains 2 devices, Circuit 2 contains 2 devices.
Circuit 1 contains 6 nets, Circuit 2 contains 6 nets.

Contents of circuit 1: Circuit: 'dff2'
Circuit dff2 contains 8 device instances.
Class: inverter instances: 4
Class: tg instances: 2
Class: tgl instances: 2
Circuit contains 11 nets.
Contents of circuit 2: Circuit: 'dff'
Circuit dff contains 8 device instances.
Class: inverter instances: 4
Class: tg instances: 2
Class: tgl instances: 2
Circuit contains 11 nets.

Circuit 1 contains 8 devices, Circuit 2 contains 8 devices.
Circuit 1 contains 11 nets, Circuit 2 contains 11 nets.

Final result:
Circuits match uniquely.
Logging to file "comp.out" disabled
LVS Done.
nikitamadavi@NIKITA:~$

```

Figure 12: DFF LVS

• WAVEFORM

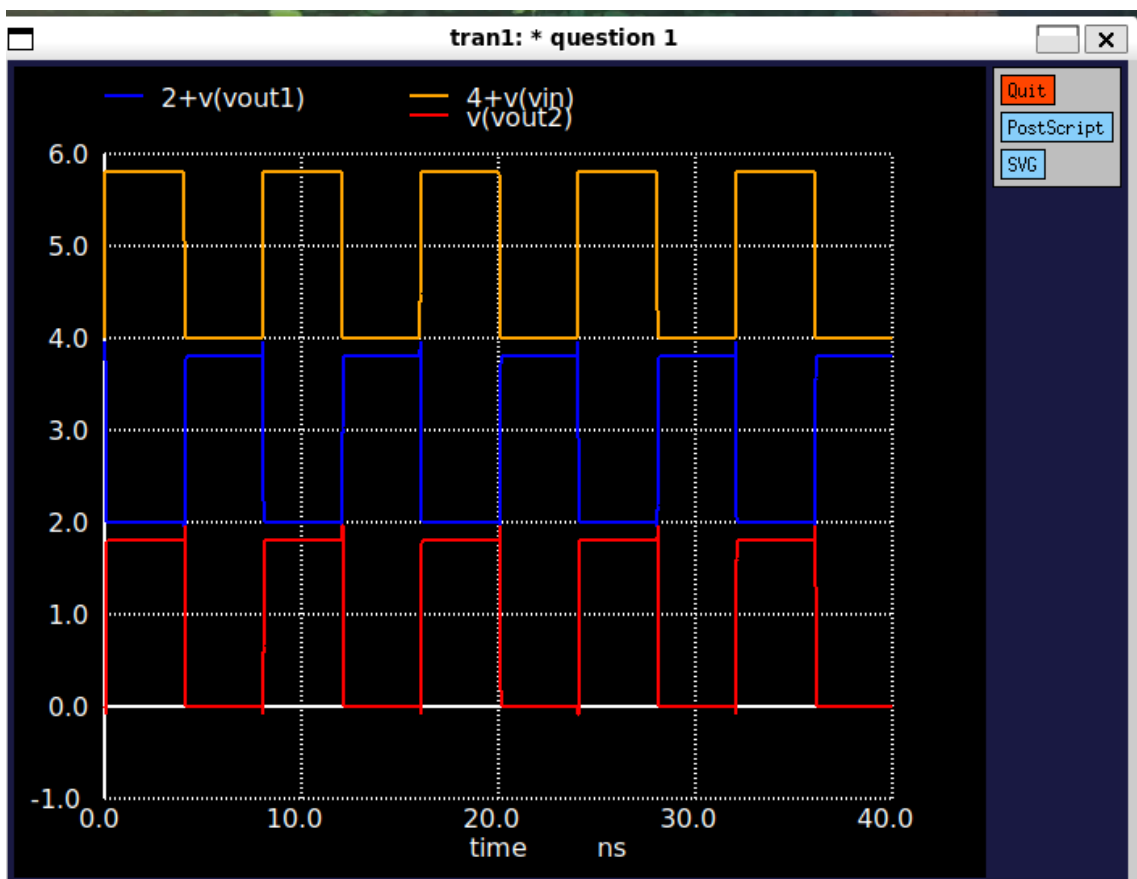


Figure 13: INVERTER WAVEFORM

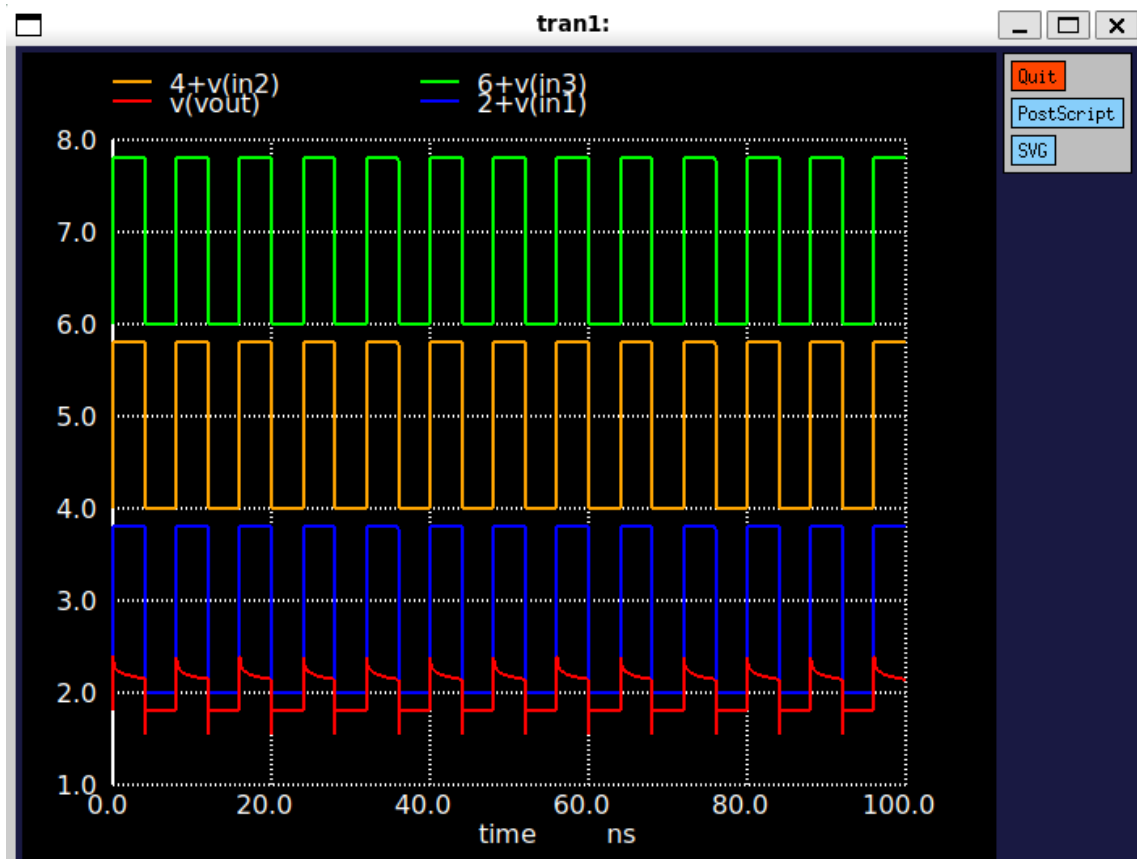


Figure 14: NAND WAVEFORM

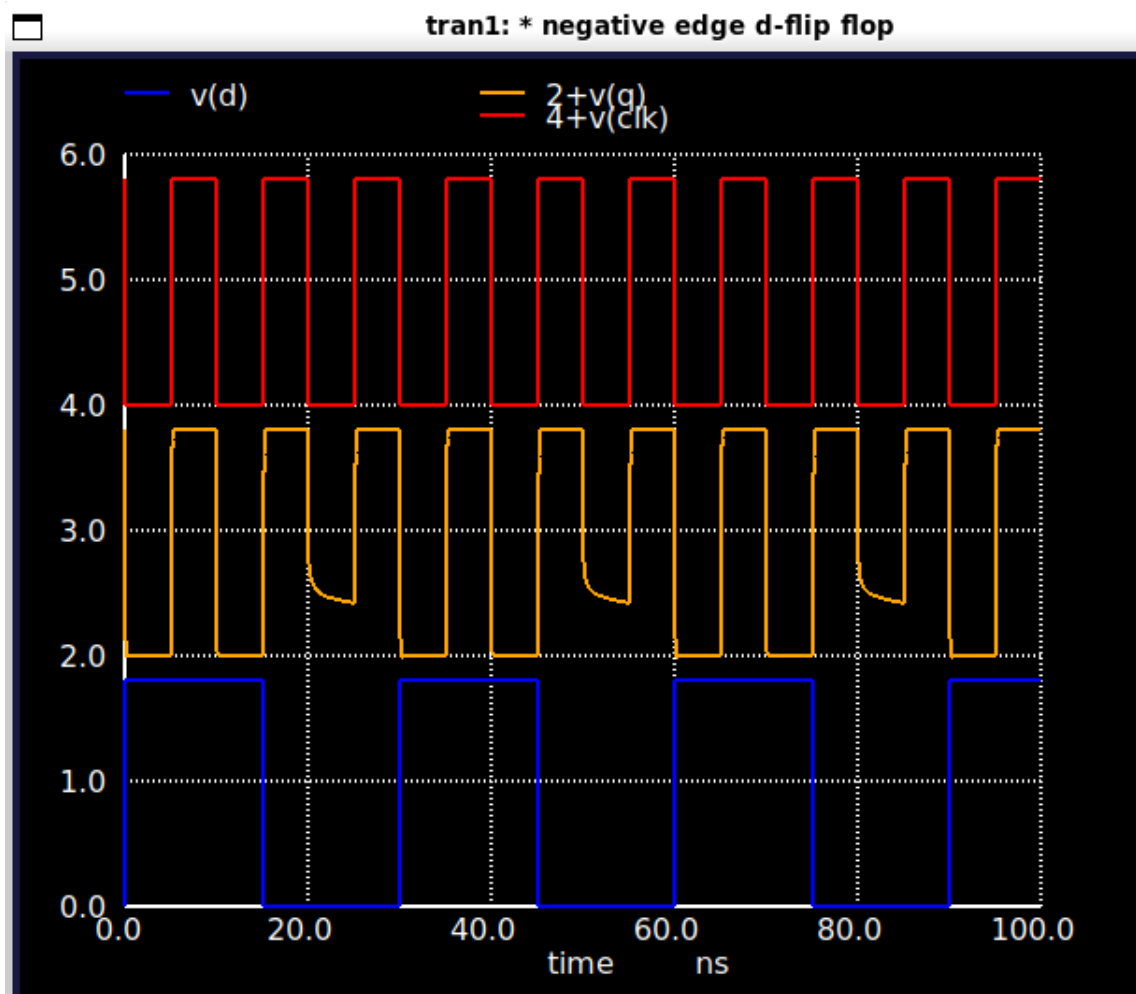


Figure 15: DFF WAVEFORM

• **TABLE OF CONTRIBUTION**

Contributor	Contributions
Anupam	<ul style="list-style-type: none">• Inverter design and layout• Post-layout code contribution• VHDL code contribution
Harsh	<ul style="list-style-type: none">• NAND gate design and layout• Post-layout code contribution• Verilog code contribution
Nikita	<ul style="list-style-type: none">• D Flip-Flop (DFF) design and layout• Post-layout code contribution• Verilog code contribution

Table 1: Project Contributions