EE 671 VLSI DESIGN

COURSE PROJECT I REPORT

Submitted by:

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Under the supervision of

Prof. Laxmeesha Somappa

- **CIRCUIT DIAGRAM**

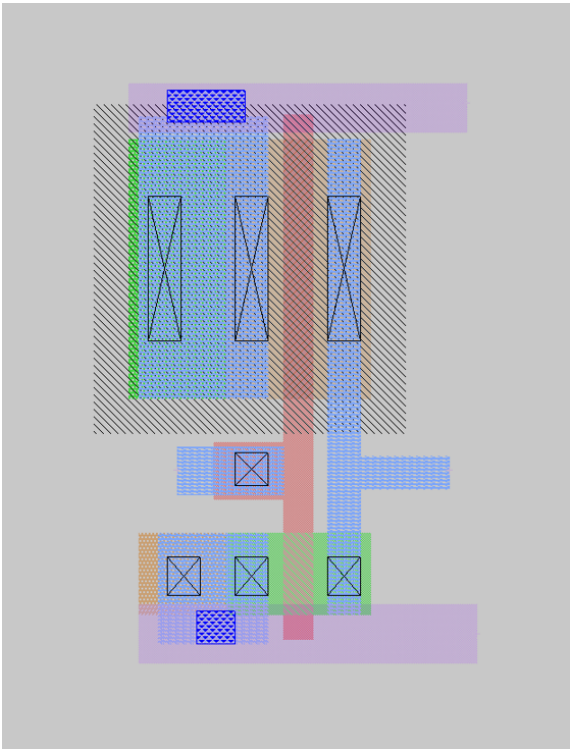

Figure 1: INVERTER

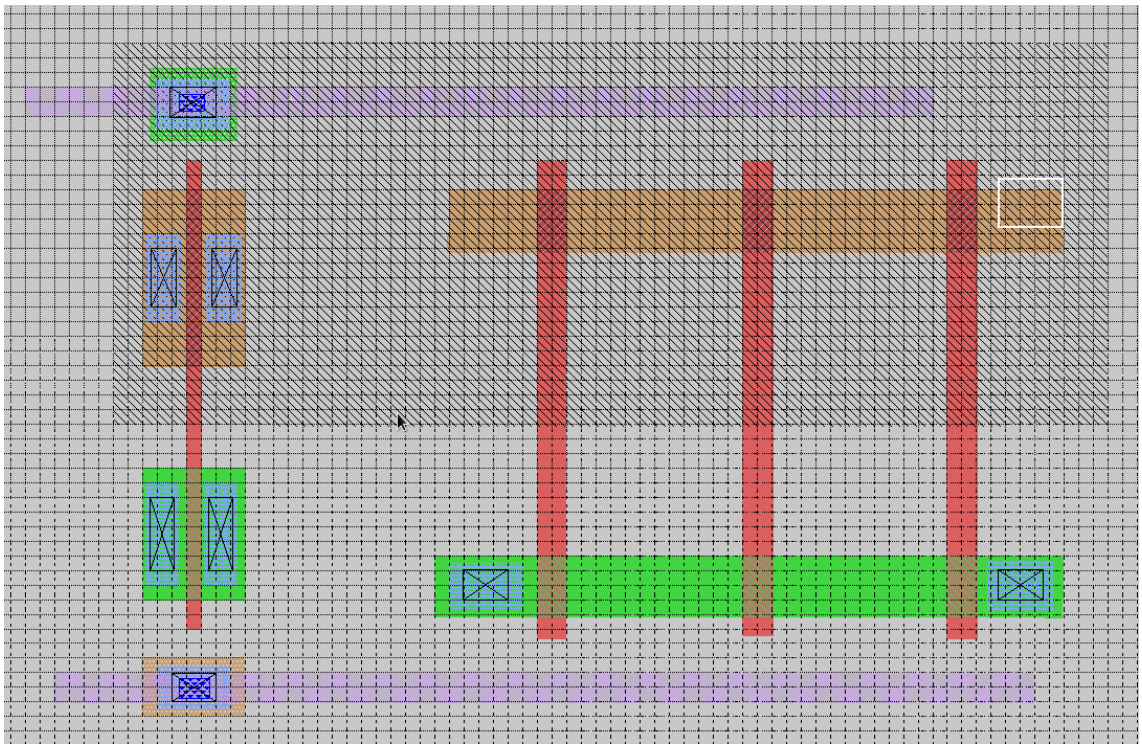

Figure 2: NAND

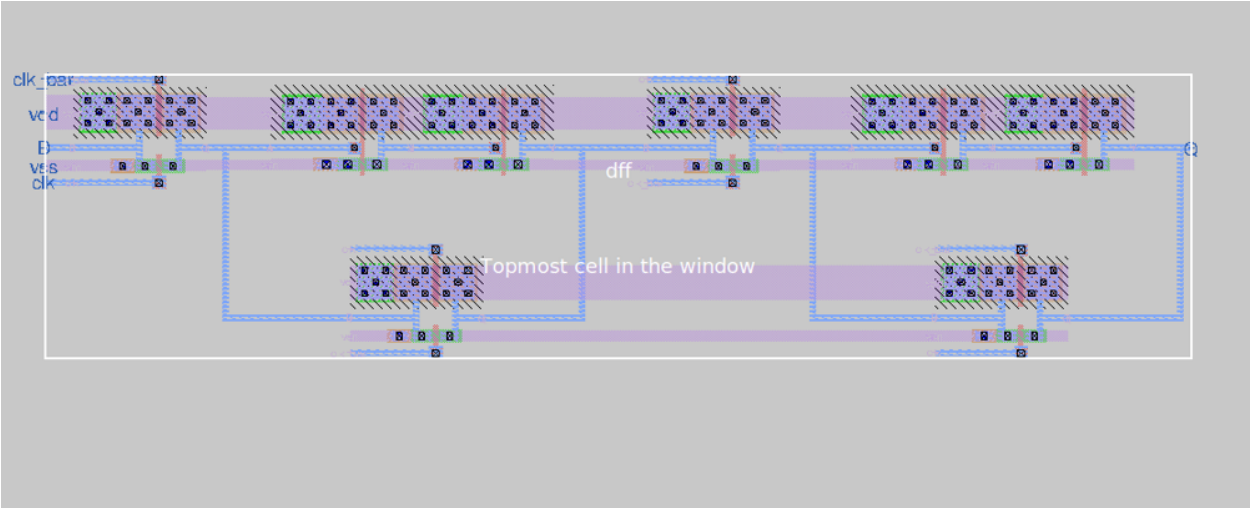

Figure 3: DFF

- **DESIGN PARAMETER TABLE**

NMOS	**Width** (μm)	**Length** (μm)
Inverter	0.45	0.15
Nand	0.9	0.15
DFF	0.45	0.15

PMOS	**Width** (μm)	**Length** (μm)
Inverter	1.33768	0.15
Nand	0.81	0.15
DFF	1.34	0.15

- **PEX**

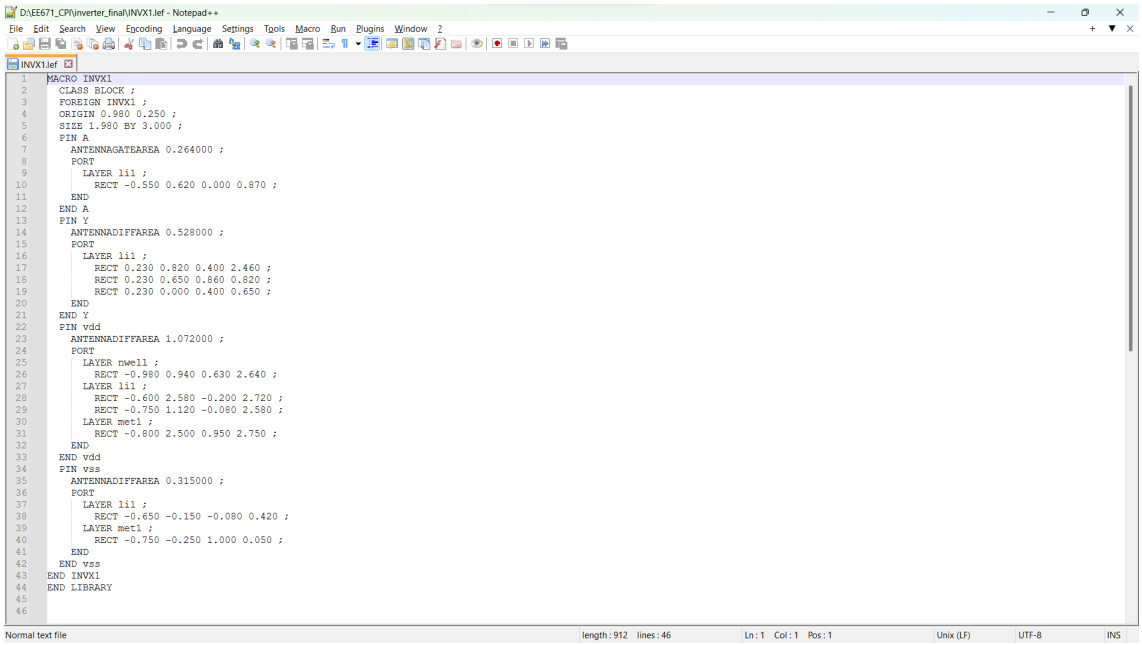

Figure 4: INVERTER PEX

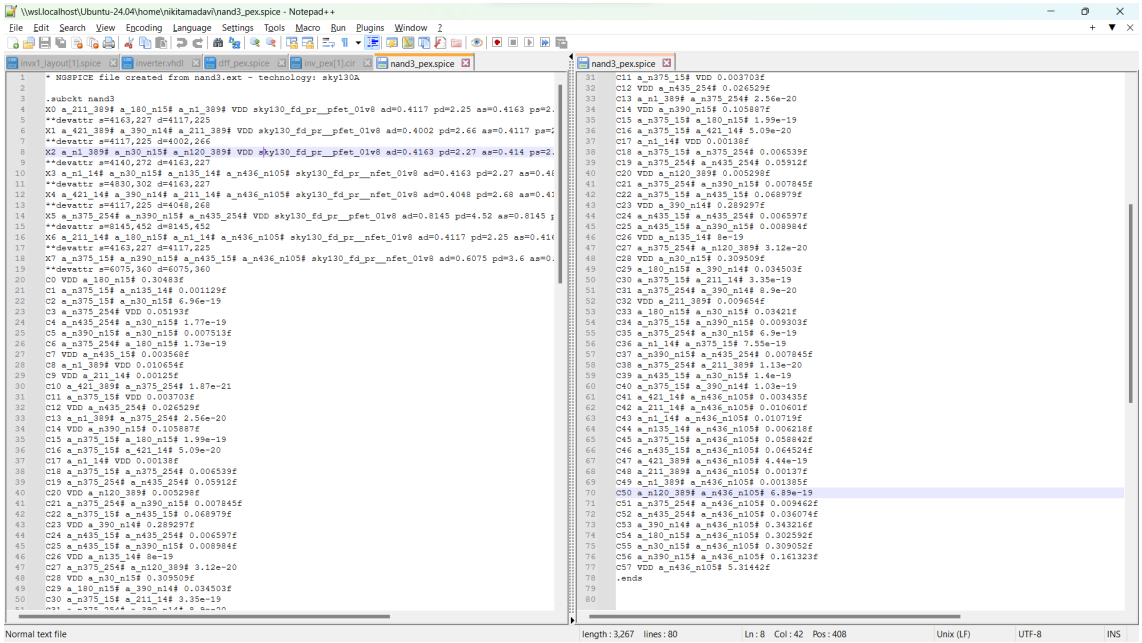

Figure 5: NAND PEX

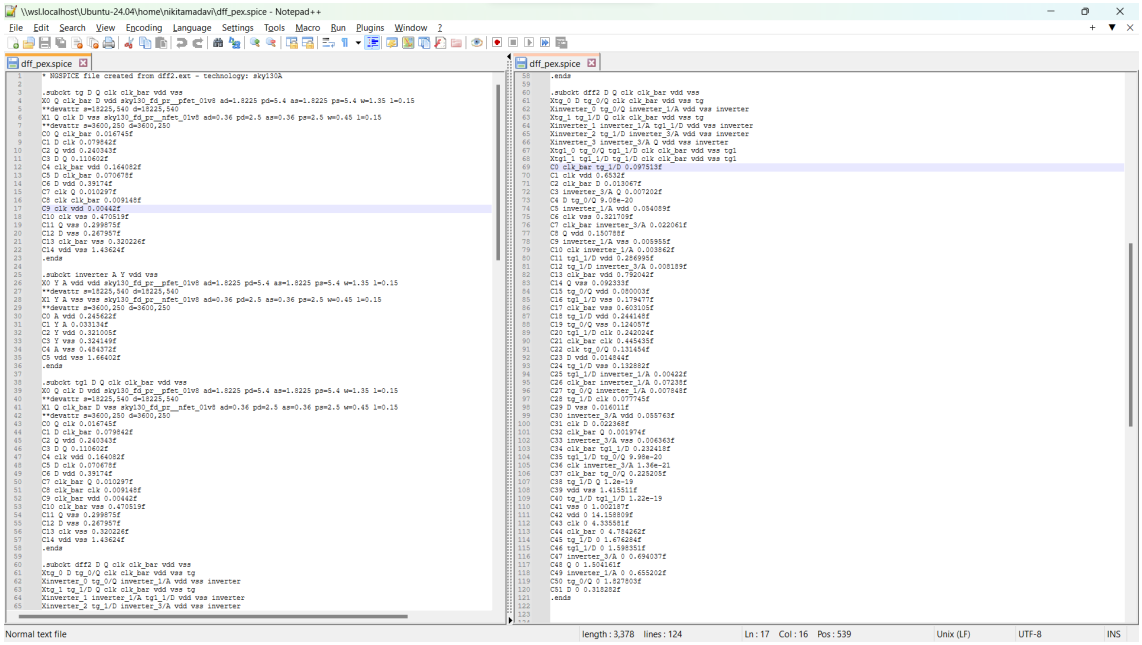

Figure 6: DFF PEX

- **DRC**

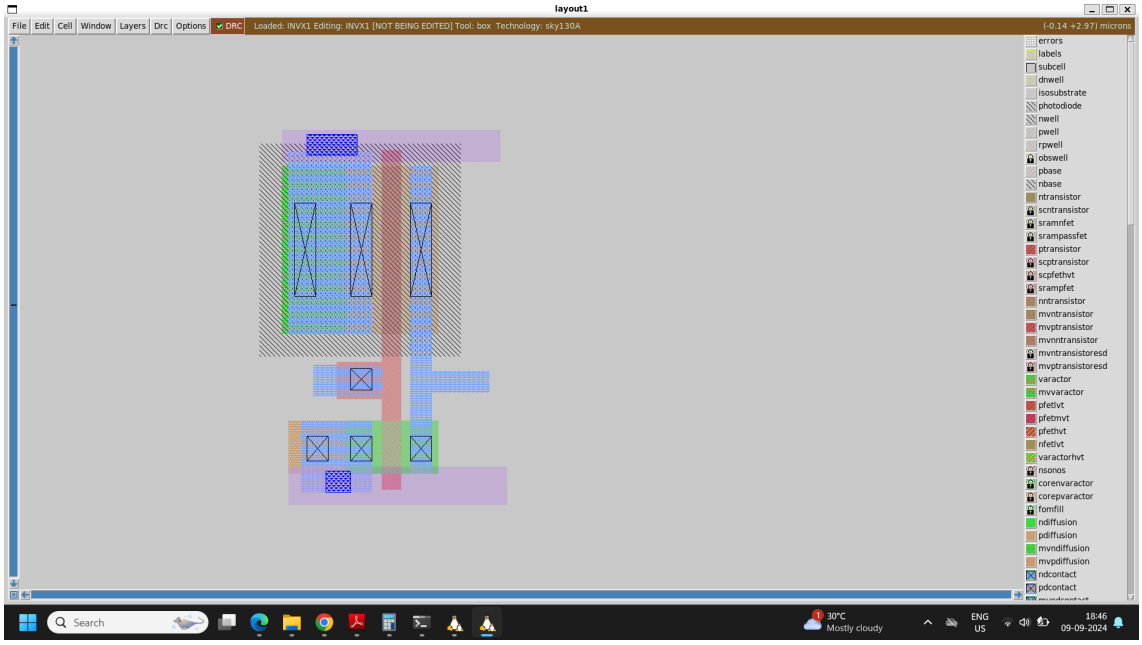

Figure 7: INVERTER DRC

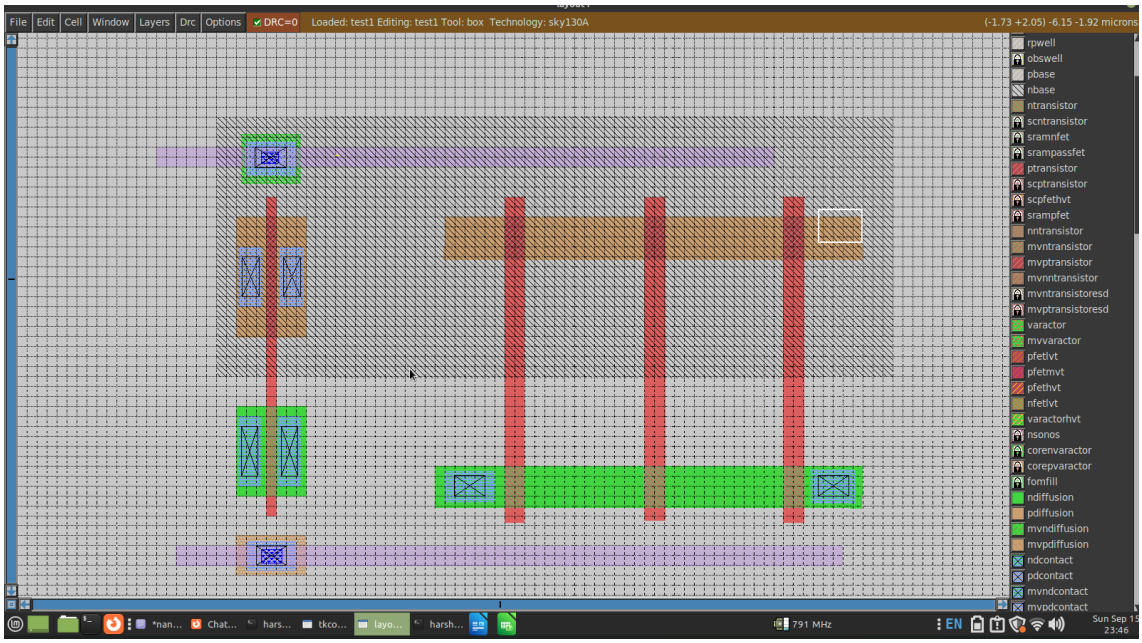

Figure 8: NAND DRC

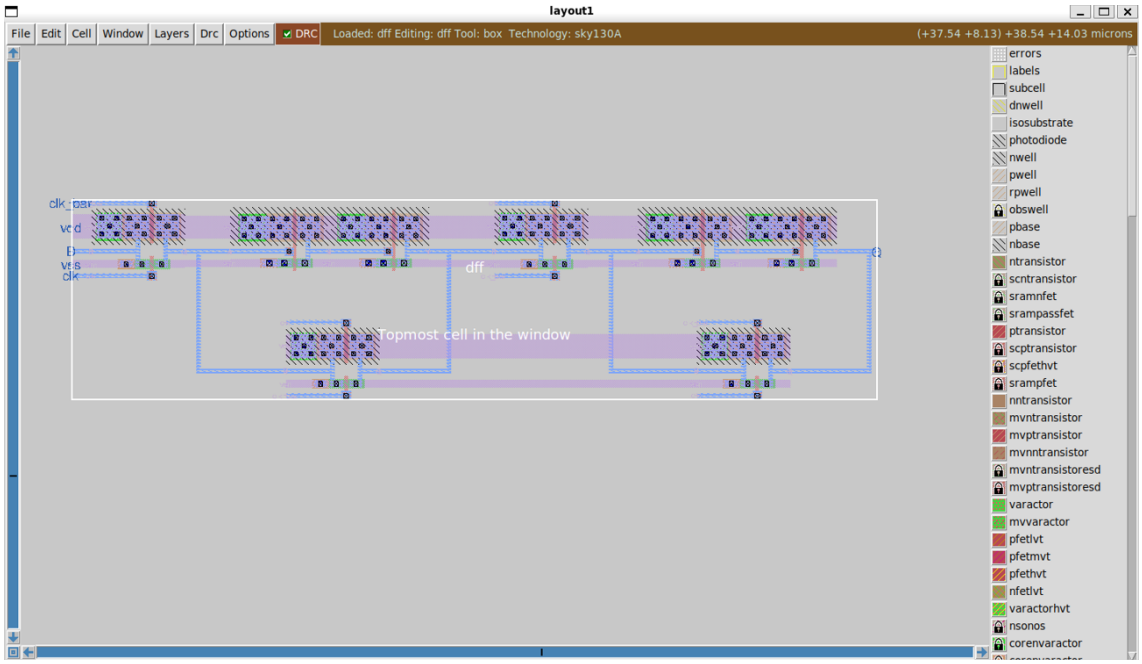

Figure 9: DFF DRC

- **LVS**

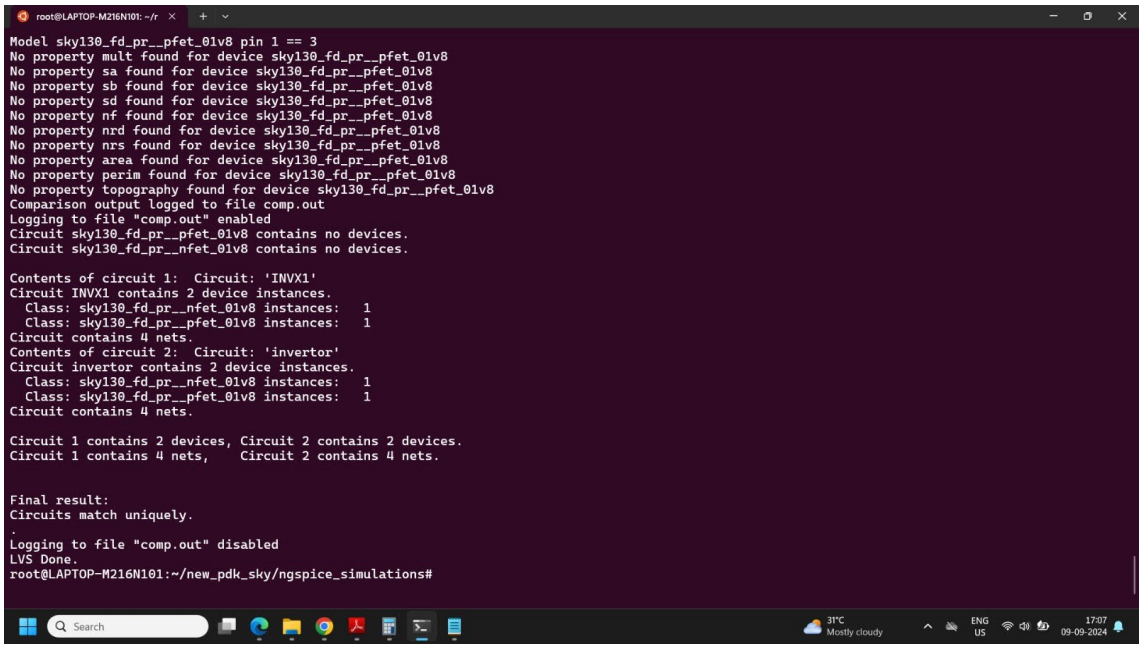

Figure 10: INVERTER LVS

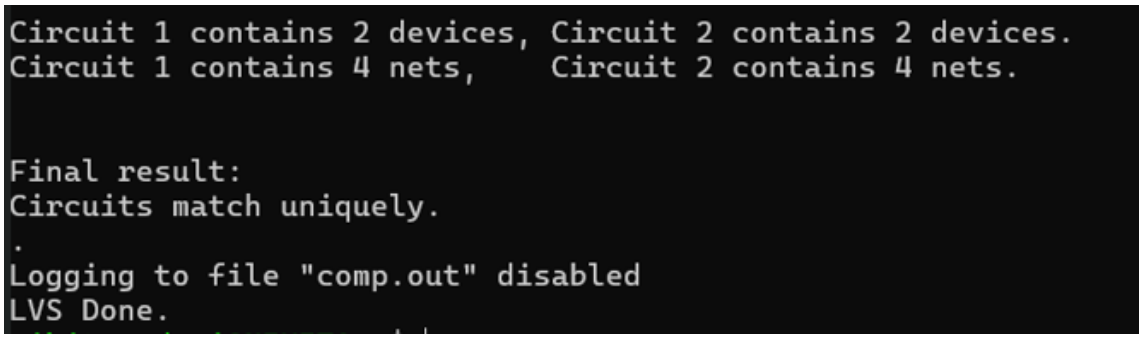

Figure 11: NAND LVS

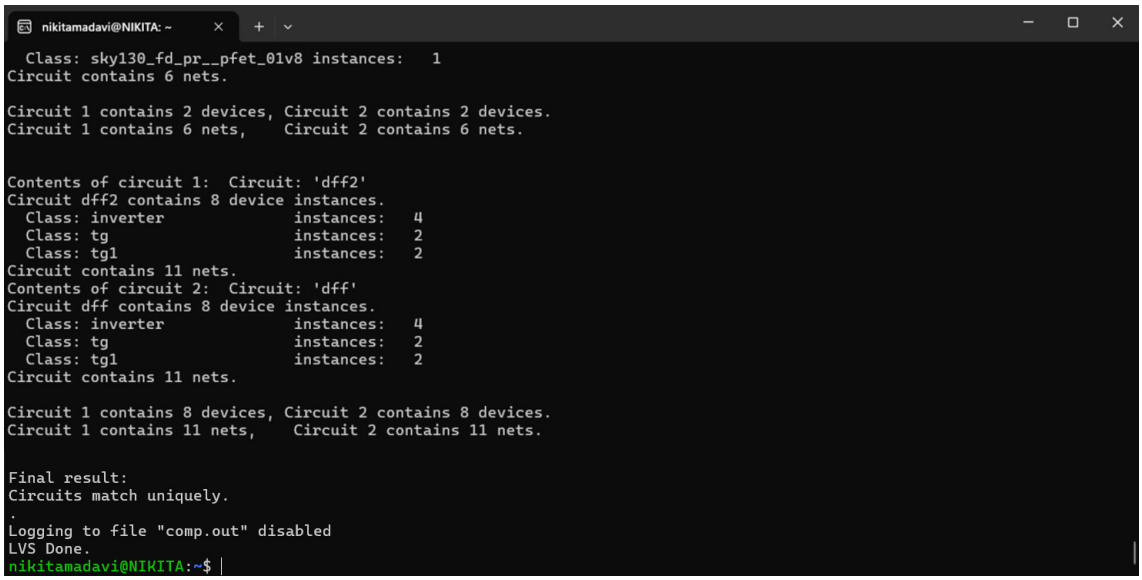

Figure 12: DFF LVS

- **WAVEFORM**

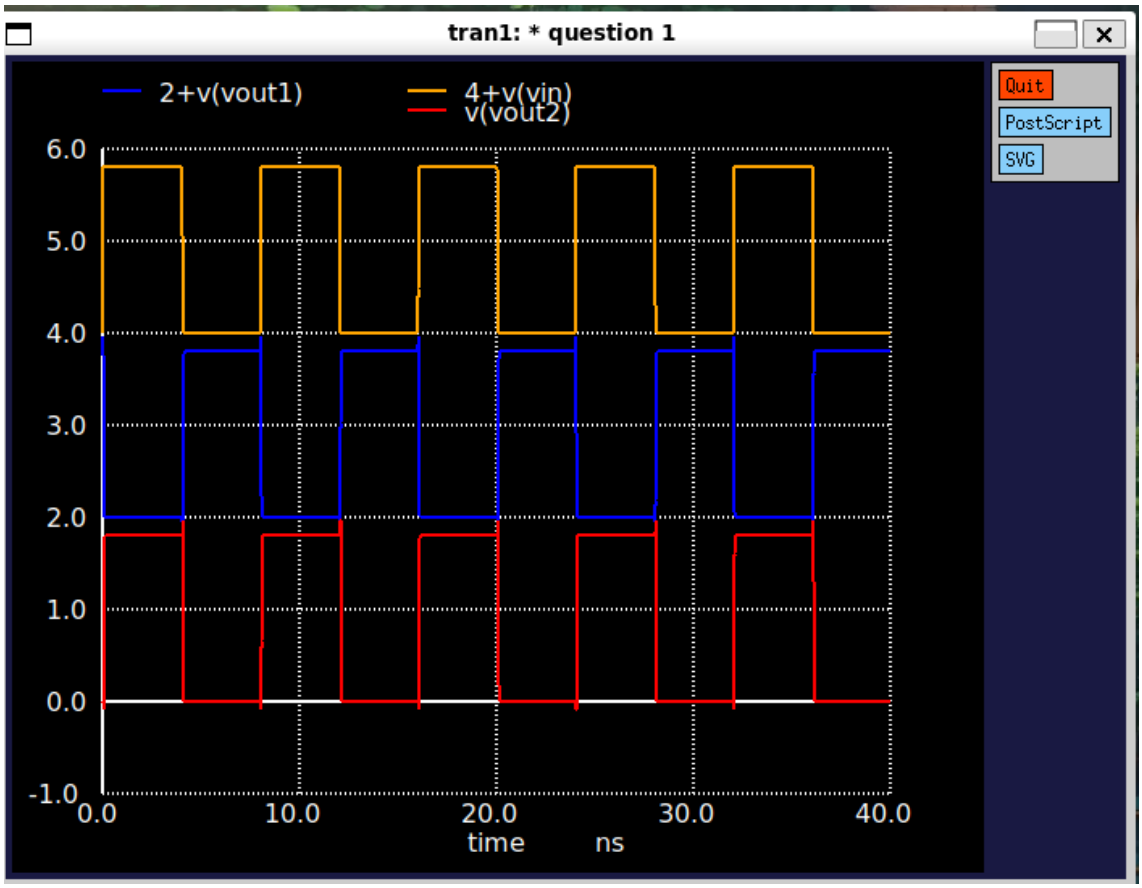

Figure 13: INVERTER WAVEFORM

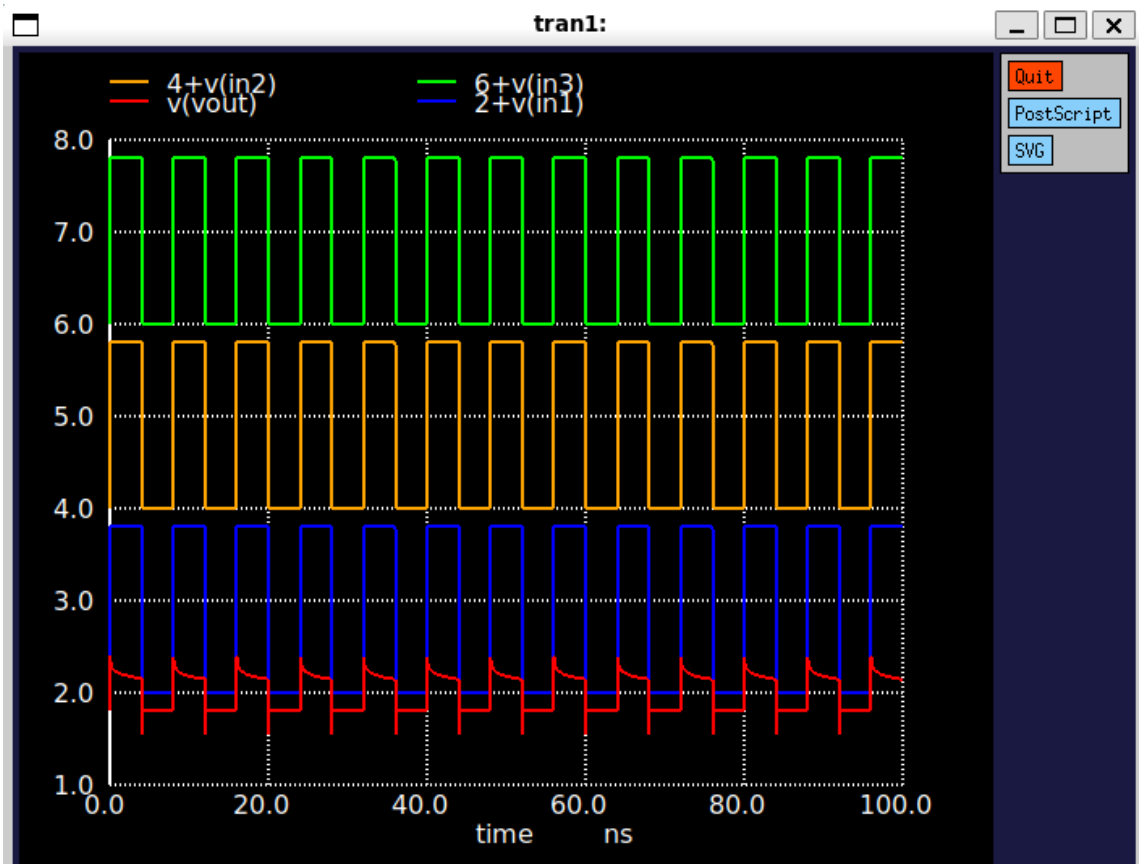

Figure 14: NAND WAVEFORM

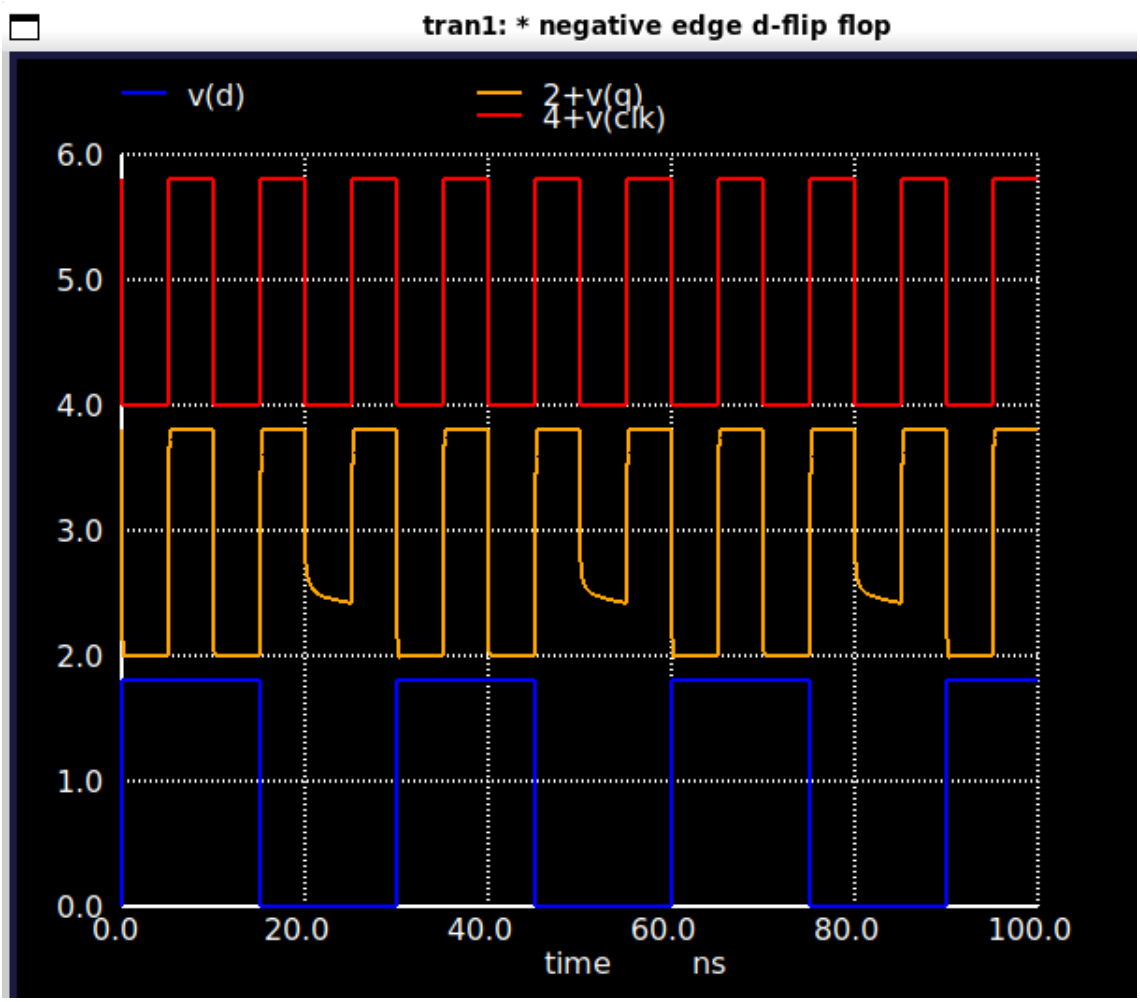

Figure 15: DFF WAVEFORM

- **TABLE OF CONTRIBUTION**

Contributor	**Contributions**
Anupam	• Inverter design and layout • Post-layout code contribution • VHDL code contribution
Harsh	• NAND gate design and layout • Post-layout code contribution • Verilog code contribution
Nikita	• D Flip-Flop (DFF) design and layout • Post-layout code contribution • Verilog code contribution

Table 1: Project Contributions