Saturday	EE 671: VLSI DESIGN 2024/2025	Due On
Aug 21, 2024	ASSIGNMENT-2	Aug 28, 2024

Note:

1. Submission is **only** through Moodle in the form of a PDF file upload.
2. All plots must be legible/readable in the submission (axes values and units)
3. For all your simulations, use V_{DD} = 1.8 V.

Introduction:

In this assignment you will (a) layout the standard cells designed in assignment-1 that are DRC (Design rule check) clean, (b) perform LVS (layout versus schematic) check, (c) perform a parasitic extraction (PEX) from the layout and (d) simulate the PEX netlist.

Tools:

(a) You will use ***Magic*** (an open-source tool) for layout, netlist extraction (with and without parasitics).
By default, Magic tool does not have information about the Sky130A PDK. To resolve this, in your terminal, perform a softlink using the following command:

```
sudo ln -s /usr/local/share/pdk/sky130A/libs.tech/magic/* /usr/local/lib/magic/sys/
```

(b) ***Netgen*** (an open-source tool) for LVS (Layout-vs-schematic). An LVS check ensures that the layout and the original circuit/schematic/Netlist represent the same thing.
To install Netgen, go to your work directory ("new_pdk_sky" in the assignment-1 install guide) and do the following:

```
git clone git://opencircuitdesign.com/netgen
cd netgen/
./configure
make
sudo make install
```

(c) ***NGSpice*** (a spice circuit simulator) tool to simulate the circuit/netlist.

Q1)

a) For the INVX1 designed in assignment-1, draw the layout using Magic tool. Invoke the tool using command:

```
magic -T sky130A &
```

The layout tool will open and you can start drawing the layout. Refer to the tutorial links shared on Moodle. The standard cell layout that you create **must** have a height of 2.72 µm and must be DRC clean. An example screenshot of an INVX1 is shown in Fig.1 for your reference.

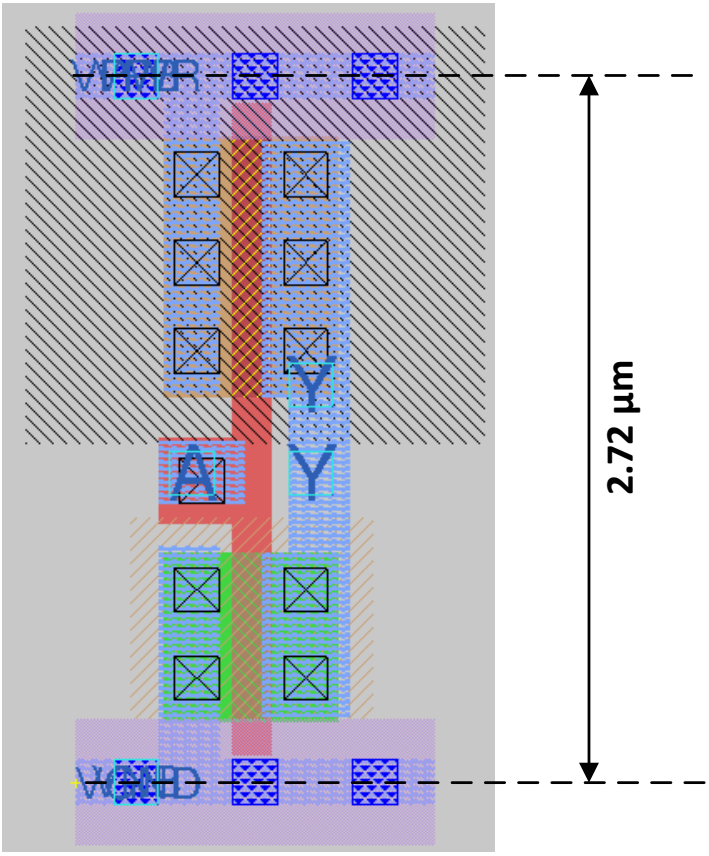

Figure 1: Example layout of INVX1 with height 2.72 um (mid-point of metal-1 VDD to mid-point of metal-1 VSS line)

In the tool, you must see  indication, indicating there are zero DRC errors.

b) We will now extract the netlist (for LVS) from this layout using Magic. In the ***Magic console***, type the following commands:

```
% extract all
% ext2spice lvs
% ext2spice -d -o invx1_layout.spice
```

You will now have a new netlist file "invx1_layout.spice", extracted from the netlist. This netlist needs to be compared with the netlist that you wrote for the INVX1 design in assignment-1. In the main terminal use ***netgen*** to run the lvs using the following command:

```
netgen -batch lvs "invx1_layout.spice INVX1" "invx1_schematic.spice INVX1" /usr/local/share/pdk/sky130A/libs.tech/netgen/sky130A_setup.tcl
```

In this command, you need to point to the two netlists (_layout.spice and _schematic.spice) and the subckt names in the netlist (INVX1 in my case). If the LVS is clean, you must obtain the following:

```
Circuit 1 contains 2 devices, Circuit 2 contains 2 devices.
Circuit 1 contains 6 nets,    Circuit 2 contains 6 nets.


Final result:
Circuits match uniquely.
.
Logging to file "comp.out" disabled
LVS Done.
```

c) We will now extract another netlist from the layout, but with all parasitic information, for our simulations. In the ***Magic console***, type the following commands:

```
% extract all
% ext2spice scale off
% ext2spice cthresh 0
% ext2spice rthresh 0
% ext2spice -d -o invx1_pex.spice -f ngspice
```

You will now have a new netlist file "invx1_pex.spice", extracted from the netlist with all parasitic information. Open this file and notice the additional parasitic caps at different nodes.
You can now use this netlist to perform simulations similar to what you did in assignment-1 (replace the original netlist with this new netlist extracted from layout).

In your report, you need to show the following:

1. Screenshot of your layout with the height of the layout annotated.
2. DRC clean screenshot.
3. LVS clean screenshot.
4. The following table:

Inverter Dynamic Characteristic	Schematic	Layout
Rise time, t_r (ps)		
Fall time, t_f (ps)		
Propagation delay, t_p (ps)		

Q2) For the strength-2 inverter (**INVX2**) designed in assignment-1, repeat the Q1 above.

EE 671 VLSI DESIGN
Assignment 2

August 29, 2024

Nikita Suresh Madavi
23M1160

Question 1

- **Invertor Dynamic Characteristic table:**

Invertor Dynamic Characteristics	Schematic	Layout
Rise time, t_r(ps)	37.79006	43.68866
Fall time, t_f(ps)	37.72625	43.90110
Propogation Delay, t_p(ps)	37.7582	43.7949

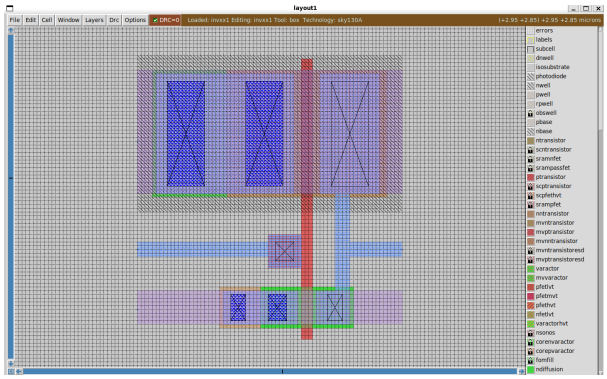

Figure 1: DRC INVX1

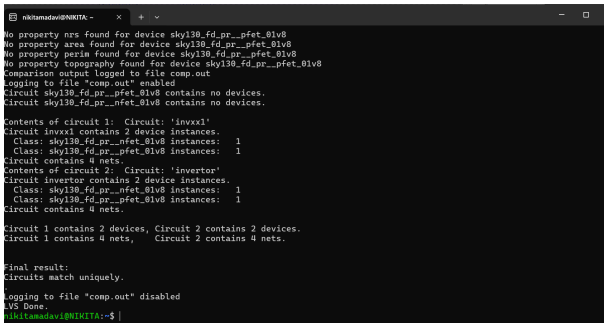

Figure 2: LVS INVX1

Question 2

- **Invertor Dynamic Characteristic table:**

Invertor Dynamic Characteristics	Schematic	Layout
Rise time, t_r(ps)	35.64919	46.50973
Fall time, t_f(ps)	32.45473	43.63494
Propogation Delay, t_p(ps)	34.0520	45.0723

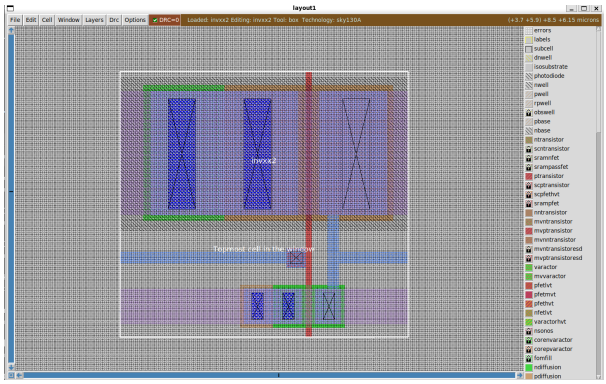

Figure 3: DRC INVX2

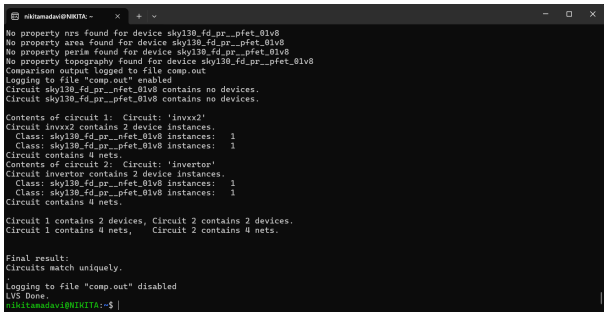

Figure 4: LVS INVX2