Saturday Aug 10, 2024	EE 671: VLSI DESIGN 2024/2025 ASSIGNMENT-1	Due On Aug 18, 2024

Note:

1. Submission is **only** through Moodle in the form of a PDF file upload.
2. All plots must be legible/readable in the submission (axes values and units)
3. Kindly install the necessary Tools and the PDK, procedure for which is mentioned in a separate file named "Sky130-Ngspice-Magic_Installation.pdf".
4. For all your simulations, use V_{DD} = 1.8 V.

Introduction:

In this assignment you will design and simulate CMOS inverters using SkyWater 130A PDK.

You will use NGSpice (a spice circuit simulator) tool to simulate the circuit. NGSpice takes a spice netlist file as an input. A sample netlist is given in the Installation guide provided.

You need to create the netlist for the schematic shown in Fig. 1 including the MOSFETs and their dimensions (Width, *W* and Length, *L*). In addition to this, we want to include the MOSFET drain and source capacitance using spice area parameters "as", "ad" and perimeter parameter "pd". These will depend on the transistor geometry. Referring to the Fig. 2, the Width of the diffusion region is *W* while its length is 4λ. Since $\lambda = L_{min}/2$, $4\lambda = 2L_{min}$.

a. The source/drain area parameters are: as = ad = $W \times 2\ L_{min}$
b. The source/drain perimeters are: ps = pd = $2 \times (W + 2L_{min})$.

Notice that the values of area and perimeter of source and drain regions will have to be recalculated when you change the widths.

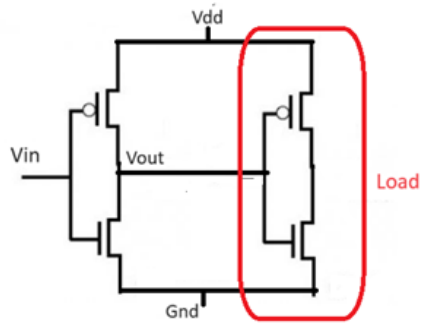

Figure 1: Inverter loaded with another inverter

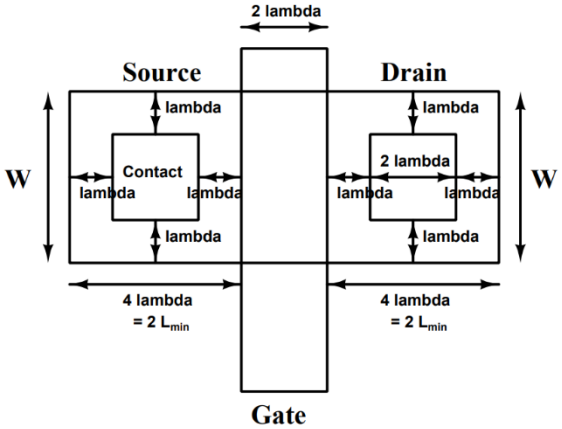

Figure 2: Illustration of diffusion area and perimeter

Q1) Design a minimum size CMOS inverter (minimum possible equal rise and fall time) with fixed NMOS and PMOS channel length of 0.15μm (this is the minimum channel length). The minimum channel width for NMOS is fixed to 0.4μm (restriction from the PDK) and the width of PMOS is to be obtained by design. The input should be a rail-to-rail square wave with rise/fall times of 20 ps, and the inverter will be loaded by another minimum size inverter (as shown in Fig. 1).
Simulate and report the following in the tabular fashion shown below:

Inverter Design Parameter	**Value**
PMOS Width (μm)	
PMOS Length (μm)	0.15
NMOS Width (μm)	0.4
NMOS Length (μm)	0.15

Inverter Dynamic Characteristic	**Value**
Rise time, t_r (ps)	
Fall time, t_f (ps)	
Propagation delay, t_p (ps)	

Once designed, **plot** (in the submission) the static transfer characteristics of this inverter by using a DC sweep on the input from 0 to VDD and report the following in the tabular fashion below:

Inverter Static Characteristic	**Value**
V_{IH} (V)	
V_{IL} (V)	
NM_H (V)	
NM_L (V)	
Switching Voltage, V_M (V)	

Q2) Let's call the inverter in Q1 as **INVX1** (strength-1 inverter). Design a strength-2 inverter (**INVX2**) and report all the tabular parameters above when the **INVX2** is loaded with **INVX1**. Comment on the results obtained.

EE 671 VLSI DESIGN
Assignment 1

August 18, 2024

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Question 1

- After the hit and trail method, to obtain PMOS width for equal rise and fall time of driving invertor keeping other parameters fixed.
  - **Invertor Design Parameter**

Invertor Design Parameters	**Values**
PMOS Width (μm)	1.449776
PMOS Length (μm)	0.15
NMOS Width (μm)	0.4
NMOS Length (μm)	0.15

- **Invertor Transfer Characteristics**
  - A DC sweep of *V(vin)* from **0 to 1.8V** was performed.After which *V(vout1)*, were vout1 is the output of driving invertor; as a function of the sweep voltage, defined a variable *var* to store the **derivative of V(vout1)**.
  - To find the noise margins, the *meas* command is used to find the points where *var* was becoming *-1*. Using this approach the values of VOL, VOH , VIL, VOL were found. Then the values of the high noise margin and the low noise margin where printed.

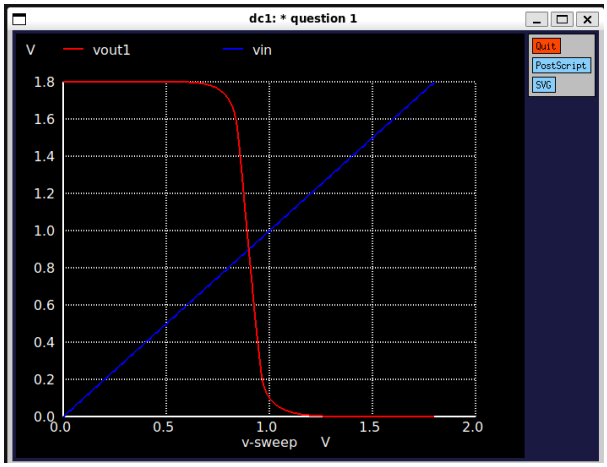

Figure 1: DC sweep of INV1

– **Invertor Dynamic Characteristic table:**

Invertor Dynamic Characteristics	Values
Rise time, t_r(ps)	29.02246
Fall time, t_f(ps)	29.02268
Propogation Delay, t_p(ps)	29.0226

– **Invertor Static Characteristic table:**

Invertor Static Characteristics	Values
V_{IH}(V)	1.022502
V_{IL}(V)	0.7736775
NM_H(V)	0.7201090
NM_L(V)	0.7016375
Switching Voltage,V_M(V)	0.8996688

Question 2

- In this question, we need to design INVX2 which as strength double as that of INVX1. To achieve that we have doubled the width of PMOS and NMOS respectively.
- The design parameters of PMOS and NMOS are as followed.
  – **Invertor Design Parameter**

Invertor Design Parameters	INV1	INV2
PMOS Width (μm)	1.449776	2.899552
PMOS Length (μm)	0.15	0.15
NMOS Width (μm)	0.4	0.8
NMOS Length (μm)	0.15	0.15

- **Invertor Transfer Characteristics**
  – A DC sweep of *V(vin)* from **0 to 1.8V** was performed.After which *V(vout1)*, were vout1 is the output of driving invertor *INVX2*; as a function of the sweep voltage, defined a variable *var* to store the **derivative of V(vout1)**.
  – To find the noise margins, the *meas* command is used to find the points where *var* was becoming *-1*. Using this approach the values of VOL, VOH , VIL, VOL were found. Then the values of the high noise margin and the low noise margin where printed.

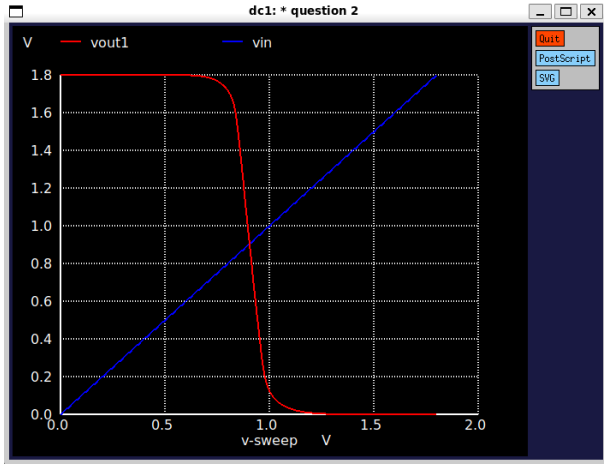

Figure 2: DC sweep of INV2

– Invertor Dynamic Characteristic table:

Invertor Dynamic Characteristics	**INV1**	**INV2**
Rise time, t_r(ps)	29.02246	21.14354
Fall time, t_f(ps)	29.02268	19.05521
Propogation Delay, t_p(ps)	29.0226	20.0994

– Invertor Static Characteristic table:

Invertor Static Characteristics	**INV1**	**INV2**
V_{IH}(V)	1.022502	1.035692
V_{IL}(V)	0.7736775	0.778408
NM_H(V)	0.721090	0.710583
NM_L(V)	0.7016375	0.7056686
Switching Voltage,V_M(V)	0.8996688	0.9045879

- **OBSERVATION**
  - The static characteristics show small changes, but they are less affected than the dynamic chharacteristics.
  - Switching voltage(VM) increases slightly for INVX2 compared to INVX1, but the difference is very small.
  - Noise margins (NMH and NML) changes though not drastically.Because :
    - VIH and VIL shift slightly due to the different transistor sizes in INV2.
    - This lead to small changes in noise margins.
  - There as significant changes in the dynamic characteristics:
    - Rise time (tr) and fall time (tf) **decreases** for *INVX2* because ***INVX2 has large transistors, allowing it to charge and discharge the load more quickly***.
    - As a result the propogation delay(tp) also **decreases**.