Monday Oct 7, 2024	EE 671: VLSI DESIGN 2024/2025 ASSIGNMENT-4	Due On Oct 14, 2024

Note:

1. This assignment will be done in groups with one submission per group.
2. Submission is **only** through Moodle in the form of a PDF file upload.
3. All plots/screenshots must be legible/readable in the submission (axes values and units).

Introduction:

In this assignment you will perform physical design of the RTL logic created from synthesis in Assignment-3. This will be done through OpenLane based open-source IC design flow. This is divided into two steps. You will first perform (a) physical design to generate all output files like lef, lib, spef, sdf, gds, RTL (post physical design) and (b) perform functional simulation and verify the post physical design RTL netlist.

Instructions to login to the VLSI lab machine:

- Each group is assigned a group id for login. Refer to your login id from here. The default password is EE671
- If you are on any unix based system, open a terminal for subsequent steps. If you are on Windows, download MobaXterm and open a terminal via MobaXterm. Ensure you are connected to IITB network.
- To login, type on the terminal: *ssh -X EE671_X@10.107.90.73* (X corresponds to the number from your login id assigned to your group). Enter the password and you are good.
- After the first login, type on the terminal: *passwd* and change your password immediately.

Q) In this assignment you will perform physical design of a 16-bit Brent-Kung tree adder based on the RTL from Assignment-3. Open the openlane prompt with the -overwrite flag (i.e., ./flow.tcl -design bkadder -tag full_guide -interactive -**overwrite**). This will overwrite the earlier runs (that you performed in assignment-3). Now, run the following commands in the openlane container (similar to assignment-3) one by one.

a. **run_synthesis**
b. **run_floorplan**
c. **run_placement**
d. **run_cts**
e. **run_routing**
f. **run_parasitics_sta**
g. **run_magic**
h. **run_magic_spice_export**
i. **run_magic_drc**
j. **run_lvs**
k. **run_antenna_check**

Exit the container after running these steps and go to the "runs" folder similar to assignment-3.

Note-1: To open Magic, go to the folder where you want to open and type the following in the terminal

a) **source ~/.bashrc**
b) **magic &**

Note-2: To open a def file, first read the lef files in the terminal using **lef read** command and then read the def using **def read** command (screenshot shown below for an example alu.def), on the Magic terminal.

```
% lef read ~/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_fd_sc_hd.lef
Reading LEF data from file /home/running_courses/EE671/EE671_55/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_fd_sc_hd.lef.
This action cannot be undone.
LEF read: Processed 56535 lines.
% lef read ~/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_ef_sc_hd.lef
Reading LEF data from file /home/running_courses/EE671/EE671_55/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_ef_sc_hd.lef.
This action cannot be undone.
LEF read: Processed 278 lines.
% def read alu.def
Reading DEF data from file alu.def.
This action cannot be undone.
  Processed 4 vias total.
  Processed 358 subcell instances total.
  Processed 33 pins total.
  Processed 2 special nets total.
  Processed 297 nets total.
DEF read: Processed 1088 lines.
```

Note-3: To open a gds file, use the **gds read** command.

Your report should have the following:

1. Read the def file after floorplan and paste the screenshot of the floorplan
2. Read the def file after placement and paste the screenshot of the placed design
3. Read the def file after cts and paste the screenshot of the design
4. Read the def file after routing and paste the screenshot of the routed design
5. Go to the signoff folder and read the final gds on Magic → select entire design → in the Cell option, click on expand to view the entire layout of the design. Your layout must look like Fig. 1 below.
6. Go to the reports/signoff folder, open the lvs.rpt file using nedit and provide a screenshot showing 0 errors
7. Go to the reports/signoff folder, open the drc.rpt file using nedit and provide a screenshot showing 0 errors
8. Go to the logs/routing folder, open the grt_sta.log and fill up the table below:

Clock Frequency (MHz)	
Worst case setup slack (ns)	
Worst case hold slack (ns)	
Design area (μm^2)	
Power Consumption (Sequential) (µW)	
Power Consumption (Combinational) (µW)	
Power Consumption (Clock) (µW)	
Total Power Consumption (µW)	

9. Verify the post physical design RTL (RTL is in the path: results/routing/<design>.nl.v) with a functional simulation using the same testbench that was used to verify the post synthesis RTL in assignment-3. Provide a screenshot of the Gtkwave waveform dump.

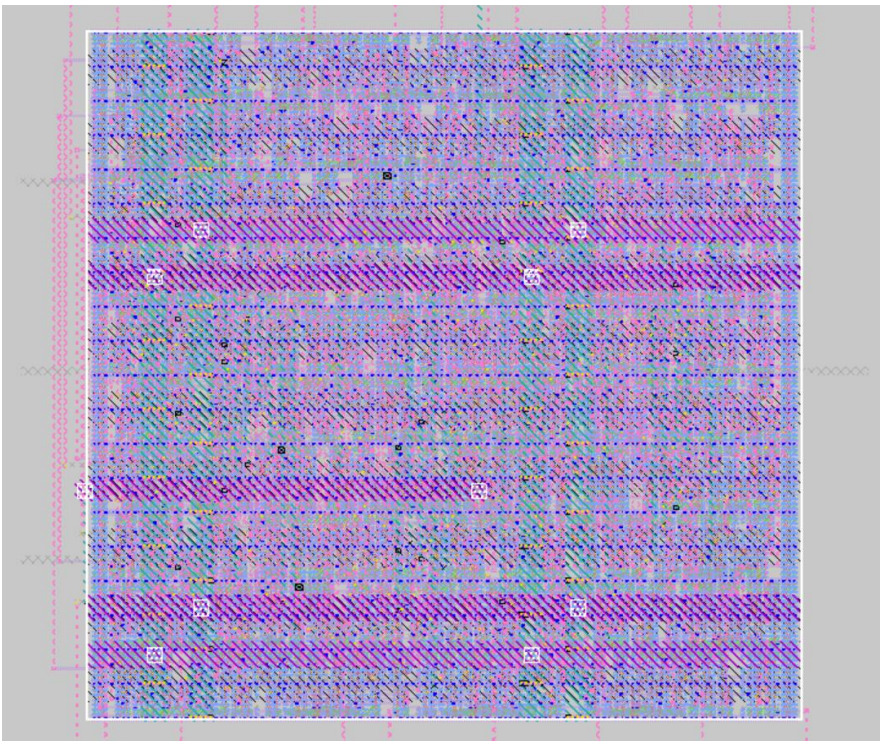

Figure 1: Example final layout (read from gds) of the alu design

Assignment 4

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Q1. The screenshot of floorplan is -

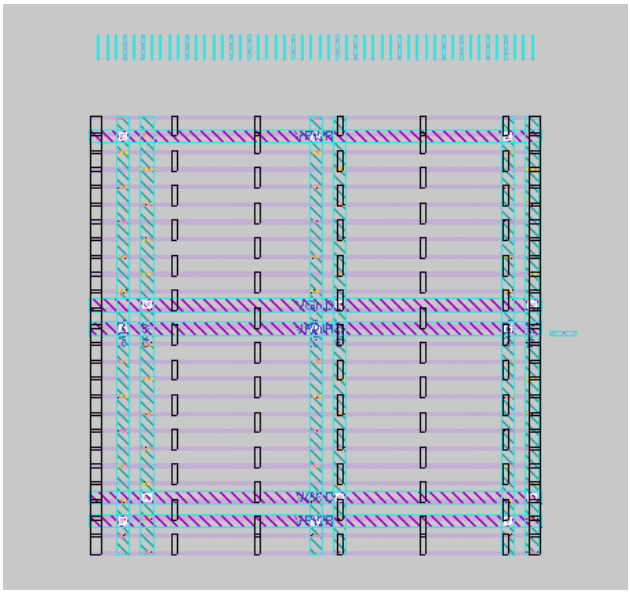

Figure 1: Screenshot of floorplan

Q2. The screenshot of placed design is -

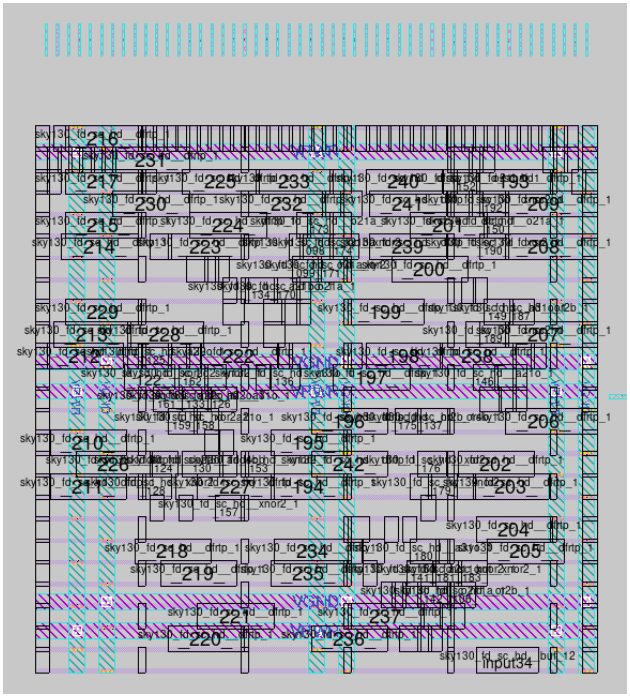

Figure 2: Screenshot after placement design

Q3. The screenshot after cts design is -

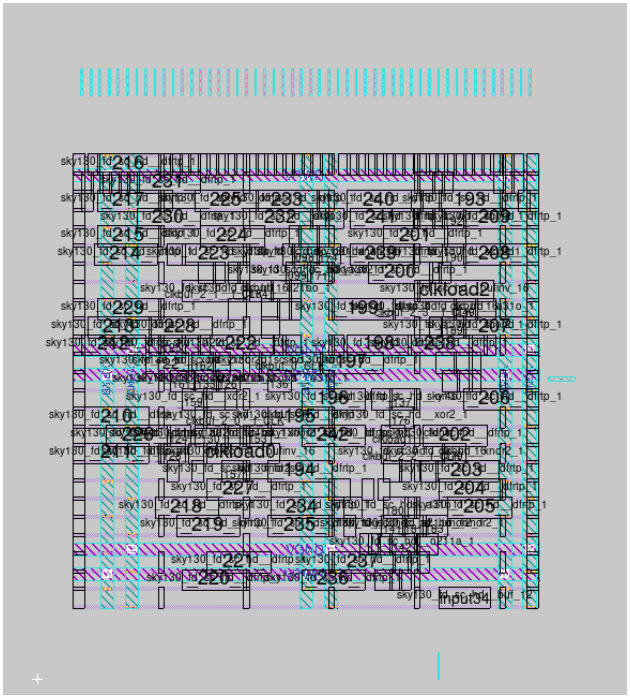

Figure 3: Screenshot of cts design

Q4. The screenshot of routed design is -

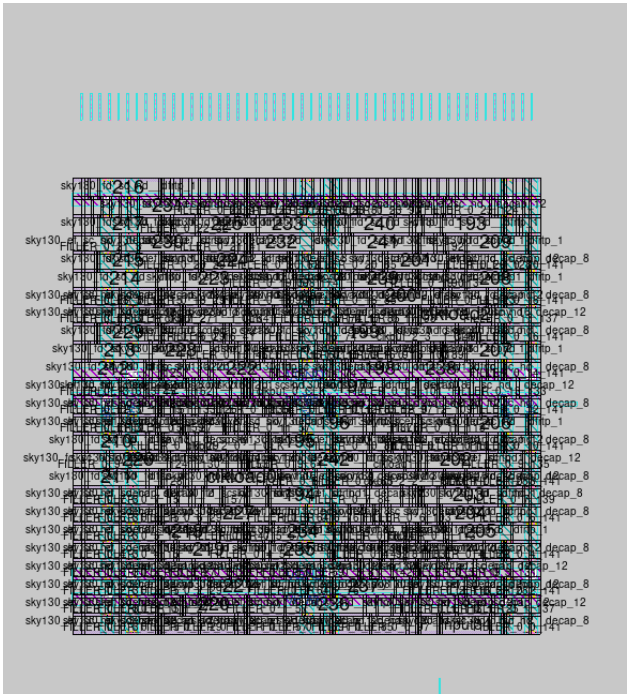

Figure 4: Screenshot of routed design

Q5. The screenshot of layout is -

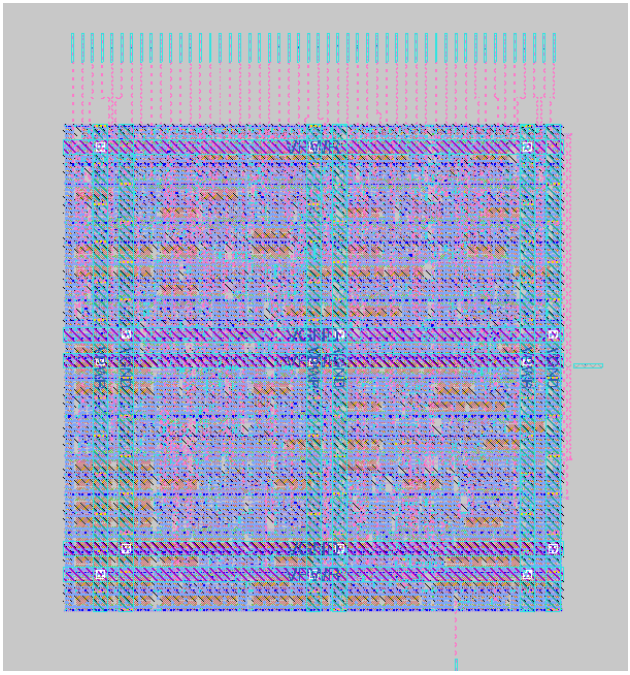

Figure 5: Screenshot of layout

Q6. The screenshot of lvs.rpt is -

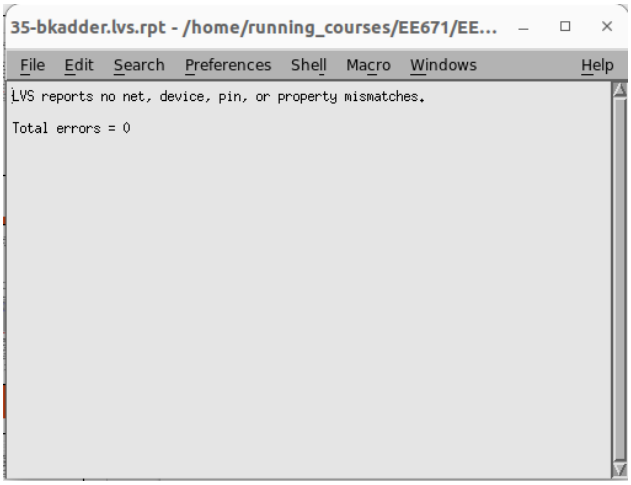

Figure 6: Screenshot of lvs.rpt

Q7. The screenshot of drc.rpt is -

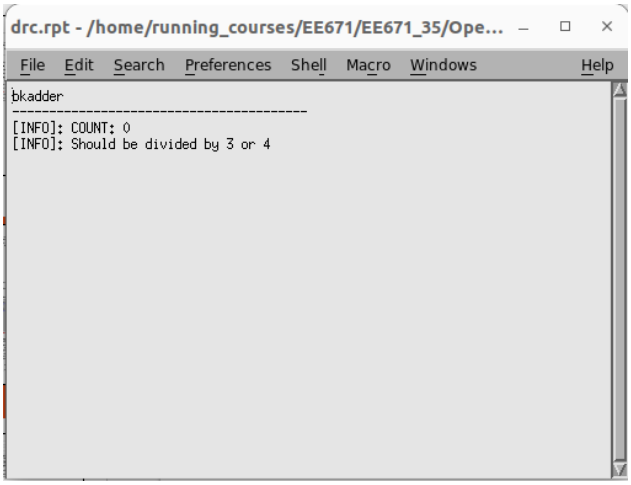

Figure 7: Screenshot of drc.rpt

Q8.

Clock Frequency (MHz)	100
Worst case setup slack (ns)	7.60
Worst case hold slack (ns)	0.47
Design area (μm^2)	2391
Power consumption (Sequential) (μW)	224
Power consumption (Combinational) (μW)	32.9
Power consumption (Clock) (μW)	192
Total power consumption (μW)	448

Table 1: Dynamic Characteristics

Q9. The screenshot of gtkwave waveform dump is -

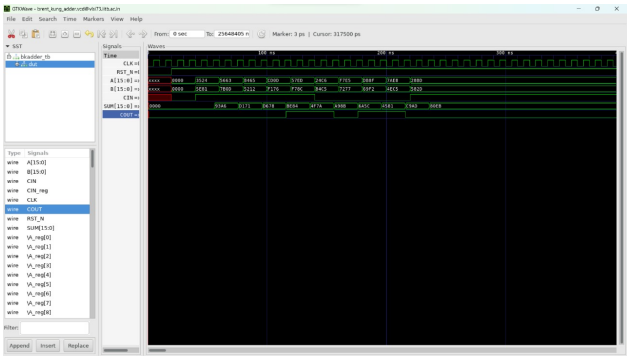

Figure 8: gtkwave waveform