For negative edge triggered D-flip flop,

1. **Input pin capacitances:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Input Pins** | **Rise Cap (pF)** | **Fall Cap (pF)** | **Average Cap (pF)** |
| D | 0.00354533 | 0.000459163 | 0.00200223 |
| CLK | 0.0102229 | 0.00145032 | 0.005111522 |

1. **Set-up Time Table:**

**(i) Rise Constraint** **(in ns)** [Input slew vs CLK slew].

|  |  |  |
| --- | --- | --- |
|  | **10 ps** | **1000 ps** |
| **10 ps** | 0.01425282 | 0.034637786 |
| **1000 ps** | 0.045176480 | 0.65359066 |

**(ii) Fall Constraint** **(in ns)** [Input slew vs CLK slew].

|  |  |  |
| --- | --- | --- |
|  | **10 ps** | **1000 ps** |
| **10 ps** | -0.018027090 | 0.0353015957 |
| **1000 ps** | -0.0193046005 | 0.0507489129 |

1. **Hold Time Table:**

**(i) Rise Constraint** **(in ns)** [Input slew vs CLK slew].

|  |  |  |
| --- | --- | --- |
|  | **10 ps** | **1000 ps** |
| **10 ps** | 0.019727646 | 0.0624721458 |
| **1000 ps** | 0.0423062338 | 0.0762065816 |

**(ii) Fall Constraint** **(in ns)** [Input slew vs CLK slew].

|  |  |  |
| --- | --- | --- |
|  | **10 ps** | **1000 ps** |
| **10 ps** | -0.0468753920 | 0.0203428917 |
| **1000 ps** | -0.0645172322 | 0.0390887286 |

1. **Transition Time Table (for Q output, CLK will have minimum slew of 10 ps):**

**(i) Output Rise Transitions** **(in ns)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | 0.01655450 | 0.01655450 | 0.01655450 |
| **10 fF** | 0.06391686 | 0.06391686 | 0.06391686 |
| **100 fF** | 0.5127856 | 0.5127856 | 0.5127856 |

**(ii) Output Fall Transitions** **(in ns)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | 0.01847117 | 0.02413608 | 0.09403371 |
| **10 fF** | 0.07297505 | 0.07297581 | 0.1746073 |
| **100 fF** | 0.5895973 | 0.5895872 | 0.5998571 |

1. **CLK-to-Q Delay Time Table**:

**(i) Cell Rise Delay (in ns)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | 4.033857 | 4.078857 | 4.528857 |
| **10 fF** | 4.066659 | 4.111659 | 4.561659 |
| **100 fF** | 4.371859 | 4.416859 | 4.866859 |

**(ii) Cell Fall Delay (in ns)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | -3.991421 | -4.018944 | -4.414897 |
| **10 fF** | -3.948992 | -3.974892 | -4.296556 |
| **100 fF** | -3.553130 | -3.578036 | -3.824397 |

1. **Static Power (all possible input combinations of CLK and D).**

|  |  |
| --- | --- |
| **Condition (CLK, D)** | **Power (nW)** |
| 00 | 0.00334618 |
| 01 | 0.0237638660 |
| 10 | 0.0359171648 |
| 11 | 0.0809045305 |

1. **Dynamic Power Table: (CLK will have minimum slew of 10 ps)**

**(i) Rise Power (in nW)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | 0.073189584 | 0.072531465 | 0.07178725162 |
| **10 fF** | 0.0725061 | 0.104385255 | 0.101387255 |
| **100 fF** | 0.4253138 | 0.7311719 | 0.1725469 |

**(ii) Fall Power (in nW)** [Input slew vs output capacitance].

**Related pin D**: (i.e., other input pins are held constant)

|  |  |  |  |
| --- | --- | --- | --- |
|  | **10 ps** | **100 ps** | **1000 ps** |
| **0.5 fF** | -0.063145658 | 0.01247831 | -0.631246987 |
| **10 fF** | -0.06194626 | 0.1010258 | -0.5032542 |
| **100 fF** | 0.06254158 | 0.1324651 | 0.7251154 |