MINI PROJECT:

Design and implementation of Comparator using CADENCE.

The simulations in 90nm and 45nm technology are as follows:

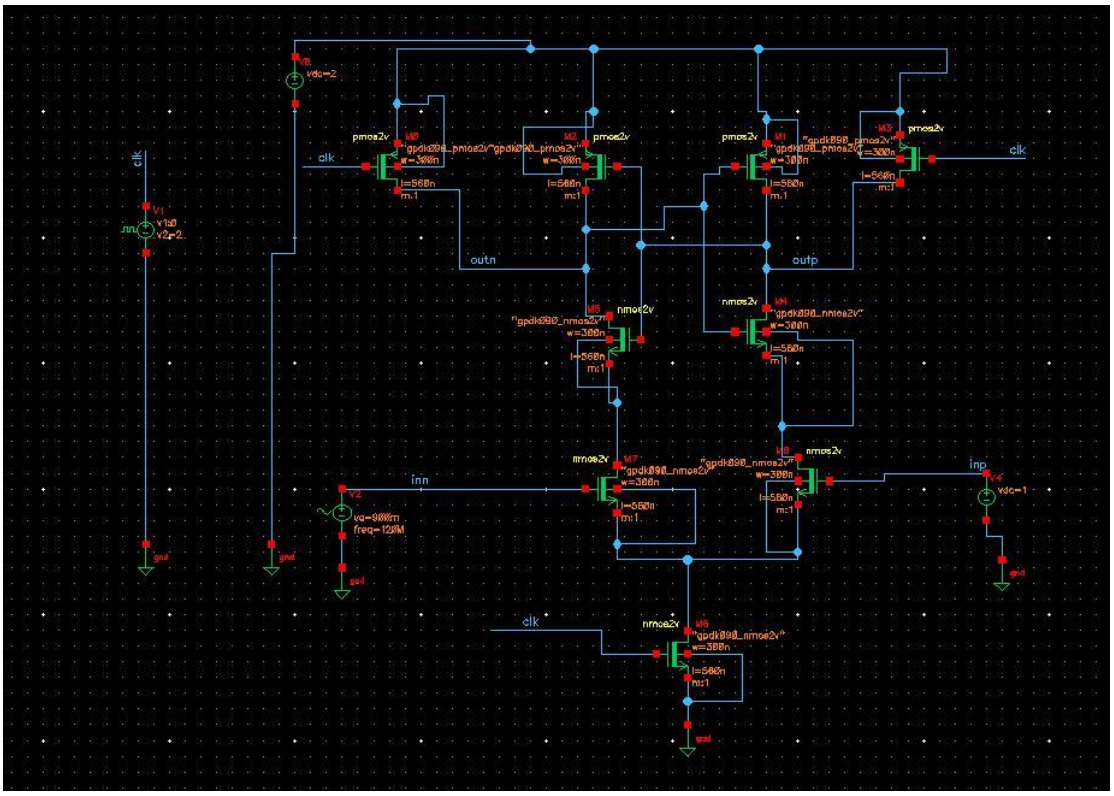

Fig shows conventional comparator schematic view in 90nm technology

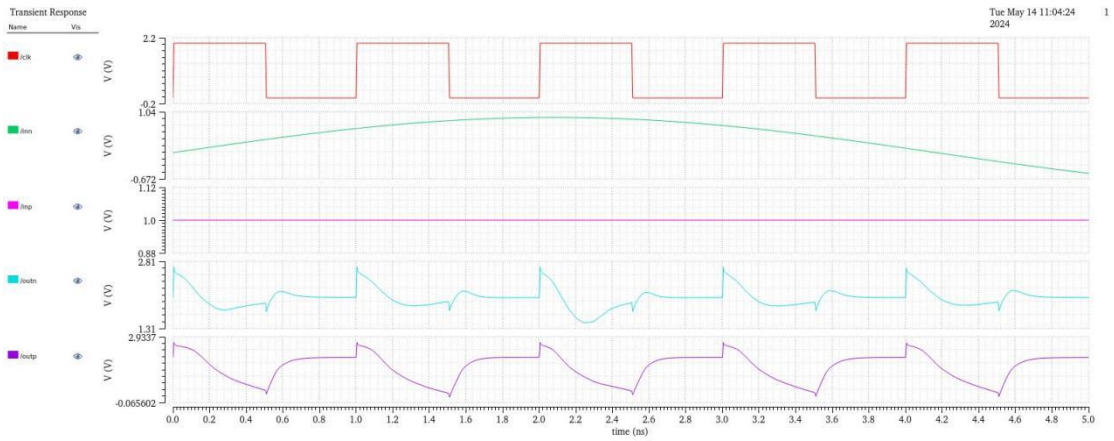

Fig shows output waveform for the conventional comparator in 90nm technology

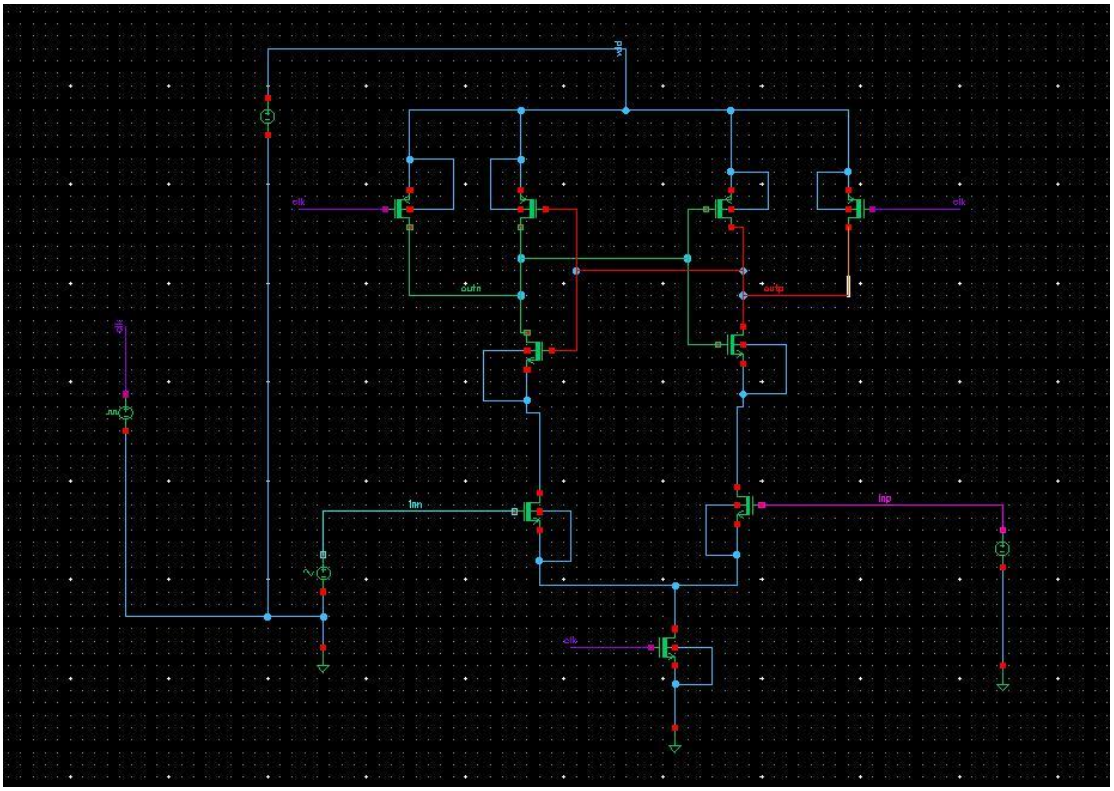

Fig shows conventional comparator schematic view in 45nm technoloogy

Fig shows output waveform for the conventional comparator in 90nm technology

The following tabular form shows the comparision of a conventional comparator in 180nm , 90nm &45nm technology

Parameter			
CMOS technolgy	180nm	90nm	45nm
Vdc	1.8	1.8	1.8v
Vsine(Amplitude)	2v	2v	2v
Delay	500ps	500ps	500ps
Vsupply	2v	2v	2v
Average Power Consumption	38.54uW	23.45uW	12.5uW
Area Occupied	51x51um	13.19x12.25mm	4.56x6.25um