Ramaiah Institute of Technology
(Autonomous Institute, Affiliated to VTU)

Department of CSE

Programme: B.E
Course: Computer Organization

Term: Jan to May 2019
Course Code: CS45

Activity V: Designing an ALU to perform arithmetic and logical functions using Logisim simulator.

Name: Kuchi Ravi Teja	Marks: /10	Date:
USN: 1MS18CS060	Signature of the Faculty:	

Objective: To simulate the working of Arithmetic and Logical Unit using simulator.

Simulator Description: Logisim is an educational tool for designing and simulating digital logic circuits. With its simple toolbar interface and simulation of circuits as you build them, it is simple enough to facilitate learning the most basic concepts related to logic circuits. With the capacity to build larger circuits from smaller sub circuits, and to draw bundles of wires with a single mouse drag, Logisim can be used (and is used) to design and simulate entire CPUs for educational purposes.

Activity to be performed by students:

List out the steps in designing ALU

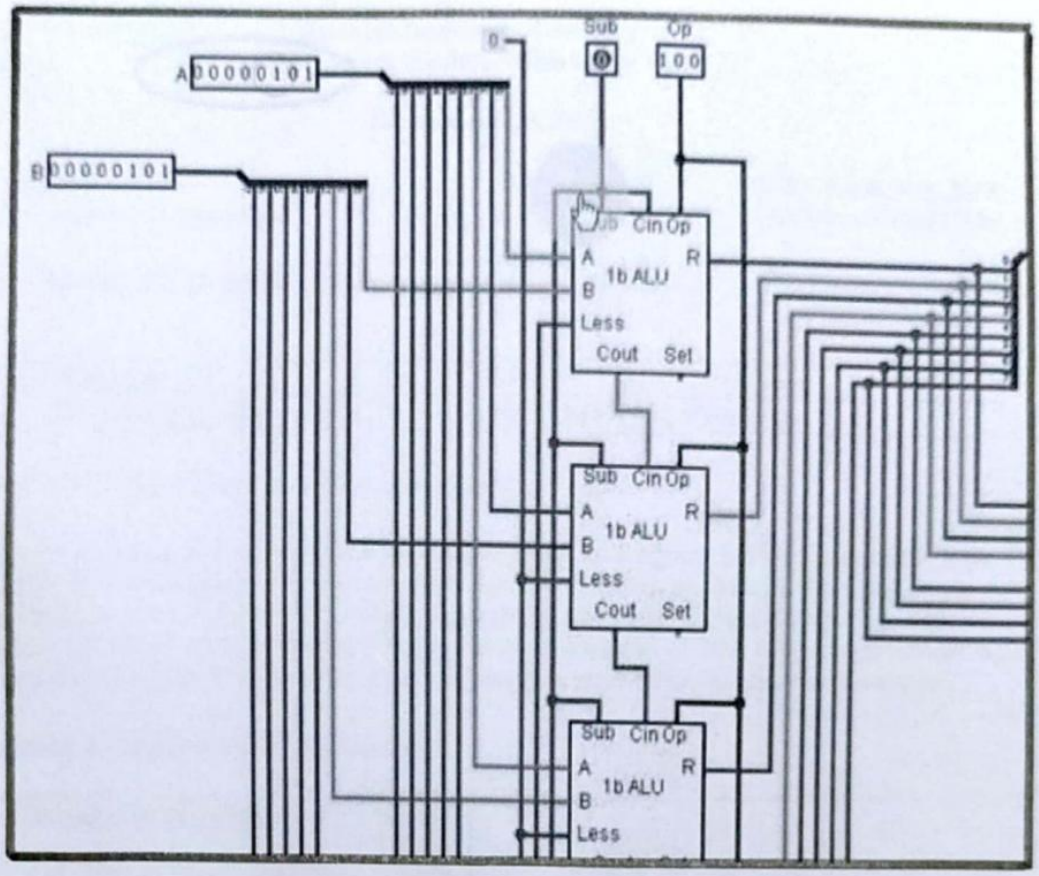
Name: Kuchi Ravi Teja
USN : 1MS18CS060

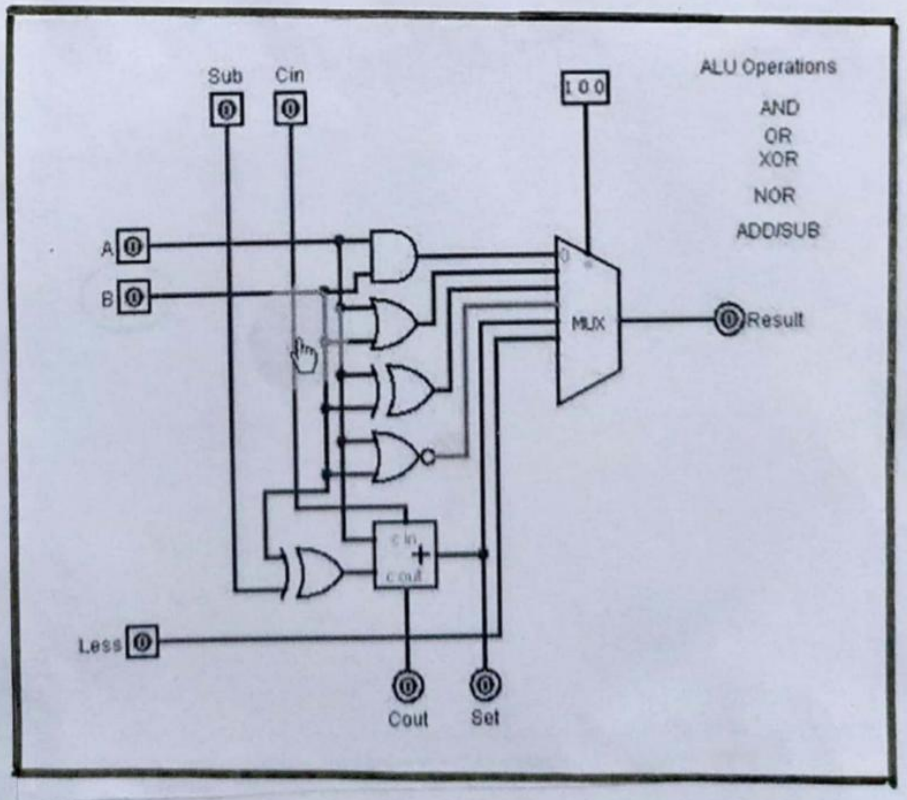
Activity V

1) list out the steps in designing ALU

1) Add the two i/p pins, Name them A & B
2) Add or, and, ex-or, nor gates & a 1 bit adder
3) Connect A's & B's of all the gates to their respective pins.
4) Add an output pin and name it Result
5) Add a 1 bit multiplexer with 3 select bits
6) connect outputs of all gates to the mux
7) connect 3-bit input pin to mux.
8) Add i/p pin to Cin, and output pin to Cout
9) Add an ex-or gate connect its O/p to Cout. The first i/p must be connected to B and the second to another i/p pin
10) Add another i/p and name it less. connect it to mux.
11) Add an output pin and name it Set, connect it to the o/p of adder circuit.

Snapshots.


A 00000101
B 00000101
0
Sub
Op
100
Sub Cin Op
A
B
1b ALU
R
Less
Cout Set
Sub Cin Op
A
B
1b ALU
R
Less
Cout Set
Sub Cin Op
A
B
1b ALU
R
Less


Sub
Cin
100
ALU Operations
AND
OR
XOR
NOR
ADD/SUB
A
B
MUX
Result
Less
Cout
Set

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Activity VI: Designing memory system using Logisim simulator.

Name: Kuchi Ravi Teja	Marks: /10	Date:
USN: 1MS18CS060	Signature of the Faculty:	

Objective: To simulate the writing operation on memory.

Simulator Description: Logisim is an educational tool for designing and simulating digital logic circuits. With its simple toolbar interface and simulation of circuits as you build them, it is simple enough to facilitate learning the most basic concepts related to logic circuits. With the capacity to build larger circuits from smaller sub circuits, and to draw bundles of wires with a single mouse drag, Logisim can be used (and is used) to design and simulate entire CPUs for educational purposes.

Activity to be performed by students:

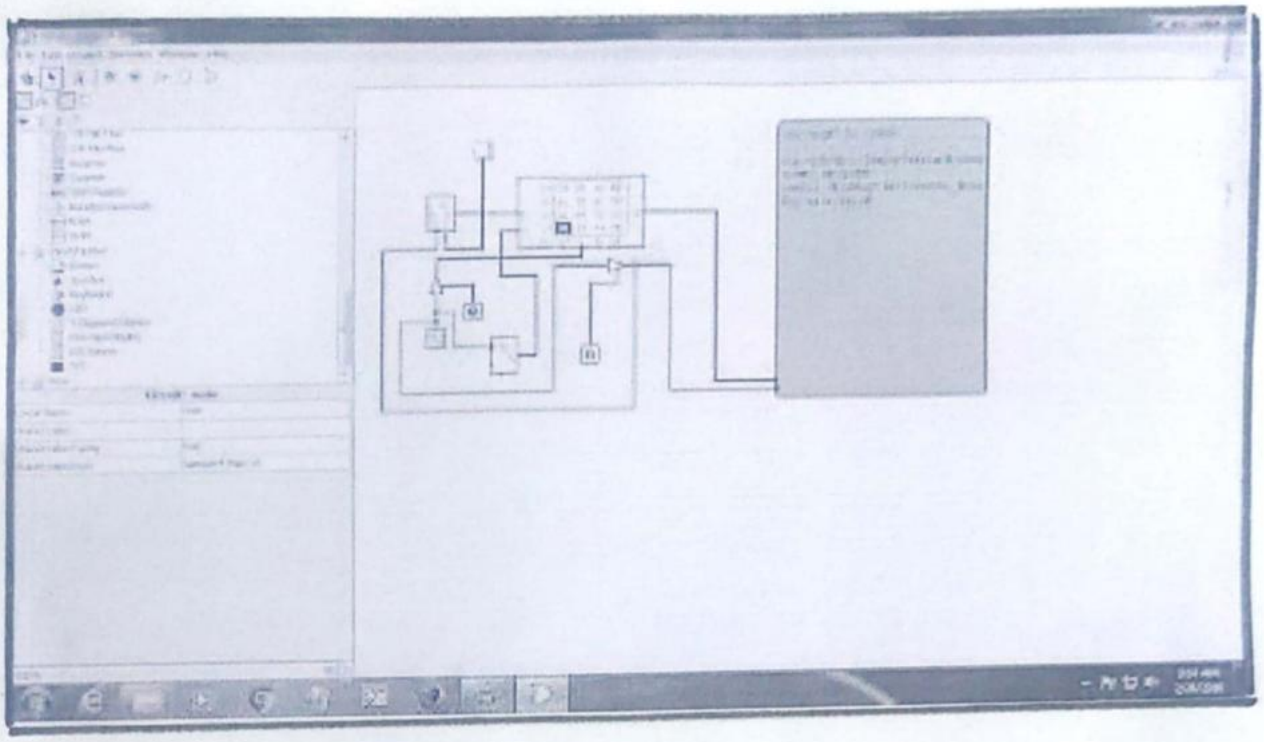
Name: Kuchi Ravi Teja | Activity VI

USN : 1MS18CS060

List out the steps in designing memory system.

1) Add a RAM with seperate load and store selected
2) Add a counter and connect Q to A of the RAM
3) Add a continuous roller buffer and connect its o/p to the RAM
4) Add a clock & connect to the i/p of buffer
5) Add a ~~clock and connect to~~ TTY unit with 32 rows & columns. Make the connections with ram
6) Add a 7-bit random number generator, connect Q to D
7) Add another controlled buffer, connecto to TTY. Also add an i/p pin to the buffer
8) Connect the output of the second buffer to the counter
9) Connect a button to the counter

Snapshots :



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Activity VII: To simulate advantages of using pipeline technique in executing a program.

Name: Kuchi Ravi Teja	Marks: /10	Date:
USN: 1MS18CS060	Signature of the Faculty:	

Objective: To learn and analyze the performance of the CPU by overlapping of instructions using CPUOS-SIM simulator.

Simulator Used: CPUOS-SIM is a software development environment for the simulation of simple computers. It was developed by Dale Skrien to help users to understand computer architectures.

Modern CPU's contain several semi-independent circuits involved in decoding and executing each machine instruction. Separate circuit elements perform each of these typical steps:

- Fetch the next instruction from memory into an internal CPU register.
- Decode the instruction to determine which function sub-circuits it requires.
- Read any input operands required from high-speed registers or directly from memory.
- Execute the operation using the selected sub-circuits.
- Write any output results to high-speed registers or directly to memory.

Separate sections of the CPU circuitry are used for each of these steps. This allows these circuit sections to be arranged into a sequential pipeline, with the output of one step feeding into the next step.

Name : Kuchi Ravi Teja
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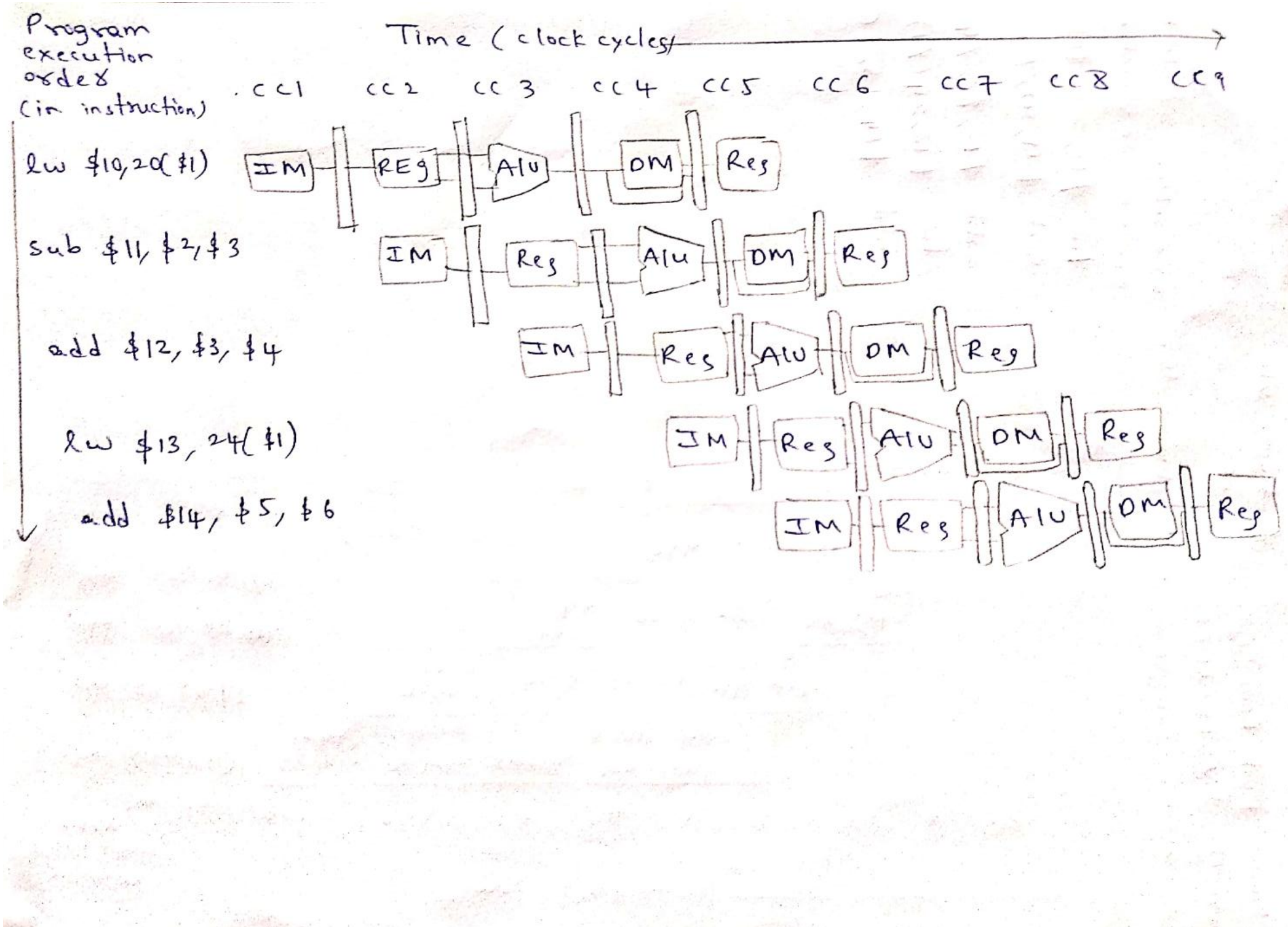
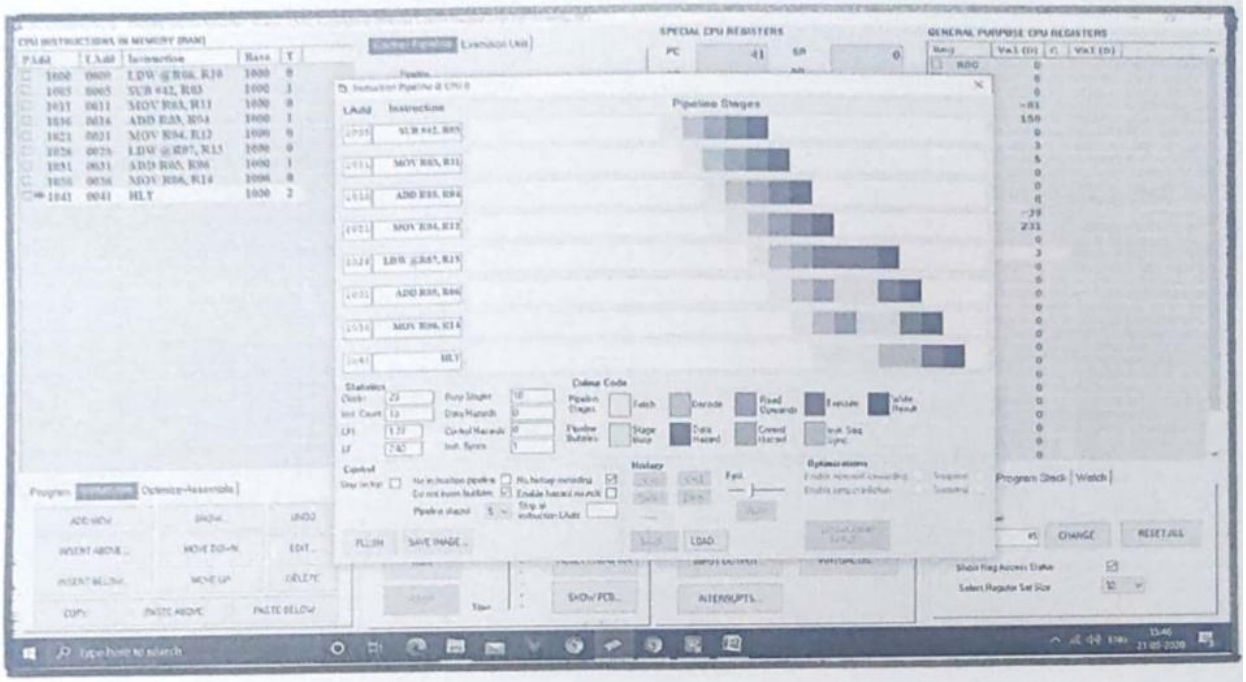
Activity VII

9) with diagram demonstrate the execution of following instructions

lw $10, 20($1)
sub $11, 42, $3
add $12, $3, $4
lw $13, 24($1)
add $14, $5, $6


Program execution order (in instruction)
Time (clock cycles)
cc1
cc2
cc3
cc4
cc5
cc6
cc7
cc8
cc9
lw $10, 20($1)
sub $11, $2, $3
add $12, $3, $4
lw $13, 24($1)
add $14, $5, $6
IM
REG
ALU
DM
Reg

Snapshots :


CPU INSTRUCTIONS IN MEMORY (RAM)
SPECIAL CPU REGISTERS
GENERAL PURPOSE CPU REGISTERS
Pipeline Stages
Program Stack
Watch
CHANGE
RESET ALL
SHOW PCB...
INTERRUPTS...
FLUSH
SAVE IMAGE...
LOAD