Ramaiah Institute of Technology
(Autonomous Institute, Affiliated to VTU)

Department of CSE

Programme: B.E **Term: Jan to May 2019**
Course: Computer Organization **Course Code: CS45**

Activity V: Designing an ALU to perform arithmetic and logical functions using Logisim simulator.

Name: Praharsh	**Marks: /10**	**Date:**
USN:1MS18CS090	**Signature of the Faculty:**	

Objective: To simulate the working of Arithmetic and Logical Unit using simulator.

Simulator Description: Logisim is an educational tool for designing and simulating digital logic circuits. With its simple toolbar interface and simulation of circuits as you build them, it is simple enough to facilitate learning the most basic concepts related to logic circuits. With the capacity to build larger circuits from smaller sub circuits, and to draw bundles of wires with a single mouse drag, Logisim can be used (and is used) to design and simulate entire CPUs for educational purposes.

Activity to be performed by students:

List out the steps in designing ALU

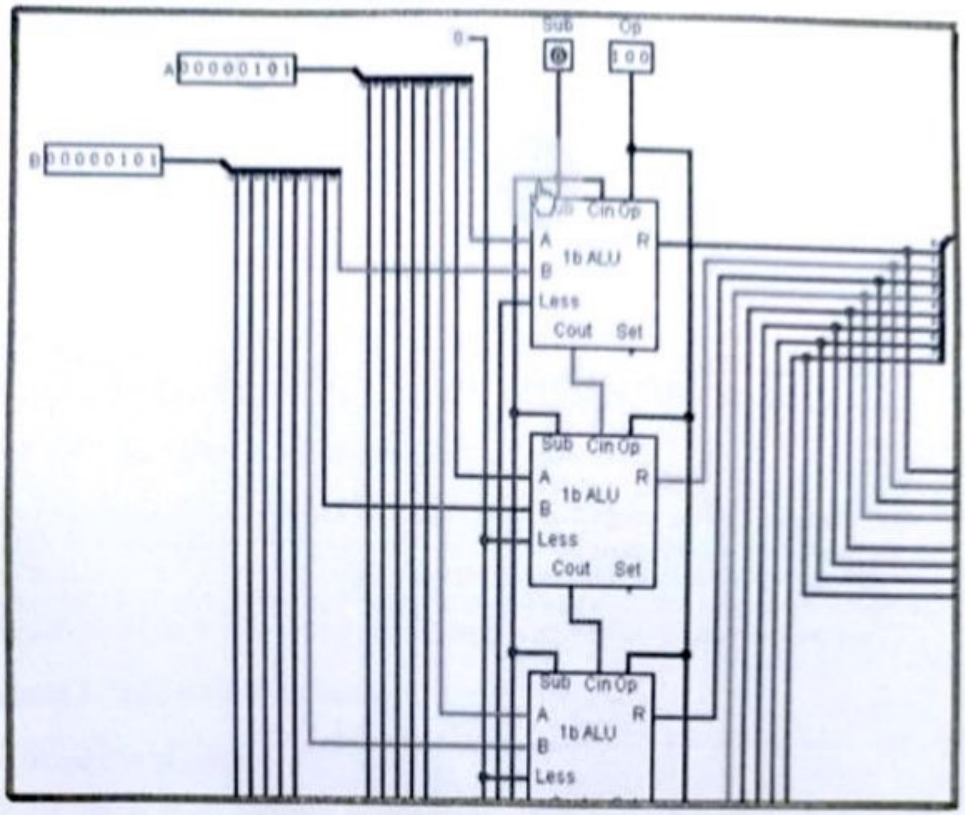
CO Lab - 5.

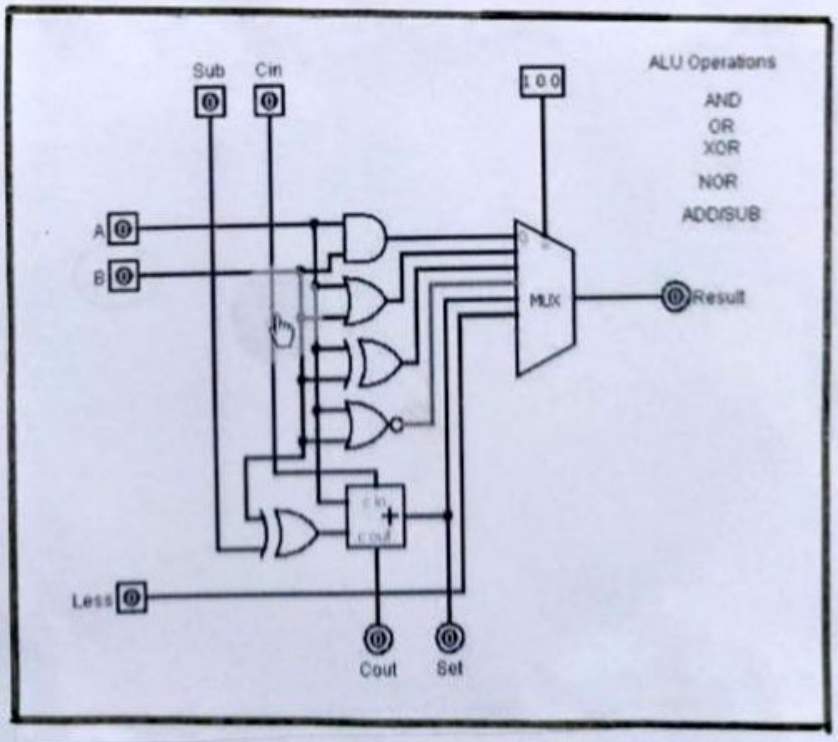
Name: Prahasrsh B.
1MS18CS090.

1) List out the steps in designing ALU

(i) Add the 2 i/p pins, name them A & B.
(ii) Add or, and ex-or, nor gate and a 1-bit address
(iii) Convert the A's & B's of all the gates to the respective pins.
(iv) Add an output pin & name it Result.
(v) Add a 1-bit multiplier with 3-select bits
(vi) Connect 3-bit input pin to mux.
(vii) Connect outputs of all the gates to the mux.
(viii) Add i/p pin to Cin, output pin to Cout.
(ix) Add ~~ip~~ & an ex-or gate. Connect its o/p to Cout. The first & i/p must be connected to B and second to another i/p pin sub.
(x) Add another i/p and name it less. Convert it to mux.
(xi) Add an output pin and name it set connect it to the o/p of adder unit.

Snapshots.





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Activity VI: Designing memory system using Logisim simulator.

Name: Praharsh	**Marks: /10**	**Date:**
USN:1MS18CS090	**Signature of the Faculty:**	

Objective: To simulate the writing operation on memory.

Simulator Description: Logisim is an educational tool for designing and simulating digital logic circuits. With its simple toolbar interface and simulation of circuits as you build them, it is simple enough to facilitate learning the most basic concepts related to logic circuits. With the capacity to build larger circuits from smaller sub circuits, and to draw bundles of wires with a single mouse drag, Logisim can be used (and is used) to design and simulate entire CPUs for educational purposes.

Activity to be performed by students:

List out the steps in designing memory system

CO Lab-6.

Name: Praharsh B.,
1MS18CS090/4B'

1) List out the steps in designing memory system

(i) Add a RAM with separate load and store selected

(ii) Add an counter and connect Q to A of the RAM.

(iii) Add a controller buffer and connect its o/p to the RAM.

(iv) Add a clock and connect to the i/p of the buffer

(v) Add a TTY unit with 32 rows and ~~the~~ columns. Make the connections with RAM.

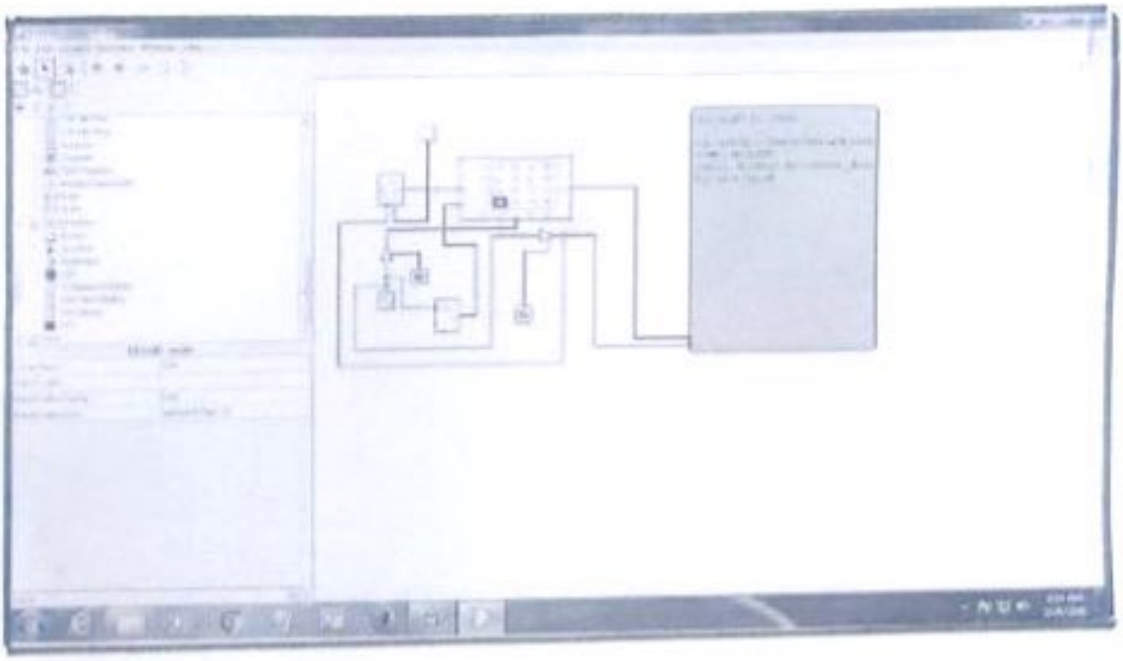
(vi) Add a 7-bit random number generator, convert Q to D.

(vii) Add another controlled buffer, convert to TTY. Also add an i/p pin to the buffer.

(viii) Convert the output of the second buffer to the counter.

(ix) Convert a button to the counter.

Snapshots :



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Programme: B.E **Term: Jan to May 2019**
Course: Computer Organization **Course Code: CS45**

Activity VII: To simulate advantages of using pipeline technique in executing a program.

Name: Praharsh	**Marks: /10**	**Date:**
USN: 1MS18CS090	**Signature of the Faculty:**	

Objective: To learn and analyze the performance of the CPU by overlapping of instructions using CPUOS-SIM simulator.

Simulator Used: CPUOS-SIM is a software development environment for the simulation of simple computers. It was developed by Dale Skrien to help users to understand computer architectures.

Modern CPU's contain several semi-independent circuits involved in decoding and executing each machine instruction. Separate circuit elements perform each of these typical steps:

- Fetch the next instruction from memory into an internal CPU register.
- Decode the instruction to determine which function sub-circuits it requires.
- Read any input operands required from high-speed registers or directly from memory.
- Execute the operation using the selected sub-circuits.
- Write any output results to high-speed registers or directly to memory.

Separate sections of the CPU circuitry are used for each of these steps. This allows these circuit sections to be arranged into a sequential pipeline, with the output of one step feeding into the next step.

Activity to be performed by students:

With diagram demonstrate the execution of the following instructions using pipelining technique.

```
lw   $10,20($1)
sub  $11, 42, $3
add  $12, $3, $4
lw   $13, 24($1)
add  $14, $5, $6
```

CO Lab-7 Name: Prahassh B 1MS18CS090 4'B'

Program execution order (in instructions)

Time (in clock cycles).

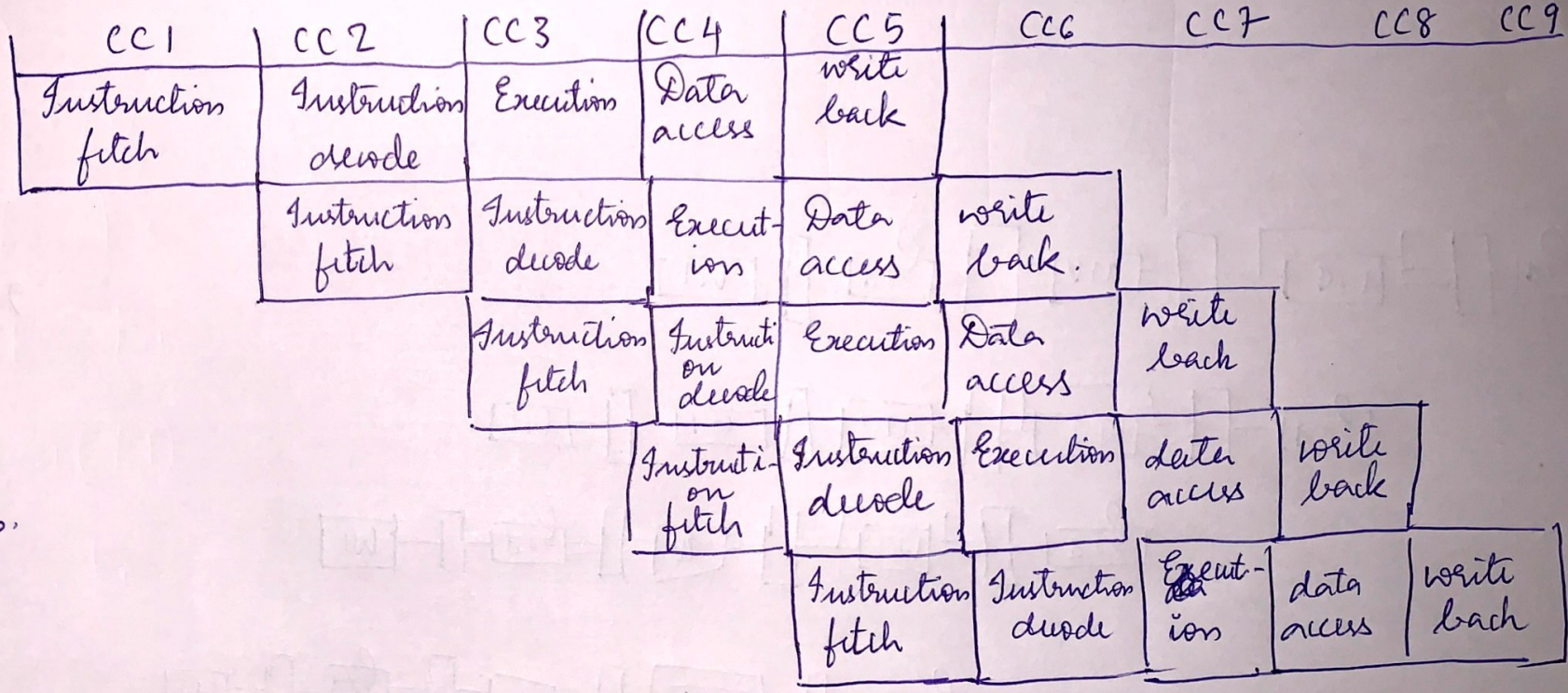
lw $10,20($1)

sub $11,$2,$3

add $12,$3,$4

lw $13,24($1)

add $14,$5,$6.



Program execution order (in instructions)

Time (in clock cycles) →

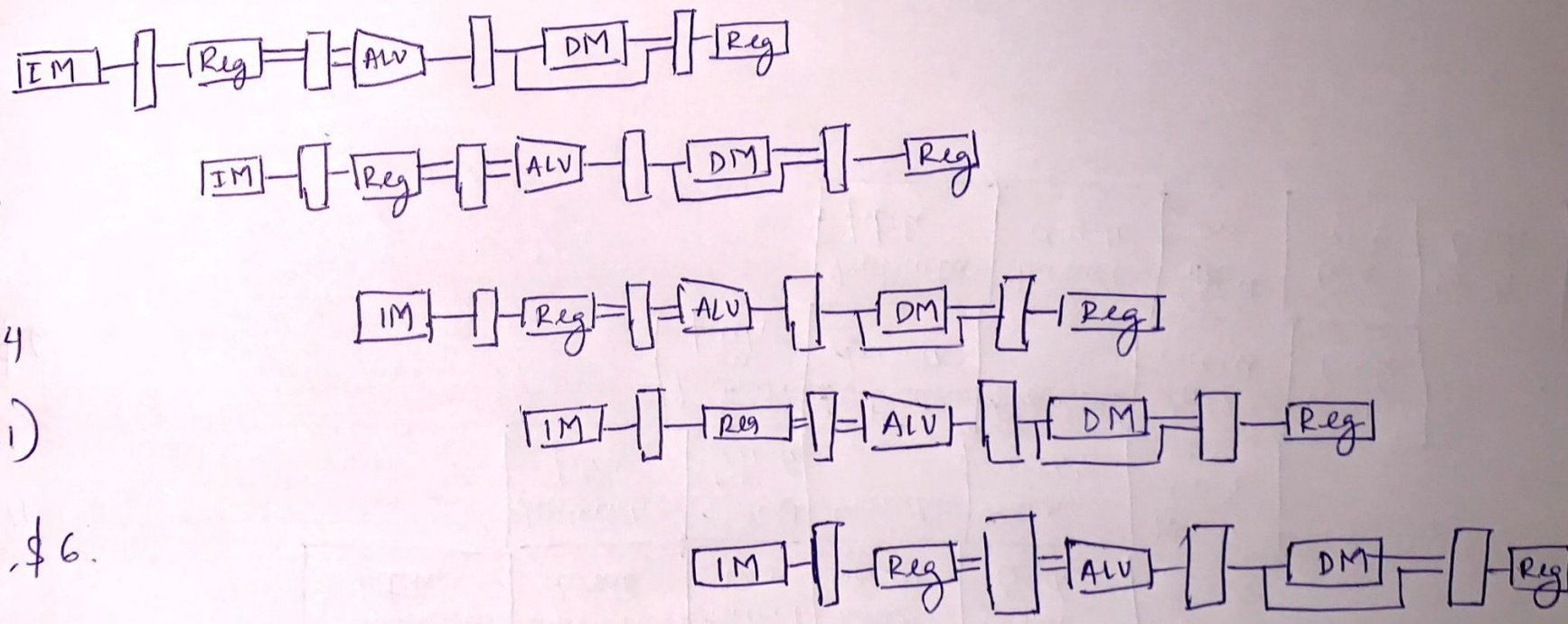
lw $10, 20($1)

sub $11, $2, $3

add $12, $3, $4

lw $13, 24($1)

add $14, $5, $6.



Snapshots :