Microprocessor Unit 5 Notes

-Compiled by Prof. Minakshi

Unit 5 Syllabus

Peripheral Devices: 8237 DMA Controller, 8255 programmable peripheral interface, 8253/8254 programmable timer/counter, 8259 programmable interrupt controller, 8251 USART and RS232C.

8237 DMA Controller

What is DMA (Direct Memory Access)?

- Direct Memory Access (DMA) transfers the block of data between the memory and peripheral devices of the system, without the participation of the processor. The unit that controls the activity of accessing memory directly is called a DMA controller.

- The processor gives the control of the system bus to the DMA controller for a few clock cycles. So, the DMA controller can accomplish the task of data transfer via the system bus.

DMA Controller Working

- Whenever an I/O device wants to transfer the data to or from memory, it sends the DMA request (DRQ) to the DMA controller. DMA controller accepts this DRQ and asks the CPU to hold for a few clock cycles by sending it the Hold request (HLD).
- CPU receives the Hold request (HLD) from DMA controller and relinquishes the bus and sends the Hold acknowledgement (HLDA) to DMA controller.
- After receiving the Hold acknowledgement (HLDA), DMA controller acknowledges I/O device (DACK) that the data transfer can be performed and DMA controller takes the charge of the system bus and transfers the data to or from memory.
- When the data transfer is accomplished, the DMA raises an interrupt to let know the processor that the task of data transfer is finished and the processor can take control over the bus again and start processing where it has left.

8237 DMA Controller

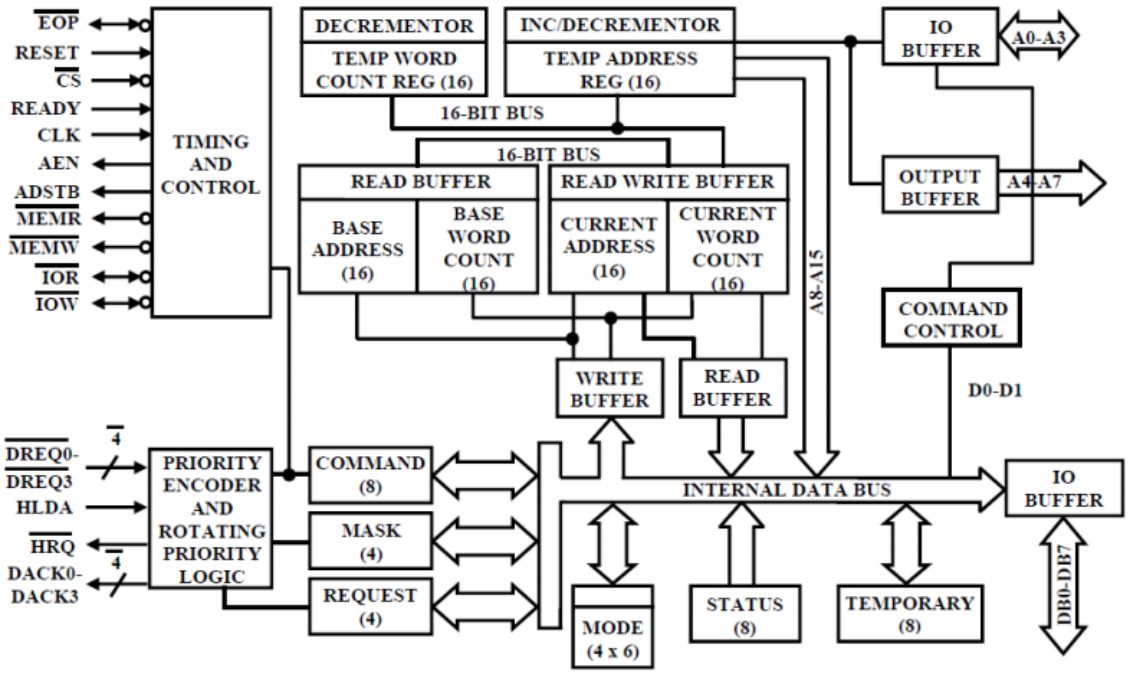
8237 DMA Controller:

- The 8237A Multimode Direct Memory Access (DMA) Controller is a peripheral interface circuit for microprocessor systems.
- It is designed to improve system performance by allowing external devices to directly transfer information from the system memory.

Features of 8237 DMA Controller:

- Enable/Disable Control of Individual DMA Requests
- Four Independent DMA Channels
- Independent Auto-initialization of all Channels
- Memory-to-Memory Transfers
- Memory Block Initialization
- Address Increment or Decrement
- Software DMA Requests
- High Performance Transfers up to 1.6M Bytes/Second with 5 MHz 8237A

Block diagram of 8237 DMA Controller:



- The 8237A contains three basic blocks of control logic along with internal registers:
    1. Timing Control Block
    2. Program Command Control Block
    3. Priority Encoder Block
- The Timing Control block generates internal timing and external control signals for the 8237A.
- The Program Command Control block decodes the various commands given to the 8237A by the microprocessor. It also decodes the Mode Control word used to select the type of DMA during the servicing.
- The Priority Encoder block resolves priority contention between DMA channels requesting service simultaneously. The 8237A has two types of priority encoding: Fixed Priority and Rotating Priority. Fixed Priority which fixes the channels in priority order based upon the descending value of their number. The second scheme is Rotating Priority. The last channel to get service becomes the lowest priority channel with the others rotating accordingly.

Register Organization of 8237:

S.No.	Register	Size
1	Base Address Registers	16
2	Base Word Count Registers	16
3	Current Address Registers	16
4	Current Word Count Registers	16
5	Temporary Address Register	16
6	Temporary Word Count Register	16
7	Status Register	8
8	Command Register	8
9	Temporary Register	8
10	Mode Registers	6
11	Mask Register	4
12	Request Register	4

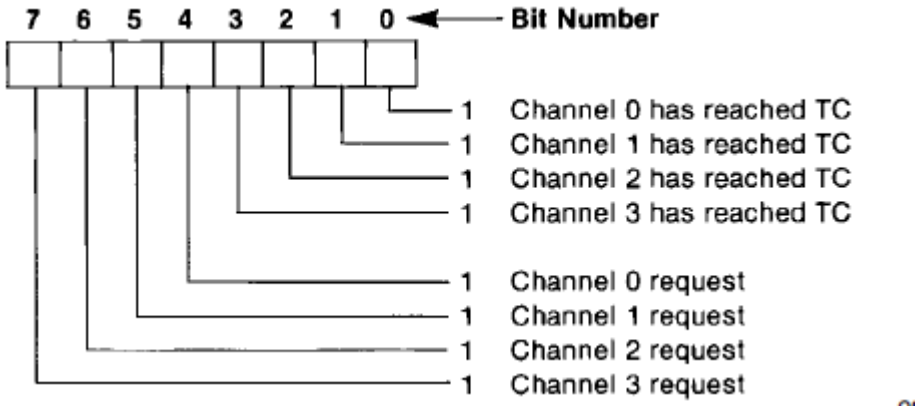
Base Address Registers and Base Word Count Registers: Each channel has a pair of Base Address and Base Word Count registers. These 16-bit registers store the original value of their associated current registers. During Auto-

initialize these values are used to restore the current registers to their original values.

Current Address Registers: This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the intermediate values of the address are stored in the Current Address register during the transfer.

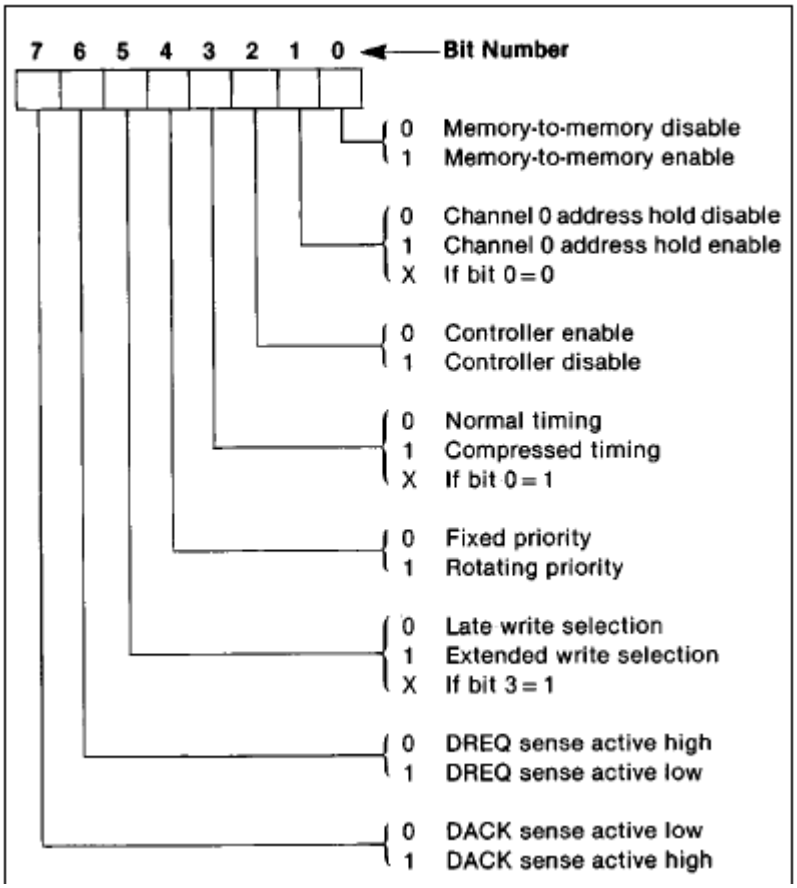
Current Word Count Registers: This register determines the number of transfers to be performed. The actual number of transfers will be one more than the number programmed in the Current Word Count register (i.e., programming a count of 100 will result in 101 transfers). The word count is decremented after each transfer.

Status Register: It contains information about the status of the devices at this point. This information includes which channels have reached a terminal count and which channels have pending DMA requests.



Command Register: This 8-bit register controls the operation of the 8237A. It is programmed by the microprocessor in the Program Condition and is cleared by Reset or a Master Clear instruction.

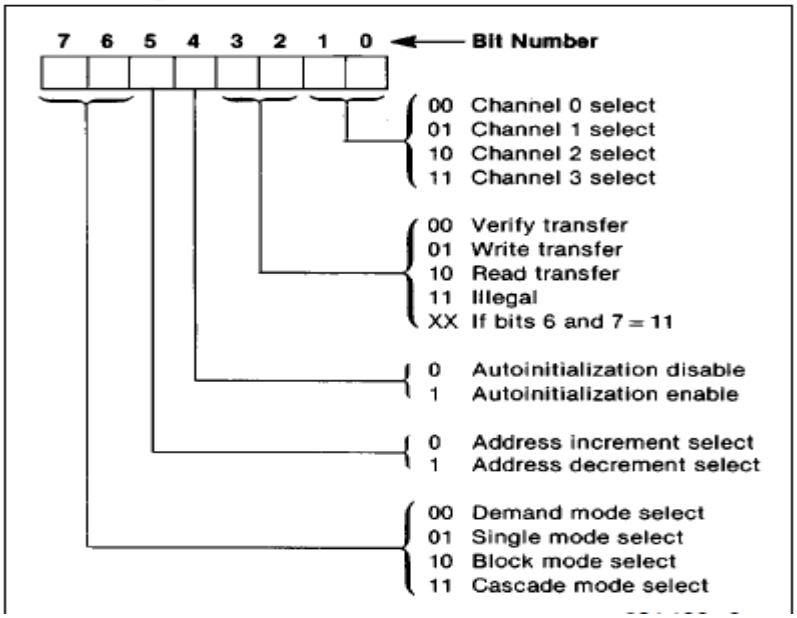
Command Register



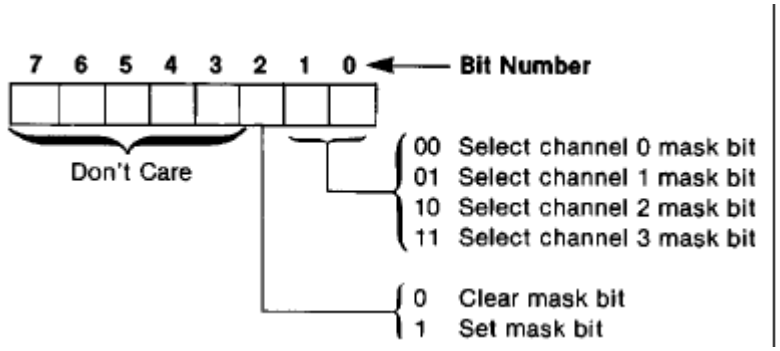
Temporary Register: The Temporary register is used **to hold data during memory-to-memory transfers**. Following the completion of the transfers, the **last word** moved can be read by the microprocessor in the Program Condition. The Temporary register always contains the last byte transferred in the previous memory-to-memory operation, unless cleared by a Reset.

Mode Registers: Each channel has a 6-bit Mode register associated with it. When the register is being written to by the microprocessor in the Program Condition, bits 0 and 1 determine which channel Mode register is to be written.

Mode Register

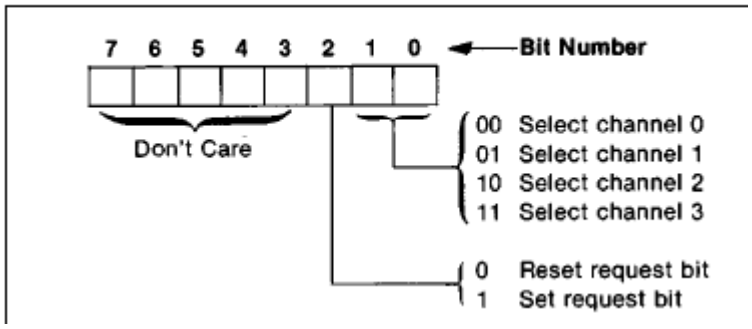


Mask Register: Each channel has associated with it a mask bit which can be set to disable the incoming DREQ (DMA Request). Each mask bit is set when its associated channel produces an EOP (End of Process) if the channel is not programmed for auto-initialize.



Request Register: The 8237A can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with it in the 4-bit Request register.

Request Register



Pin Diagram of 8237:

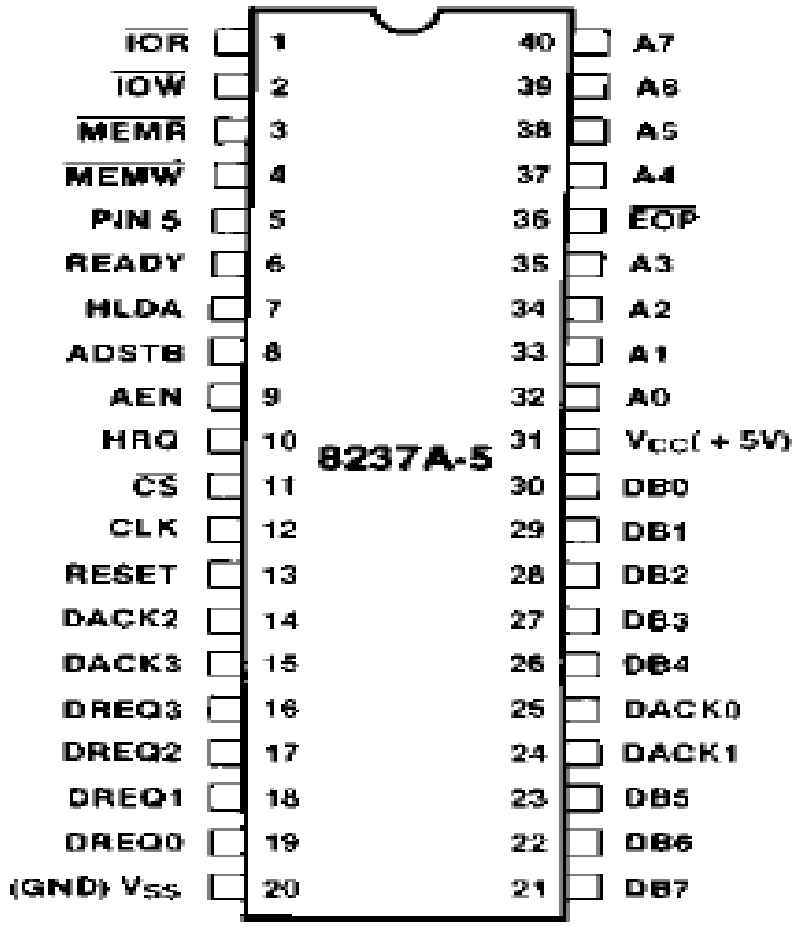


Table 1. Pin Description

Symbol	Type	Name and Function
V_{CC}		**POWER:** +5V supply.
V_{SS}		**GROUND:** Ground.
CLK	I	**CLOCK INPUT:** Clock Input controls the internal operations of the 8237A and its rate of data transfers. The input may be driven at up to 5 MHz for the 8237A-5.
$\overline{CS}$	I	**CHIP SELECT:** Chip Select is an active low input used to select the 8237A as an I/O device during the Idle cycle. This allows CPU communication on the data bus.
RESET	I	**RESET:** Reset is an active high input which clears the Command, Status, Request and Temporary registers. It also clears the first/last flip/flop and sets the Mask register. Following a Reset the device is in the Idle cycle.
READY	I	**READY:** Ready is an input used to extend the memory read and write pulses from the 8237A to accommodate slow memories or I/O peripheral devices. Ready must not make transitions during its specified setup/hold time.
HLDA	I	**HOLD ACKNOWLEDGE:** The active high Hold Acknowledge from the CPU indicates that it has relinquished control of the system busses.
DREQ0–DREQ3	I	**DMA REQUEST:** The DMA Request lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. In fixed Priority, DREQ0 has the highest priority and DREQ3 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of DREQ signal. Polarity of DREQ is programmable. Reset initializes these lines to active high. DREQ must be maintained until the corresponding DACK goes active.
DB0–DB7	I/O	**DATA BUS:** The Data Bus lines are bidirectional three-state signals connected to the system data bus. The outputs are enabled in the Program condition during the I/O Read to output the contents of an Address register, a Status register, the Temporary register or a Word Count register to the CPU. The outputs are disabled and the inputs are read during an I/O Write cycle when the CPU is programming the 8237A control registers. During DMA cycles the most significant 8 bits of the address are output onto the data bus to be strobed into an external latch by ADSTB. In memory-to-memory operations, data from the memory comes into the 8237A on the data bus during the read-from-memory transfer. In the write-to-memory transfer, the data bus outputs place the data into the new memory location.
$\overline{IOR}$	I/O	**I/O READ:** I/O Read is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to read the control registers. In the Active cycle, it is an output control signal used by the 8237A to access data from a peripheral during a DMA Write transfer.
$\overline{IOW}$	I/O	**I/O WRITE:** I/O Write is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to load information into the 8237A. In the Active cycle, it is an output control signal used by the 8237A to load data to the peripheral during a DMA Read transfer.

Table 1. Pin Description (Continued)

Symbol	Type	Name and Function
$\overline{EOP}$	I/O	**END OF PROCESS:** End of Process is an active low bidirectional signal. Information concerning the completion of DMA services is available at the bidirectional $\overline{EOP}$ pin. The 8237A allows an external signal to terminate an active DMA service. This is accomplished by pulling the $\overline{EOP}$ input low with an external $\overline{EOP}$ signal. The 8237A also generates a pulse when the terminal count (TC) for any channel is reached. This generates an $\overline{EOP}$ signal which is output through the $\overline{EOP}$ line. The reception of $\overline{EOP}$, either internal or external, will cause the 8237A to terminate the service, reset the request, and, if Autoinitialize is enabled, to write the base registers to the current registers of that channel. The mask bit and TC bit in the status word will be set for the currently active channel by $\overline{EOP}$ unless the channel is programmed for Autoinitialize. In that case, the mask bit remains unchanged. During memory-to-memory transfers, $\overline{EOP}$ will be output when the TC for channel 1 occurs. $\overline{EOP}$ should be tied high with a pull-up resistor if it is not used to prevent erroneous end of process inputs.
A0–A3	I/O	**ADDRESS:** The four least significant address lines are bidirectional three-state signals. In the Idle cycle they are inputs and are used by the CPU to address the register to be loaded or read. In the Active cycle they are outputs and provide the lower 4 bits of the output address.
A4–A7	O	**ADDRESS:** The four most significant address lines are three-state outputs and provide 4 bits of address. These lines are enabled only during the DMA service.
HRQ	O	**HOLD REQUEST:** This is the Hold Request to the CPU and is used to request control of the system bus. If the corresponding mask bit is clear, the presence of any valid DREQ causes 8237A to issue the HRQ.
DACK0–DACK3	O	**DMA ACKNOWLEDGE:** DMA Acknowledge is used to notify the individual peripherals when one has been granted a DMA cycle. The sense of these lines is programmable. Reset initializes them to active low.
AEN	O	**ADDRESS ENABLE:** Address Enable enables the 8-bit latch containing the upper 8 address bits onto the system address bus. AEN can also be used to disable other system bus drivers during DMA transfers. AEN is active HIGH.
ADSTB	O	**ADDRESS STROBE:** The active high, Address Strobe is used to strobe the upper address byte into an external latch.
$\overline{MEMR}$	O	**MEMORY READ:** The Memory Read signal is an active low three-state output used to access data from the selected memory location during a DMA Read or a memory-to-memory transfer.
$\overline{MEMW}$	O	**MEMORY WRITE:** The Memory Write is an active low three-state output used to write data to the selected memory location during a DMA Write or a memory-to-memory transfer.
PIN5	I	**PIN5:** This pin should always be at a logic HIGH level. An internal pull-up resistor will establish a logic high when the pin is left floating. It is recommended however, that PIN5 be connected to V_{CC}.

Modes of Operation in 8237 A:

The 8237A is designed to operate in two major cycles. These are called Idle and Active cycles.

Idle cycle:

The idle cycle is when no channel is requesting service, the 8237A will enter the Idle cycle and perform ‘‘SI (Inactive state)’’ states.

Active Cycle:

When the 8237A is in the idle cycle and a non-masked channel requests a DMA service, the device will output an HRQ (Hold Request) to the microprocessor and enter the Active cycle. It is in this cycle that the DMA service will take place, in one of four modes:

- Single Transfer Mode
- Block Transfer Mode
- Demand Transfer mode
- Cascade Mode

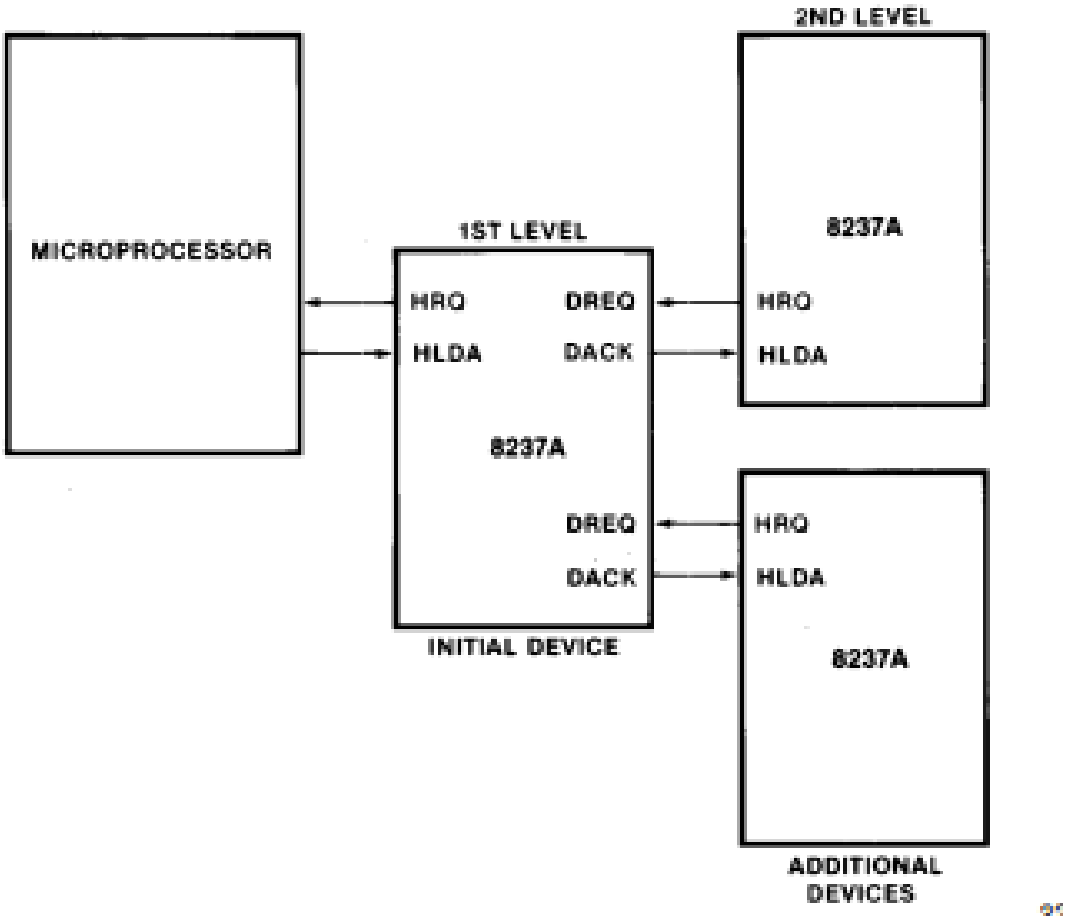
Single Transfer Mode: In Single Transfer mode, the device is programmed to make one transfer only. The word count will be decremented. DREQ must be held active until DACK becomes active in order to be recognized. If DREQ is held active throughout the single transfer, HRQ will go inactive and release the bus to the system. It will again go active and, upon receipt of a new HLDA, another single transfer will be performed.

Block Transfer Mode: In Block Transfer mode, the device is activated by DREQ to continue making transfers during the service until a TC (Terminal count), caused by word count going to FFFFH, or an external End of Process (EOP) is encountered. DREQ need only be held active until DACK becomes active. Again, an auto-initialization will occur at the end of the service if the channel has been programmed for it.

In Demand Transfer mode, the device is programmed to continue making transfers until a TC or external EOP is encountered or until DREQ goes inactive. Thus transfers may continue until the I/O device has exhausted its data capacity. After the I/O device has had a chance to catch up, the DMA service is re-established by means of a DREQ.

Cascade Mode: This mode is used to cascade more than one 8237A together for simple system expansion. The HRQ and HLDA signals from the additional 8237A are connected to the DREQ and DACK signals of a channel of the initial 8237A. This allows the DMA requests of the additional device to propagate through the priority network circuitry of the preceding device.

Cascading of 8237:



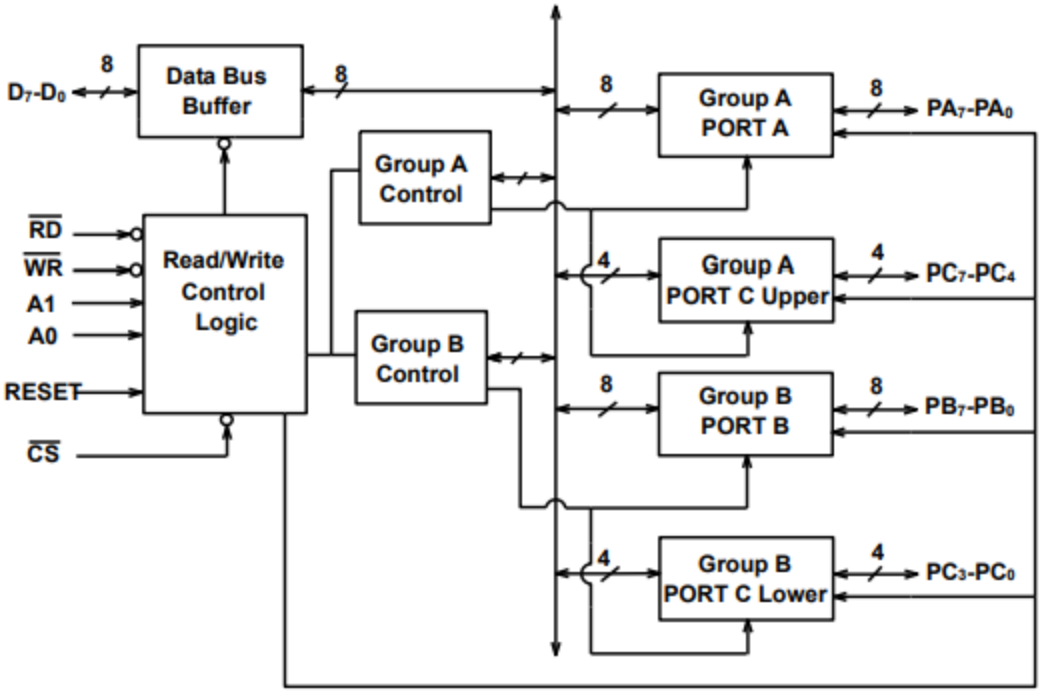
8255

PROGRAMMABLE PERIPHERAL INTERFACE

8255 programmable peripheral interface:

- The Intel 8255A is a general-purpose programmable, parallel I/O device designed for use with Intel Microprocessor.
- It can be programmed to transfer data under various conditions from simple I/O to Interrupt I/O.
- The 8255A has 24 I/O PINS that can be grouped primarily in two 8 Bit parallel ports A & B, with the remaining 8 bits as port C. The 8 bits of port C can be used as individual bits or be grouped in two 4bit ports. C upper and C lower. The functions of these ports are defined by writing a control word in the control register.

Block Diagram of 8255:



CONTROL LOGIC: The control section has six lines.

RD' (Read): This control signal enables the Read operation. When the signal is low, the CPU reads data from a selected I/O port of the 8255A.

WR' (Write): This control signal enables the write operation. When the signal goes low, the CPU writes into a selected I/O port or the control register.

RESET (Reset): This is an active high signal; it clears the control register and sets all ports in the input mode.

CS', A0 and A1: These are **device select signals**. CS' is connected to a decoded address and A0 & A1 are generally connected to CPU address lines A0 & A1 respectively. The various operation and port selection is given in the following table.

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Input –Output operation
0	0	0	1	0	PORT A ⟶ Data bus
0	1	0	1	0	PORT B ⟶ Data bus
1	0	0	1	0	PORT C ⟶ Data bus
0	0	1	0	0	Data bus ⟶ PORT A
0	1	1	0	0	Data bus ⟶ PORT B
1	0	1	0	0	Data bus ⟶ PORT C
1	1	1	0	0	Data bus ⟶ CWR

Functional Description:

This support chip is a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. It is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

To communicate with peripherals through the 8255A, three steps are necessary.

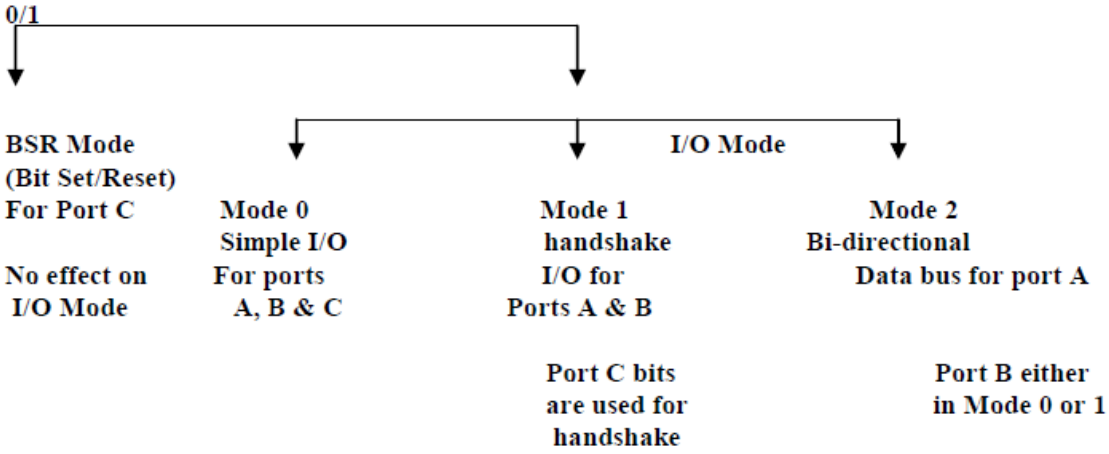
- Determine the addresses of ports A, B, and C and of the control register according to the Chip Select logic and address lines A0 and A1.
- Write a control word in the control register.
- Write I/O instructions to communicate with peripherals through ports A, B, and C.

Modes of Operation

All the functions of 8255A, classified according to two modes: the Bit Set/Reset (BSR) mode and the I/O mode. The I/O mode is further divided into three modes: Mode 0, Mode 1, and Mode 2.

- The BSR Mode is used to set or reset the bits in port C.

- In Mode 0 all ports functions as simple I/O ports.
- Mode 1 is a Handshake mode where by ports A&B uses bits from port C as Handshake signals. In the handshake mode, two types of I/O data transfer can be implemented: status checks and interrupt.
- In Mode 2, port A can be set up for bi-directional data transfer using handshake signals from port C.



In mode 0, all ports function as simple I/O ports for each of the three ports. In the first mode, mode-0, each group may be programmed in either input mode or output mode (PORT A, PORT B, PORT C lower, PORT C upper). In mode 0, the ports do not have handshaking and interrupt capability.

In mode-1, the second mode, only port A and B can be programmed either as input or output port. In this mode, handshake signals are exchanged between processor and peripherals prior to the data transfer. PORT C lines are used for handshaking and interrupt control signals.

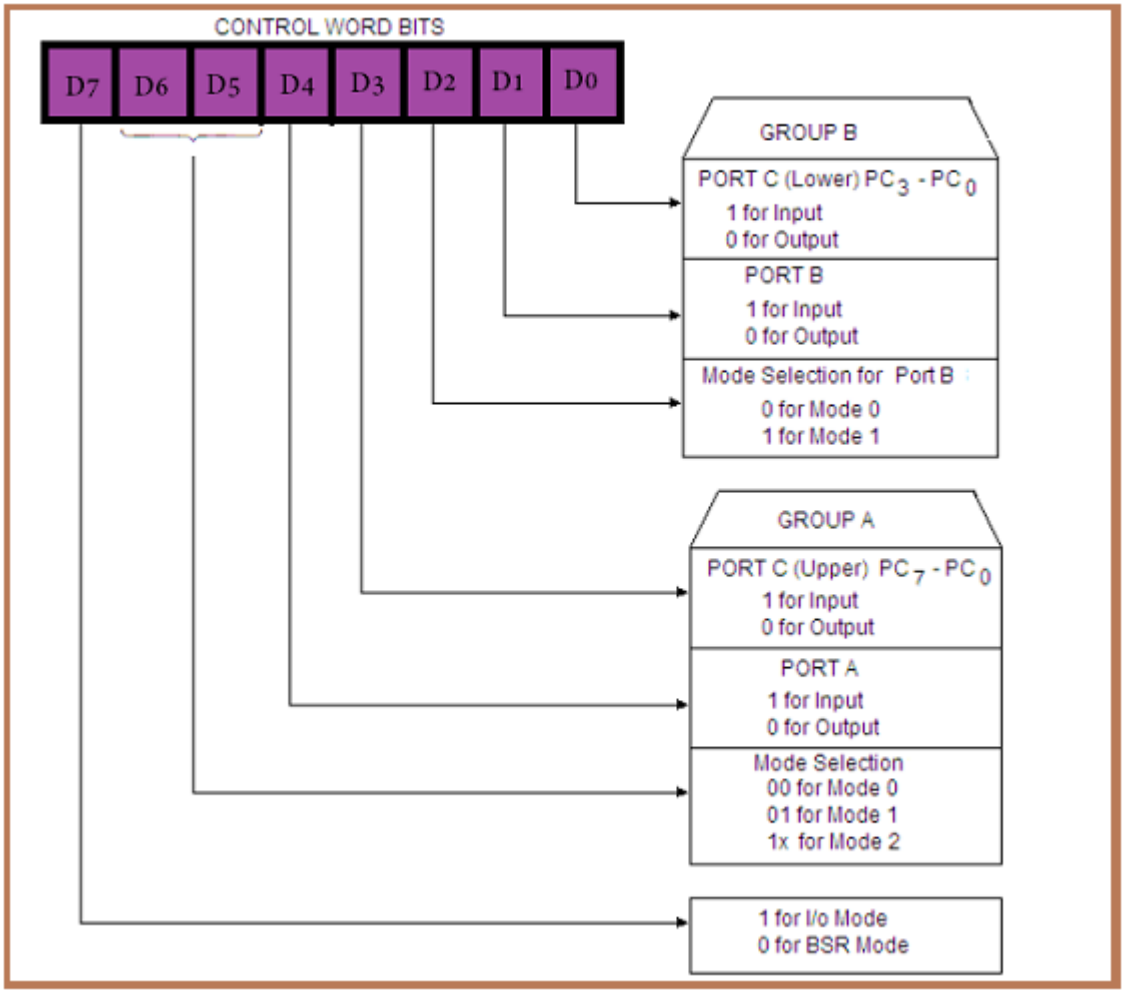
In mode 2, port A is a bidirectional port used as a bidirectional bus and five lines (PORT C upper 4 lines and borrowing one line from PORT C lower) for handshaking and control signals. Only port A can be programmed to work in mode 2. Interrupt generation and enable/disable functions are also available.

Control Word

A control register is an 8-bit register stores the Control word which specifies an I/O function for each port. This register can be accessed to write a control word when A0 and A1 are at logic 1. The register is not accessible for a Read operation.

Bit D7 of the control register specifies either the I/O function or the Bit Set/Reset function.

If bit D7=1, bits D6-D0 determine I/O functions in various modes. If bit D7=0, port C operates in the Bit Set/Reset (BSR) mode.

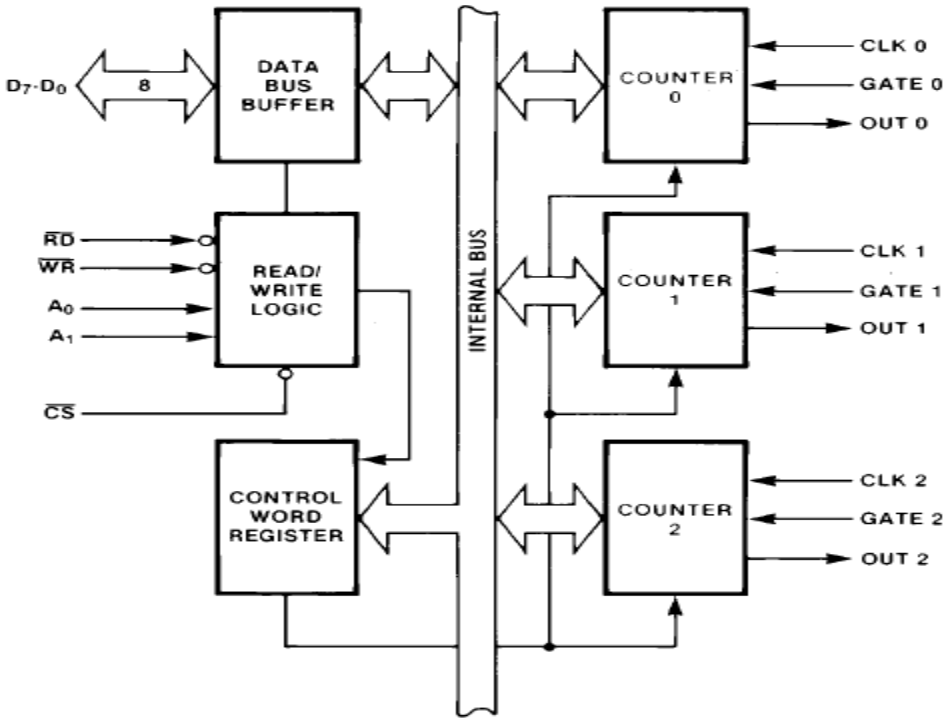


8254

PROGRAMMABLE TIMER/COUNTER

- The Intel 8254 is a counter/timer device designed to solve the common timing control problems in microcomputer system design.
- It provides **three** independent 16-bit counters.
- Handles Inputs from DC to 10 MHz
  - 8 MHz 8254
  - 10 MHz 8254-2
- Binary or BCD Counting
- Single +5V Supply
- It supports Six Programmable Counter Modes. All modes are software programmable.
- The 8254 is a superset of the 8253.

Bock diagram of timer counter and its pin diagram:



Timer Counter Pin Diagram:

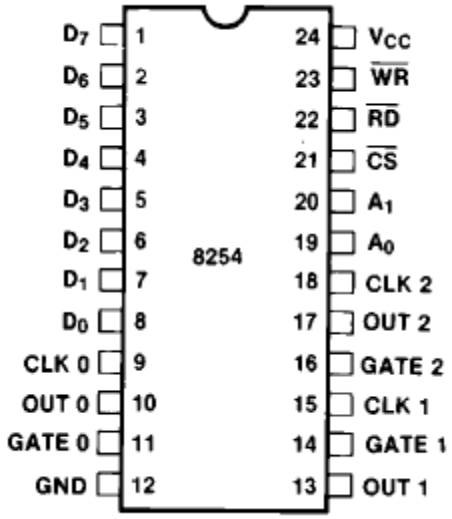


Table 1. Pin Description

Symbol	Pin No.	Type	Name and Function
D_7–D_0	1–8	I/O	**DATA:** Bi-directional three state data bus lines, connected to system data bus.
CLK 0	9	I	**CLOCK 0:** Clock input of Counter 0.
OUT 0	10	O	**OUTPUT 0:** Output of Counter 0.
GATE 0	11	I	**GATE 0:** Gate input of Counter 0.
GND	12		**GROUND:** Power supply connection.
V_{CC}	24		**POWER:** + 5V power supply connection.
$\overline{WR}$	23	I	**WRITE CONTROL:** This input is low during CPU write operations.
$\overline{RD}$	22	I	**READ CONTROL:** This input is low during CPU read operations.
$\overline{CS}$	21	I	**CHIP SELECT:** A low on this input enables the 8254 to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and $\overline{WR}$ are ignored otherwise.
A_1, A_0	20–19	I	**ADDRESS:** Used to select one of the three Counters or the Control Word Register for read or write operations. Normally connected to the system address bus.

A_1	A_0	Selects
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Word Register

CLK 2	18	I	**CLOCK 2:** Clock input of Counter 2.
OUT 2	17	O	**OUT 2:** Output of Counter 2.
GATE 2	16	I	**GATE 2:** Gate input of Counter 2.
CLK 1	15	I	**CLOCK 1:** Clock input of Counter 1.
GATE 1	14	I	**GATE 1:** Gate input of Counter 1.
OUT 1	13	O	**OUT 1:** Output of Counter 1.

Control Word Format

$A_1,A_0 = 11$ $\overline{CS} = 0$ $\overline{RD} = 1$ $\overline{WR} = 0$

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC—Select Counter

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (see Read Operations)

M—Mode

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

RW—Read/Write

RW1	RW0	
0	0	Counter Latch Command (see Read Operations)
0	1	Read/Write least significant byte only
1	0	Read/Write most significant byte only
1	1	Read/Write least significant byte first, then most significant byte

BCD

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

NOTE:
Don't care bits (X) should be 0 to insure compatibility with future Intel products.

Modes of Operation:

Each of the three counters of 8253/8254 can be programmed to operate in six different modes of operation to produce the desired output.

MODE 0: INTERRUPT ON TERMINAL COUNT

MODE 1: HARDWARE RETRIGGERABLE ONE-SHOT

MODE 2: RATE GENERATOR

MODE 3: SQUARE WAVE MODE

MODE 4: SOFTWARE TRIGGERED STROBE

MODE 5: HARDWARE TRIGGERED STROBE (RETRIGGERABLE)

Each timer requires a clock input.

- The counters are **negative edge triggered** down counter, i.e., whenever there is HIGH to LOW transition at the CLK input, the count value is decremented by 1.
- The down counting is controlled by the gate.

- The output pin of the timer may be used to generate different signals, e.g., an interrupt request signal in the interrupt related modes**.**

Mode-0: Interrupt on Terminal Count:

Mode 0 is typically used for event counting. In mode 0 operation, when a count value is loaded in a counter it starts decrementing the count value by one for each input clock pulse (provided the GATE is high) and asserts the output as high when the count is zero. This low to high transition of the counter output can be used as an interrupt to the processor to initiate an activity. In mode 0, the 8254 counts as long as GATE is high.

MODE 1: HARDWARE RETRIGGERABLE ONESHOT:

In mode 1, the counter functions as a retriggerable monostable multivibrator (one shot). In mode, the output OUT will be initially high. The GATE acts as a trigger pulse to start the count process. When a low to high transition of GATE signal occurs, the count value is loaded in the counter and the count is decremented by one for each clock pulse. When the count value is loaded in the OUTPUT goes low

And it becomes high when count value is zero. Therefore, the mode 1 produces the logic low pulse output whose width is equal to the duration of the count.

MODE 2: RATE GENERATOR or Timed interrupt generator:

This mode-2 is used to generate a periodic low pulse of width equal to **one clock period**. If a count value of N is loaded in the counter then the output will go low, **once in N clock periods**. OUT then goes high again, the Counter reloads the initial count and the process is repeated. Mode 2 is periodic; the same sequence is repeated indefinitely. For mode 2 operation, GATE should always be high.

MODE 3: SQUARE WAVE MODE: In mode 3, the counter generates a square wave at the output pin. The frequency of the square wave will be given by the frequency of the input clock signal divided by the count value loaded in the count register. If the count value N is even the output will be alternatively high for N/2 clock periods and low for N/2 clock periods. If the count value N is

an odd number then the output will be alternatively high for (N+1)/2 clock periods and low for (N-1)/2 clock periods (either when the count value is odd the output high period will be more than low periods by 1 clock period).

MODE 4: SOFTWARE TRIGGERED STROBE:

The mode-4 is used to generate a single logic low pulse after a delay. In this mode, when a count value N is loaded in the counter, a logic low pulse of width equal to one clock period is generated in the (N+1)th clock pulse. Here the delay time is N clock period. This signal is often used as strobe signal in parallel data transfer scheme. The mode-4 is called software triggered strobe because the counter starts its operation once the count value is written into count register by a software instruction. However the GATE input signal should remain high throughout the mode 4 operation.

MODE 5: HARDWARE TRIGGERED STROBE

(RETRIGGERABLE)

The mode-5 is same as that of mode 4 except that the counter is initiated by a low to high transition of GATE signal. In mode 4 the counter will start decrementing the count value immediately after the write operation of the count value by the processor. But in mode 5 the counter will wait for a low to high transition of GATE signal after the write operation of count value by the processor.

Difference between 8253 and 8254:

8253	**8254**
Its operating frequency is 0 - 2.6 MHz	Its operating frequency is 0 - 10 MHz
It uses N-MOS technology	It uses H-MOS technology
Read-Back command is not available	Read-Back command is available
Reads and writes of the same counter cannot be interleaved.	Reads and writes of the same counter can be interleaved.

8259

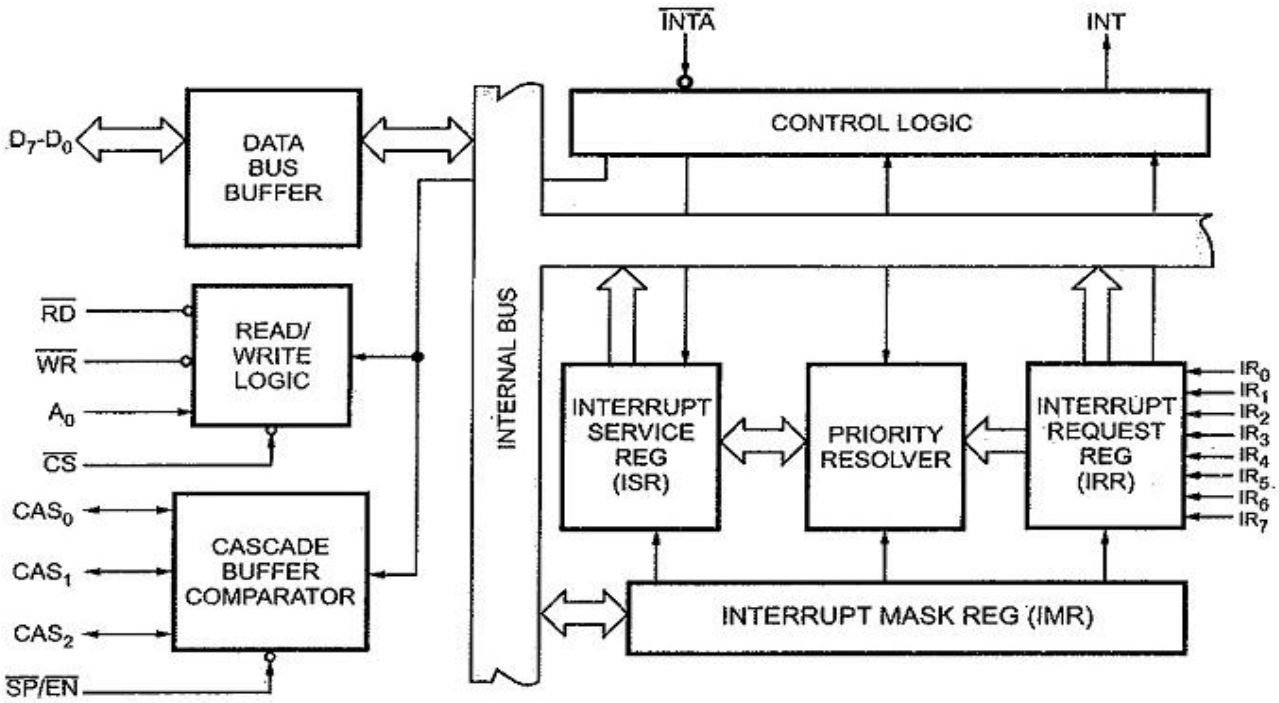
Programmable Interrupt Controller

8259 Interrupt Controller:

The Programmable Interrupt Controller (PIC) functions as an overall manager in an Interrupt-Driven system environment. It accepts requests from the peripheral equipment, determines which of the incoming requests is of the highest importance (priority), ascertains whether the incoming request has a higher priority value than the level currently being serviced, and issues an interrupt to the CPU based on this determination.

- The Intel 8259A Programmable Interrupt Controller handles up to eight vectored priority interrupts for the CPU.
- It is cascaded for up to 64 vectored priority interrupts without additional circuitry. It has 28 pins.
- It uses NMOS technology and requires a single +5V supply. Circuitry is static, requiring no clock input.

Block diagram of 8259 interrupt controller



Data Bus Buffer:

The data bus buffer allows the 8085 to send control words to the 8259A and read a status word from 8259 Programmable Interrupt Controller.

Read/Write Logic:

The RD and WR inputs control the data flow on the data bus when the device is selected by asserting its chip select (CS) input low.

Control Logic:

If the 8259A is properly enabled, the interrupt request will cause the 8259A to assert its INT output pin high. If this pin is connected to the INTR pin of an 8085 and if the 8085 Interrupt Enable (IE) flag is set, then this high signal will cause the 8085 to respond INTR.

Interrupt Request Register (IRR):

The IRR is used to store all the interrupt levels which are requesting the service.

Interrupt Service Register (ISR):

The Interrupt Service Register (ISR) stores all the levels that are currently being serviced.

Interrupt Mask Register (IMR):

Interrupt Mask Register (IMR) stores the masking bits of the interrupt lines to be masked. This register can be programmed by an Operation Command Word (OCW).

Priority Resolver:

The priority resolver determines the priorities of the bits set in the IRR. The bit corresponding to the highest priority interrupt input is set in the ISR during the INTA input.

Cascade Buffer Comparator:

This section generates control signals necessary for cascade operations. It also generates Buffer-Enable signals. 8259 Programmable Interrupt Controller can be cascaded with other 8259s in order to expand the interrupt handling capacity to sixty-four levels. In such a case, the former is called a master, and the latter are called slaves. The 8259 can be set up as a master or a slave by the SP/EN pin.

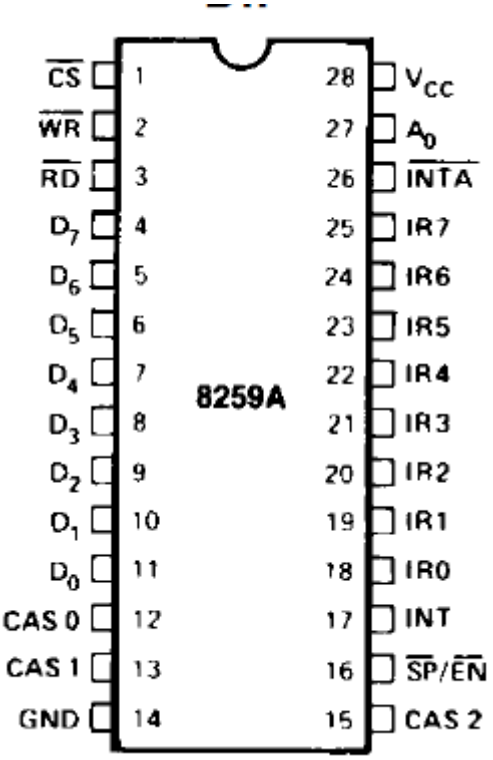
CAS0— CAS2

For a master 8259, the CAS0-CAS2 pins are output pins, and for slave 8259, these are input pins. When the 8259 is a master (that is, when it accepts interrupt requests from other 8259s), the CALL opcode is generated by the Master in response to the first INTA. The vector address must be released by the slave 8259.

SP / EN (Slave Program /Enable Buffer):

The SP/EN signal is tied high for the master. However it is grounded for the slave.

Pin Diagram of 8259:



Symbol	Pin No.	Type	Name and Function
V_{CC}	28	I	**SUPPLY:** +5V Supply.
GND	14	I	**GROUND**
$\overline{CS}$	1	I	**CHIP SELECT:** A low on this pin enables $\overline{RD}$ and $\overline{WR}$ communication between the CPU and the 8259A. INTA functions are independent of CS.
$\overline{WR}$	2	I	**WRITE:** A low on this pin when CS is low enables the 8259A to accept command words from the CPU.
$\overline{RD}$	3	I	**READ:** A low on this pin when CS is low enables the 8259A to release status onto the data bus for the CPU.
D_7–D_0	4–11	I/O	**BIDIRECTIONAL DATA BUS:** Control, status and interrupt-vector information is transferred via this bus.
CAS_0–CAS_2	12, 13, 15	I/O	**CASCADE LINES:** The CAS lines form a private 8259A bus to control a multiple 8259A structure. These pins are outputs for a master 8259A and inputs for a slave 8259A.
$\overline{SP}/\overline{EN}$	16	I/O	**SLAVE PROGRAM/ENABLE BUFFER:** This is a dual function pin. When in the Buffered Mode it can be used as an output to control buffer transceivers (EN). When not in the buffered mode it is used as an input to designate a master (SP = 1) or slave (SP = 0).
INT	17	O	**INTERRUPT:** This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin.
IR_0–IR_7	18–25	I	**INTERRUPT REQUESTS:** Asynchronous inputs. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged (Edge Triggered Mode), or just by a high level on an IR input (Level Triggered Mode).
$\overline{INTA}$	26	I	**INTERRUPT ACKNOWLEDGE:** This pin is used to enable 8259A interrupt-vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
A_0	27	I	**AO ADDRESS LINE:** This pin acts in conjunction with the $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ pins. It is used by the 8259A to decipher various Command Words the CPU writes and status the CPU wishes to read. It is typically connected to the CPU A0 address line (A1 for 8086, 8088).

INTERRUPT SEQUENCE

The normal sequence of events during an interrupt depends on the type of CPU being used:

1. One or more of the INTERRUPT REQUEST lines (IR7-0) are raised high, setting the corresponding IRR bit(s).
2. The 8259A evaluates these requests, and sends an INT to the CPU, if appropriate.
3. The CPU acknowledges the INT and responds with an INTA pulse.
4. Upon receiving an INTA from the CPU group, the highest priority ISR bit is set, and the corresponding IRR bit is reset. The 8259A will

also release a CALL instruction code (11001101) onto the 8-bit Data Bus through its D7-0 pins.

5. This CALL instruction will initiate two more INTA pulses to be sent to the 8259A from the CPU group.
6. These two INTA pulses allow the 8259A to release its pre-programmed subroutine address onto the Data Bus. The lower 8-bit address is released at the first INTA pulse and the higher 8-bit address is released at the second INTA pulse.
7. This completes the 3-byte CALL instruction released by the 8259A. In the AEOI mode the ISR bit is reset at the end of the third INTA pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt sequence.

The 8259A accepts two types of command words generated by the CPU:

1. Initialization Command Words (ICWs): Before normal operation can begin, each 8259A in the system must be brought to a starting point by a sequence of 2 to 4 bytes timed by WR pulses.

2. Operation Command Words (OCWs): These are the command words which command the 8259A to operate in various interrupt modes. These modes are:

a. Fully nested mode

b. Rotating priority mode

c. Special mask mode

d. Polled mode

The OCWs can be written into the 8259A anytime after initialization.

Modes of operation:

The various modes of operation of the Block Diagram of 8259 Programmable Interrupt Controller are:

- Fully Nested Mode,
- Special Fully Nested Mode (SFNM)
- Rotating Priority Mode,

- Special Masked Mode, and
- Polled Mode.

Fully Nested Mode:

After initialization, the 8259A operates in fully nested mode so it is called default mode. The 8259 continues to operate in the Fully Nested Mode until the mode is changed through Operation Command Words.

Special Fully Nested Mode (SFNM):

In the FNM, on the acknowledgement of an interrupt, further interrupts from the same level are disabled. In Special Fully Nested Mode, when an interrupt request from a slave is being serviced, the slave is allowed to place further requests if these requests are of a higher priority than the request currently being serviced

Rotating Priority Mode:

The Rotating Priority mode can be set in automatic rotation and specific rotation. In automatic rotation mode, a device, after being serviced, receives the lowest priority. In the specific rotation mode, the lowest priority can be assigned to any interrupt input (IR0 to IR7)

Special Masked Mode:

In the special mask mode it inhibits further interrupts at that level and enables interrupts from all other levels (lower as well as higher) that are not masked. Thus any interrupt may be selectively enabled by loading the mask register.

Polled Mode:

The microprocessor checks the status of interrupt requests by issuing poll command. The microprocessor reads contents of 8259A after issuing poll command.

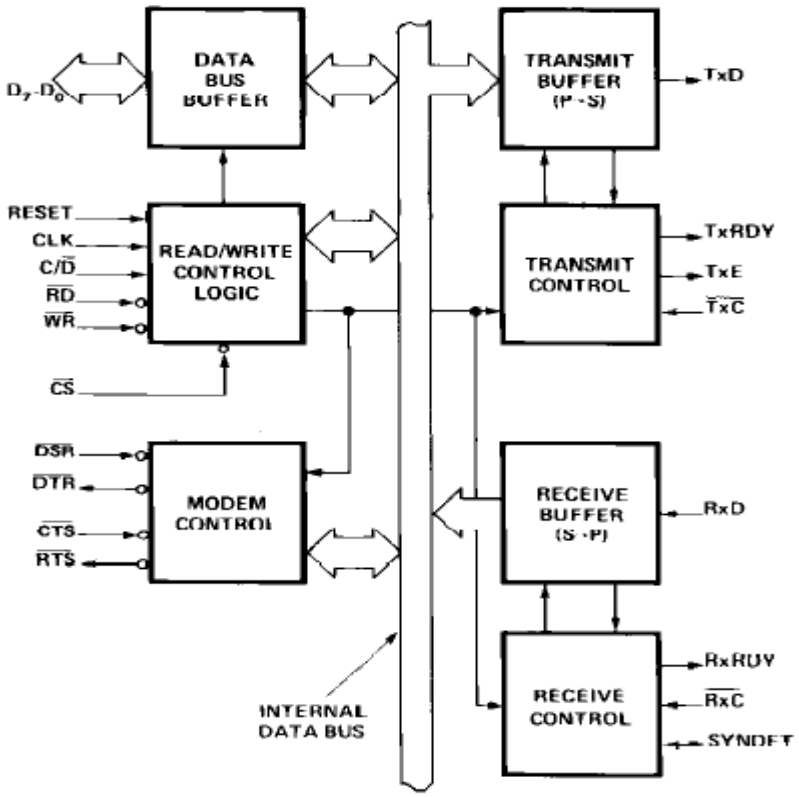
8251

Universal Synchronous/ Asynchronous Receiver/ Transmitter (USART)

USART:

- It is designed for data communications with Intel's microprocessors.
- It is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique.
- The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU.
- It is made with HMOS technology.

Block Diagram of 8251 USART:



The functional block diagram of 825 1A consists five following sections:

• Read/Write control logic

• Transmitter

• Receiver

• Data bus buffer

• Modem control

The Read/Write Control logic determines the functions of the 8251A according to the control word written into its control register. This section has three registers: control register, status register and data buffer.

- When C/D (bar) is high, the control register is selected for writing control word or reading status word.
- When C/D (bar) is low, the data buffer is selected for read/write operation.
- When the reset is high, it forces 8251A into the idle mode.
- The clock input is necessary for 8251A for communication with CPU

Transmitter

The transmitter section accepts parallel data from CPU and converts them into serial data. The transmitter section is double buffered, i.e., it has a buffer register to hold an 8-bit parallel data and another register called output register to convert the parallel data into serial bits.

- If buffer register is empty, then TxRDY is goes to high.
- If output register is empty then TxEMPTY goes to high.
- The clock signal, TxC (low) controls the rate at which the bits are transmitted by the USART.

Receiver

• The CPU reads the parallel data from the buffer register.

• When the input register loads a parallel data to buffer register, the RxRDY line goes high.

• The clock signal RxC (low) controls the rate at which bits are received by the USART.

• During asynchronous mode, the signal SYNDET/BRKDET will indicate the break in the data transmission.

• During synchronous mode, the signal SYNDET/BRKDET will indicate the reception of synchronous character.

Modem control

• The MODEM control unit allows to interface a MODEM to 8251A and to establish data communication through MODEM over telephone lines.

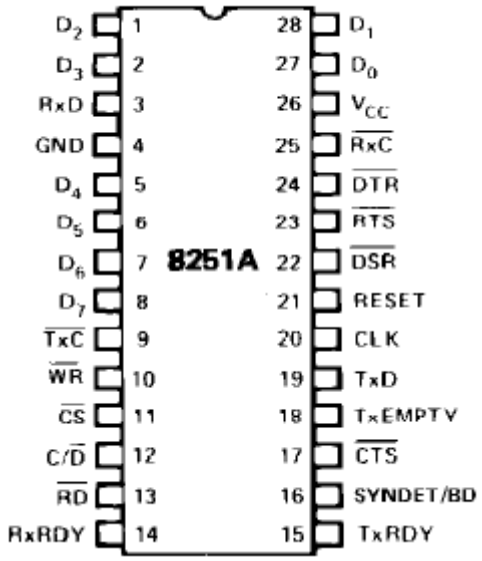
• This unit takes care of handshake signals for MODEM interface.

• The 825 1A can be either memory mapped or I/O mapped in the system.

• The data lines D0 - D7 are connected to D0 - D7 of the processor to achieve parallel data transfer.

• The RESET and clock signals are supplied by the processor. Here the processor clock is directly connected to 8251A. This clock controls the parallel data transfer between the processor and 8251A.

Pin Diagram of 8251 USART:



Pin	Description
D_0-D_7	Parallel data
$C/\overline{D}$	Control register or Data buffer select
$\overline{RD}$	Read control
$\overline{WR}$	Write control
$\overline{CS}$	Chip Select
CLK	Clock pulse (TTL)
RESET	Reset
$\overline{TxC}$	Transmitter Clock
TxD	Transmitter Data
$\overline{RxC}$	Receiver Clock
RxD	Receiver Data
RxRDY	Receiver Ready
TxRDY	Transmitter Ready
$\overline{DSR}$	Data Set Ready
$\overline{DTR}$	Data Terminal Ready
SYNDET/ BRKDET	Synchronous Detect / Break Detect
$\overline{RTS}$	Request To Send Data
$\overline{CTS}$	Clear To Send Data
TxEMPTY	Transmitter Empty
V_{CC}	Supply (+5V)
GND	Ground (0 V)

RS232C

RS-232C (Recommended standard-232C), a standard interface approved by the Electronic Industries Alliance (EIA) for connecting serial devices.

RS-232C is a long-established standard ("C" is the current version) that describes the physical interface and protocol for relatively low-speed serial data communication between computers and related devices. It was defined by an industry trade group, the Electronic Industries Association (EIA), originally for teletypewriter devices.

RS-232C is the interface that your computer uses to talk to and exchange data with your modem and other serial devices. Somewhere in your PC, typically on a Universal Asynchronous Receiver/Transmitter (UART) chip on your motherboard, the data from your computer is transmitted to an internal or external modem (or other serial device) from its Data Terminal Equipment (DTE) interface. Since data in your computer flows along parallel circuits and serial devices can handle only one bit at a time, the UART chip converts the groups of bits in parallel to a serial stream of bits. As your PC's DTE agent, it also communicates with the modem or other serial device, which, in accordance with the RS-232C standard, has a complementary interface called the Data Communications Equipment (DCE) interface.

In 1987, the EIA released a new version of the standard and changed the name to EIA-232-D. And in 1991, the EIA teamed up with Telecommunications Industry association (TIA) and issued a new version of the standard called EIA/TIA-232-E. Many people, however, still refer to the standard as RS-232C, or just RS-232.

Almost all modems conform to the EIA-232 standard and most personal computers have an EIA-232 port for connecting a modem or other device. In addition to modems, many display screens, mice, and serial printers are designed to connect to an EIA-232 port. In EIA-232 parlance, the device that connects to the interface is called a Data Communications Equipment (DCE)

and the device to which it connects (e.g., the computer) is called a Data Terminal Equipment (DTE).

The EIA-232 standard supports two types of connectors -- a 25-pin D-type connector (DB-25) and a 9-pin D-type connector (DB-9). The type of serial communications used by PCs requires only 9 pins so either type of connector will work equally well.