

Appendix

Schematics

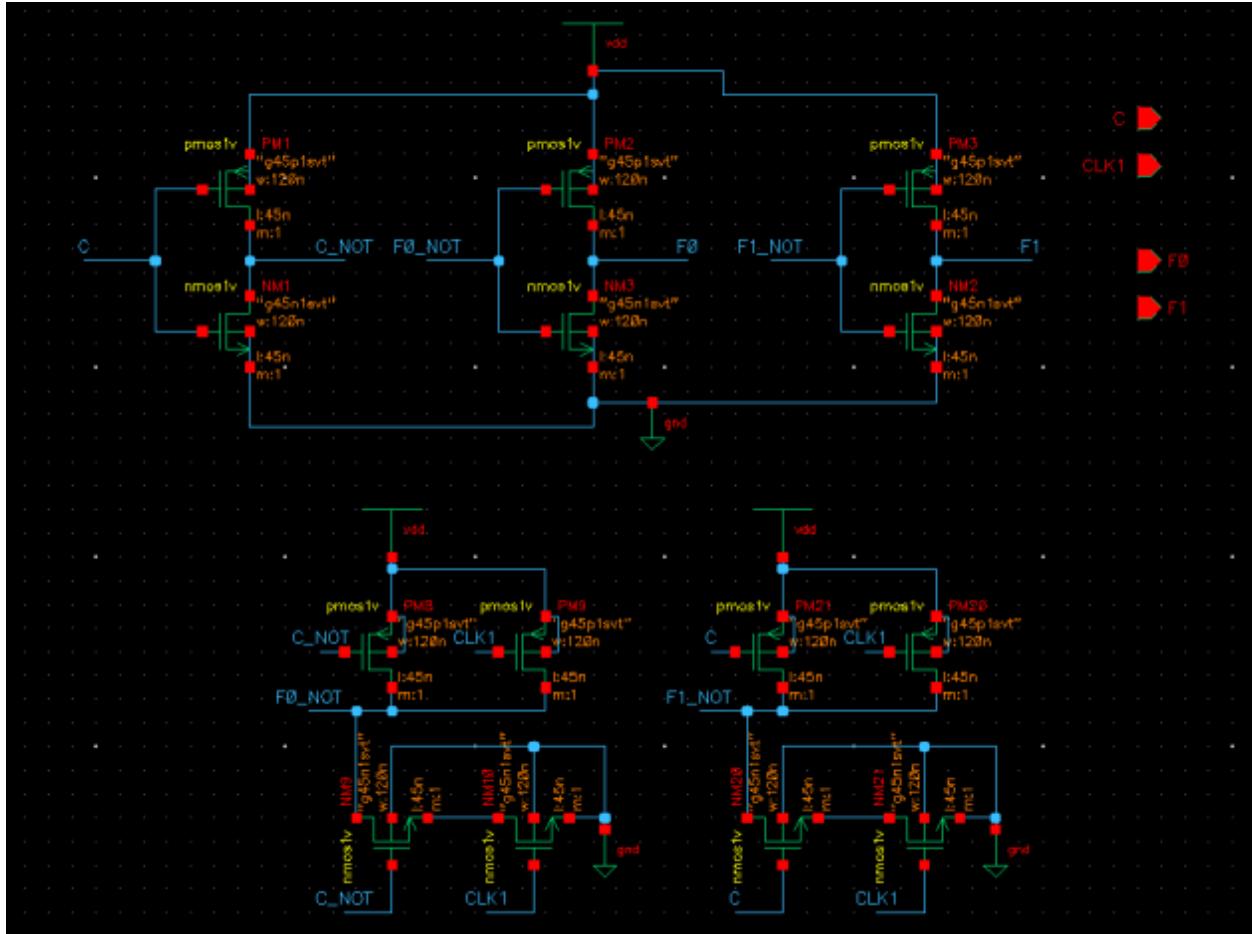


Fig. 11. Column Decoder schematic

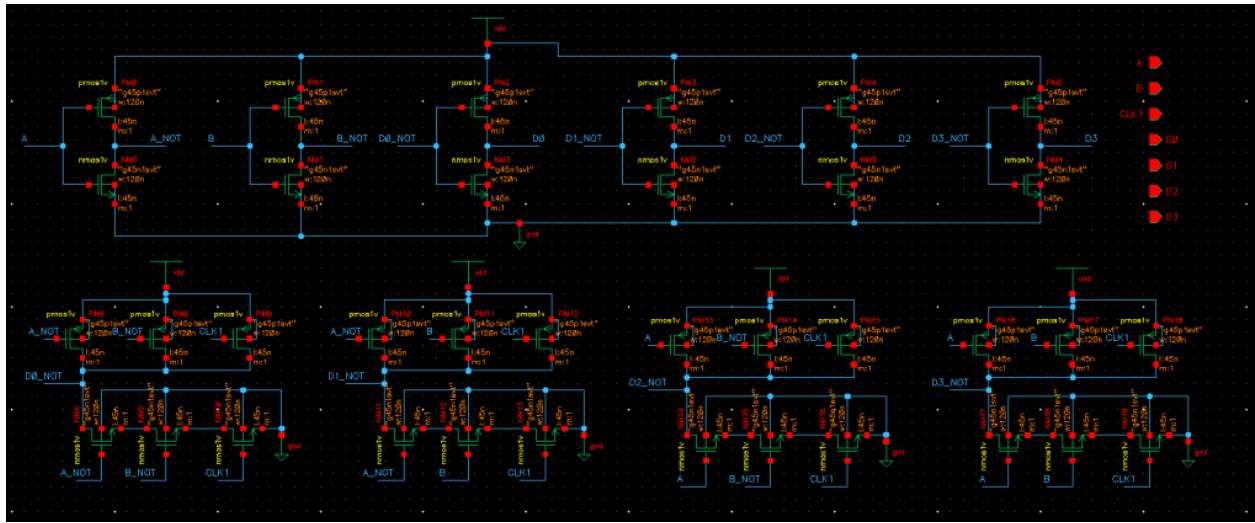


Fig. 12. Row Decoder schematic

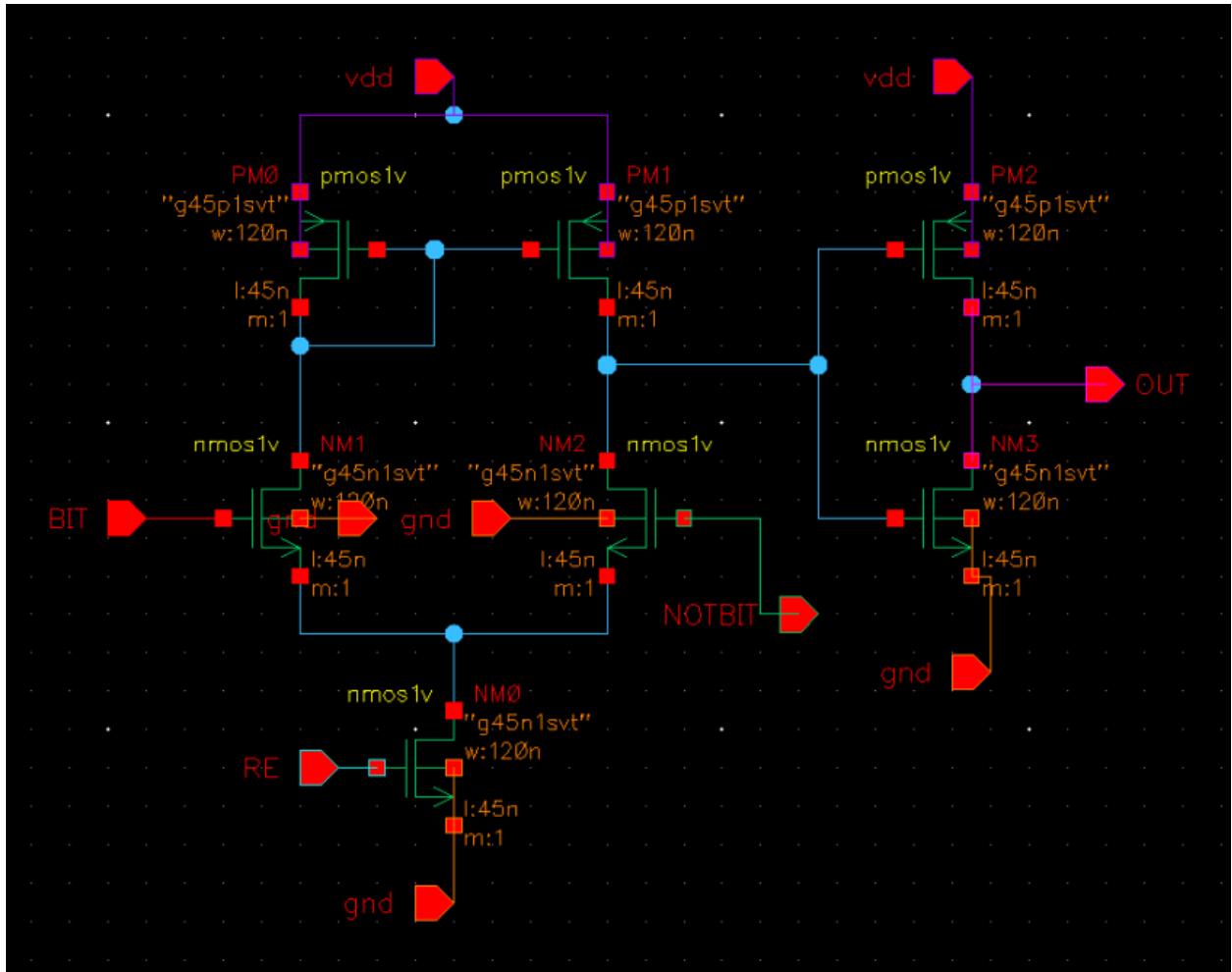


Fig. 13. Sense Amplifier with differential amplifier and inverting buffer

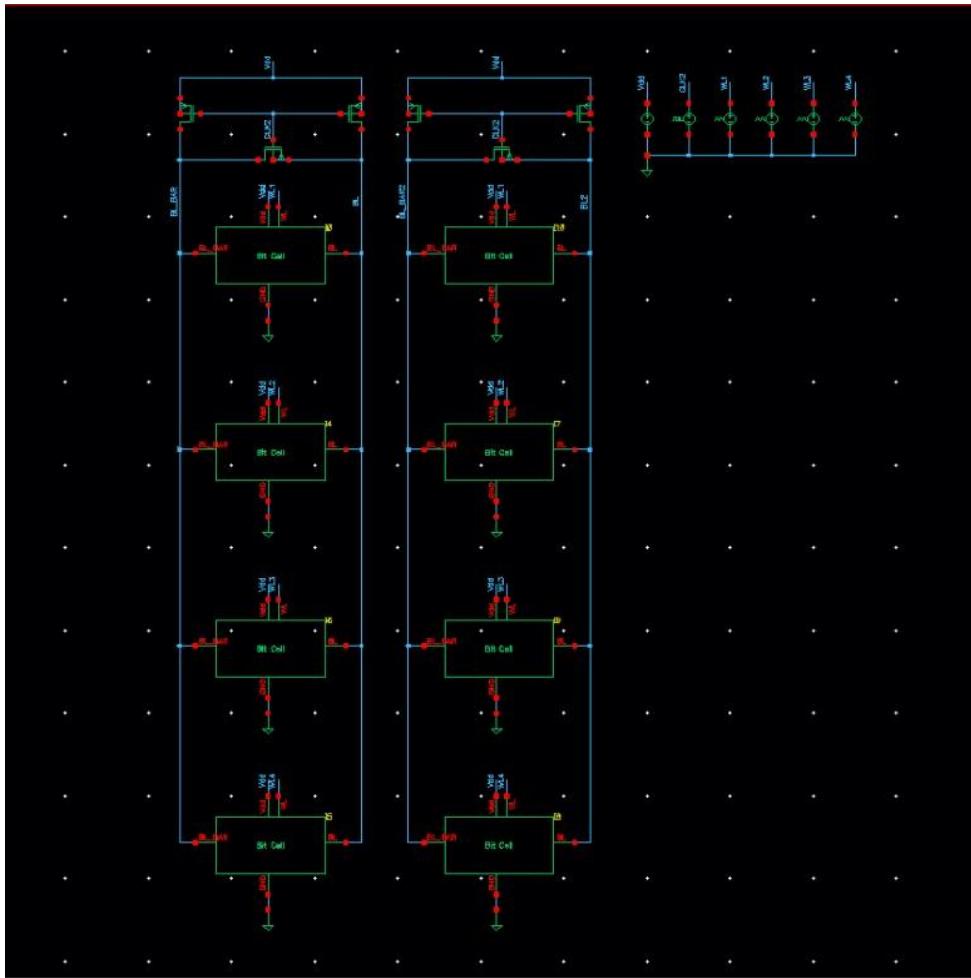


Fig. 14. Entire SRAM Array schematic

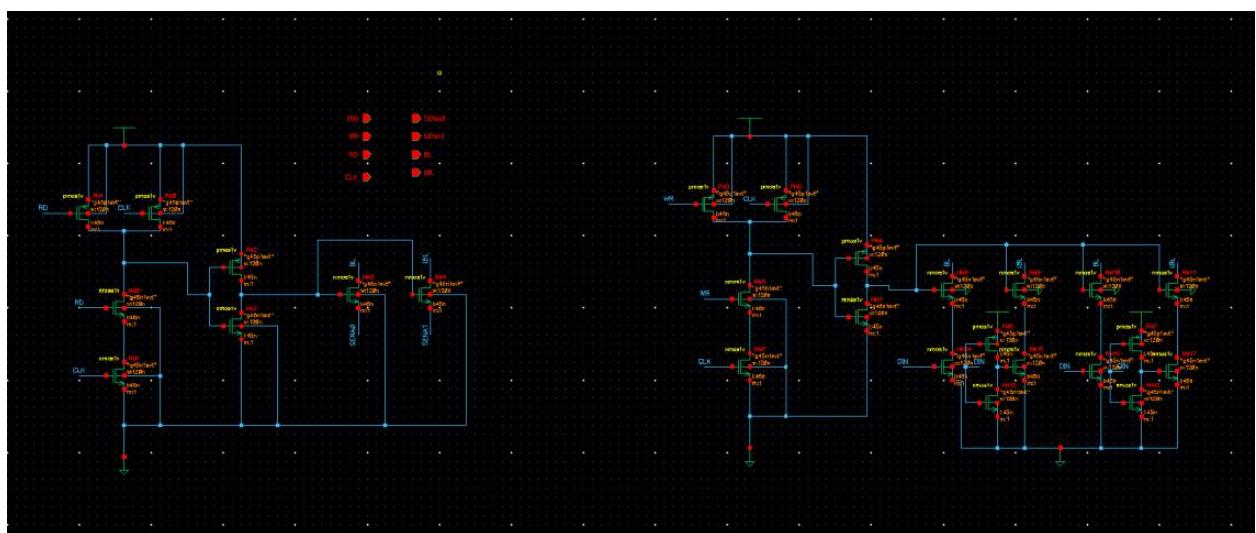


Fig. 15. Read/Write control schematic

Layout

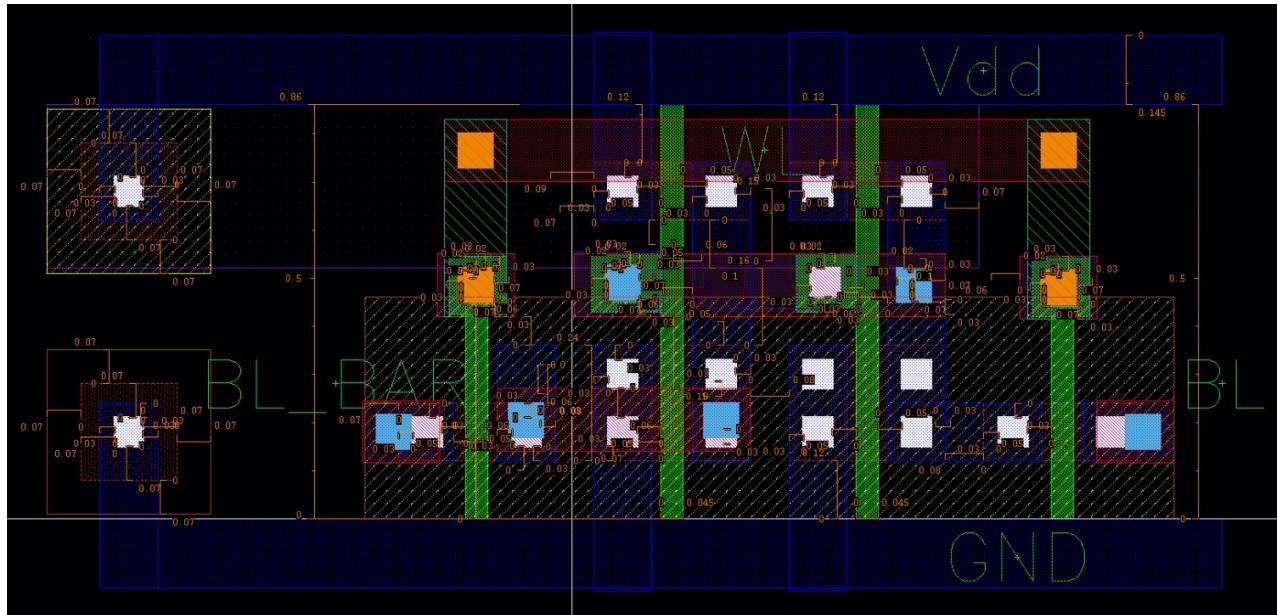


Fig. 16. Single SRAM cell layout

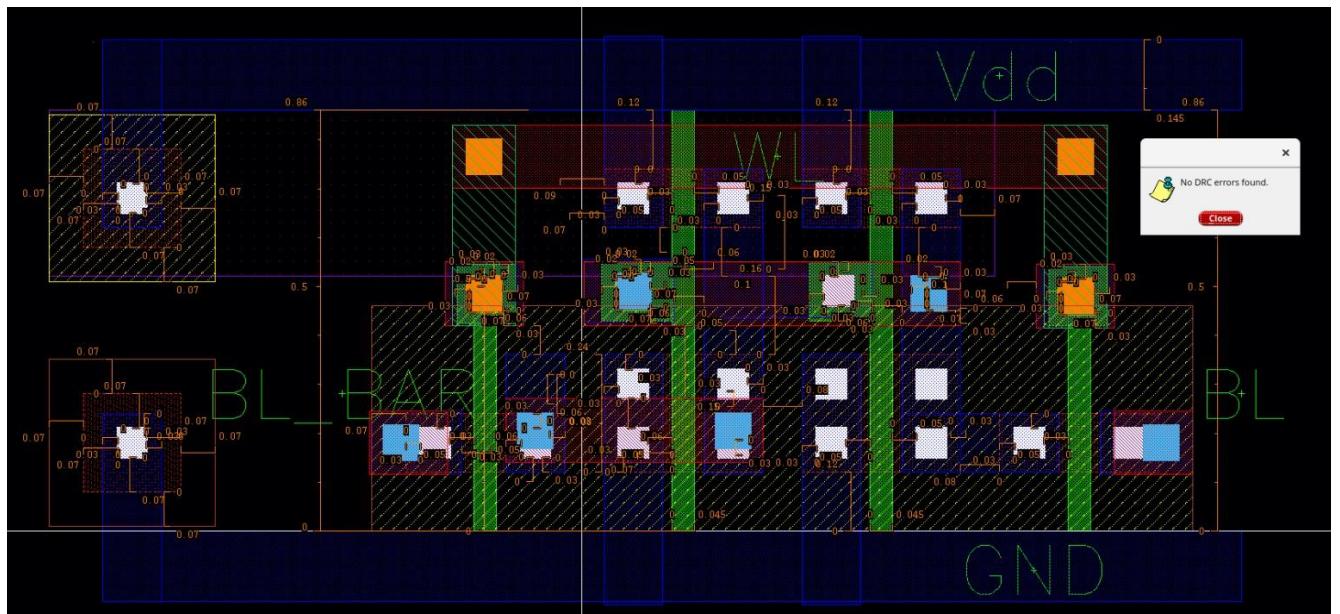


Fig. 17. DRC for single SRAM cell

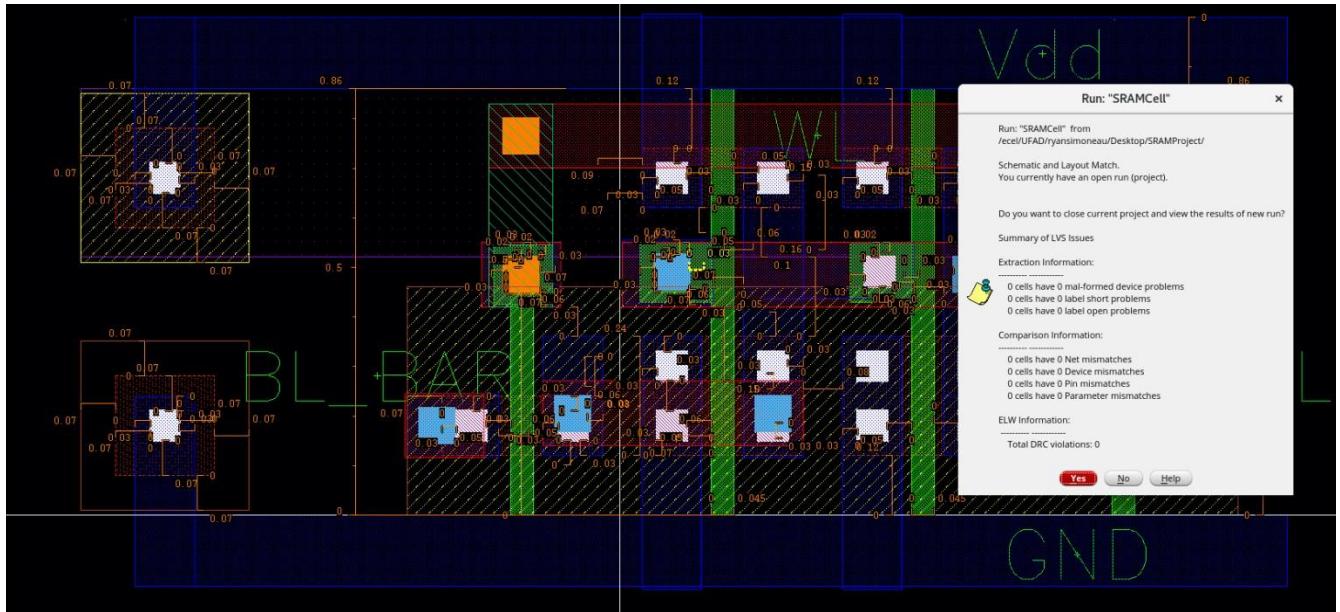


Fig. 18. LVS check for single SRAM cell

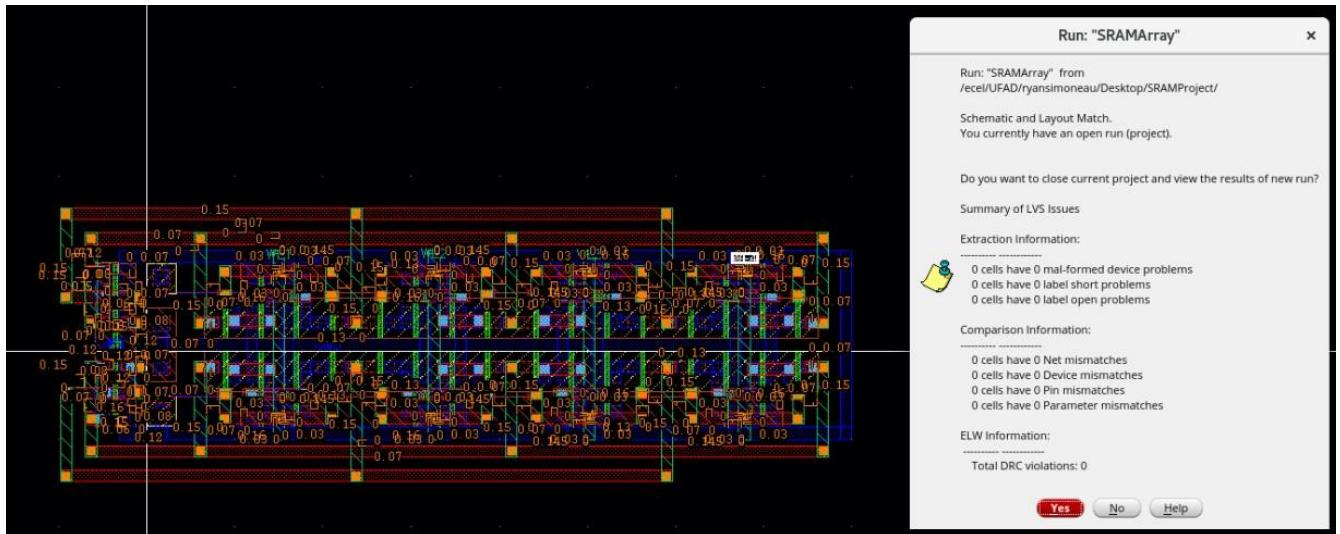


Fig. 19. LVS check for full Array

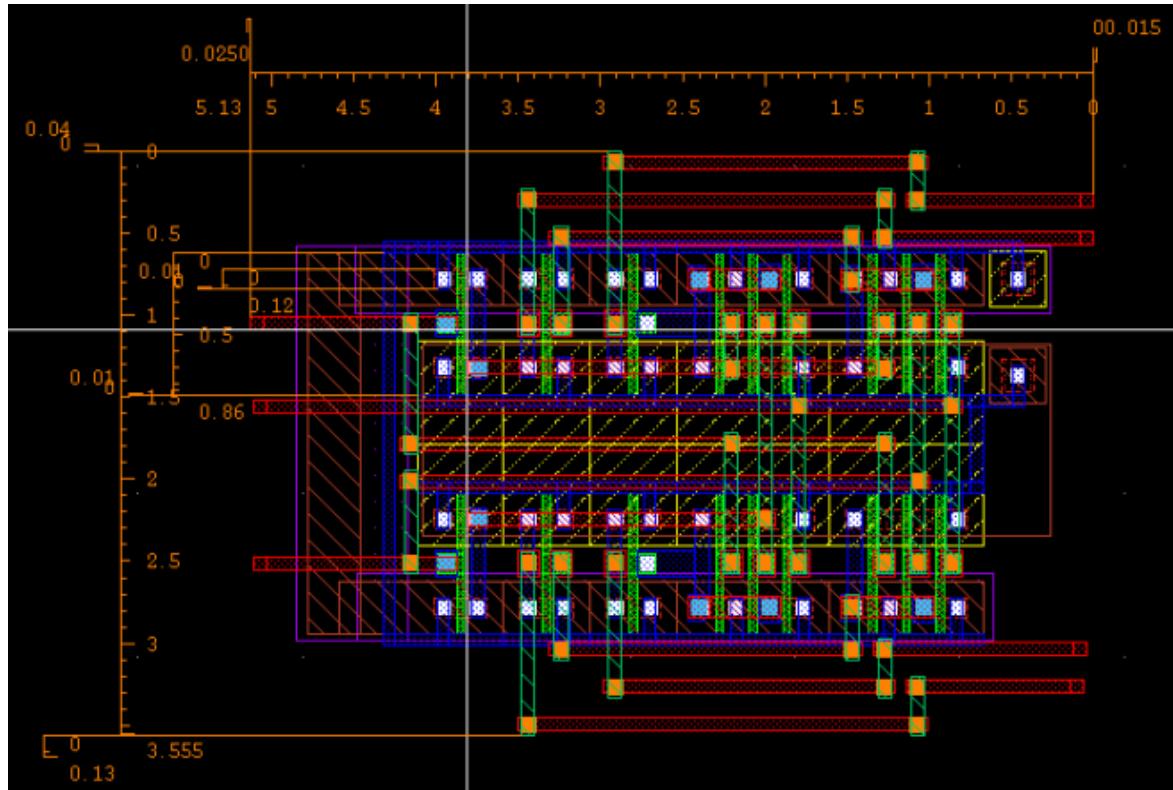


Fig. 20. Row Decoder measurements

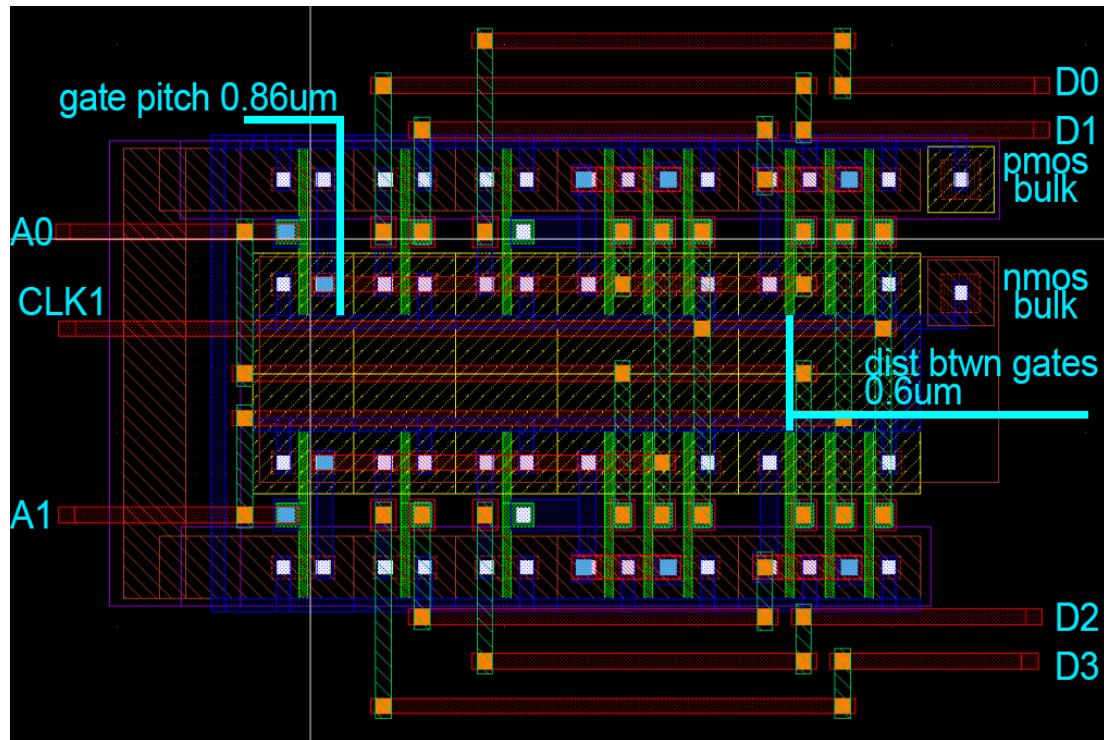


Fig. 20.1 Row Decoder layout

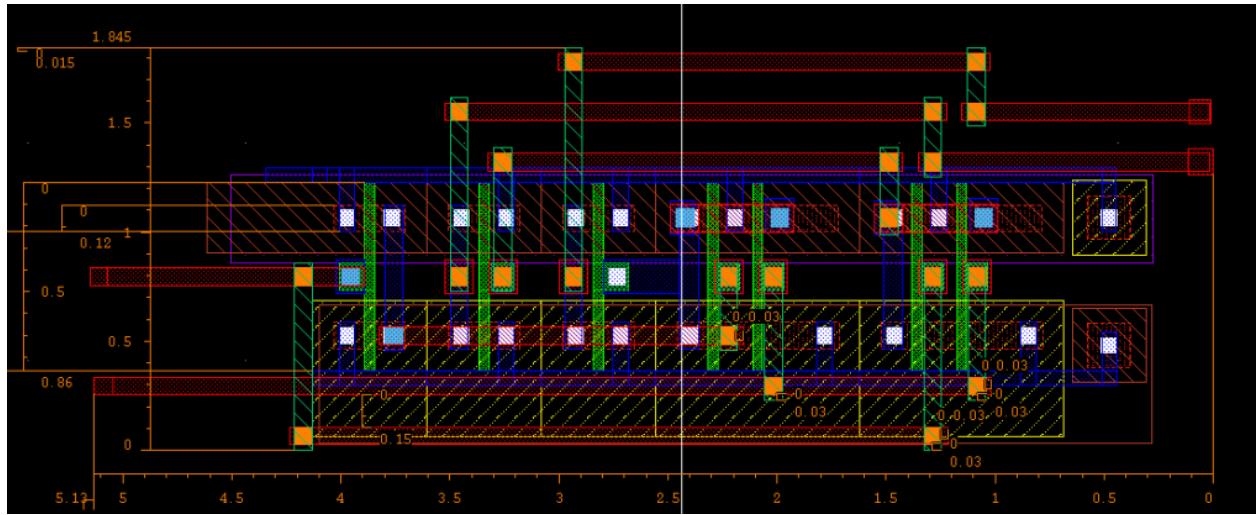


Fig. 20.2 Column Decoder layout

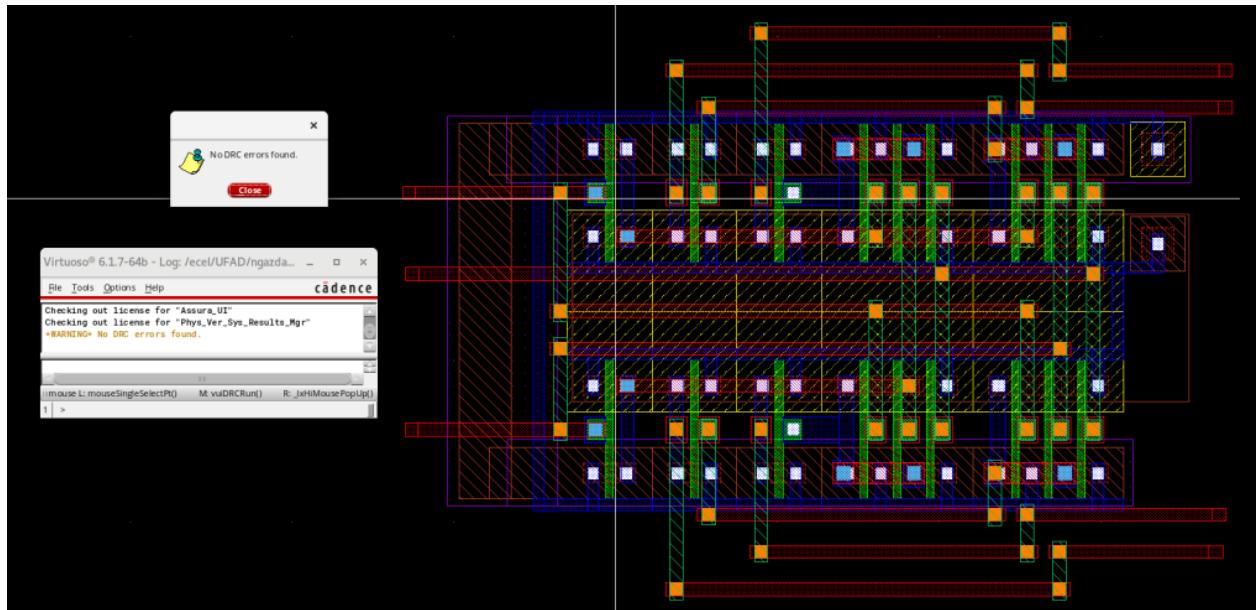


Fig. 20.1 DRC for row decoder

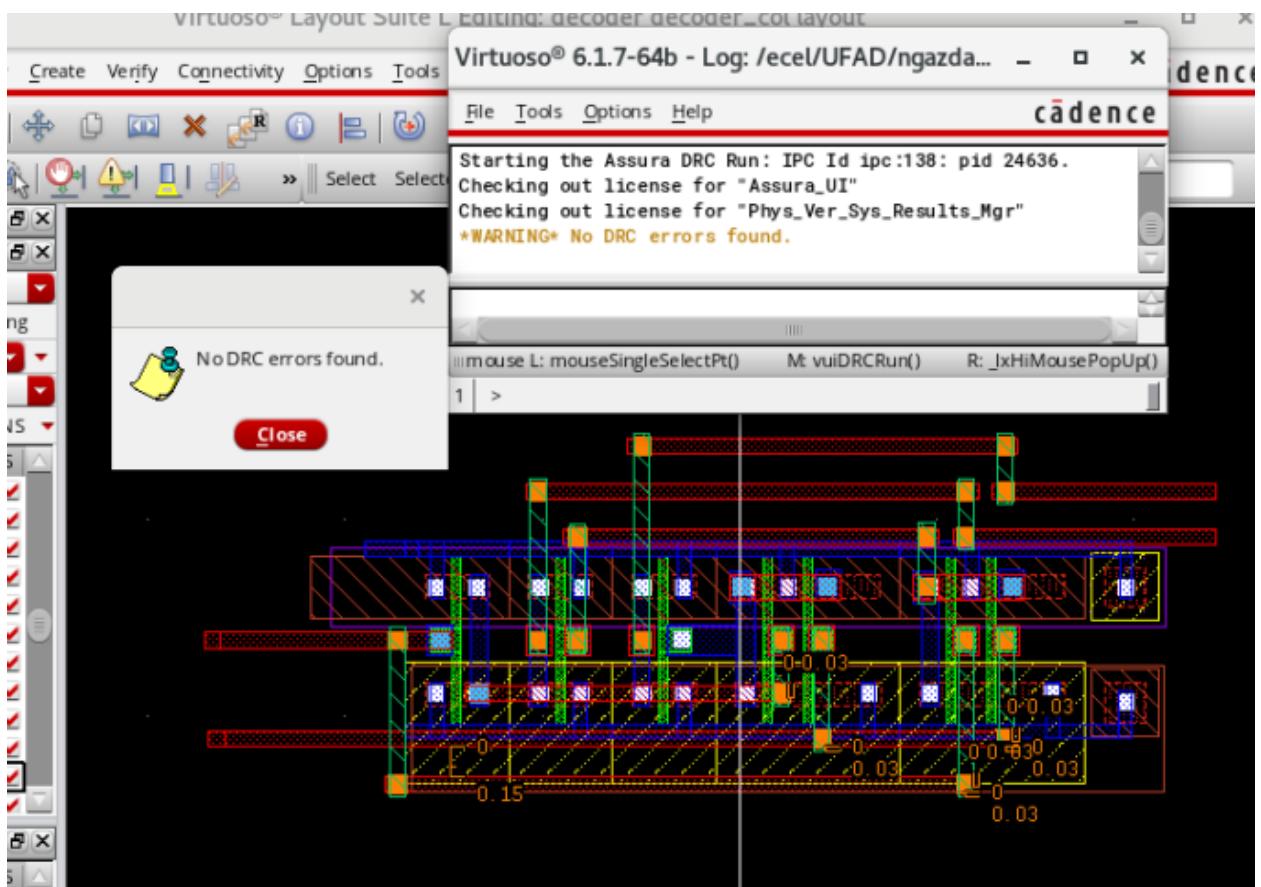


Fig. 21.2 DRC for column decoder

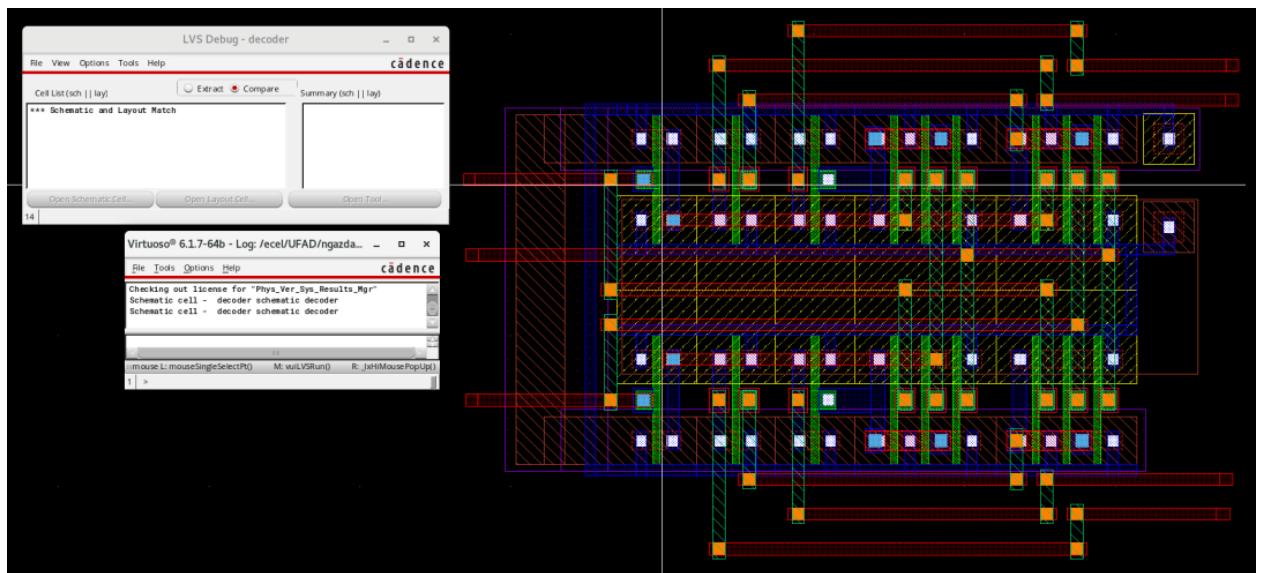


Fig. 22.1 LVS for row decoder

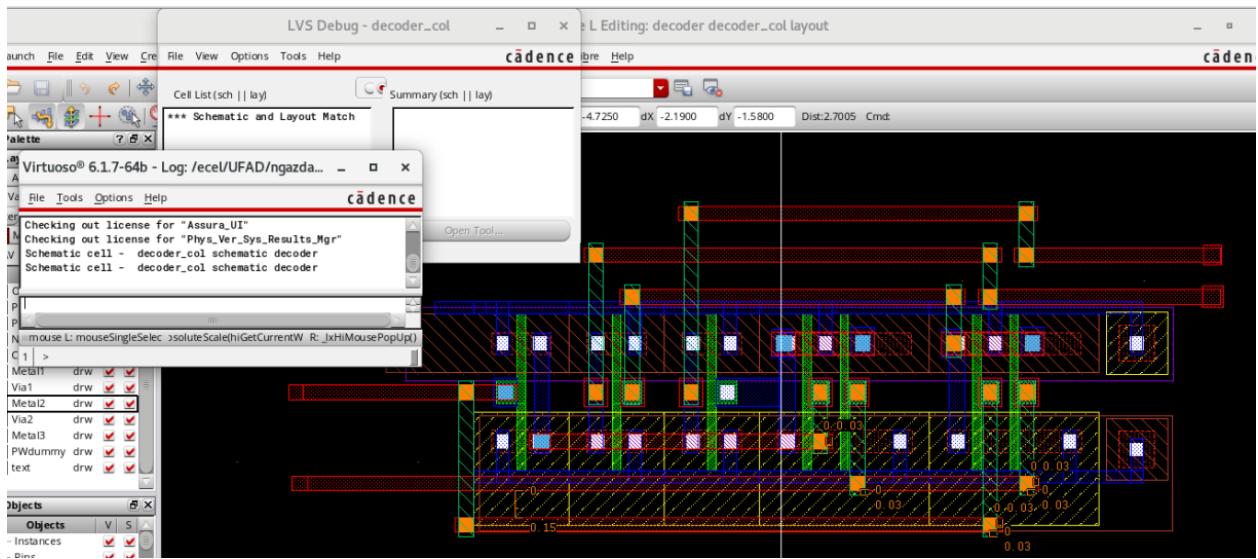


Fig. 22.2 LVS for column decoder

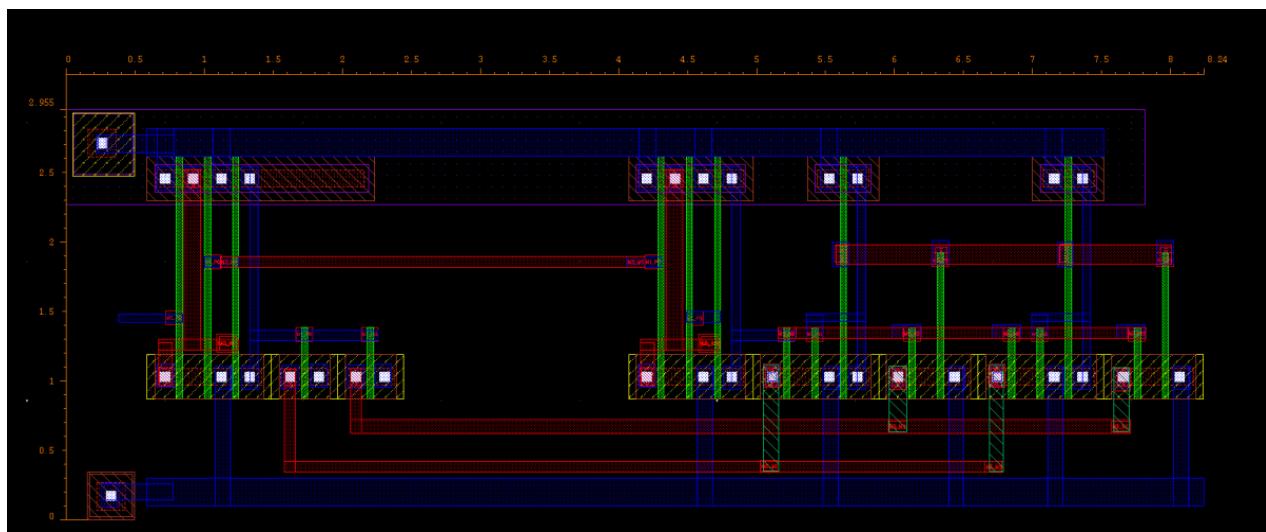


Fig. 23. Read-Write Control layout

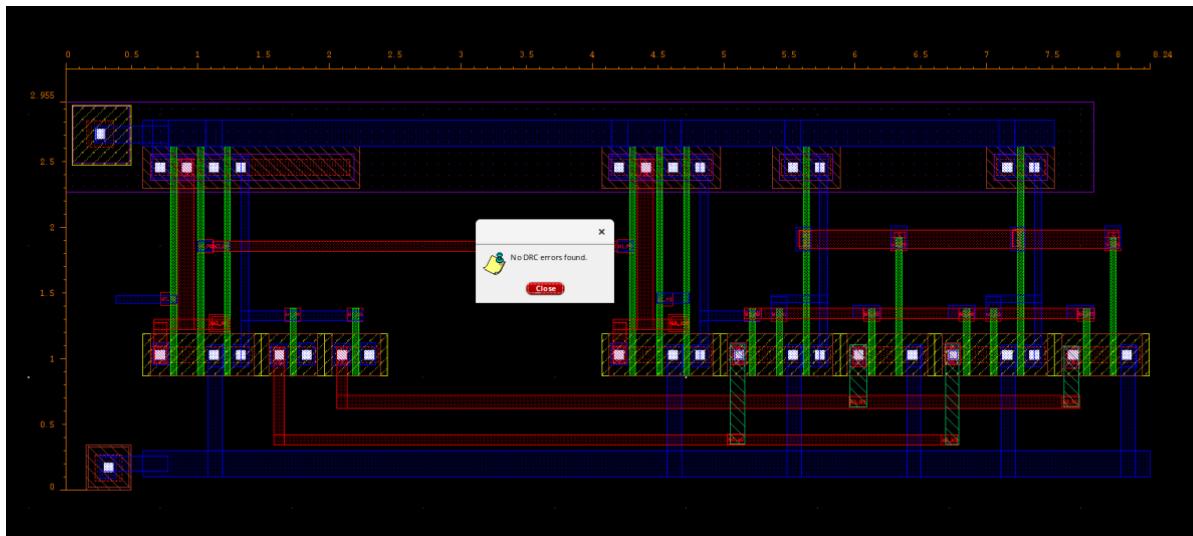


Fig. 24. DRC for Read-Write Control

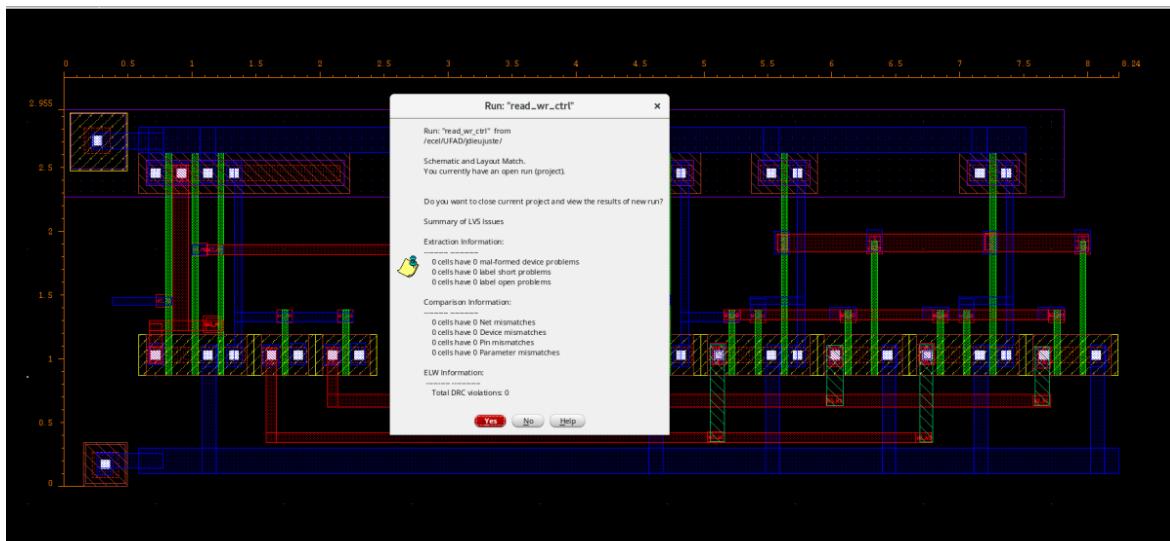


Fig. 25. LVS for Read-Write Control

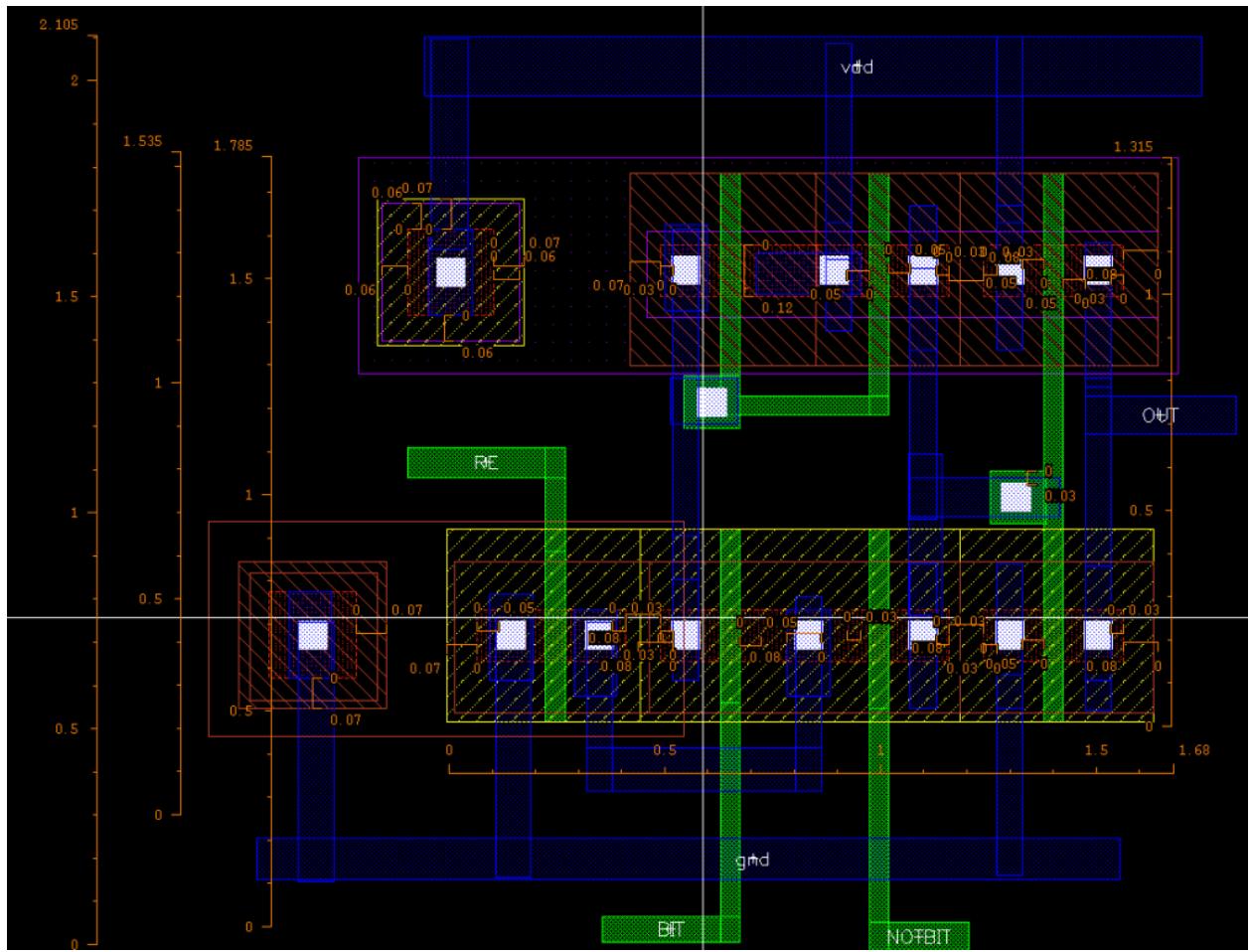


Fig. 26. Sense Amplifier layout

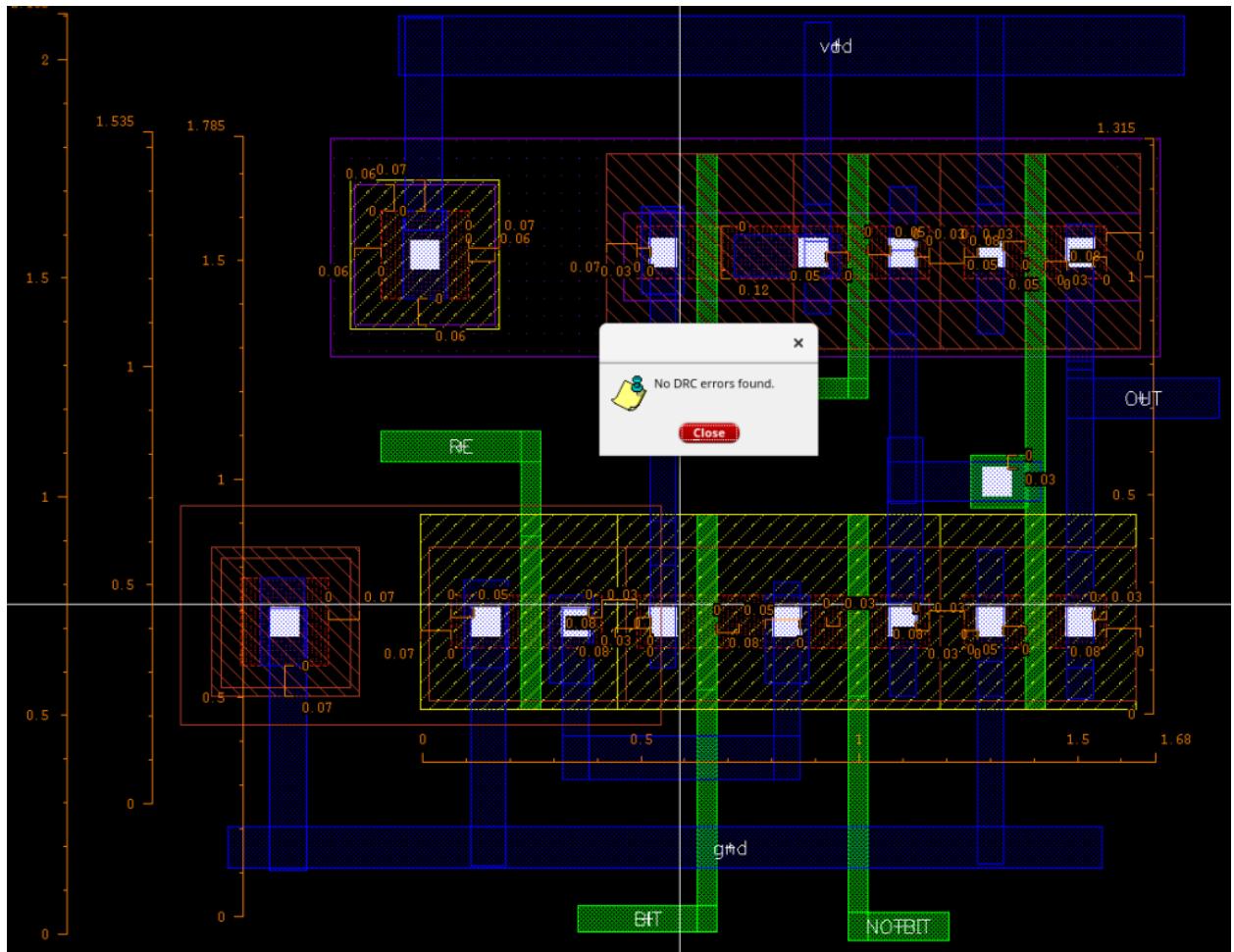


Fig. 27. DRC for Sense Amplifier layout

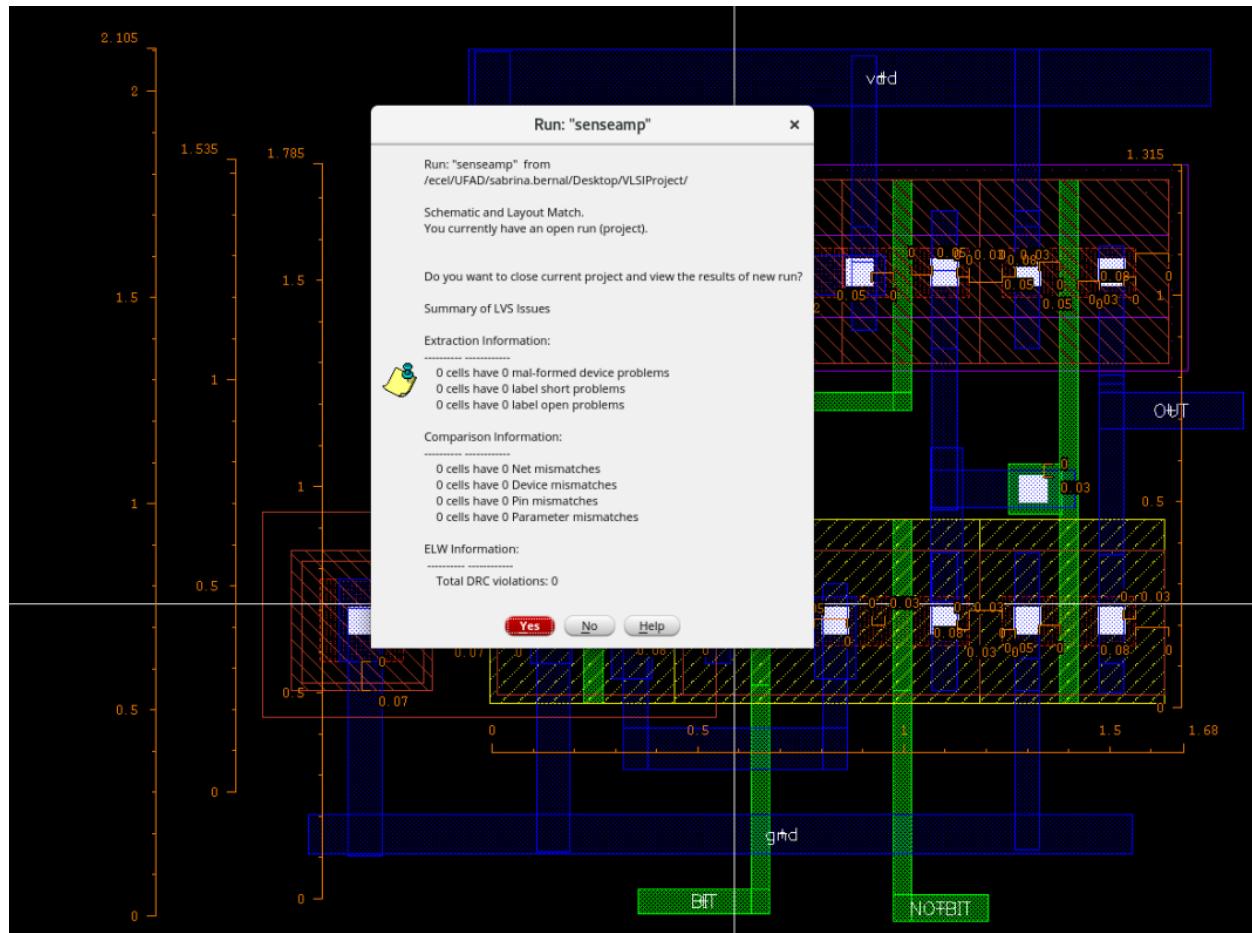


Fig. 28. LVS for Sense Amplifier layout

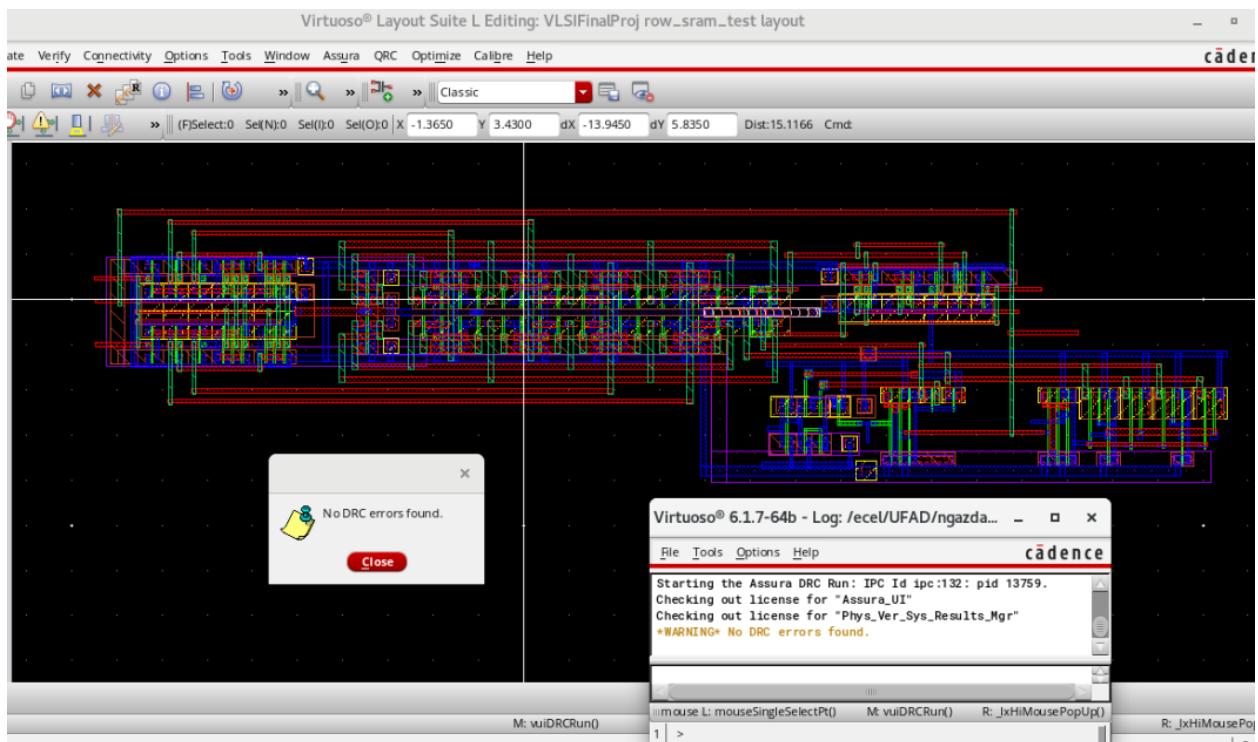


Fig. 29. DRC Full SRAM array

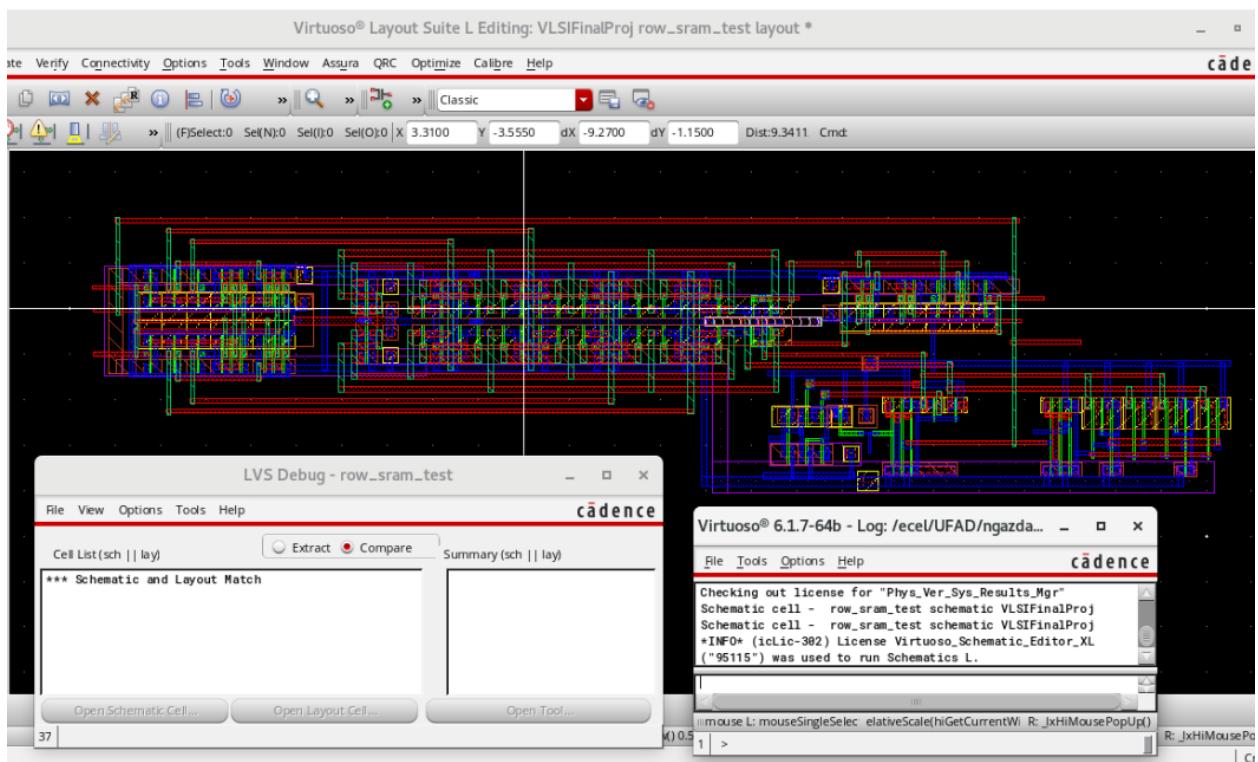


Fig. 30. LVS for Full SRAM array

Simulations

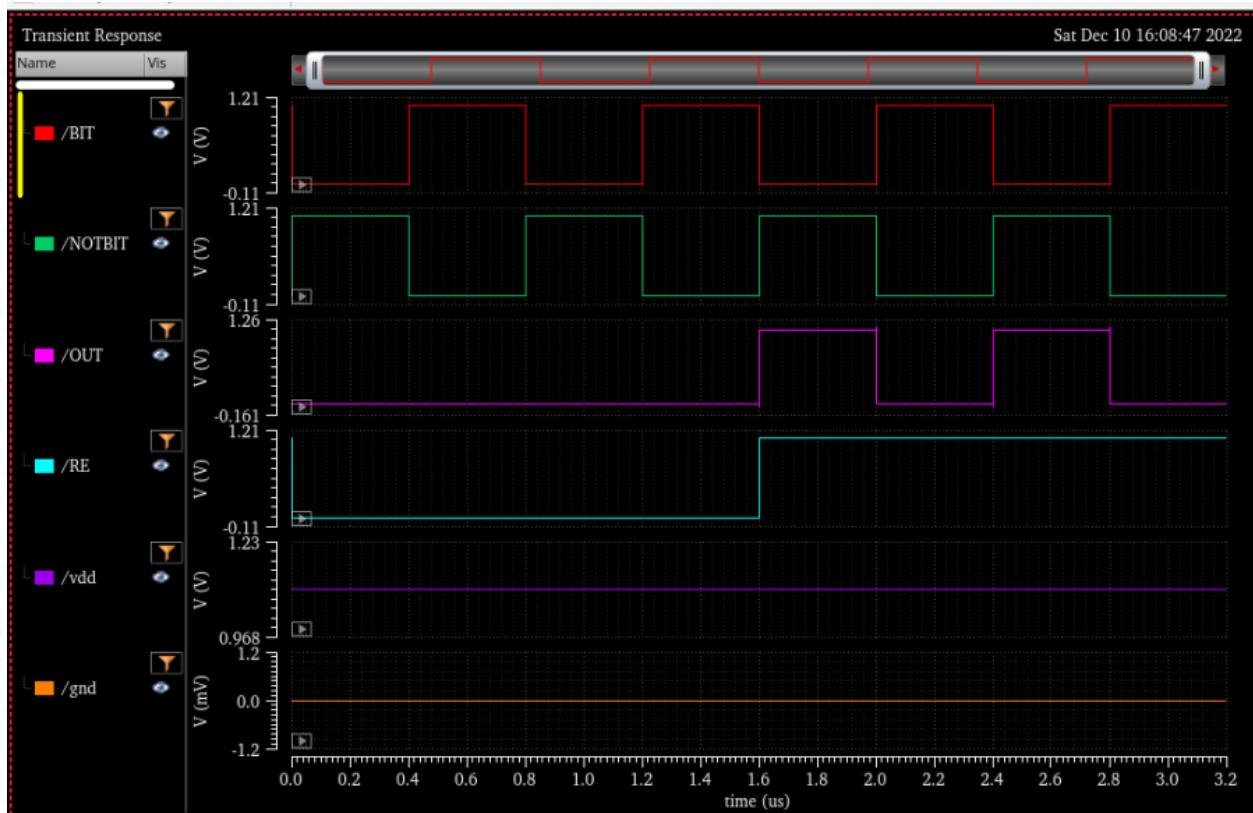


Fig. 31. Sense Amplifier simulation (with only one inverting buffer)

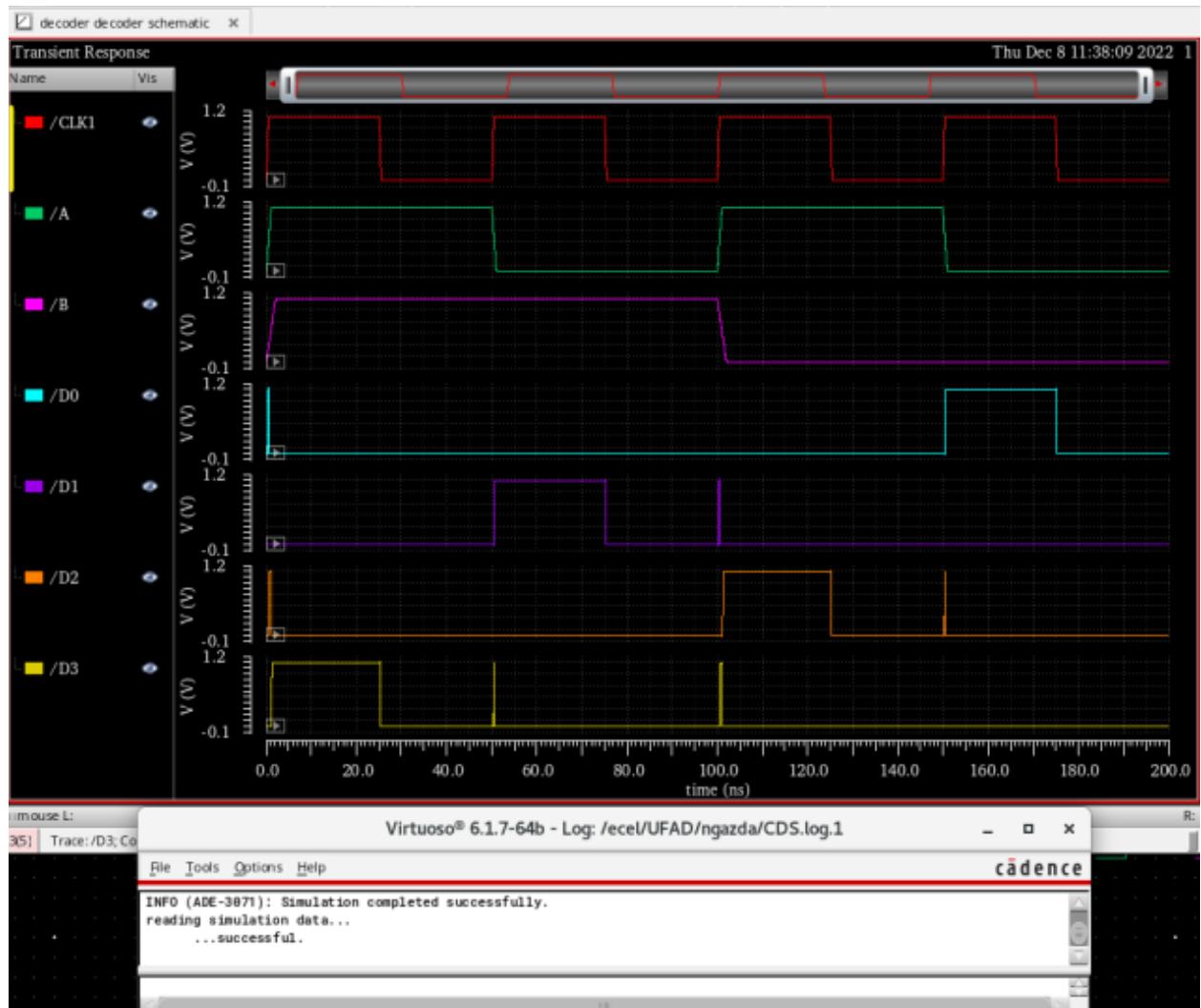


Fig. 32. Row Decoder Simulation

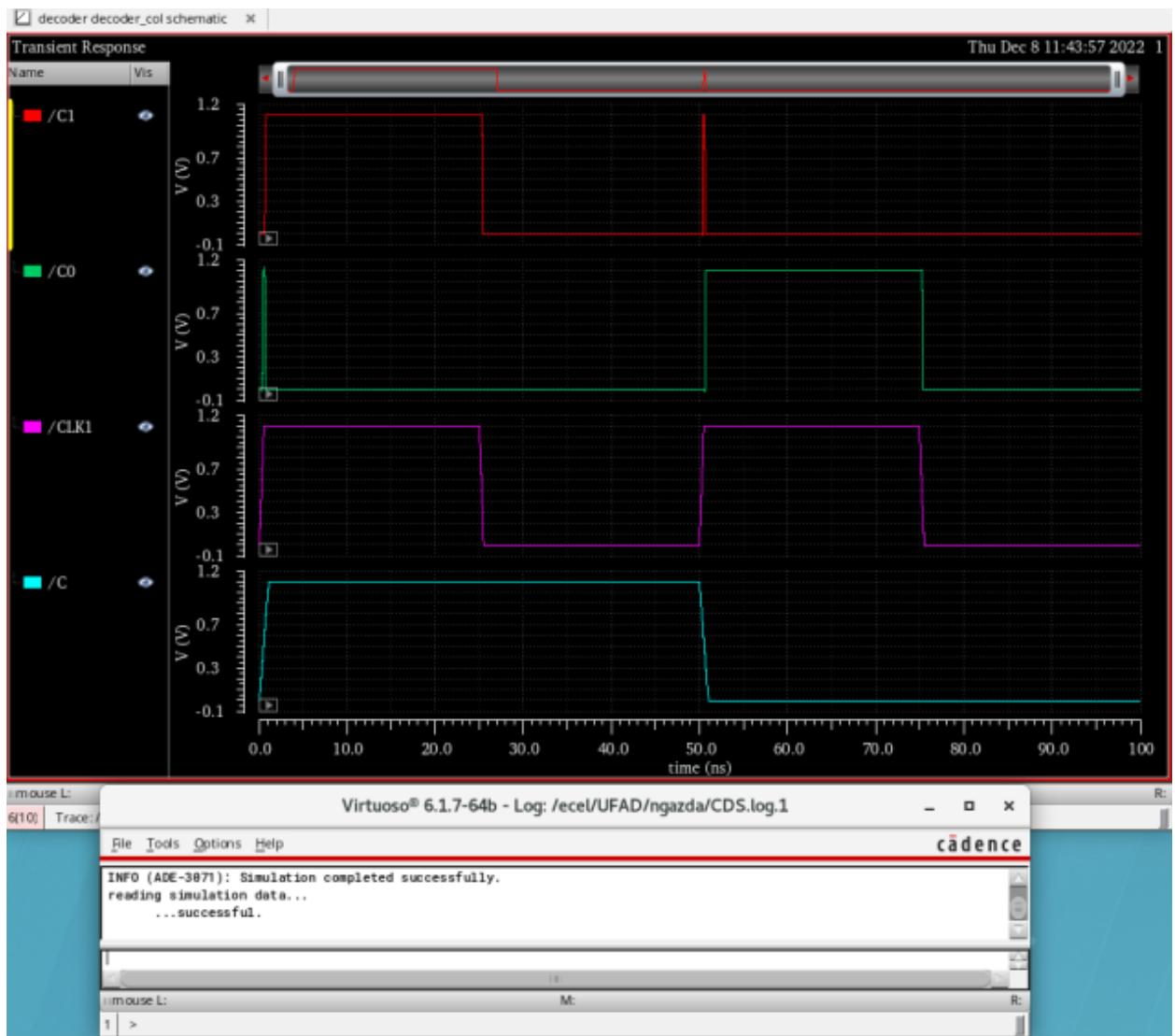


Fig. 33. Column Decoder Simulation