VLSI Final Project Report

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Schematic

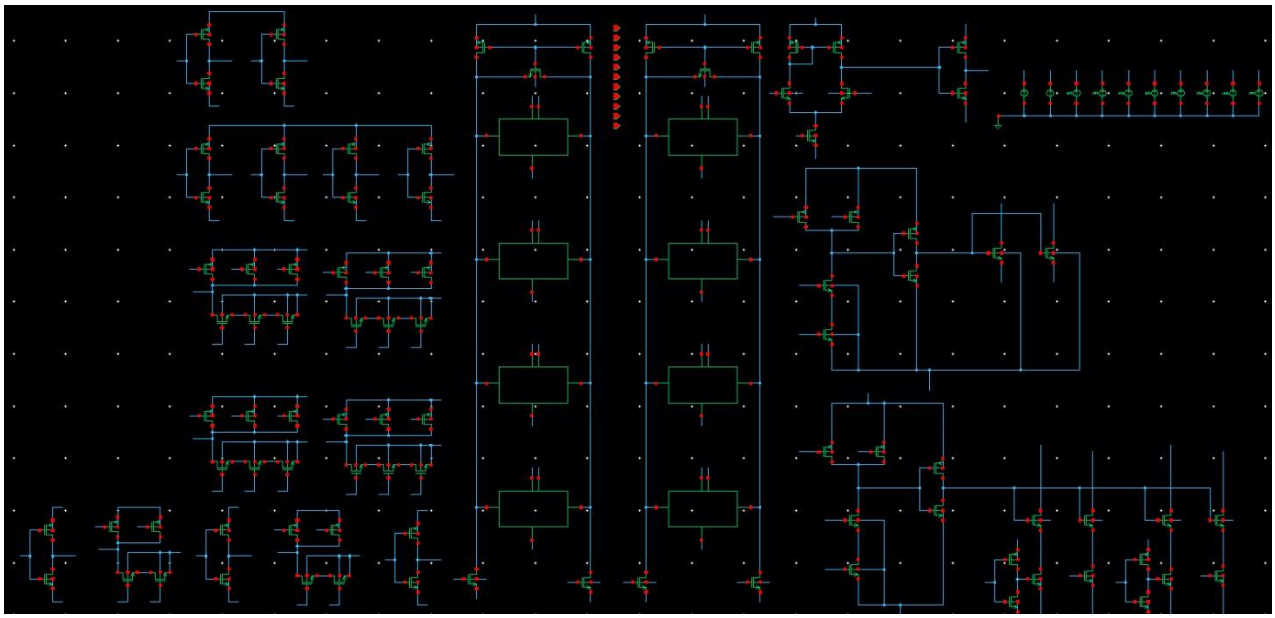

Fig. 1. Schematic of full SRAM array

Simulation

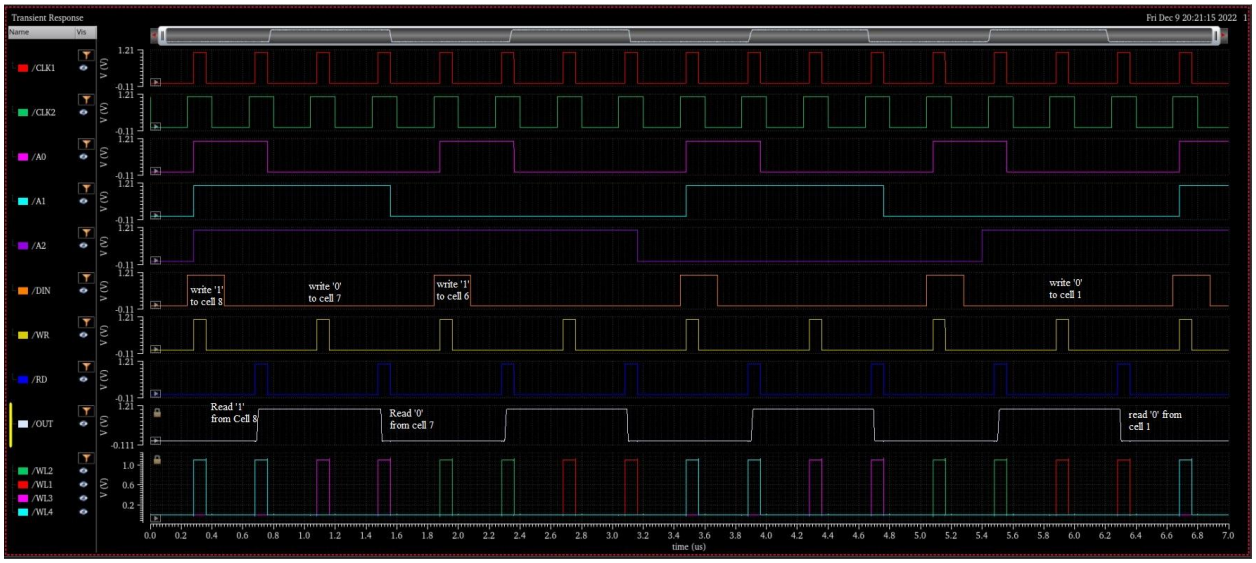

Fig. 2. Writing and Reading the array

Fig. 3. Precharge simulation

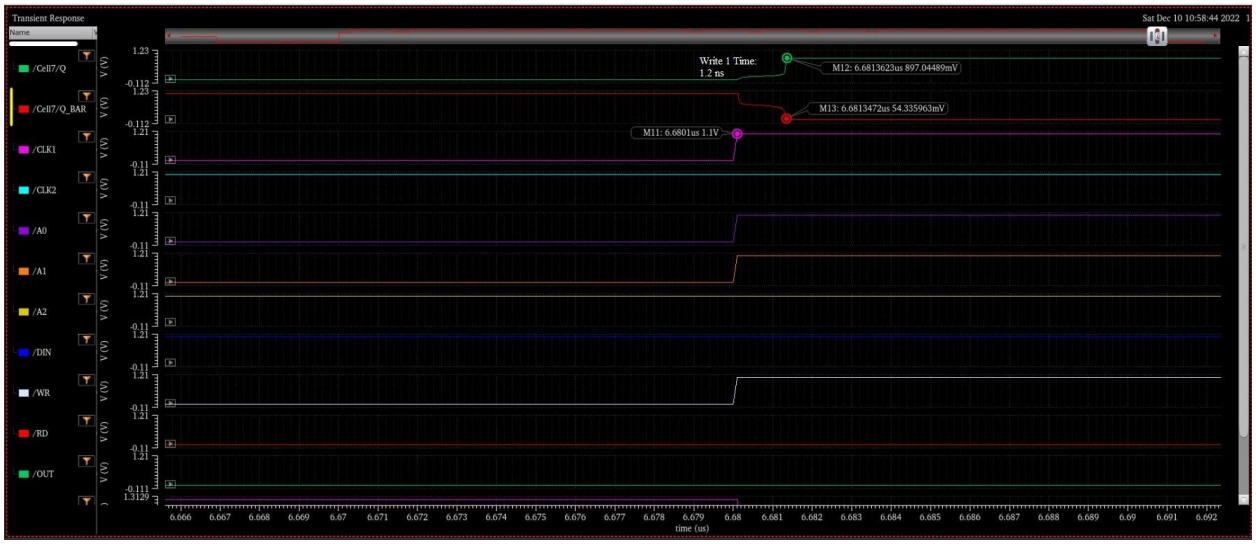

Fig. 4. Write times for 1 simulation

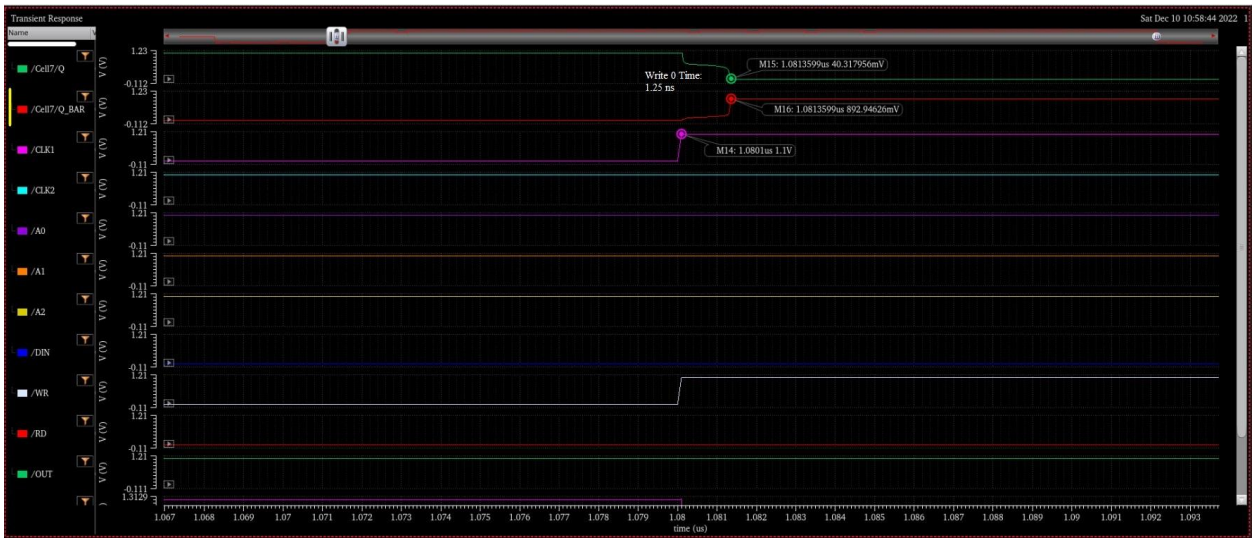

Fig. 5. Write times for 0 simulation

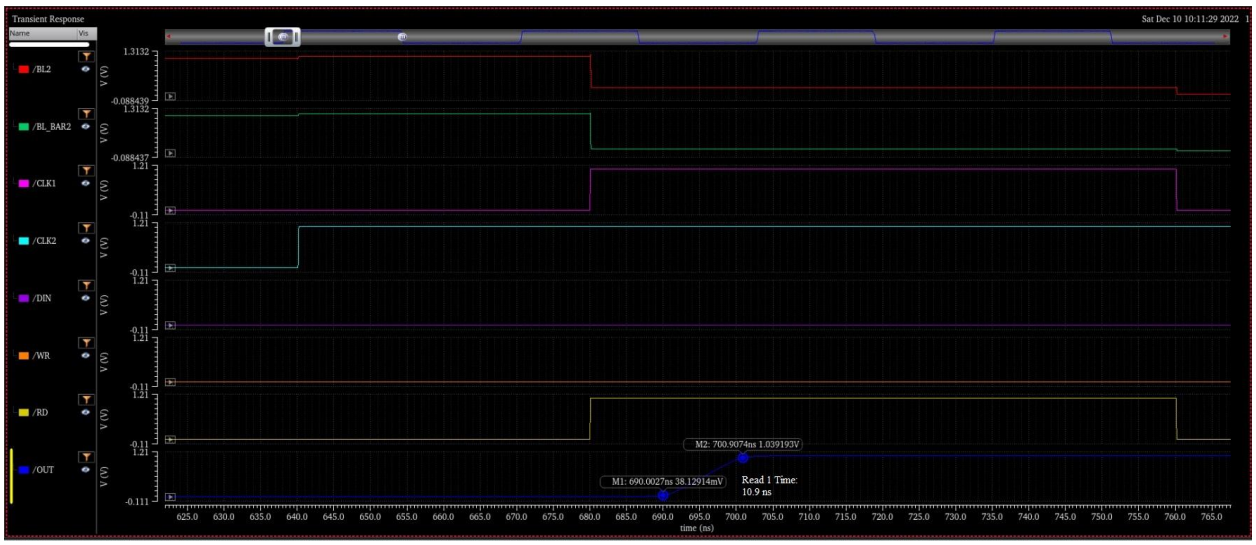

Fig. 6. Read times for 1 simulation

Fig. 7. Read times for 0 simulation

Design Considerations

Some design considerations were setting Metal2 layers for horizontal connections and Metal 3 for vertical connections for consistency and to avoid shorts. The gate pitch of the decoder was set to 0.86um. For the sense amplifier, contacts and gates were shared between transistors to minimize overall area and material. The width for some PMOS transistors were scaled to increase the voltage of some outputs.

Full Layout

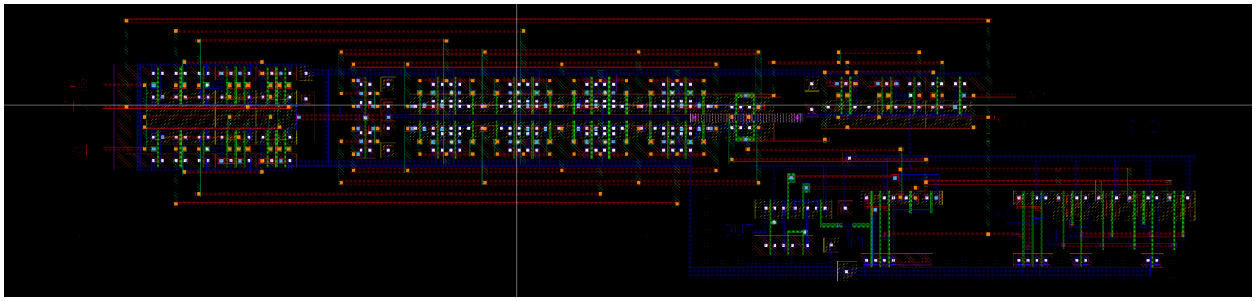

Fig. 8. Full layout, with row decoder on left, followed immediately by sram array and the column decoder to the right. Below the column decoder in the second row is the sense amplifier, and in the bottom right of the layout is the read/write control.

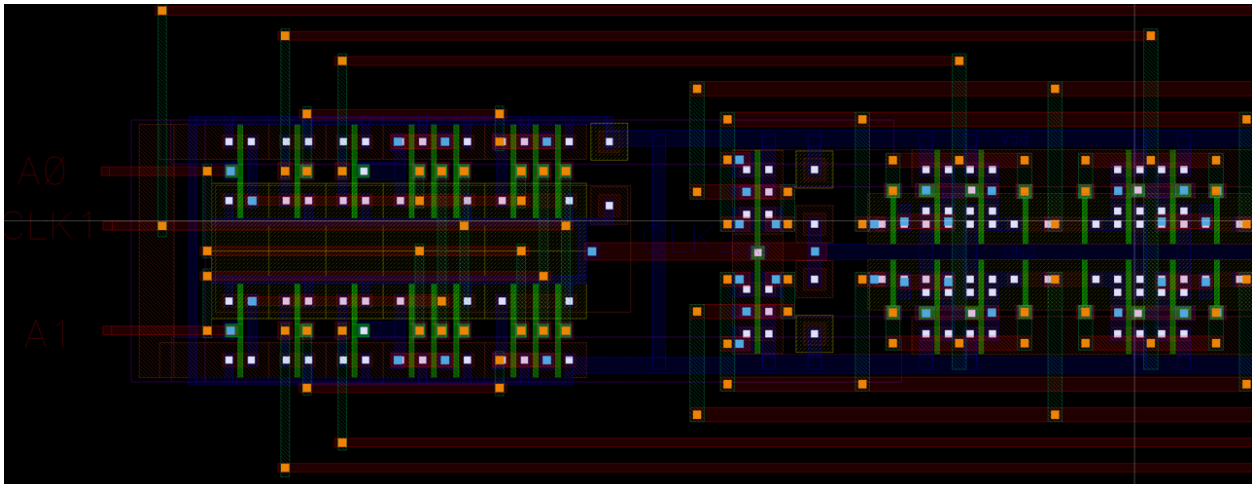

Fig. 9. Leftmost region of the final layout featuring the decoded address connections between the row decoder and the sram array.

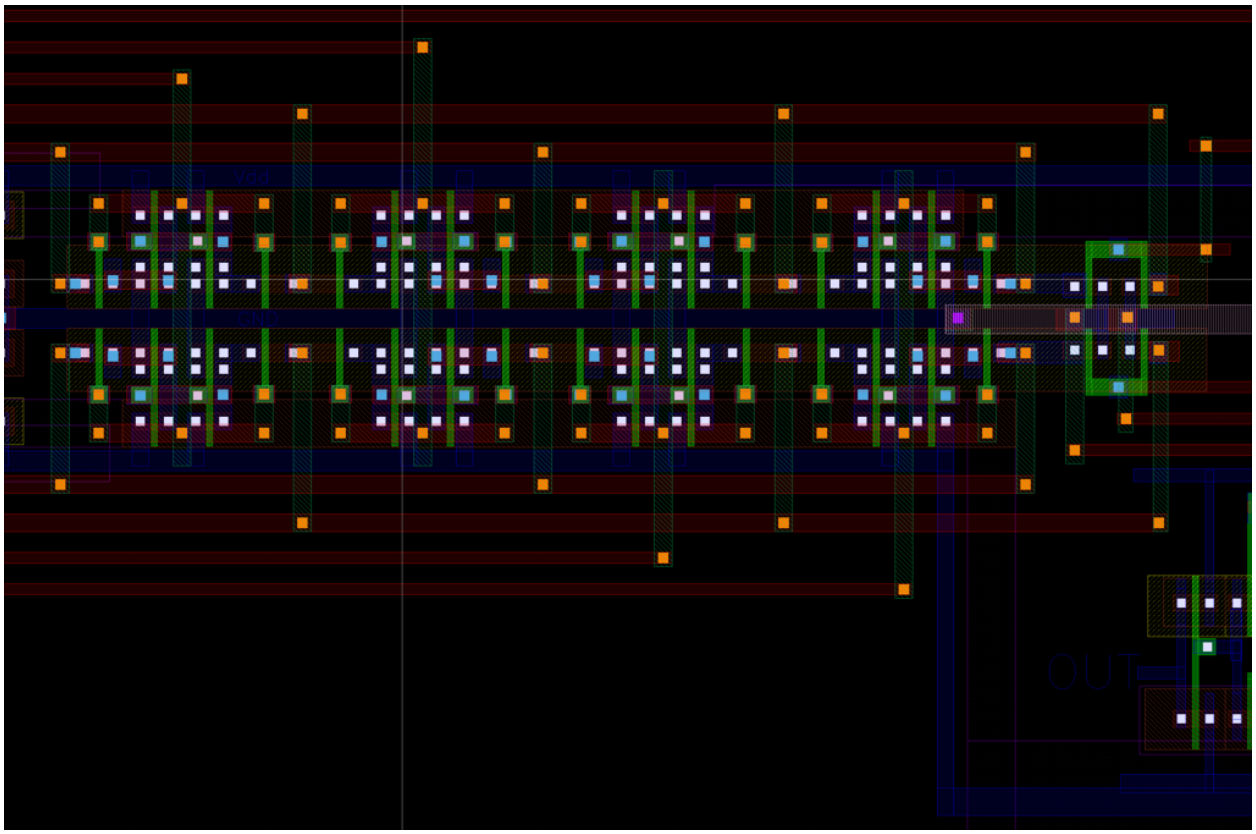

Fig. 10. Rest of the SRAM array showing the rest of the connections between the row decoder and SRAM

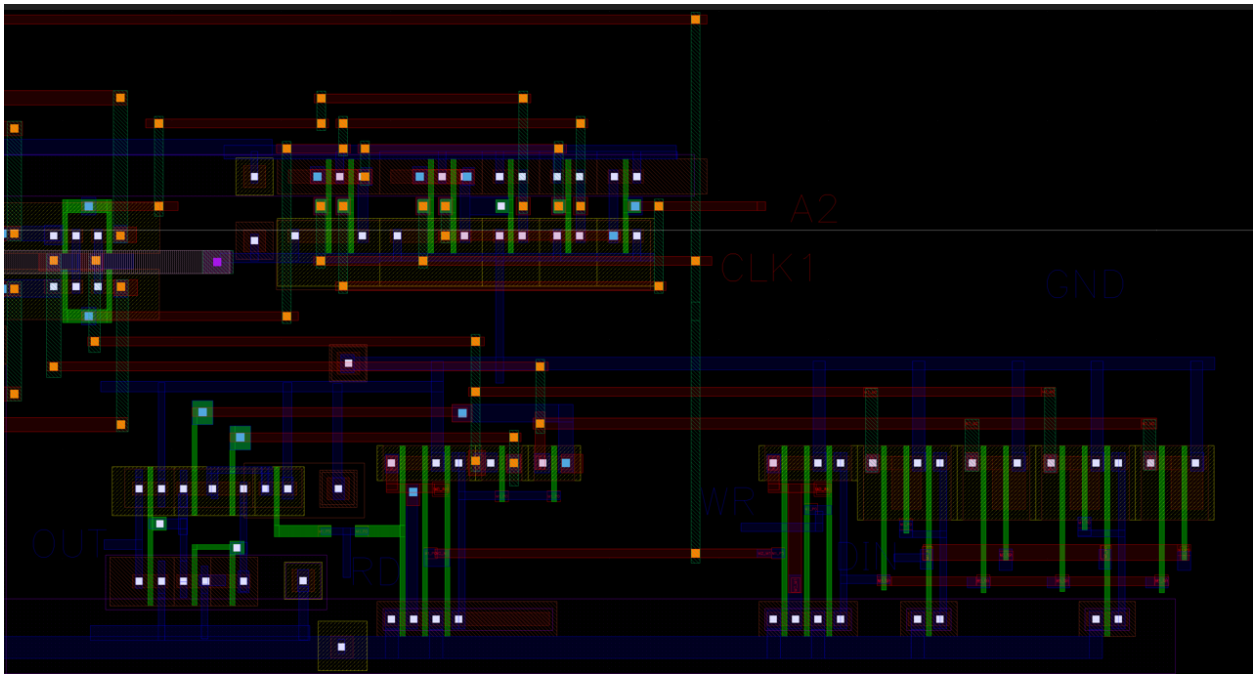

Fig. 11. Rightmost region of final layout featuring the column decoder, sense amplifier, and read write control. The column decoder outputs the decoded column to the 4 transistors connected to the bitlines of the SRAM array, which feed into the read/write control layout. The read/write control feeds a read signal and the read-controlled bitlines into the sense amplifier, which has the output OUT.

Conclusion

Overall, we thought that the material we learned in this project and for this course in general was interesting and useful for real world applications, such as using Virtuoso for layouts and schematics for transistor devices.

Description of work for each team member:

Janica Dieujuste (UFID: 58597233): Created schematic and layout for read and write control
Nikodem Gazda (UFID: 34669660): Created schematic and layout for column and row address decoders, debugged, assembled final layout
Sabrina Bernal (UFID: 6456-9196): Created schematic and layout for sense amplifier
Ryan Simoneau (UFID:8978-9911): Created schematic and layout for SRAM and debugged