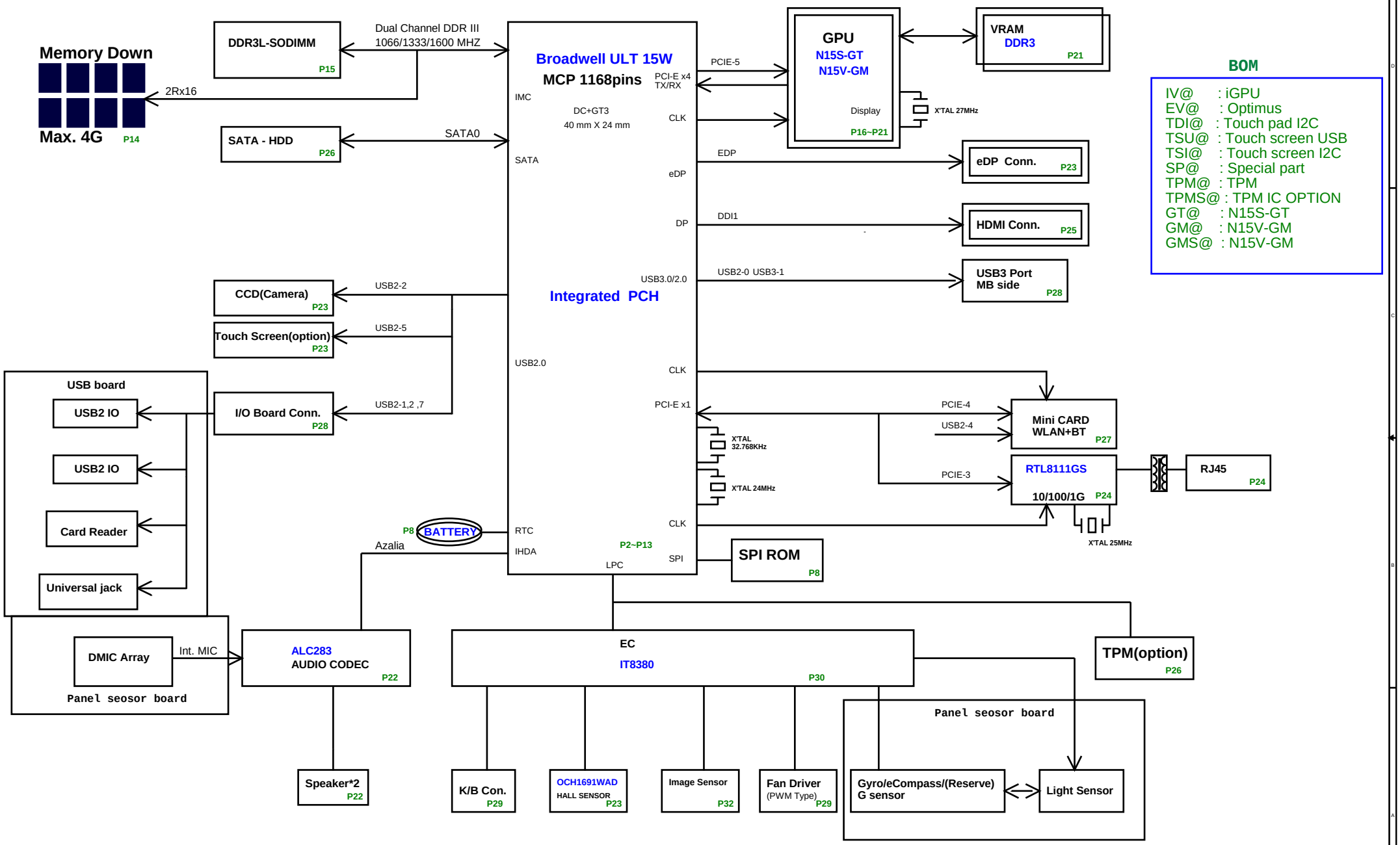
ZQX_DDR3 BDW ULT SYSTEM BLOCK DIAGRAM

01



BOM

IV@ : iGPU
EV@ : Optimus
TDI@ : Touch pad I2C
TSU@ : Touch screen USB
TSI@ : Touch screen I2C
SP@ : Special part
TPM@ : TPM
TPMS@ : TPM IC OPTION
GT@ : N15S-GT
GM@ : N15V-GM
GMS@ : N15V-GM

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PROJECT : ZQX

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	Block Diagram	1B

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SP@ : i3-4010U i3-4020U i5-4210U

Haswell ULT (DISPLAY,eDP)

02

U28A HSW_ULT_DDR3L

HDMI

[25] INT_HDMITX2N C54 DDI1_TXN0
[25] INT_HDMITX2P C55 DDI1_TXP0
[25] INT_HDMITX1N B58 DDI1_TXN1
[25] INT_HDMITX1P C58 DDI1_TXP1
[25] INT_HDMITX0N B55 DDI1_TXN2
[25] INT_HDMITX0P A55 DDI1_TXP2
[25] INT_HDMICLK- A57 DDI1_TXN3
[25] INT_HDMICLK+ B57 DDI1_TXP3

C51 DDI2_TXN0
C50 DDI2_TXP0
C53 DDI2_TXN1
B54 DDI2_TXP1
C49 DDI2_TXN2
B50 DDI2_TXP2
A53 DDI2_TXN3
B53 DDI2_TXP3

DDI

EDP

EDP_TXN0 C45 EDP_TXN0 → EDP_TXN0 [23]
EDP_TXP0 B46 EDP_TXP0 → EDP_TXP0 [23]
EDP_TXN1 A47 EDP_TXN1 → EDP_TXN1 [23]
EDP_TXP1 B47 EDP_TXP1 → EDP_TXP1 [23]

EDP_TXN2 C47
EDP_TXP2 C46
EDP_TXN3 C49
EDP_TXP3 B49

eDP Panel

EDP_AUXN A45 EDP_AUXN → EDP_AUXN [23]
EDP_AUXP B45 EDP_AUXP → EDP_AUXP [23]

EDP_RCOMP D20 EDP_RCOMP — R229 24.9/F_4 — +VCCIOA_OUT
EDP_DISP_UTIL A43 DP_UTIL — R551 *0_4 PCH_BRIGHT
R552 *0_4

eDP_RCOMP
Trace length < 100 mils
Trace width = 20 mils
Trace spacing = 25 mils

1 OF 19

U28I HSW_ULT_DDR3L

[23] PCH_BRIGHT PCH_BRIGHT B8 EDP_BKLCTL
[23] PCH_BLON PCH_BLON A9 EDP_BKLEN
[23] EDP_VDD_EN C6 EDP_VDDEN

eDP SIDEBAND

PCI_PIRQA# U6 PIRQA/GPIO77 +3V
PCI_PIRQB# P4 PIRQB/GPIO78 +3V
PCI_PIRQC# N4 PIRQC/GPIO79 +3V
PCI_PIRQD# N2 PIRQD/GPIO80 +3V
TP94 PCI_PME# AD4 PME +3V_S5

PCIE

TPD_INT# D U7 GPIO55 +3V
DGPU_SELECT# L1 GPIO52 +3V
[10] BOARD_ID4 BOARD_ID4 L3 GPIO54 +3V
[10] BOARD_ID1 BOARD_ID1 R5 GPIO51 +3V
[10] BOARD_ID2 BOARD_ID2 L4 GPIO53 +3V

DISPLAY

DDPB_CTRLCLK B9 → HDMI_DDCCLK_SW [25]
DDPB_CTRLDATA C9 → HDMI_DDCDATA_SW [25]
DDPC_CTRLCLK D9
DDPC_CTRLDATA D11

DDPB_AUXN C5
DDPC_AUXN B6
DDPB_AUXP B5
DDPC_AUXP A6

DDPB_HPD C8 → INT_HDMI_HPD [25]
DDPC_HPD A8
EDP_HPD D6 → EDP_HPD [23]
R537 100K_4

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+3V
PCI_PIRQA# R184 10K_4
PCI_PIRQB# R142 10K_4
PCI_PIRQC# R141 10K_4
PCI_PIRQD# R491 10K_4

+3V
TPD_INT# D R159 10K_4
DGPU_SELECT# R488 10K_4
DGPU_SELECT#,0=defalt,1=iGPU

Add 10/31

+3V
[28,29] TPD_INT# — 3 — Q19 2N7002K — 1 — TPD_INT# D
2

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	Haswell 3/5 (DDI/eDP)	1B
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Change Data and DQS to interleave.

Haswell ULT (DDR3L)

U28C — HSW_ULT_DDR3L

DDR CHANNEL A

3 OF 19

Haswell Processor (DDR3)

U28D — HSW_ULT_DDR3L

DDR CHANNEL B

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+VREF_CA_CPU → +VREF_CA_CPU [14]

+VREFDQ_SA_M3 → +VREFDQ_SA_M3 [14]

+VREFDQ_SB_M3 → +VREFDQ_SB_M3 [15]

Power tracking

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PROJECT : ZQX

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	Haswell 2/5 (DDR3 I/F)	1B

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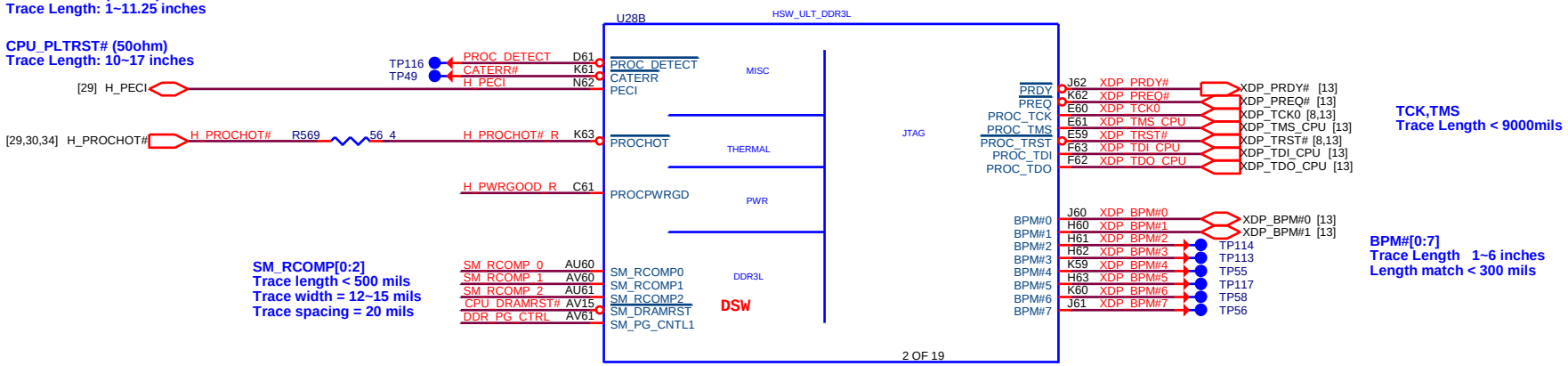
03

Haswell ULT (SIDEBAND)

H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 iches

H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches

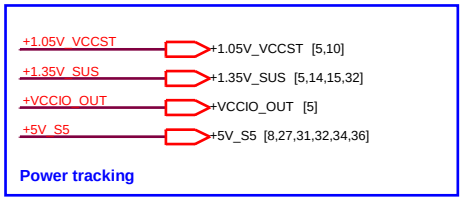
CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches



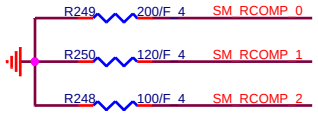
TCK,TMS
Trace Length < 9000mils

BPM#[0:7]
Trace Length 1~6 inches
Length match < 300 mils

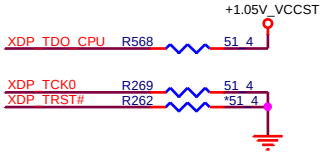
SM_RCOMP[0:2]
Trace length < 500 mils
Trace width = 12~15 mils
Trace spacing = 20 mils



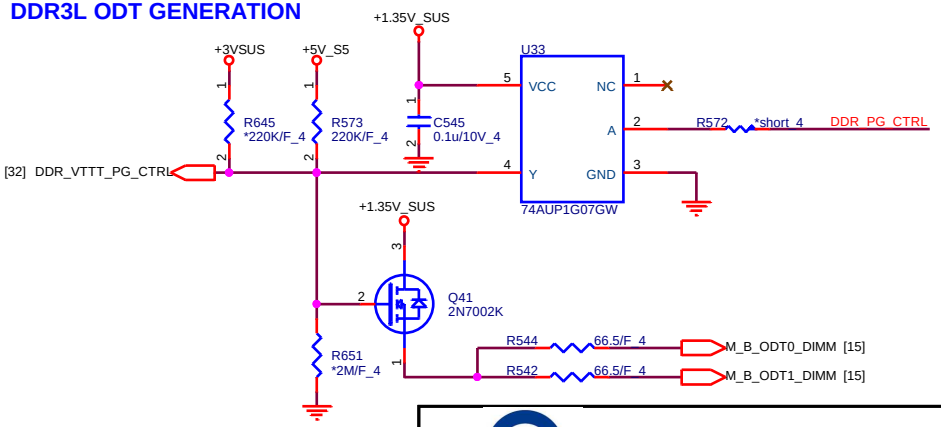
DRAM COMP



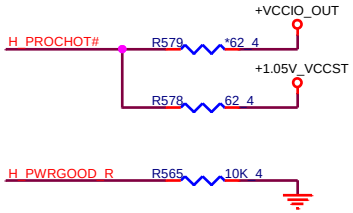
XDP PU/PD



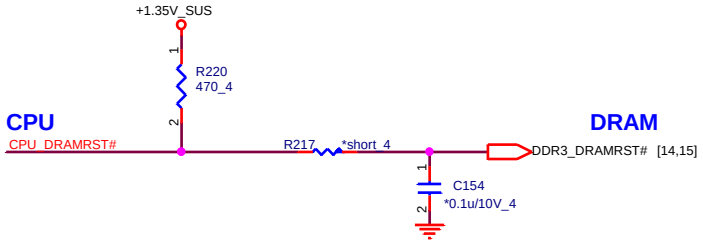
DDR3L ODT GENERATION



PU/PD of CPU



DRAMRST



Quanta Computer Inc.
PROJECT : ZQX

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	Haswell 1/5 (PEG/DMI/FDI)	1B
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Haswell ULT (POWER)

VDDQ Output Decoupling Recommendations		
330uFx2	7343	BOT socket side
22uFx11	0805	5 onTOP, 6 on BOT inside socket cavity
10uFx10	0805	5 onTOP, 5 on BOT inside socket cavity

VCC Output Decoupling Recommendations		
470uFx4	7343	TOP socket side
22uFx8	0805	4 on TOP, 4 on BOT near socket edge
22uFx11	0805	TOP, inside socket cavity
10uFx11	0805	BOT, inside socket cavity

Power tracking

+3V [2,7,8,9,10,11,13,14,15,16,17,18,21,22,23,24,25,26,27,28,29,31,32,33,34,35,36]
+1.05V [11,13,30,33,34,35]
+1.35V_SUS [4,14,15,32]
+1.05V_VCCST [4,10]
+VCCIN [34]

+1.35V_SUS
R231 0_1206
R239 0_1206

+1.35V_CPU 1.4A

+1.35V_CPU
C220 10u/6.3V_6
C216 10u/6.3V_6
C277 10u/6.3V_6
C219 10u/6.3V_6
C276 10u/6.3V_6
C217 10u/6.3V_6
C470 *470u/2V_7343
C494 2.2u/6.3V_6
C215 2.2u/6.3V_6
C278 2.2u/6.3V_6
C218 2.2u/6.3V_6

U28L — HSW_ULT_DDR3L

TP57 ULT_RVSD_61 L59 RSVD
TP54 ULT_RVSD_62 J58 RSVD
AH26 VDDQ
AJ31 VDDQ
AJ33 VDDQ
AJ37 VDDQ
AN33 VDDQ
AP43 VDDQ
AR48 VDDQ
AY35 VDDQ
AY40 VDDQ
AY44 VDDQ
AY50 VDDQ
F59 VCC
TP61 ULT_RVSD_63 N58 RSVD
TP68 ULT_RVSD_64 AC58 RSVD
+VCCIN R566 100/F_4 VCC_SENSE_R E63 VCC_SENSE
[34] VCC_SENSE R582 *short_4
TP47 ULT_RVSD_65 AB23 RSVD
300mA +VCCIO_OUT A59 VCCIO_OUT
300mA +VCCIOA_OUT E20 VCCIOA_OUT
TP44 ULT_RVSD_66 AD23 RSVD
TP48 ULT_RVSD_67 AA23 RSVD
TP64 ULT_RVSD_68 AE59 RSVD
H_CPU_SVIDART# L62 VIDALERT
H_CPU_SVIDCLK N63 VIDSCLK
H_CPU_SVIDDAT L63 VIDSOUT
[13] VCCST_PWRGD VCCST_PWRGD B59 VCCST_PWRGD
[34] VRON_CPU VRON_CPU F60 VR_EN
[10,34] IMVP_PWRGD IMVP_PWRGD C59 VR_READY
D63 VSS
[13] PWR_DEBUG R277 *short_4 PWR_DEBUG H59 PWR_DEBUG
+1.05V_VCCST R570 150_6 P62 VSS
TP51 ULT_RVSD_69 P60 RSVD_TP
TP52 ULT_RVSD_70 P61 RSVD_TP
TP50 ULT_RVSD_71 N59 RSVD_TP
TP62 ULT_RVSD_72 N61 RSVD_TP
TP70 ULT_RVSD_73 T59 RSVD
TP69 ULT_RVSD_74 AD60 RSVD
TP59 ULT_RVSD_75 AD59 RSVD
TP66 ULT_RVSD_76 AA59 RSVD
TP65 ULT_RVSD_77 AE60 RSVD
TP60 ULT_RVSD_78 AC59 RSVD
TP53 ULT_RVSD_79 AC58 RSVD
TP63 ULT_RVSD_80 U59 RSVD
TP67 ULT_RVSD_81 V59 RSVD
AC22 VCCST
AE22 VCCST
+1.05V_VCCST AE23 VCCST
AB57 VCC
AD57 VCC
AG57 VCC
C24 VCC
C28 VCC
C32 VCC
+VCCIN VCC

HSW ULT POWER

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VCC C36
VCC C40
VCC C44
VCC C48
VCC C52
VCC C56
VCC E23
VCC E25
VCC E27
VCC E29
VCC E31
VCC E33
VCC E35
VCC E37
VCC E39
VCC E41
VCC E43
VCC E45
VCC E47
VCC E49
VCC E51
VCC E53
VCC E55
VCC E57
VCC F24
VCC F28
VCC F32
VCC F36
VCC F40
VCC F44
VCC F48
VCC F52
VCC F56
VCC G23
VCC G25
VCC G27
VCC G29
VCC G31
VCC G33
VCC G35
VCC G37
VCC G39
VCC G41
VCC G43
VCC G45
VCC G47
VCC G49
VCC G51
VCC G53
VCC G55
VCC G57
VCC H23
VCC J23
VCC K23
VCC K57
VCC L22
VCC M23
VCC M57
VCC P57
VCC U57
VCC W57

C521 *330u_2.5V_3528

+VCCIN 32A

+VCCIN
C236 22u/6.3V_8
C257 22u/6.3V_8
C269 22u/6.3V_8
C285 22u/6.3V_8
C267 22u/6.3V_8
C255 22u/6.3V_8
C238 22u/6.3V_8
C254 22u/6.3V_8
C252 22u/6.3V_8
C274 22u/6.3V_8
C235 22u/6.3V_8
C523 22u/6.3V_8
C282 22u/6.3V_8
C260 22u/6.3V_8
C262 22u/6.3V_8
C264 22u/6.3V_8
C265 22u/6.3V_8
C259 22u/6.3V_8
C237 22u/6.3V_8
C250 22u/6.3V_8
C245 22u/6.3V_8
C271 22u/6.3V_8
C253 22u/6.3V_8
C256 22u/6.3V_8
C242 *22u/6.3V_8
C247 *22u/6.3V_8
C248 *22u/6.3V_8
C243 *22u/6.3V_8
C266 *22u/6.3V_8
C268 *22u/6.3V_8

+1.05V R555 *0_8 +VCCIO_OUT
C528 *4.7u/6.3V_6

+1.05V_VCCST
R564 *10K_4
VRON_CPU R580 10K_4 IMVP_PWRGD

+1.05V +1.05V_VCCST
R235 *short_8
C240 *4.7u/6.3V_6

SVID

+VCCIO_OUT +1.05V_VCCST
R260 *130/F_4
R259 130/F_4
H_CPU_SVIDDAT R258 *short_4 VR_SVID_DATA [34]

Layout note: need routing together and ALERT need between CLK and DATA.

Place PU resistor close to CPU

+1.05V_VCCST +VCCIO_OUT
R265 75_4
R266 *75_4
Place PU resistor close to CPU
H_CPU_SVIDART# R263 43_4 VR_SVID_ALERT# [34]
H_CPU_SVIDCLK R268 *short_4 VR_SVID_CLK [34]

HWPG_1.05V for DDR=1.5V

10/30 reserve
DDR=1.5V ,This block POP

+1.05V R556 *4.7K_4
+3V R558 *4.7K_4
+3V R559 *4.7K_4
HWPG_1.05V [29]
R557 *100K/F_4
C535 *1000p/50V_4
Q38 *MMBT3904-7-F
C534 *1000p/50V_4
Q40 *DTC144EU

VCCST PWRGD

+1.05V_VCCST
R587 10K_4
VCCST_PWRGD R588 *short_4 VCCST_PWRGD_R_4
C558 *0.1u/10V_4
+3V_S5
C573 0.1u/10V_4
U37
VCC NC A Y GND
74AUP1G07GW
VCCST_PWRGD_EN
R612 *0_4
R613 *0_4
R604 *short_4
HWPG_1.05V_S5 [13,29,33]
APWORK [7,29]
PCH_PWROK [7,29]

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	Haswell 4/5 (POWER)	1B
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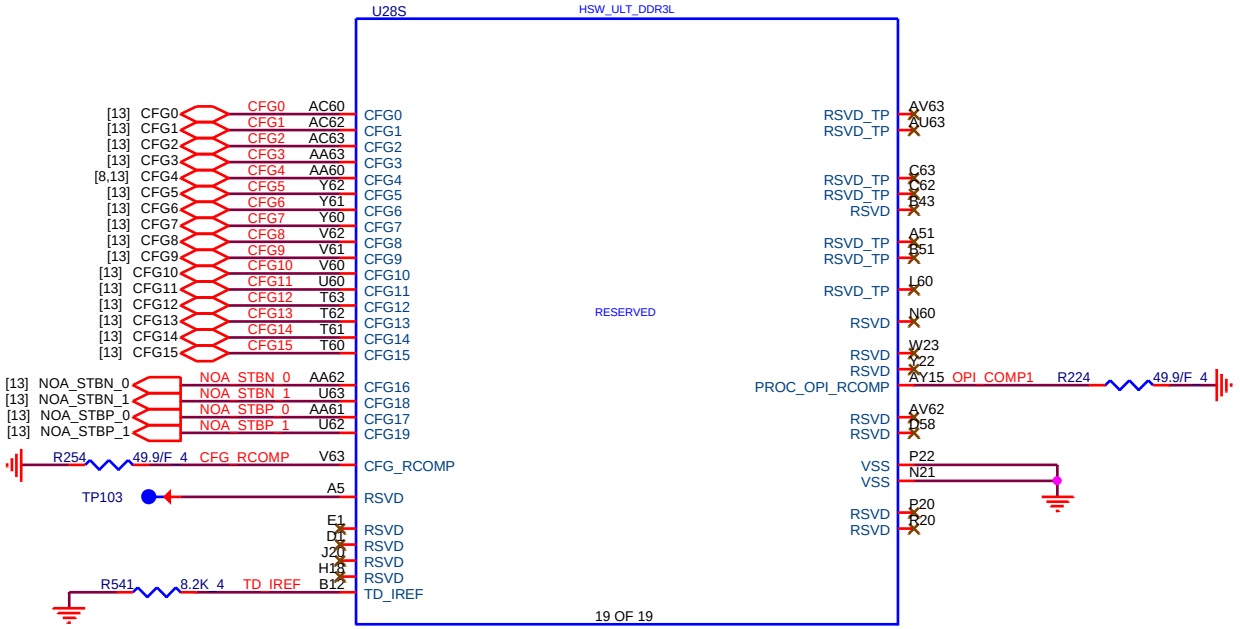
Haswell ULT (CFG,RSVD)

06



Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	**(DEFAULT) NORMAL OPERATION; NO STALL**	STALL	CFG0 R270 *1K_4
CFG1 PCH/ PCH LESS MODE SELECTION	**(DEFAULT) NORMAL OPERATION**	PCH-LESS MODE	CFG1 R264 *1K_4
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	**DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT**	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG3 R561 *1K_4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	**DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS**	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R577 *1K_4
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	**VRS SUPPORTING SVID PROTOCOL ARE PRESENT**	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R560 *1K_4
CFG10 SAFE MODE BOOT	**POWER FEATURES ACTIVATED DURING RESET**	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R308 *1K_4

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Size	Document Number	Rev
	Haswell 5/5 (CFG/GND)	1B

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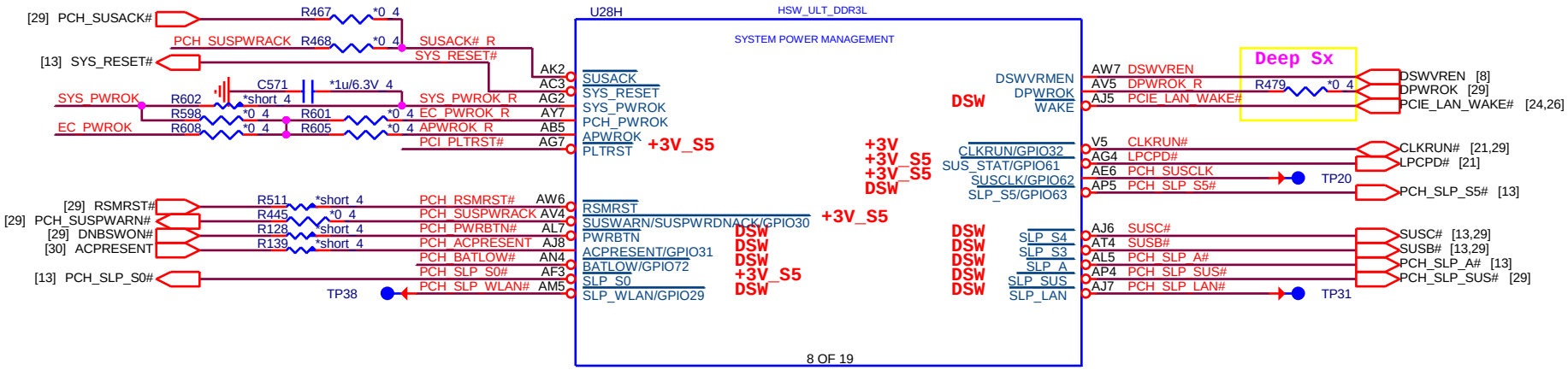
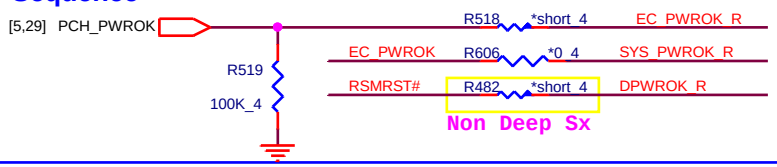
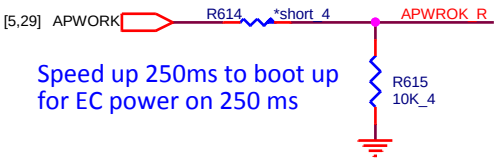
Haswell ULT PCH (PM)

07

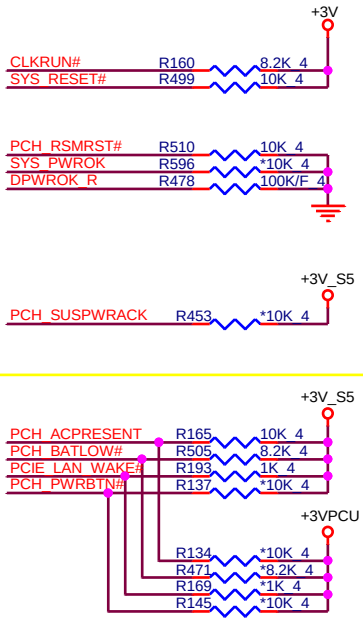


Power Sequence

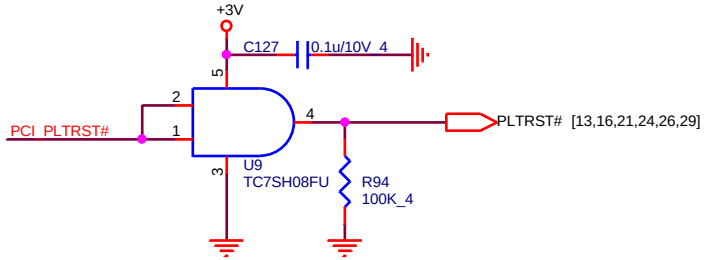




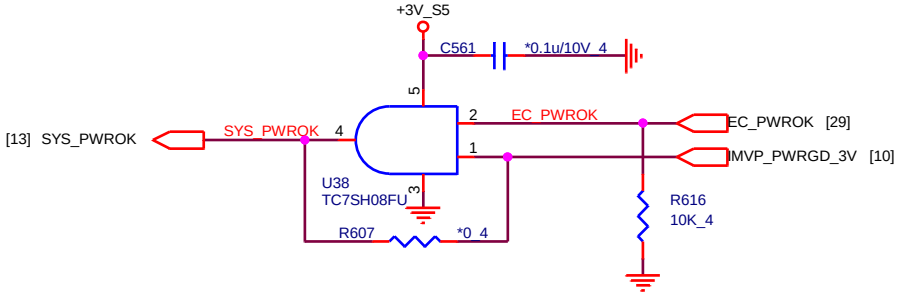
PCH PM PU/PD



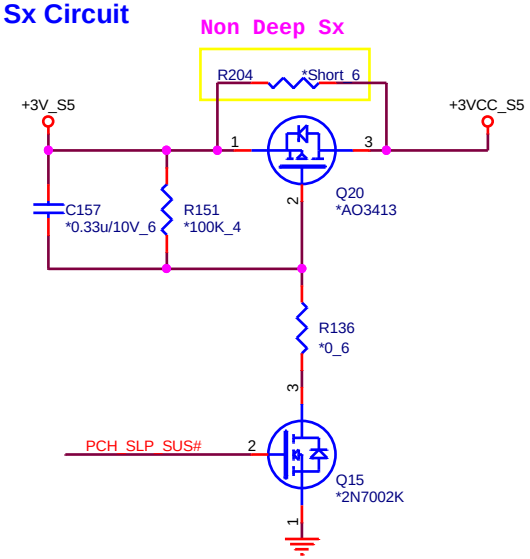
PLTRST# Buffer



SYSPWOK



Deep Sx Circuit



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Size	Document Number	Rev
	LPT 1/6 (DMI/FDI/VGA)	1B
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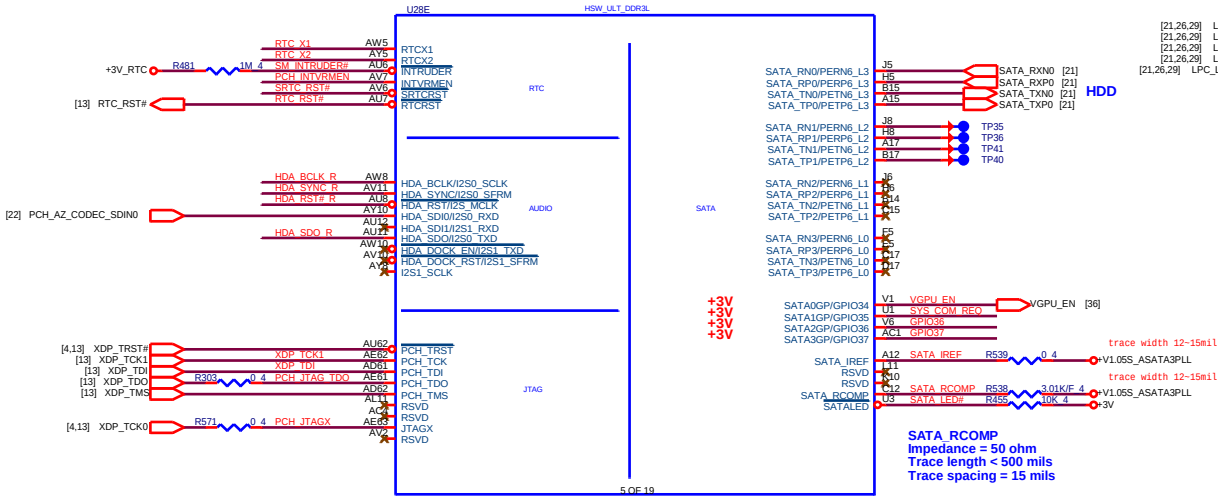
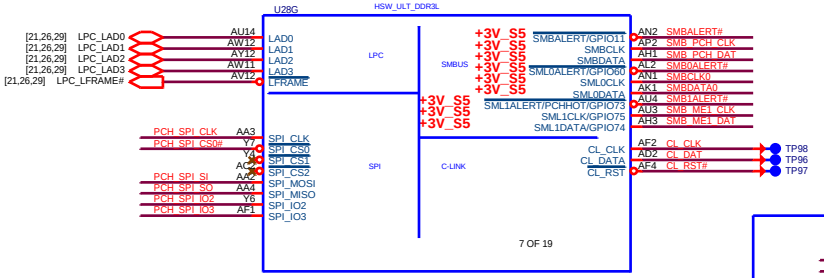
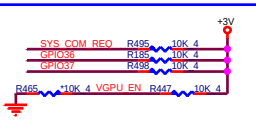
Haswell ULT PCH (RTC/HDA/SATA/SPI)

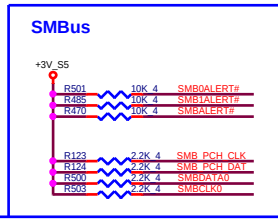
Haswell ULT PCH(LPC,SPI,SMBUS,C-LINK,THERMAL)

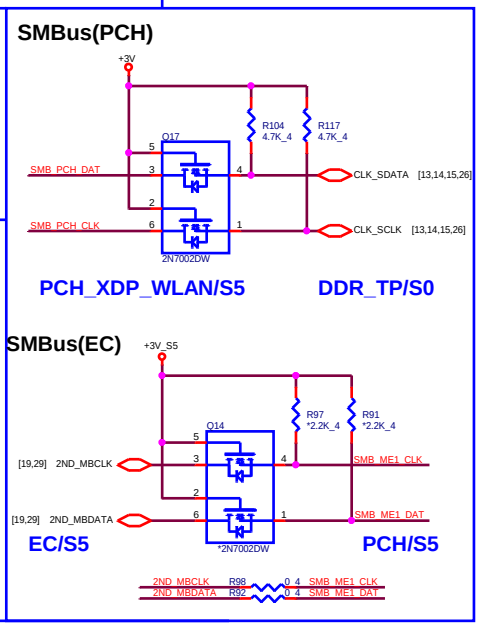
08

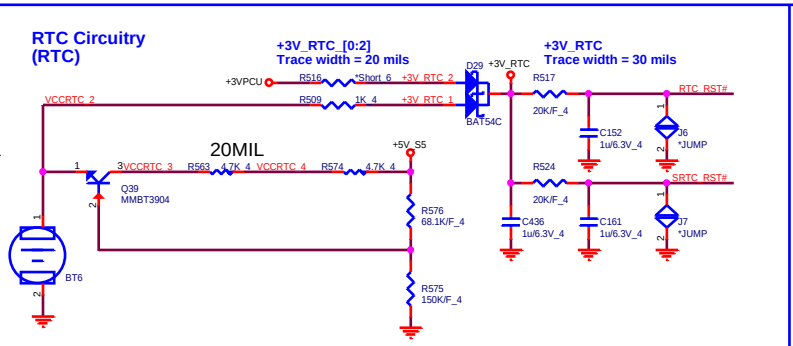


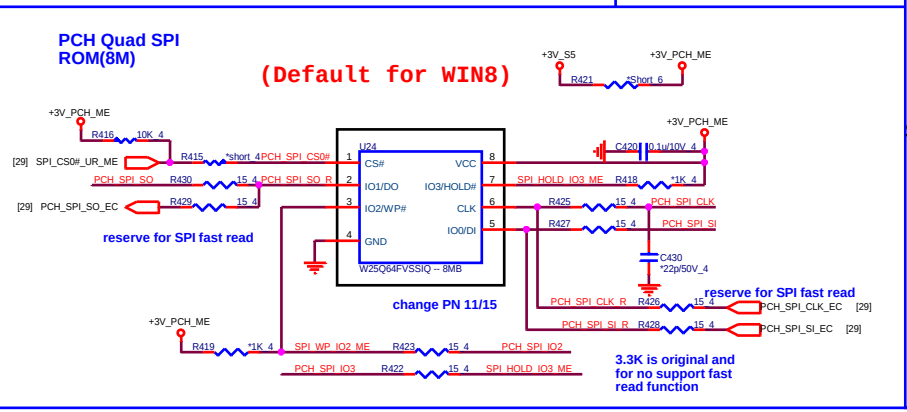


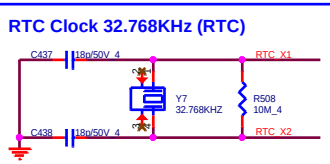


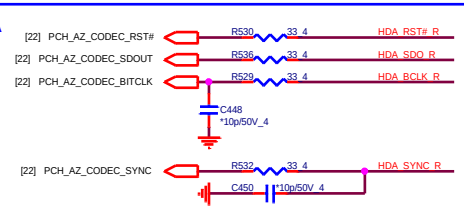


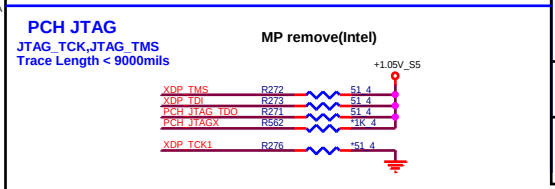






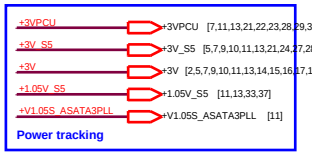






ULT Strapping Table

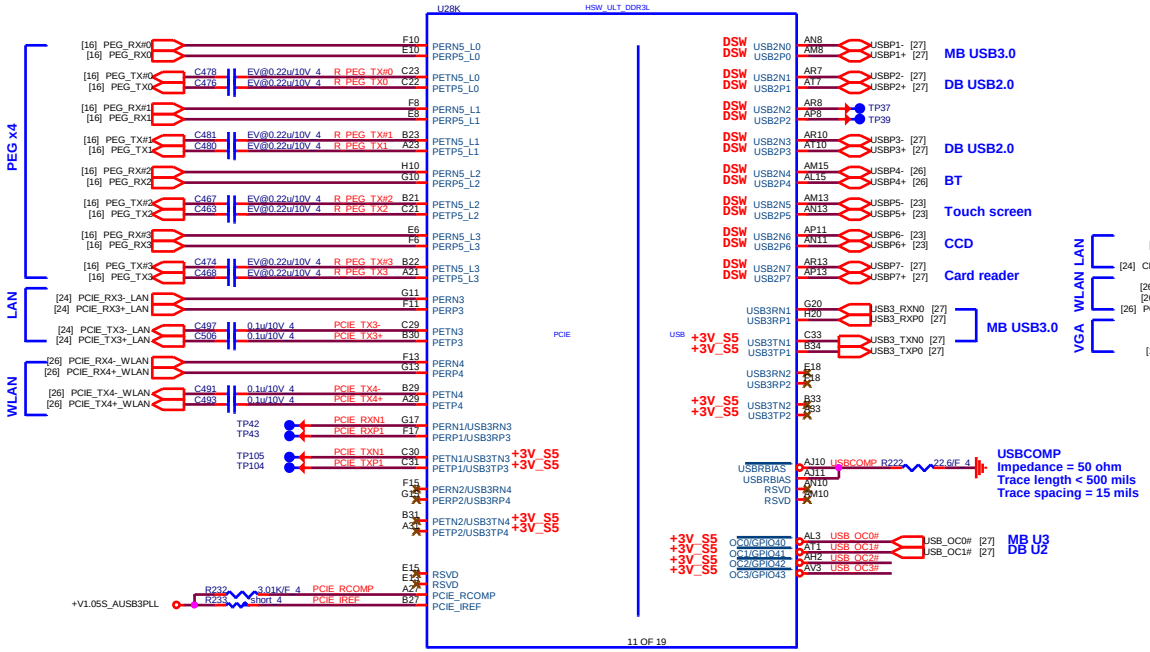
Pin Name	Strap description	Sampled	Configuration	note
GPIO81(SPKR)	No reboot on TCO Timer expiration	PWROK	0 = Default enable (iPD 20K) 1 =Disable No-Reboot mode	
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Default can program ME (iPD 20K) 1 =can't program ME	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	1=Should be always pull-up	
GPIO66	Top-Block Swap override		0 = Default disable (iPD 20K) 1 = Enable TBS function	
GPIO86	Boot BIOS Strap Bit		0 = Default SPI (iPD 20K) 1 =LPC	
GPIO15	TLS(Transport layer security)		0 = Default enable w/o confidentiality(iPD 20K) 1 =Default enable with confidentiality	
CFG4	DP presence strap		0 = Enable an external display port is connected to the eDP 1 =disable	
DSWVREN	Deep Sx well on die VR enable		1=Should be always pull-up	



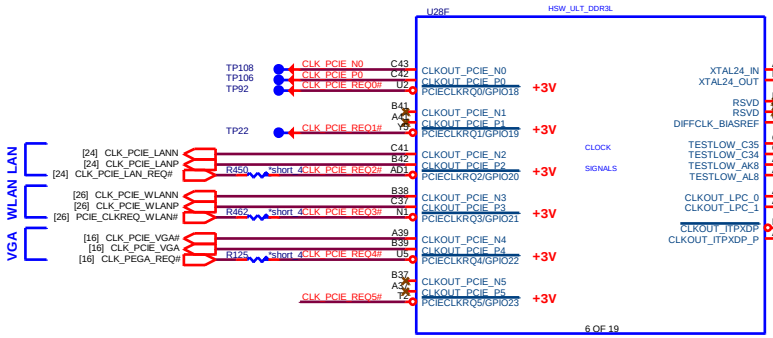
Quanta Computer Inc.
PROJECT : ZQX

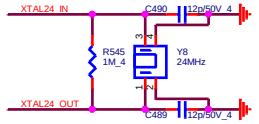
Size	Document Number	Rev
	LPT 2/6 (SATA/HDA/SPI)	1B
Date: Wednesday, September 03, 2014	Sheet 8 of 43	

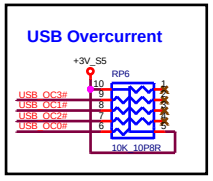
Haswell ULT PCH (PCIE,USB3.0,USB2.0)



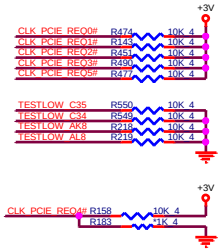
Haswell ULT PCH (CLOCK)

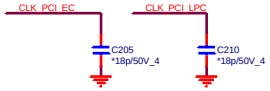


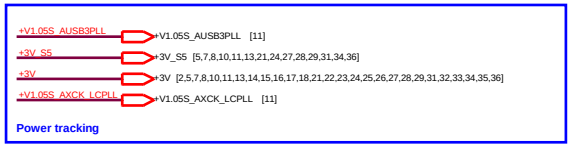




Swap for layou 11/14





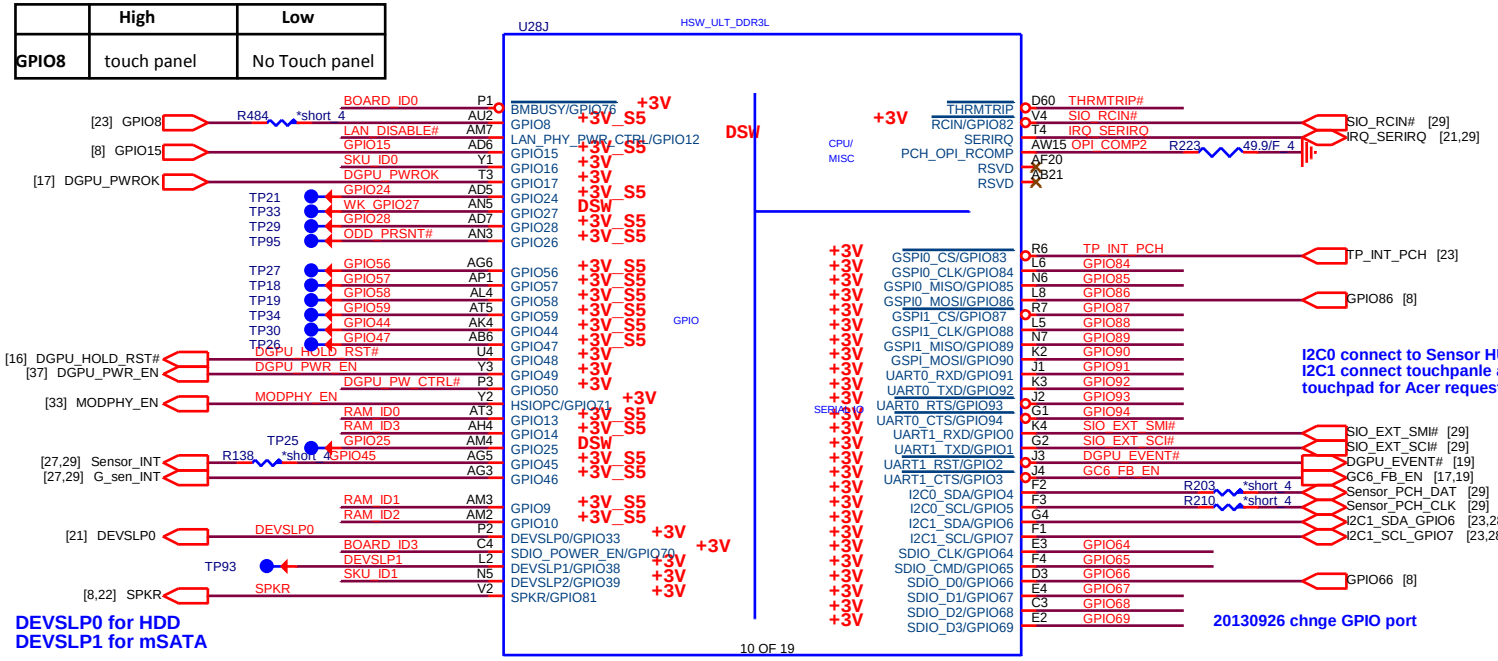


09

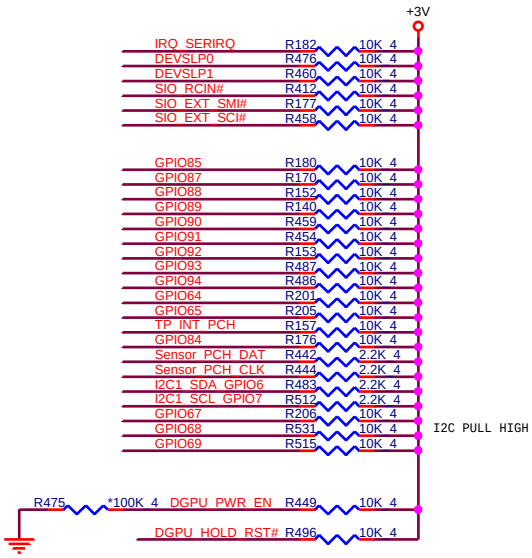
Quanta Computer Inc.			
PROJECT : ZQX			
Size	Document Number: LPT 3/6 (PCIE/USB/CLK)		Rev: 1B
Date: Wednesday, September 03, 2014	Sheet 9	of 43	

Haswell ULT PCH (GPIO,CPU/MISC,NCTF)

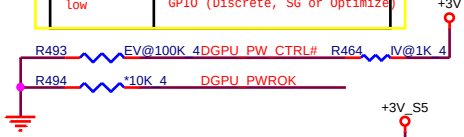
	High	Low
GPIO8	touch panel	No Touch panel

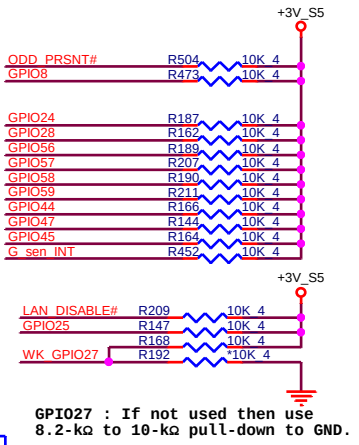


PCH GPIO PU/PD

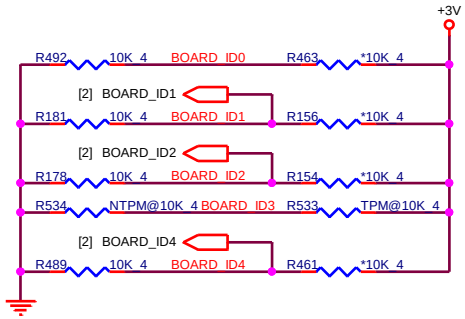


high	UMA Only
low	GPU power is control by PCH GPIO (Discrete, SG or Optimize)



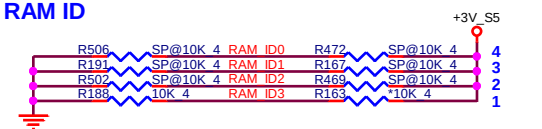


Board ID



	Low	High
BOARD_ID0	Reserved (Default)	Reserved
BOARD_ID1	Enable on board memory	Disable on board memory
BOARD_ID2	Default(LOW)	
BOARD_ID3	No DTPM	DTPM
BOARD_ID4	Reserved (Default)	Reserved

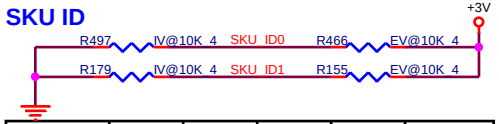
RAM ID



Vender	RAM_ID	Q PN	Mfr. PN	Freq.
Hynix	0000	AKD5JGETW04	H5TC4G63AFR-PRBA(A)	1600MHz
	0001			
Elpida	0010	AKD5JGST407	EDJ4216EFBG-GN-LF	1600MHz
Hynix	0011	AKD5PGSTW03	H5TC4G63MFR-PBA(M)	1600MHz
MICRON	0100	AKD5JGSTL08	MT41K256M16HA-125	1600MHz
Kingston	0101			

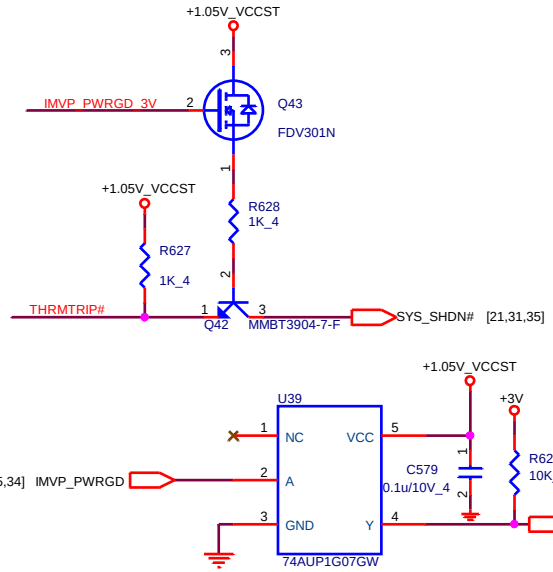
1234

SKU ID



	SKU_ID1	SKU_ID0	VGA H/W Signal	Setup Menu	
UMA Only	0	0	UMA	Hidden	UMA boot
dGPU Only	0	1	GPU	Hidden	GPU boot
Switchable (Mux)	1	0	UMA+GPU	dGPU/SG	UMA boot
Optimize (Muxless)	1	1	UMA	UMA/SG	UMA boot

CPU thermal trip

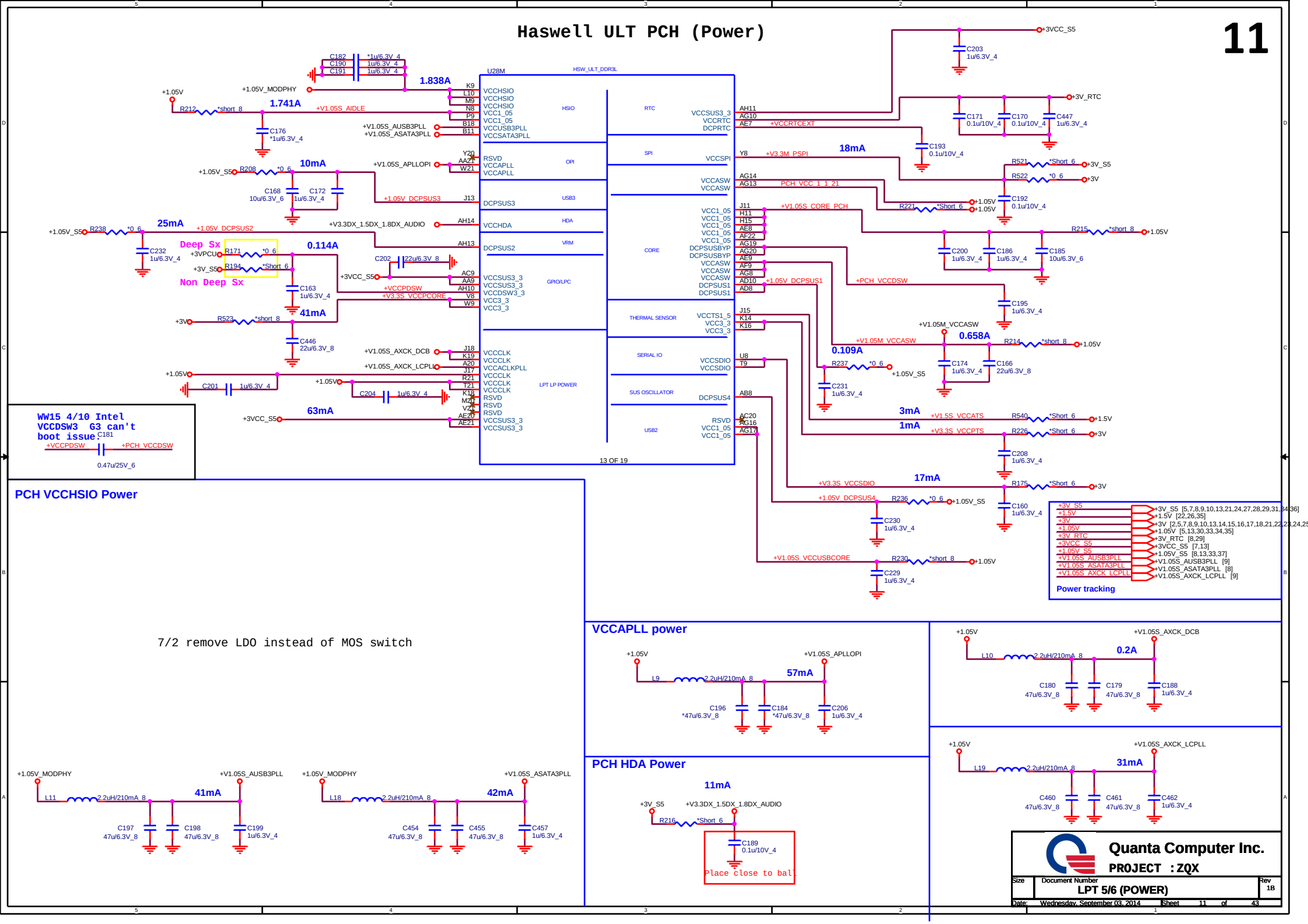


Quanta Computer Inc.
PROJECT : ZQX

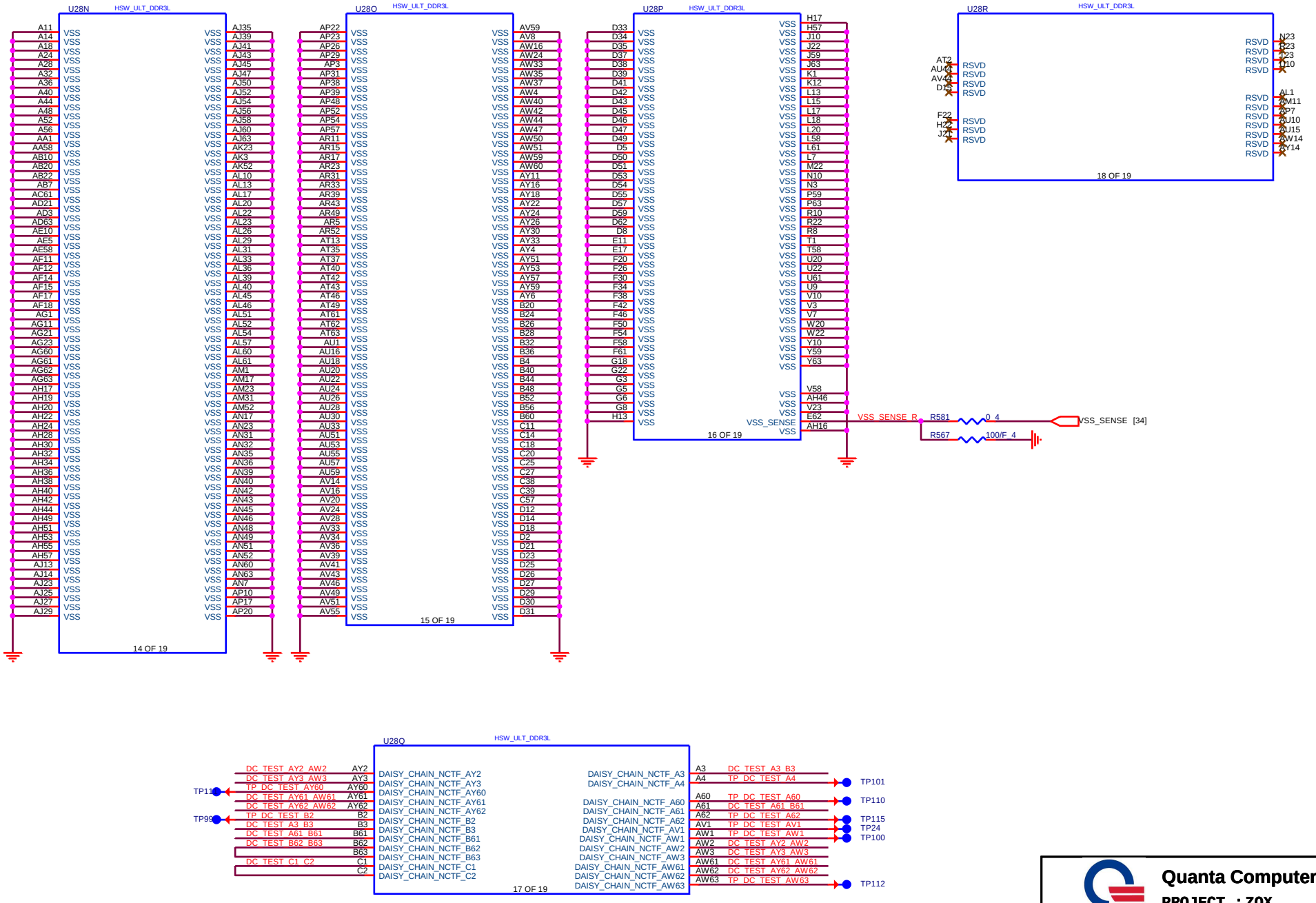
Size	Document Number	Rev
	LPT 4/6 (GPIO/MISC)	1B

Date: Wednesday, September 03, 2014 Sheet 10 of 43

Haswell ULT PCH (Power)



Haswell ULT (GND)

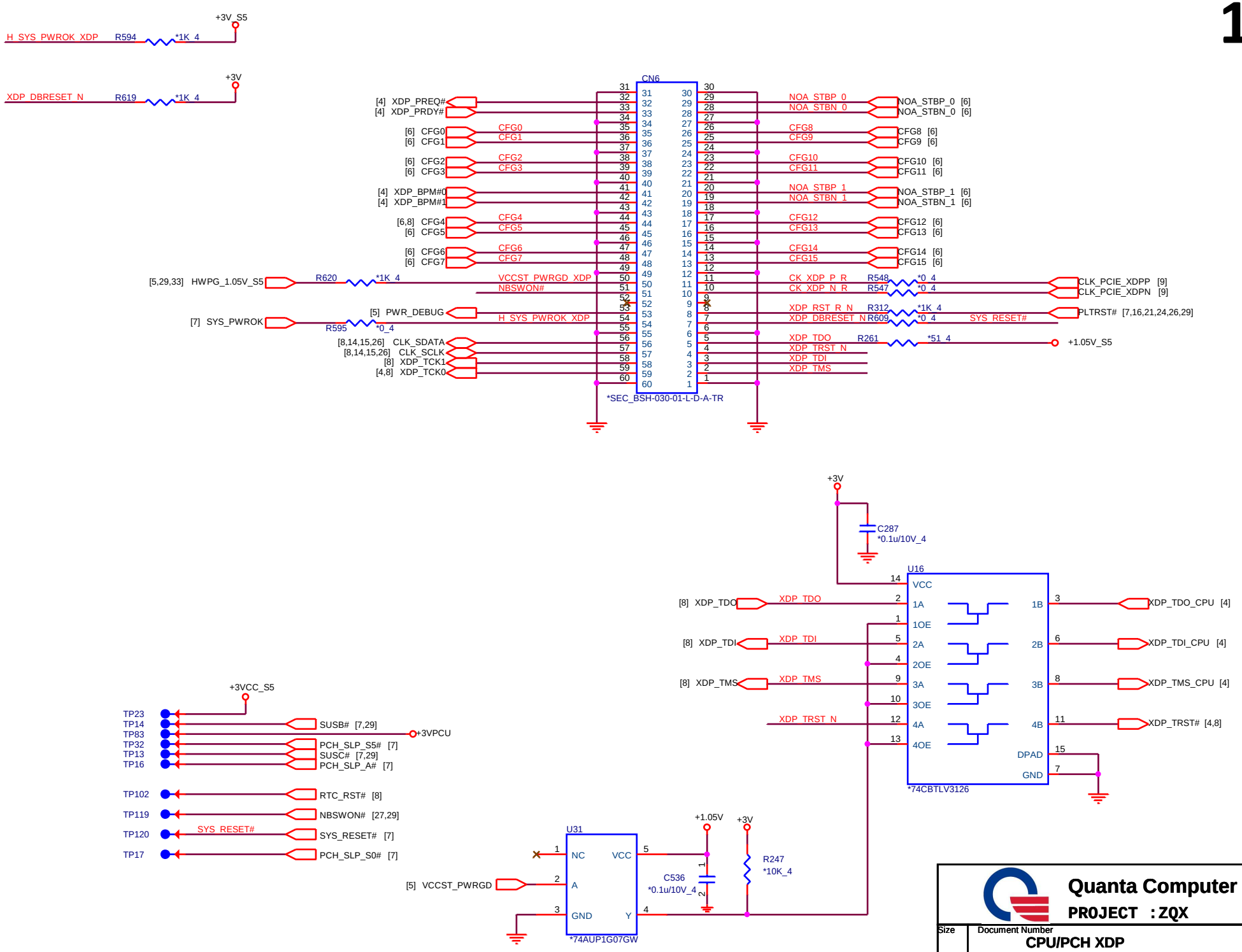


Quanta Computer Inc.

PROJECT : ZQX

Size	Document Number	Rev
	LPT 6/6 (GND)	1B

Date: Wednesday, September 03, 2014 Sheet 12 of 43



Quanta Computer Inc.

PROJECT : ZQX

Size	Document Number	Rev
	CPU/PCH XDP	1B

Date: Wednesday, September 03, 2014 Sheet 13 of 43

BYTE0_0-7
BYTE1_8-15
BYTE2_16-23
BYTE3_24-31
BYTE5_40-47
BYTE4_32-39
BYTE7_56-63
BYTE6_48-55

SO-DIMMB SPD Address is 0XA4
SO-DIMMB TS Address is 0X34

Vendor	P/N	
Hynix		
Elpida	AKD5JGST400	DDR3L 1333Mhz 4Gb
	AKD5JGST404	DDR3L 1600Mhz 4Gb

SP : ELPIDA DRAM P/N : AKD5JGST400
HYNIX DRAM P/N : AKD5JGQTW01

Power tracking

Place these Caps near Memory Down

Place these Caps near Memory Down CA & DQ pin

M1 solution

Vref_CA

M3 solution

Vref_DQ

Change to 36 ohm

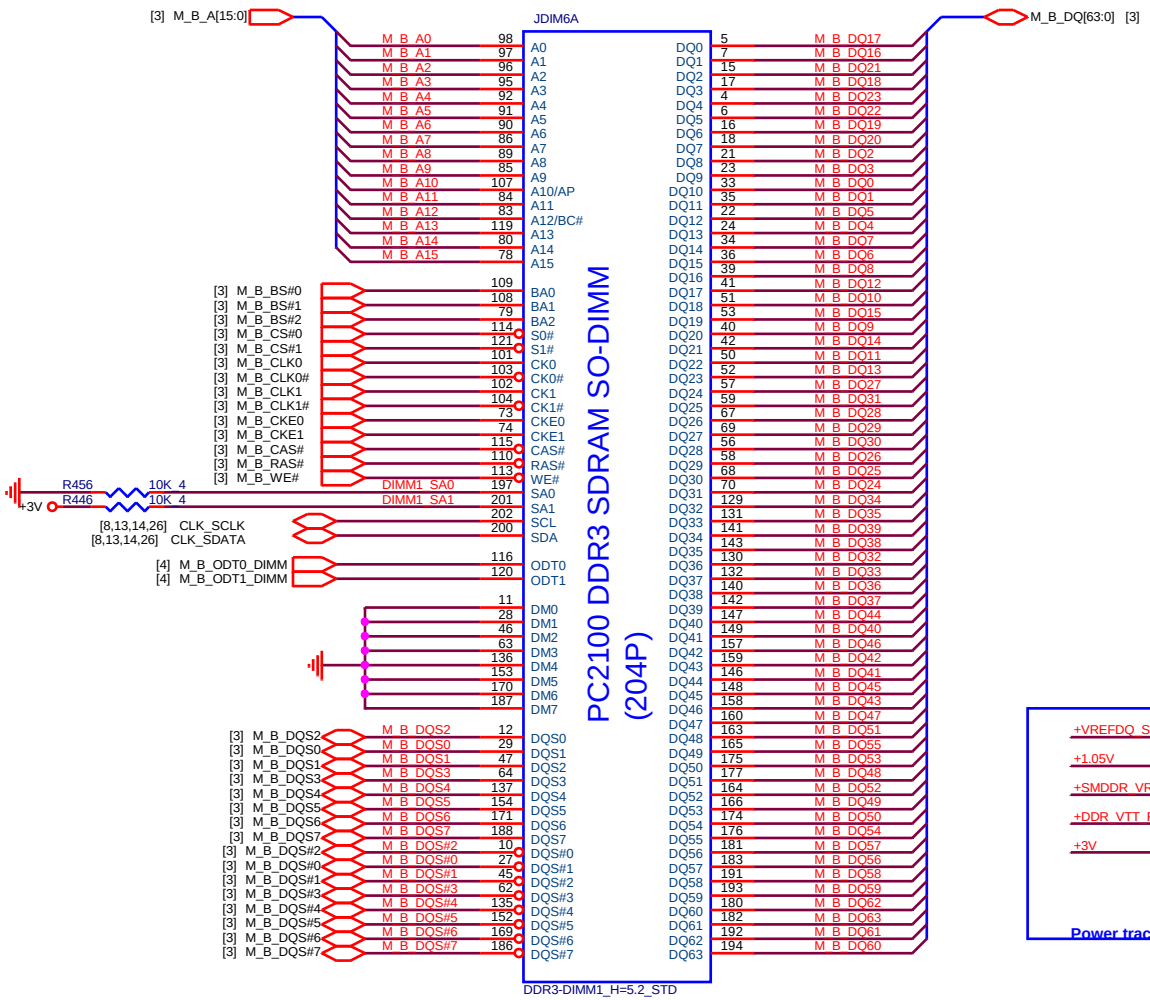
WP =1 : WRITE DISABLE

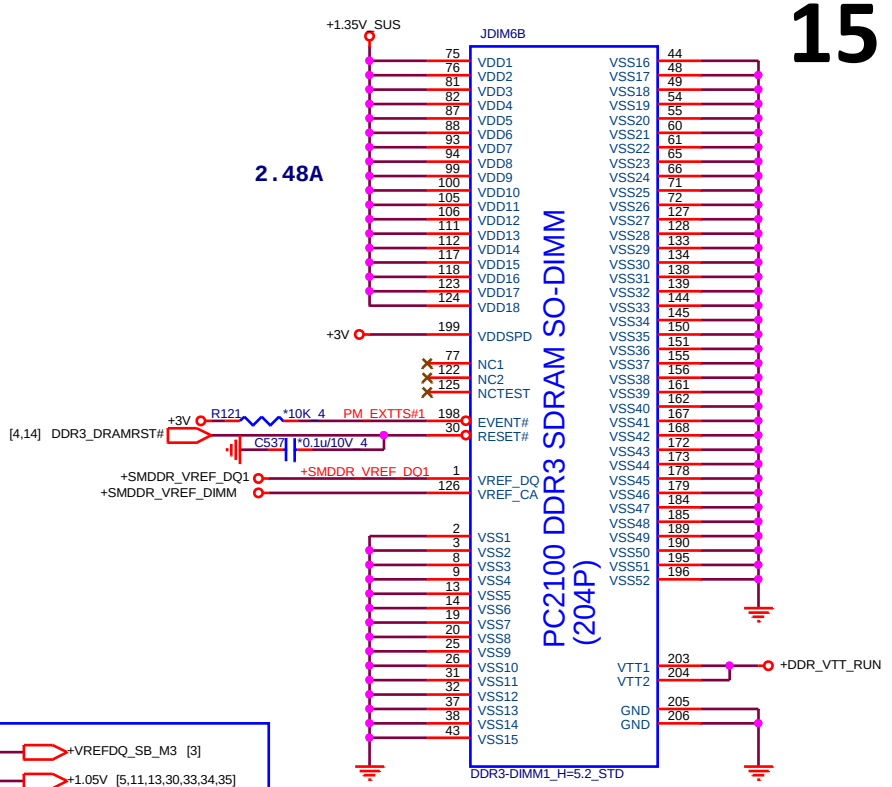
SPD address:A2

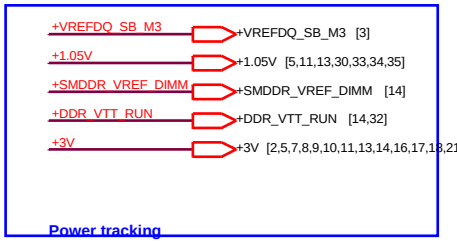
Modify connection on 10/25

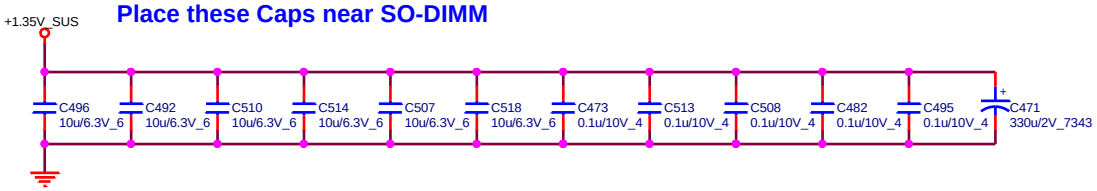
change to 3.3p 10/28

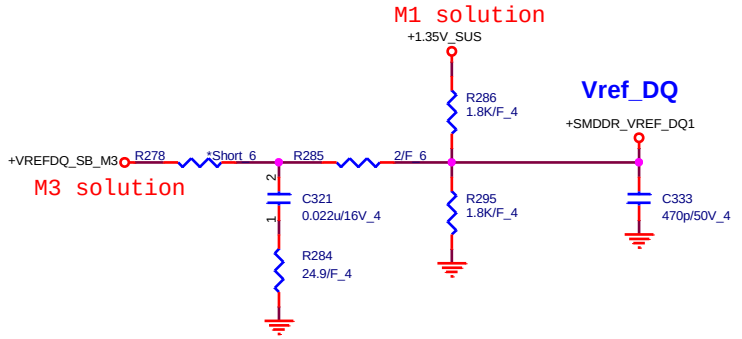
Quanta Computer Inc.
PROJECT : ZQX
DDR3 MEMORY DOWNx16 A

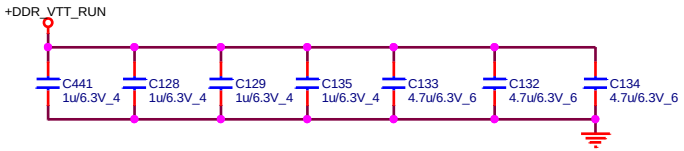


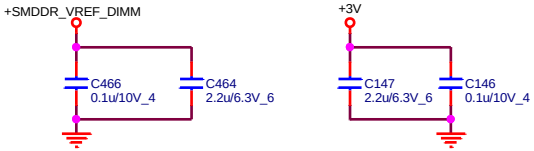












Quanta Computer Inc.
PROJECT : ZQX

Size	Document Number	Rev
	DDRIII SO-DIMM-1	1B
Date: Wednesday, September 03, 2014	Sheet 15 of 43	

PEX_IOVDD + PEX_IOVDDQ = 1.042A

PEX_PLL_HVDD +
PEX_SVDD_3V3 = 143mA

PEX_PLLVDD = 130mA

VDD33 = 56mA

8mils width
(0.2MM)

Follow Z09 to isolate CLK_REQ#

Un-stuff Sys_PEX_RST_MON# , stuff PEGX_RST# for not GC6
stuff Sys_PEX_RST_MON# for GC6

NVDD = 32.22 ~ 26.66 A

VDD33
+3V_GFX/
+3V_MAIN

NVDD
+VGPU_CORE

PXE_VDD
+1.05V_GFX

FBVDDQ
+1.35_GFX

N15x Power on sequance

Power down sequence

First Rail to Power Down

Last Rail to Power Down

Quanta Computer Inc.			
PROJECT : ZQX			
Size	Document Number	N14M-GS (PCIE I/F) /NVDD	Rev 1B
Date: Wednesday, September 03, 2014		Sheet 16 of 43	

EC_FB_CLAMP R50 *0_4
R43 EV@10K/F_4 FB_CLAMP F3
For GC6 2.0 and 1.0
no stuff GC6_FB_EN

PV modify
FBA_ODT_L FBA_CMD2 R45 EV@10K/F_4
FBA_ODT_H FBA_CMD18 R385 EV@10K/F_4
FBA_RST# FBA_CMD5 R56 EV@10K/F_4
FBA_CKE_L FBA_CMD3 R41 EV@10K/F_4
FBA_CKE_H FBA_CMD19 R82 EV@10K/F_4

U20B
NC GF119
FB_CLAMP GF117
2/14 FBA

TP78 FBA_CMD1
TP11 FBA_CMD17
TP79 FBA_CMD31

+1.5V_GFX
R53 *60.4_4 F22 FBA_DEBUG0
R58 *60.4_4 J22 FBA_DEBUG1

[20] VMA_CLK0 D24 FBA_CLK0
[20] VMA_CLK0# D25 FBA_CLK0
[20] VMA_CLK1 N22 FBA_CLK1
[20] VMA_CLK1# M22 FBA_CLK1

D18 FBA_WCK01
C18 FBA_WCK01
D17 FBA_WCK23
D16 FBA_WCK23
T24 FBA_WCK45
U24 FBA_WCK45
V24 FBA_WCK67
V25 FBA_WCK67

+1.05V_GFX
FB_PLLAVDD = 55mA
L8 EV@BLM15PX331SN1D +FB_PLLAVDD F16 FB_PLLAVDD
P22 FB_PLLAVDD
H22
C69 EV@22U/6.3VS_6
C64 EV@0.1U/10V_4
C22 EV@0.1U/10V_4
C34 EV@0.1U/10V_4
FB_DLLAVDD = 15mA

FB_DLLAVDD GF119
FB_PLLAVDD GF117
INT
ESP@N14P-GV2

FB_VREF_PROBE D23

VMA_DQ[63:0] VMA_DQ[63:0] [20]

FBVDDQ + FBVDD = 3.116A

+1.5V_GFX
C29 EV@0.1U/10V_4
C52 EV@0.1U/10V_4
C48 EV@1U/10V_6
C54 EV@1U/10V_6
C35 EV@4.7U/6.3V_6
C93 EV@10U/6.3V_6
C83 EV@22U/6.3VS_6
C36 EV@4.7U/6.3V_6

U20D
12/14 FBVDDQ
ESP@N14P-GV2

FB_CAL_PD_VDDQ D22 FB_CAL_PD_VDDQ R44 EV@40.2/F_4
FB_CAL_PU_GND C24 FB_CAL_PU_GND R32 EV@42.2/F_4
FB_CALTERM_GND B25 FB_CALTERM_GND R29 EV@51.1/F_4
+1.5V_GFX

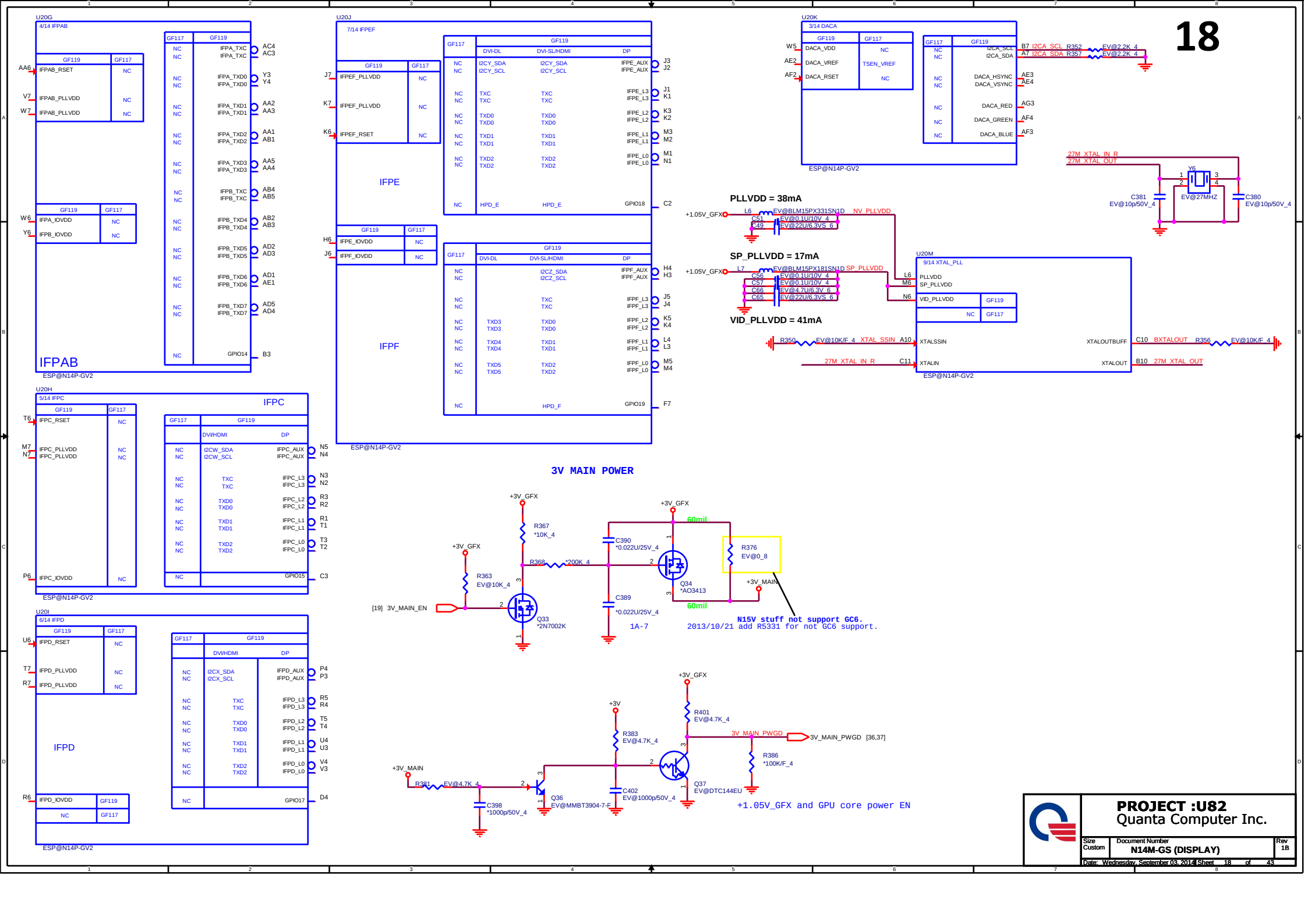
U20F
13/14 GND
ESP@N14P-GV2

VMA_DM[7:0] [20]
VMA_WDQS[7:0] [20]
VMA_RDQS[7:0] [20]

[37] HWPG_1.5VGFX R364 EV@4.7K_4 DGPU_POK4
Q32 EV@METR3904-G
C383 *1000P/50V_4
DGPU_PGOK-1
+3V
R347 EV@4.7K_4
C378 EV@1000P/50V_4
Q31 EV@DTC144EUA
R349 EV@100K/F_4
+3V_GFX
R358 EV@4.7K_4
DGPU_PWROK [10]

+3V
C377 EV@0.1U/10V_4
C375 *0.1u/10V_4
GPU_PWR_GD ,PD at GPU power side
[36] GPU_PWR_GD R337 EV@0_4
[10,19] GC6_FB_EN R348 EV@0_4
[19,29] EC_FB_CLAMP R342 *0_4
U19 EV@SN74AHC1G32DCKR
R346 EV@100K/F_4
FBVDDQ_EN [37]
stuff EC_FB_CLAMP for not GC6
stuff GC6_FB_EN for GC6
For support GC6

PROJECT :U82
Quanta Computer Inc.
Size Custom | Document Number N14M-GS (MEMORY/GND) | Rev 1B
Date: Wednesday, September 03, 2014 | Sheet 17 of 43



PROJECT	U82
Company	Quanta Computer Inc.
Size	Custom
Document Number	N14M-GS (DISPLAY)
Rev	1B
Date	Wednesday, September 03, 2014
Sheet	18 of 43

For N15S-GT sku
N15S-GT device ID=0x0FE4
R3=40.3k pull down.
1.ROM_SCLK =4.99K pull down
2.ROM_SO = 4.99K pull down
3.ROM_SI= Memory strap setting
3.STRAP0 = 50k Pull pu.
4.Strap4~1 = reserve Pull pu and Pull down

For N15V-GL-B and N15V-GM-B sku
Board_ID0=
H=N15V-GM,L=N15V-GL
Device ID=0x1140
R3= N.C.
1.ROM_SCLK =10K pull down.
2.ROM_SI= 10k pull down
3.ROM_SO= 10k pull down
4.Strap3~0 = RVL memory binary mode setting.
5.Strap4 =10k pull down

U20L
10/14 MISC2
ESP@N14P-GV2

R3

N15S Based on RVL.
N15V pull down10k.

Pull Down 4.99k for N15S-GT.
Pull Down 10k for N15V.

N15S-GT
STRAP1---> 50k PU
N15V-GM\GL
STRAP4---> 10k PD

Default: HYNIX

N15S Strap0 pull up 50k, strap1~4 reverve only.
N15V Strap4 pull down 10k, strap0~3 based on RVL binary setting.

Logical Strap Bit Mapping

	PU-VDD	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

U20N
8/14 MISC1
ESP@N14P-GV2

EC/S5
VGA/VGA
EV@2N7002DW

N15S -> GPIO0 un-stuff Q24 and EC_FB_CLAMP.
GPIO6 Unstuff Q26\R70 and FB_CLAMP_REQ#.

VRAM Configuration Table

ROM_SI	DESCRIPTION	Vendor	Vendor P/N	QCI P/N	STN P/N
0000	DDR3(L) 256MBx16x4, 64bit,1000MHz(	HYNIX	H5TC4G63AFR-11C	AKD5PGWTW05	AKD5PGWTW13
0010(0101)	DDR3(L) 256MBx16x4, 64bit,,1000MHz(900MHz)	SAMSUNG	K4W4G1646D-BC1A		
0110(1001)	DDR3(L) 128MBx16x4, 64bit,1000MHz(900MHz)	HYNIX	H5TC2G63FFR-11C		
0111(1010)	DDR3(L) 128MBx16x4, 64bit,1000MHz(900MHz)	MICRO	MT41J128M16JT-093G:K		
1000(1011)	DDR3(L) 128MBx16x4, 64bit,,1000MHz(900MHz)	SAMSUNG	K4W2G1646Q-BC1A		
0001(0100)	DDR3(L) 128MBx16x4, 64bit,1000MHz(900MHz)	MICRO	MT41J256M16HA-093G:E		

Strap [3:0]	DESCRIPTION	Vendor	Vendor P/N	QCI P/N		Note
0100	DDR3(L) 256MBx16x4, 64bit,1000MHz(900MHz)	HYNIX	H5TC4G63AFR-11C			
1100	DDR3(L) 128MBx16x4, 64bit,1000MHz(900MHz)	HYNIX	H5TC2G63FFR-11C			
0001	DDR3(L) 128MBx16x4, 64bit,1000MHz(900MHz)	MICRO	MT41J128M16JT-093G:K			
1101	DDR3(L) 128MBx16x4, 64bit,1000MHz(900MHz)	MICRO	MT41J256M16HA-093G:E			

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM VREF_CTL	MEMMORY VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

GPIO ASSIGNMENTS

dGPU_OPP# = EC control
GPIO12 AC detect
AC high
DC low

PROJECT :U82
Quanta Computer Inc.
Size: Custom
Document Number: N14M-GS (GPIO/STRAPS)
Rev: 1B
Date: Wednesday, September 03, 2014 Sheet 19 of 43

CHANNEL A: 256MB/512MB DDR3

HYU 256Mx16, PN : AKD5PGWTW08---AKD5PGWTW07
HYU 128Mx16, PN : AKD5MZDTW03---AKD5MZDTW02
QBC TOP B/S
SAM 256Mx16, PN : AKD5PZDT501---AKD5PZDT500
SAM 128Mx16, PN : AKD5MGGT535---AKD5MGGT534

[17] VMA_DQ[63..0]
[17] VMA_DM[7..0]
[17] VMA_WDQS[7..0]
[17] VMA_RDQS[7..0]

VRAM6 — ESP@VRAM _DDR3_HYNIX_256MX16
VRAM8 — ESP@VRAM _DDR3_HYNIX_256MX16
VRAM7 — ESP@VRAM _DDR3_HYNIX_256MX16
VRAM9 — ESP@VRAM _DDR3_HYNIX_256MX16

Should be 240 Ohms +-1% — R55 EV@243/F_4
Should be 240 Ohms +-1% — R365 EV@243/F_4
Should be 240 Ohms +-1% — R79 EV@243/F_4
Should be 240 Ohms +-1% — R384 EV@243/F_4

R31 EV@162/F_4
R374 EV@1.33K/F_4
R372 EV@1.33K/F_4
C388 EV@0.1U/10V_4
R8 EV@1.33K/F_4
R13 EV@1.33K/F_4
C14 EV@0.1U/10V_4
R84 EV@162/F_4
R76 EV@1.33K/F_4
R73 EV@1.33K/F_4
C87 EV@0.1U/10V_4
R402 EV@1.33K/F_4
R387 EV@1.33K/F_4
C406 EV@0.1U/10V_4

C403 C30 C41 C27 EV@1U/6.3V_4
C379 C50 C401 C418 C384 C399 EV@1U/6.3V_4
C111 C397 C121 C53 C413 C68 C71 C400 EV@1U/6.3V_4
C109 C63 C387 C382 C385 C414 C78 EV@0.1U/10V_4
C396 C410 C120 C386 C108 EV@0.1U/10V_4

PROJECT :U82
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DGPU Memory (DDR3)	1B

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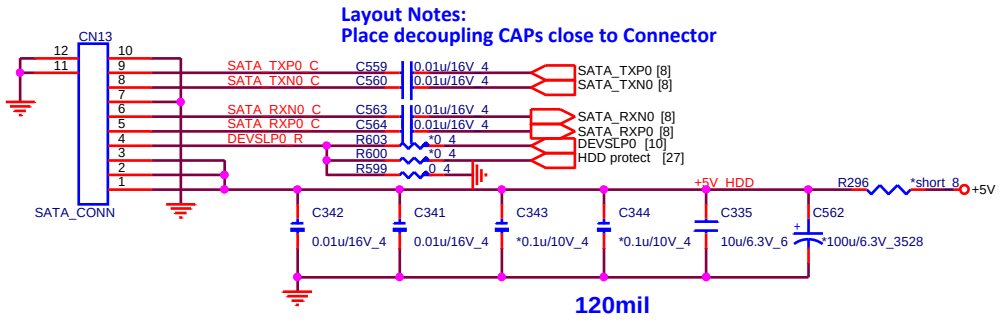
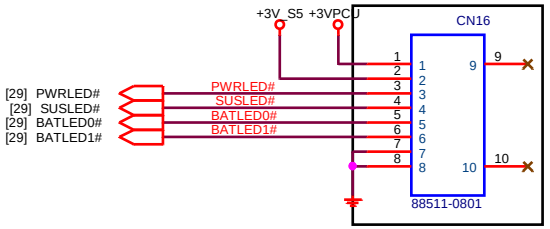
FFC SATA HDD



+3VPCU	+3VPCU [7,8,11,13,22,23,28,29,30,31,35,36,37]
+3V_S5	+3V_S5 [5,7,8,9,10,11,13,24,27,28,29,31,34,36]
+3V	+3V [2,5,7,8,9,10,11,13,14,15,16,17,18,22,23,24,25,26,27,28,29,31,32,33,34,35,36]
+5V	+5V [22,23,25,28,31,35]

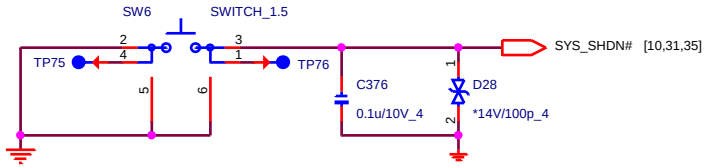
Power tracking

LED(UIF)

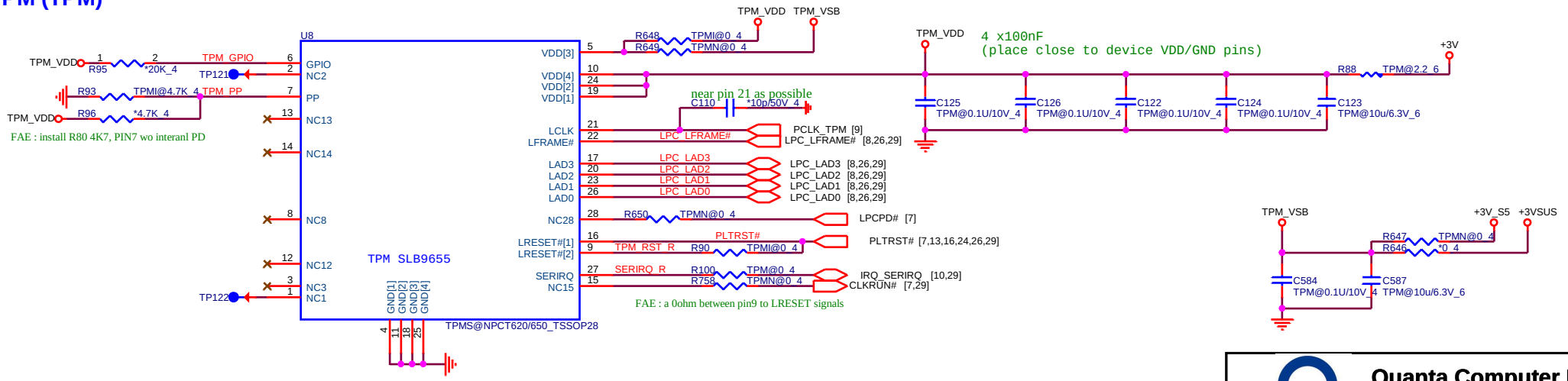


Change CN6 PN for ME request

3/5VPCU reset switch (CLG)



TPM (TPM)



Quanta Computer Inc.

PROJECT : ZQX

Size	Document Number	Rev
	SATA-HDD/ TPM	1B

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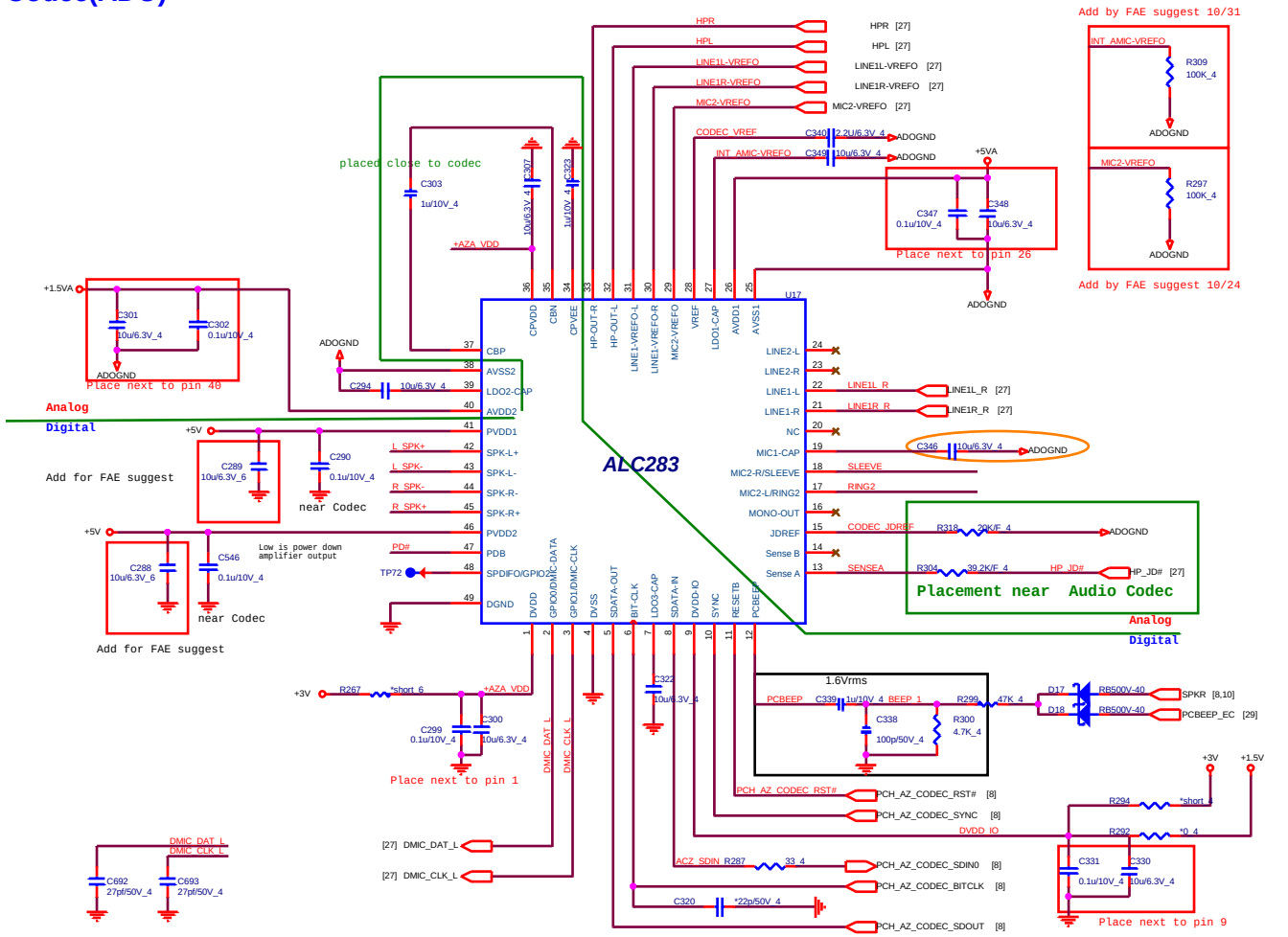
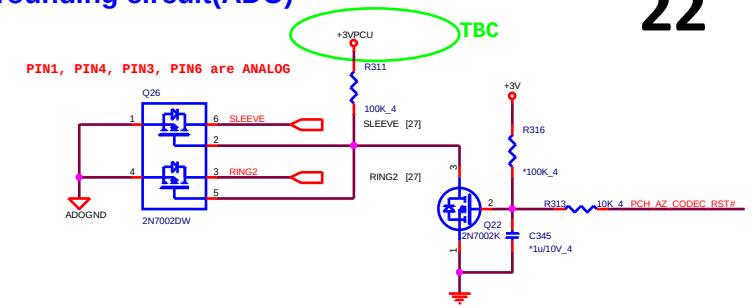
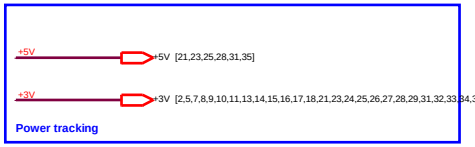
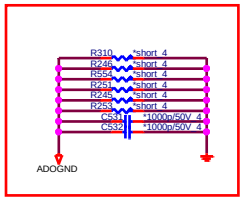
Codec(ADO)



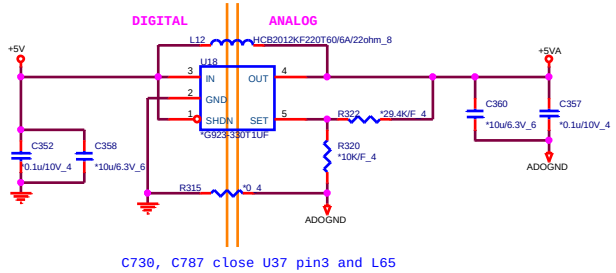
Grounding circuit(ADO)



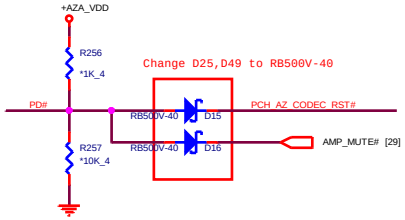




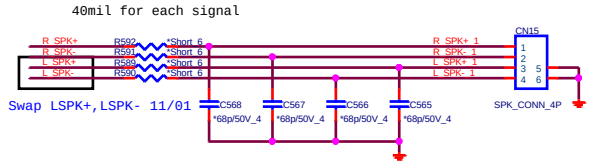
Codec PWR 5V(ADO)



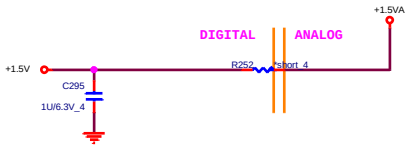
Mute(ADO)



Internal Speaker



Codec PWR 3V/1.5V(ADO)



Quanta Computer Inc. PROJECT : ZQX			
Size	Document Number ALC283/HP/SPK		Rev 1B
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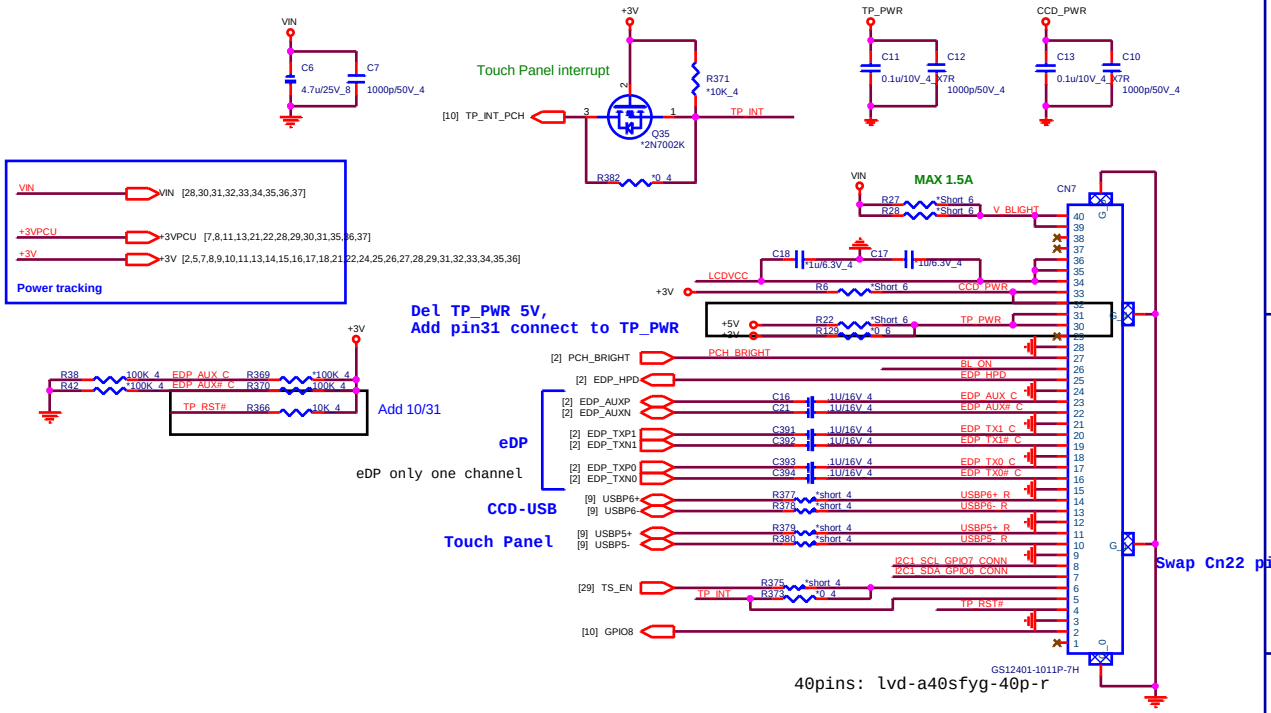
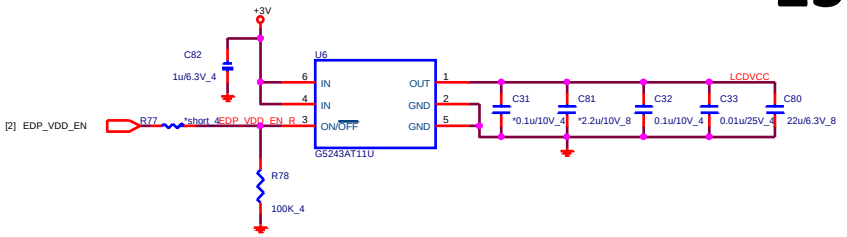
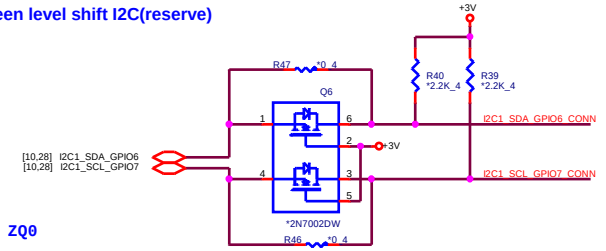
LCD CONNECTOR



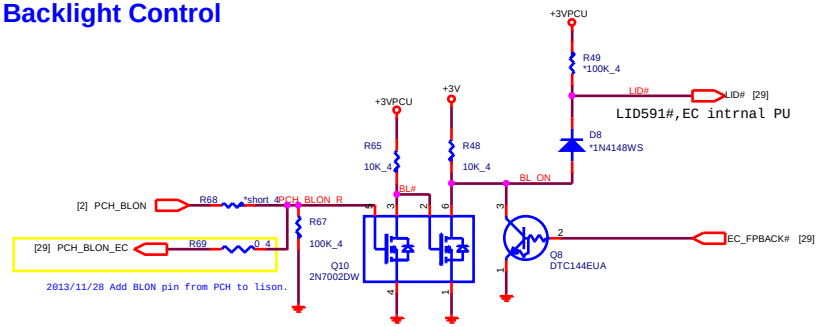
LCD Power



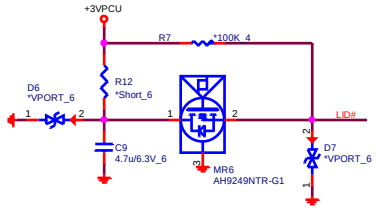
Touch screen level shift I2C(reserve)



Backlight Control



LID



1st : AL009249000 -- BCD
2nd : AL001691000 -- OCS

Quanta Computer Inc.
PROJECT : ZQX

Size	Document Number	Rev
	CRT/LVDS/CAMERA/LID	1B

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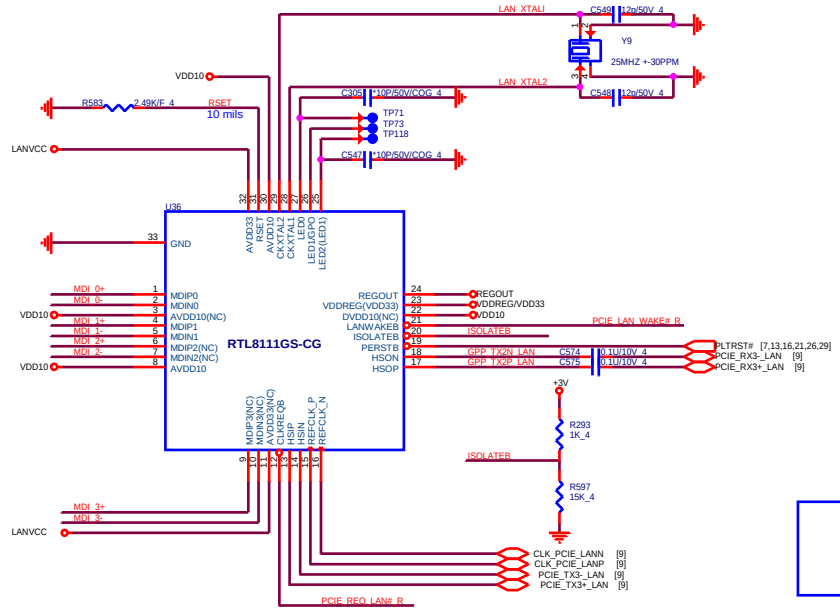
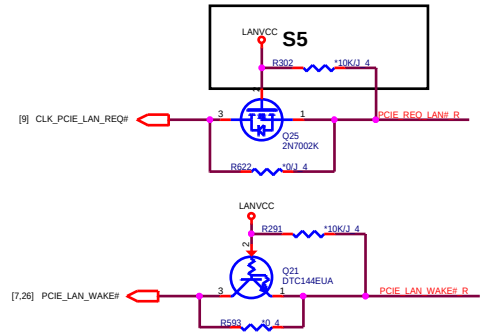
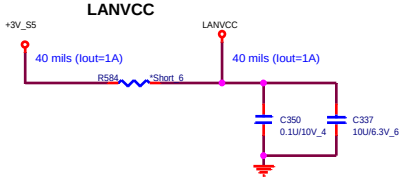
LAN



change to LANCC and add PU res for FAE suggest

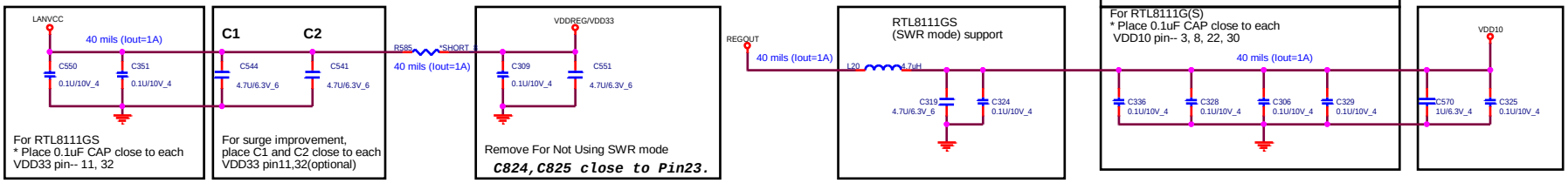


LANVCC



Power trace tracking

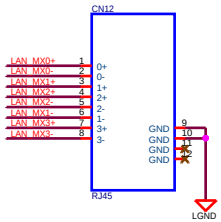
[5,7,8,9,10,11,13,21,27,28,29,31,34,36]
[2,5,7,8,9,10,11,13,14,15,16,17,18,21,22,23,25,26,27,28,29,31,32,33,34,35,36]
+3V_S5
+3V



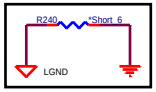
Tramsformer

change 1 ohm to to shortpad for FAE suggest

RJ45 Connector



Add 11/14



Quanta Computer Inc.
PROJECT : ZQX

Size	Document Number	Rev
	LAN (RTL8111GS)	1B
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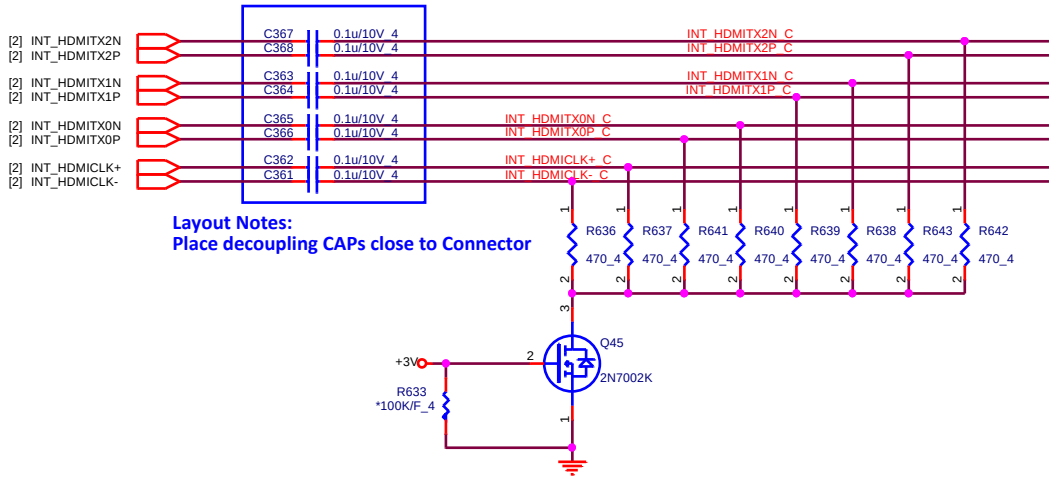
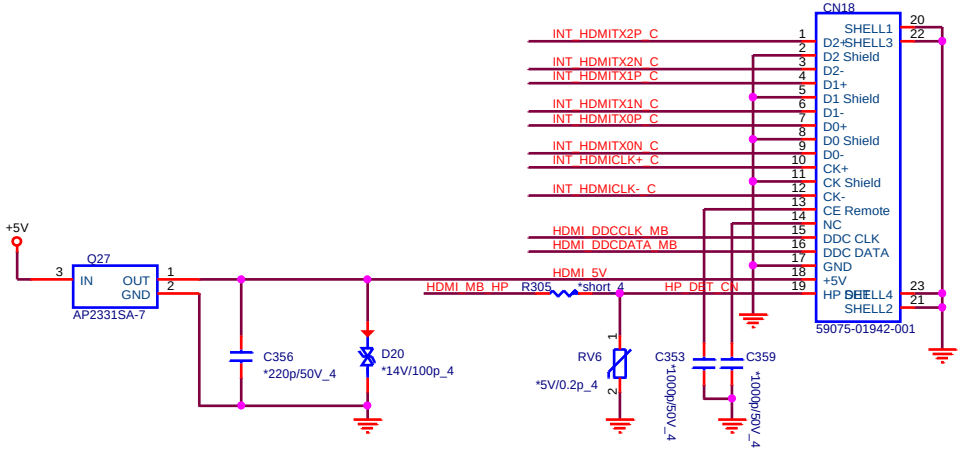
HDMI Cost Reduced level shift (HDM)

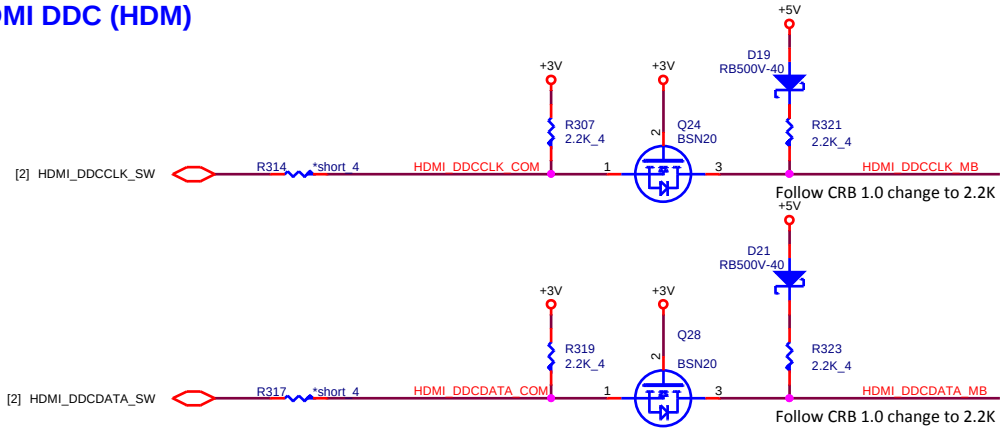


Layout Notes:
Place decoupling CAPs close to Connector

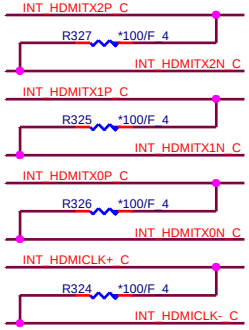
HDMI connector (HDM)



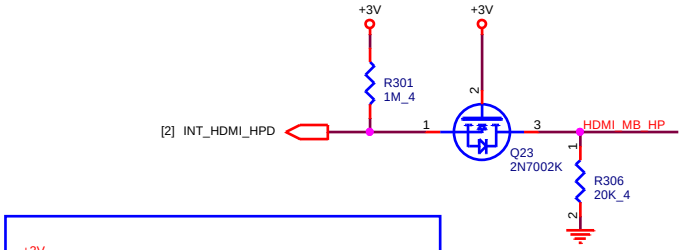
HDMI DDC (HDM)



EMI (EMC)



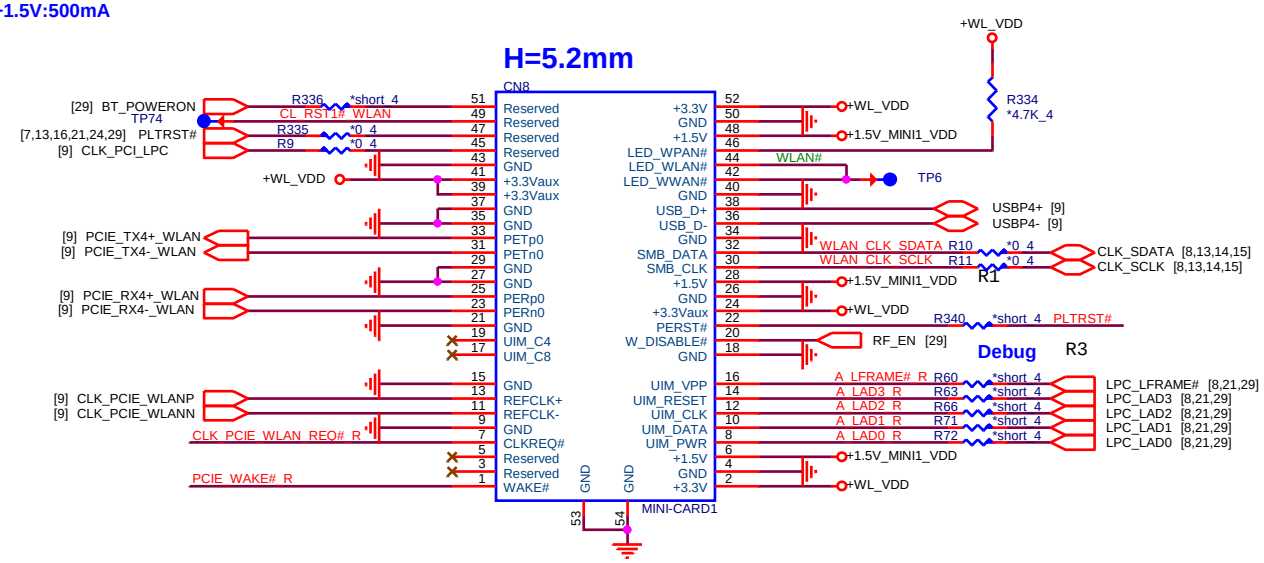
HDMI-detect (HDM)

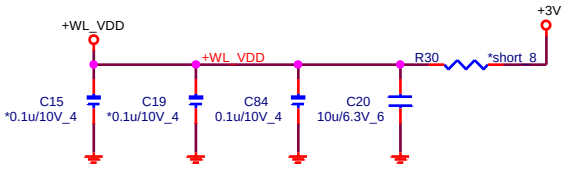


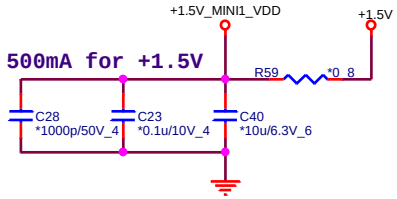
Quanta Computer Inc.		
PROJECT : ZQX		
Size	Document Number: HDMI (PS8101)	Rev: 1B
Date: Wednesday, September 03, 2014	Sheet 25 of 43	

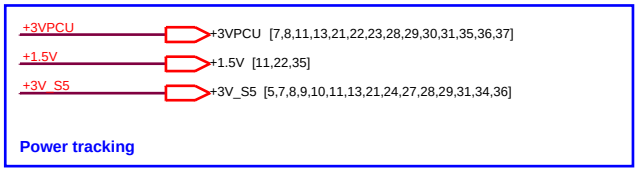
MINI-CARD WLAN(MPC)

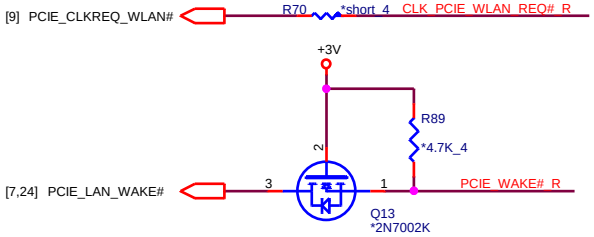
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA











Quanta Computer Inc.
PROJECT : ZQX

Size	Document Number	Rev
	Mini Card/mSATA	1B

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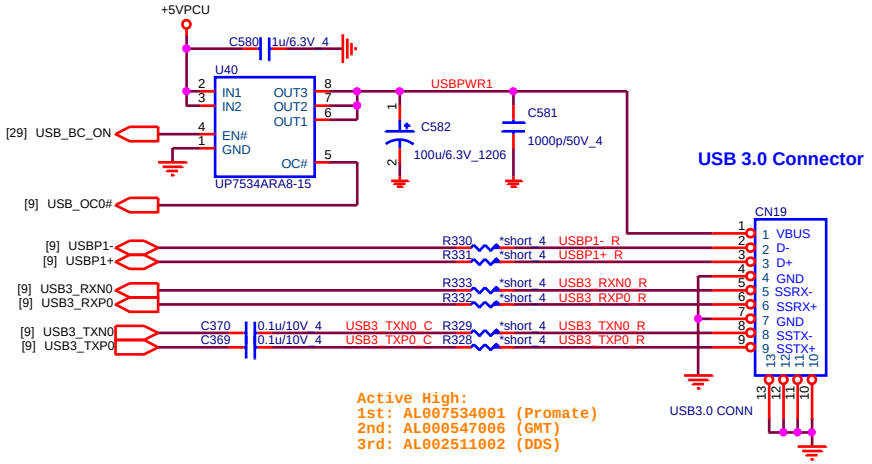
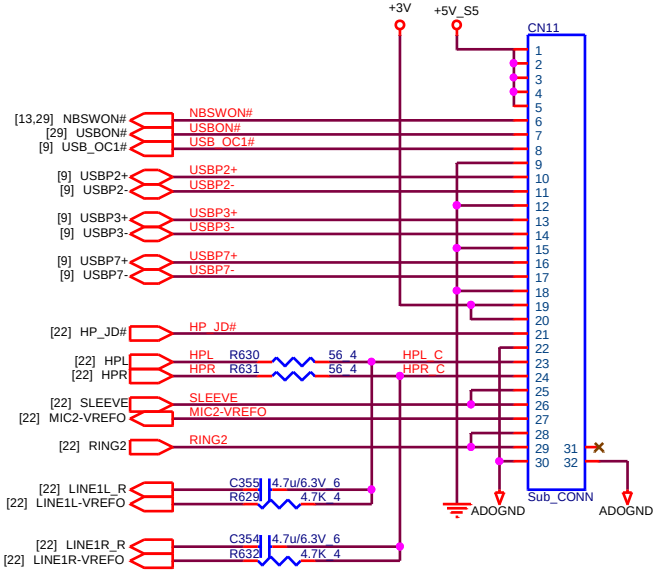
USB3.0

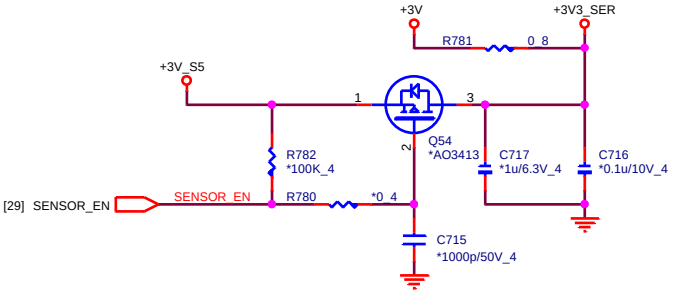


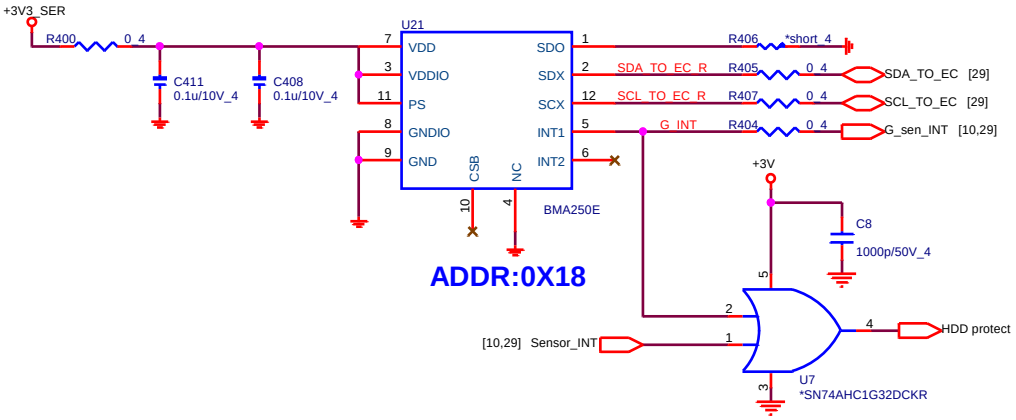
Active High:
1st: AL007534001 (Promate)
2nd: AL000547006 (GMT)
3rd: AL002511002 (DDS)

USB2.0
I/O board
For Universal Audio jack Function



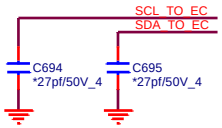
G Sensor

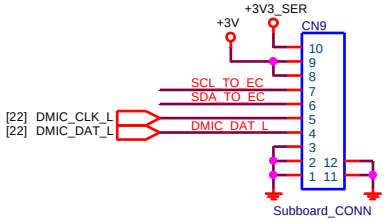




ADDR:0X18

Sensor board





+5VPCU → +5VPCU [31,32,33]
+3V → +3V [2,5,7,8,9,10,11,13,14,15,16,17,18,21,22,23,24,25,26,28,29,31,32,33,34,35,36]
+5V_S5 → +5V_S5 [4,8,31,32,34,36]

Power tracking

Quanta Computer Inc.
PROJECT : ZQX

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	INT&EXT USB	1B
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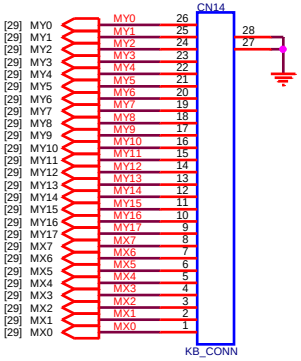
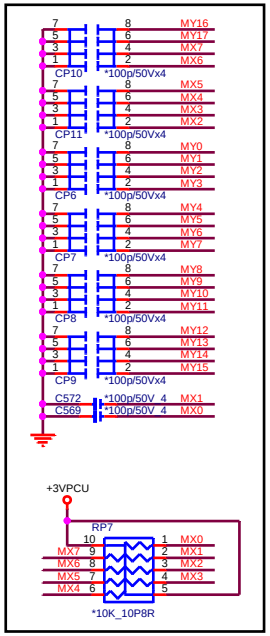
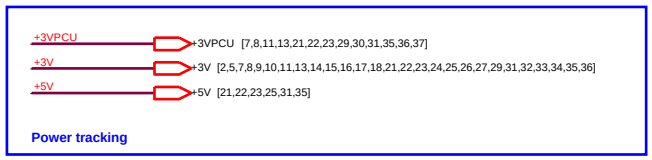
K/B (KBC)



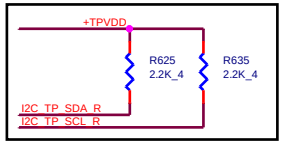


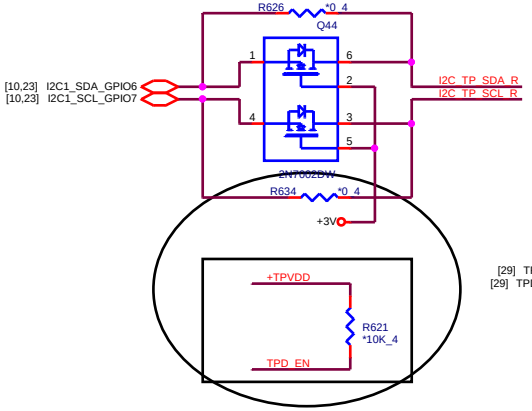


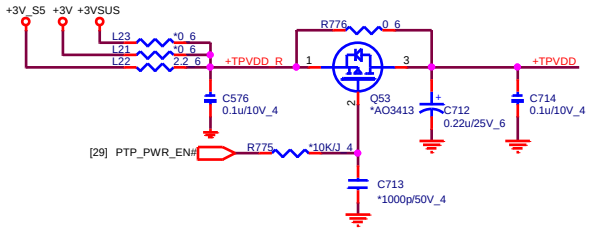
TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)

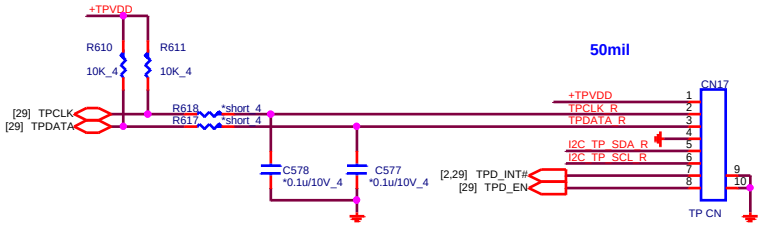
28

Modify on 11/08,
add touchpad i2c PU RES

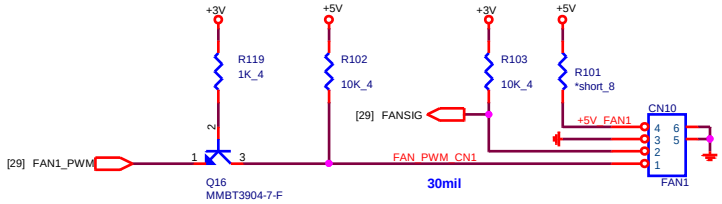




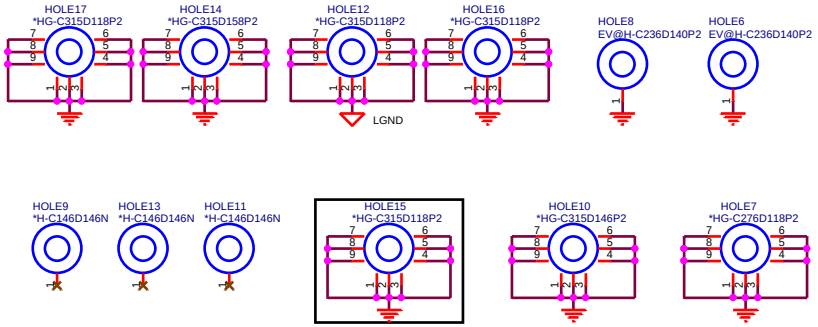




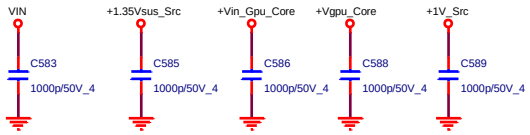
CPU FAN (THM)



HOLE



EMI



Quanta Computer Inc.
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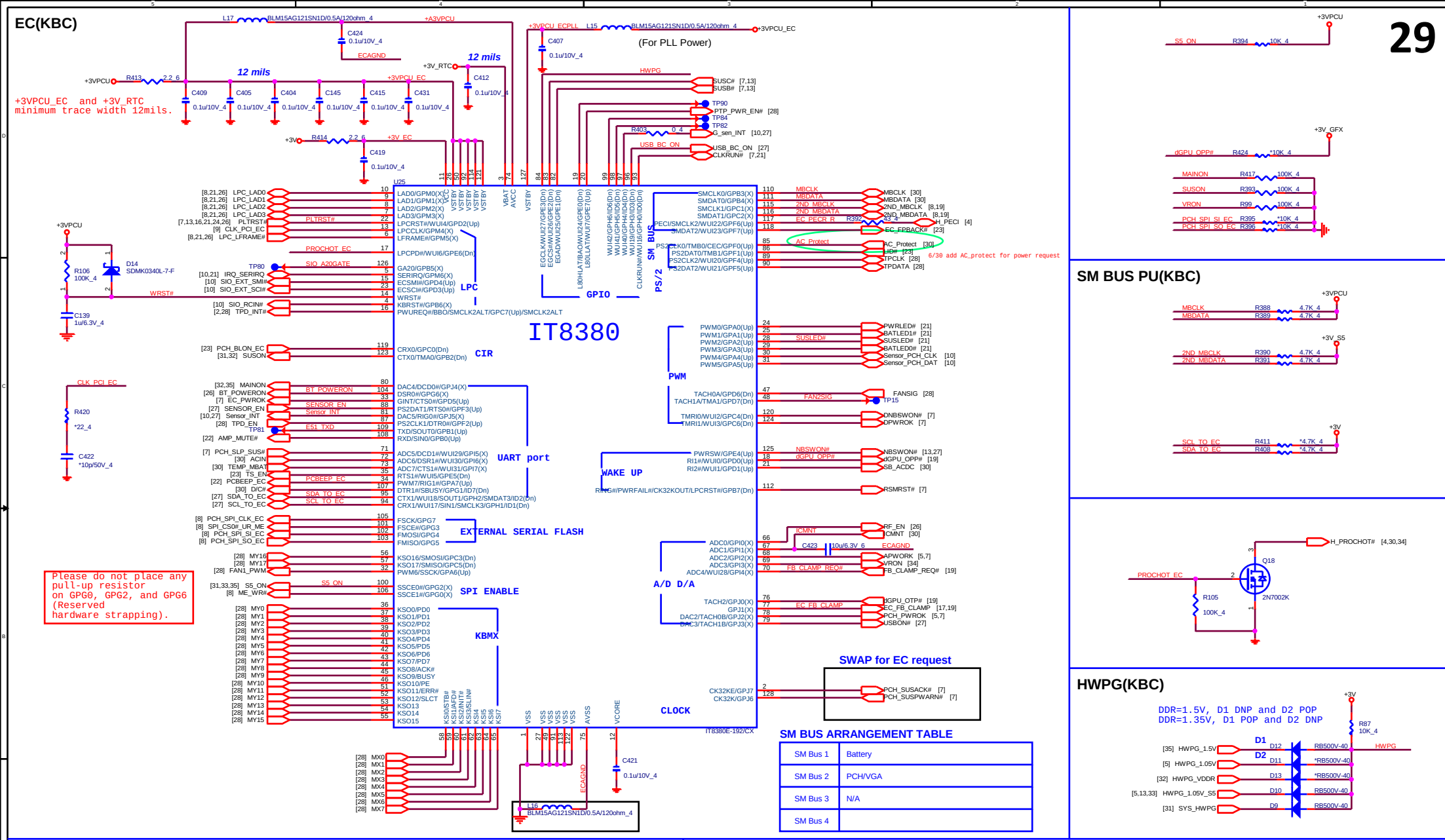
EC(KBC)



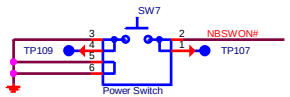
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH/VGA
SM Bus 3	N/A
SM Bus 4	

SM BUS PU(KBC)

HWPG(KBC)

For test only



iRST

Quanta Computer Inc.	PROJECT : ZQX
Size	Document Number: KBC IT8380 — Rev: 1B
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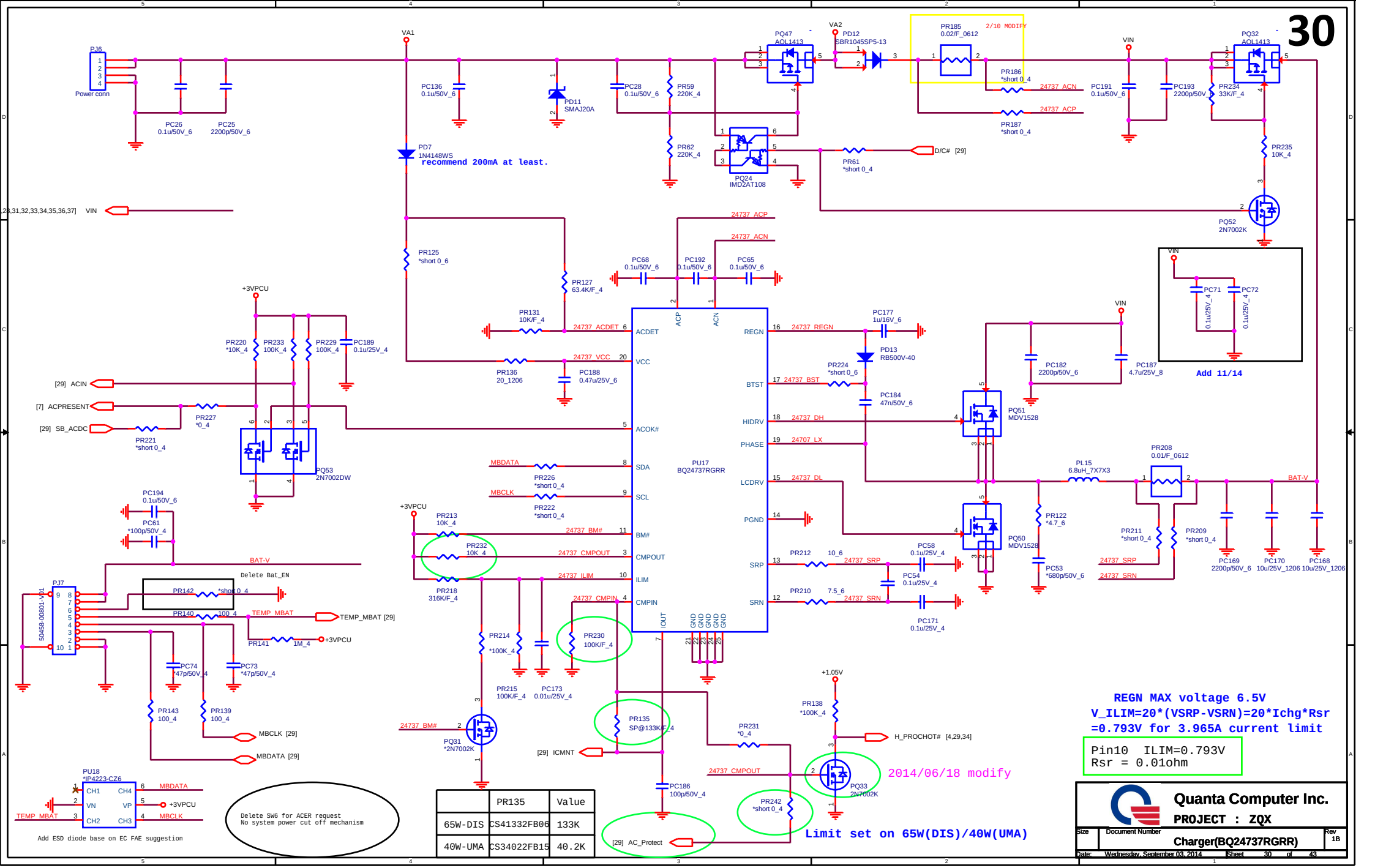

	PR135	Value
65W-DIS	CS41332FB06	133K
40W-UMA	CS34022FB15	40.2K

Quanta Computer Inc.
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Charger(BQ24737RGRR) | 1B
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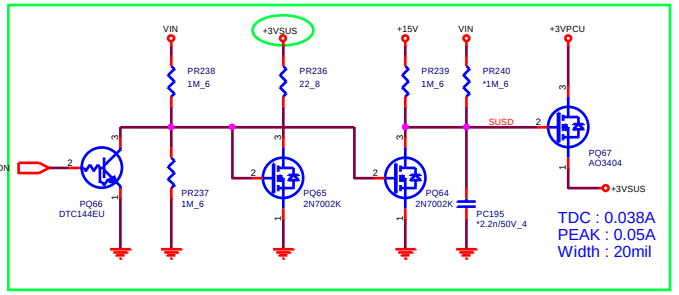
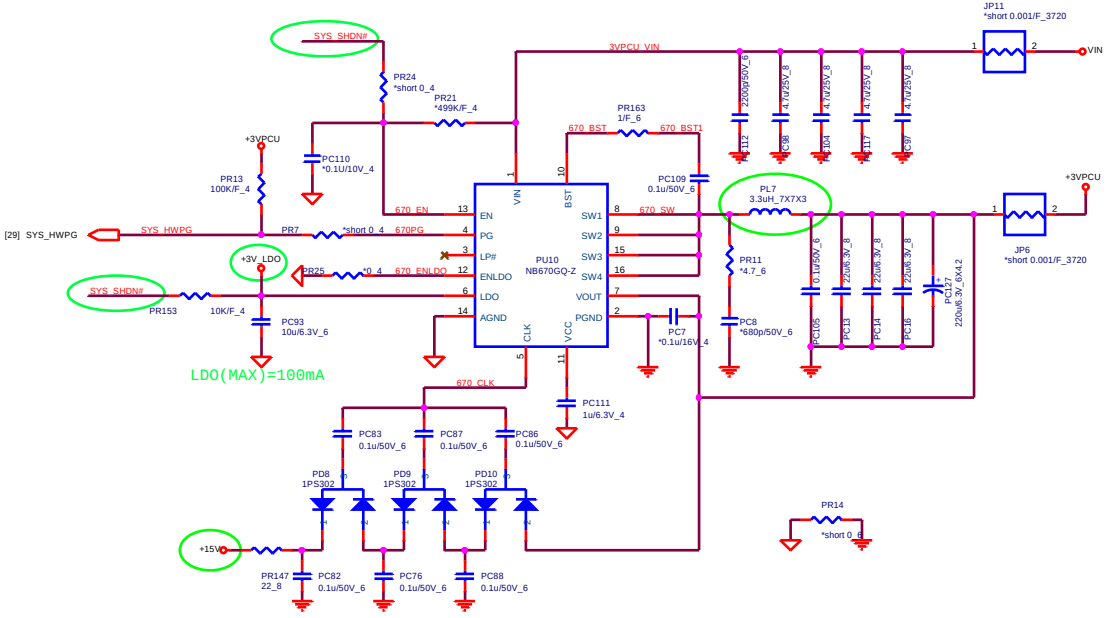
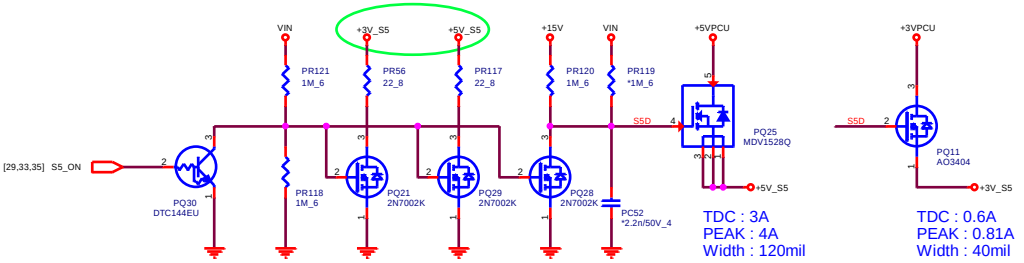
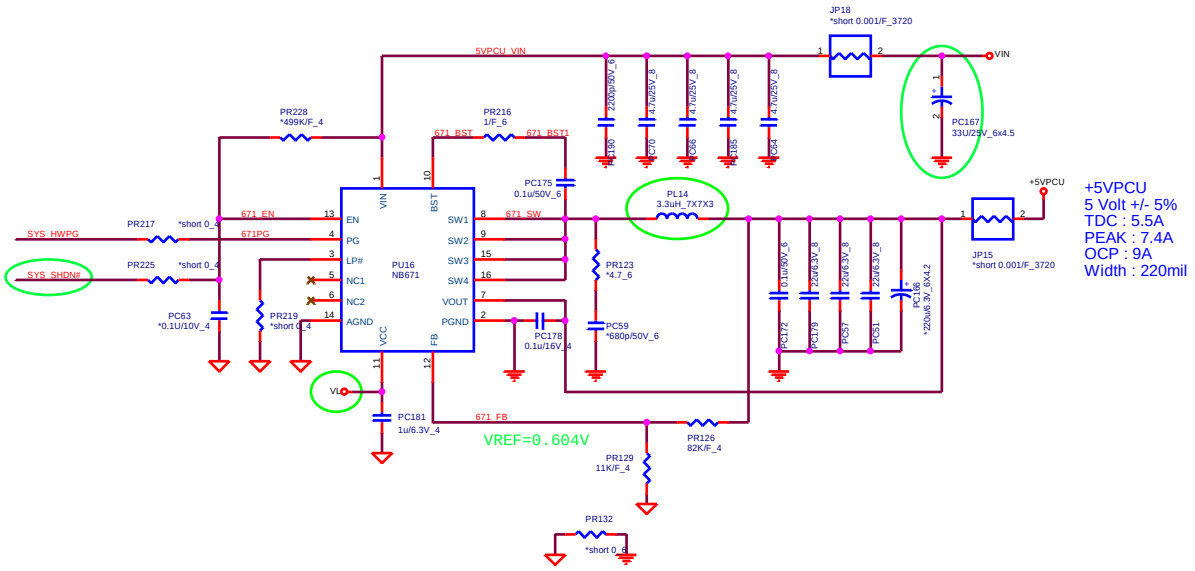
SYS_SHDN# SYS_SHDN# [10,21,35]
MAIND MAIND [33,35]

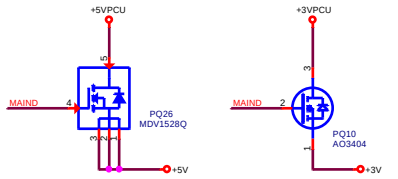
1/13 Adding +3VSUS power for touch pad
(By acer request)











Quanta Computer Inc.
PROJECT : ZQX
Size | Document Number | SYSTEM 5V/3V (TPS51225) | Rev 1B
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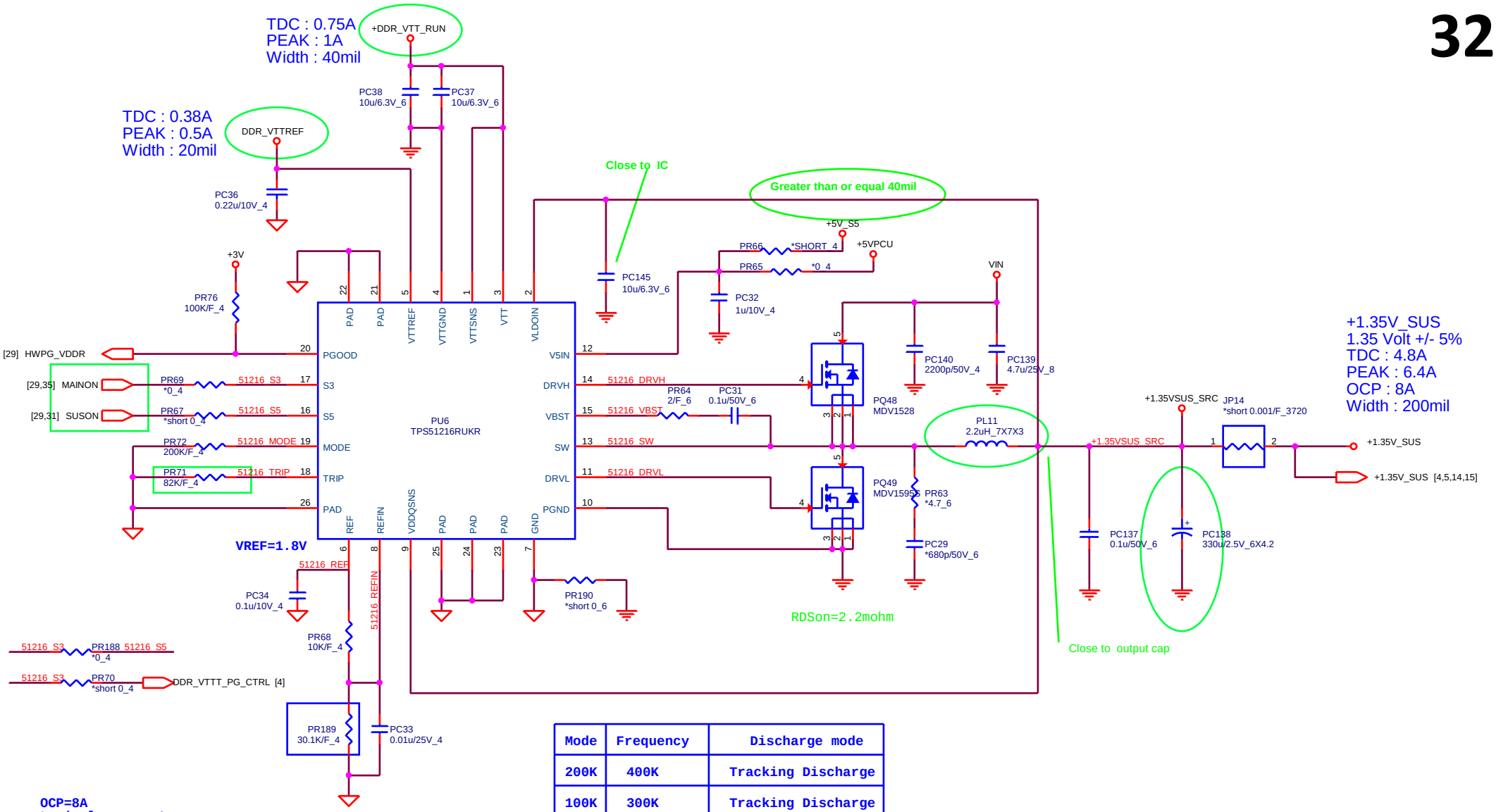

OCP=8A
L ripple current
=(19-1.35)*1.35/(2.2u*400k*19)
=1.425A
Vtrip=8-(1.425/2)*14mohm
=102.024mV
Rlimit=102.024mV/10uA*8=81.62Kohm

DDR=1.35V
PR84=10K/F_4
PR86=30.1K/F_4

Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.
PROJECT : ZQX

Size	Document Number	Rev
	DDR 1.35V(TPS51216)	1B

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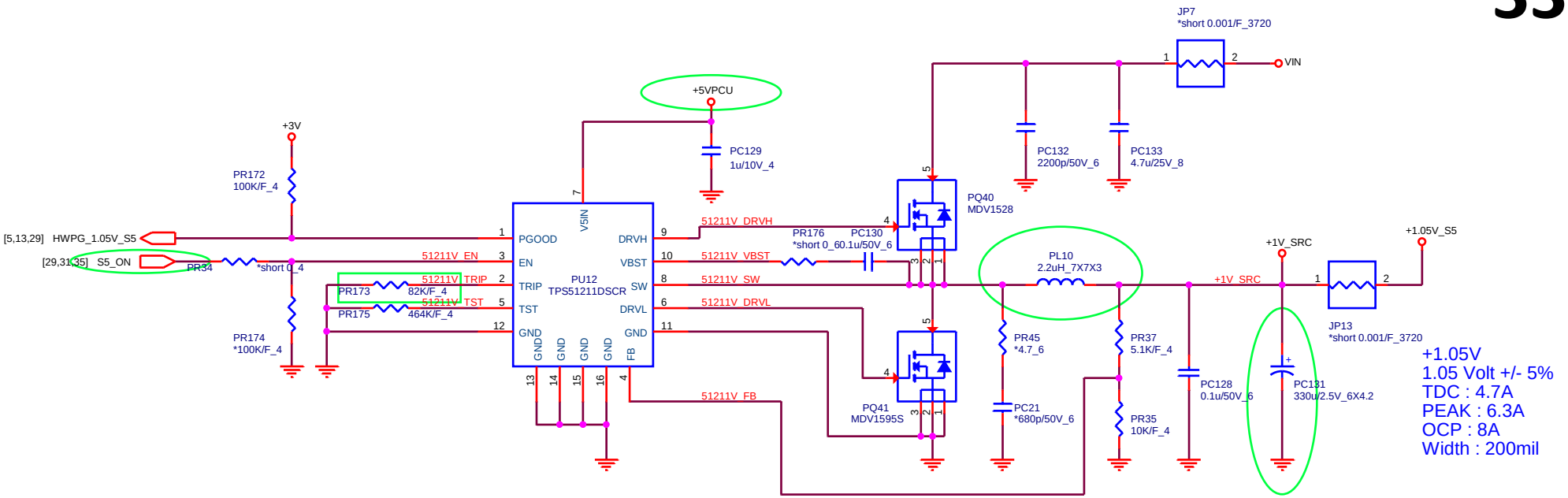
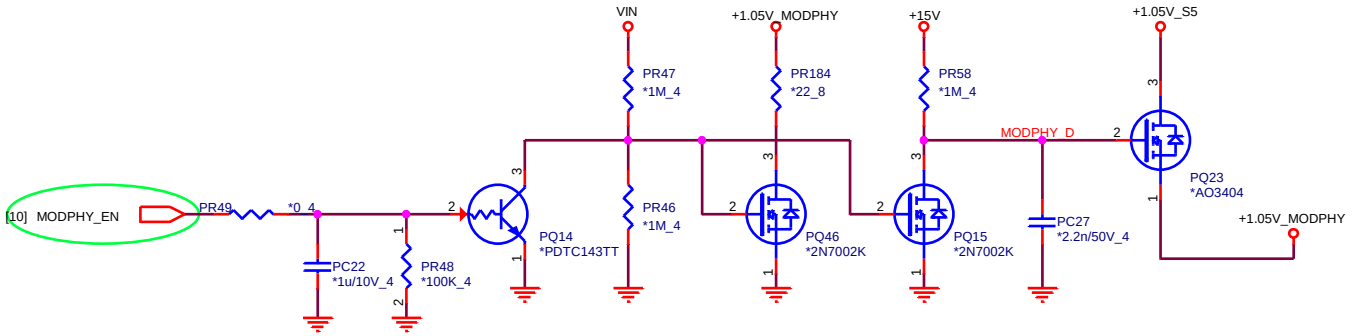


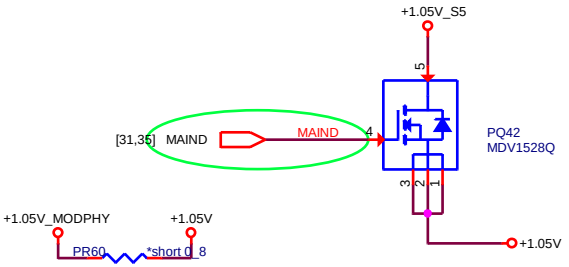
+1.05V
1.05 Volt +/- 5%
TDC : 4.7A
PEAK : 6.3A
OCP : 8A
Width : 200mil

OCP=8A
L ripple current
=(19-1.05)*1.05/(2.2u*290k*19)
=1.555A
Vtrip=8-(1.555/2)*14mohm
=101.12mV
Rlimit=101.12mV/10uA*8=80.89Kohm

VFB=0.7V



+1.05V_MODPHY
TDC : 1.43A
PEAK : 1.9A
Width : 80mil



TDC : 2.31A
PEAK : 3.08A
Width : 100mil

Quanta Computer Inc.
PROJECT : ZQX

Size	Document Number	Rev
	+1.05V_S5 (TPS51211)	1B
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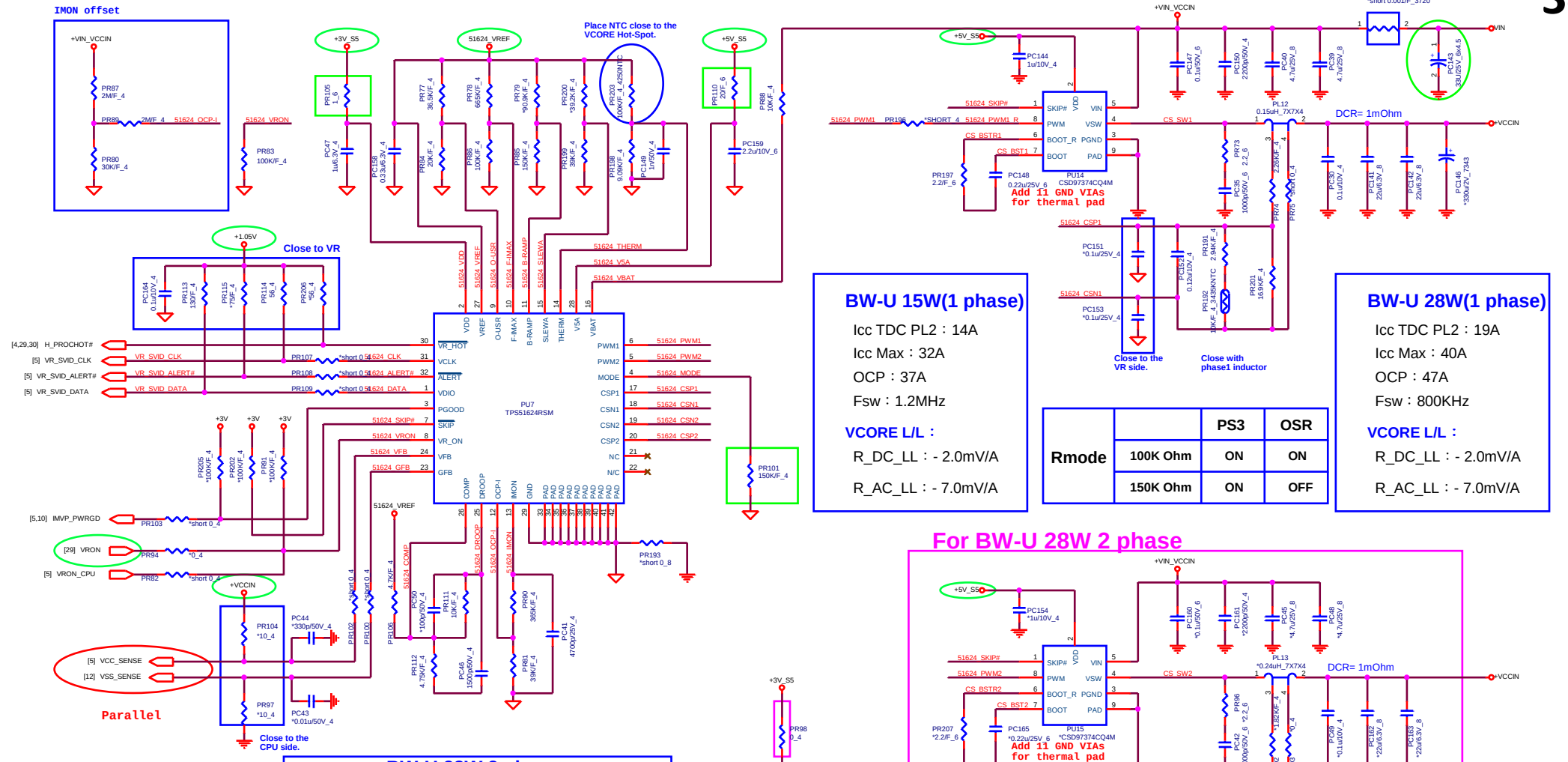

BW-U 15W(1 phase)

Icc TDC PL2：14A

Icc Max：32A

OCP：37A

Fsw：1.2MHz

VCORE L/L：

R_DC_LL：- 2.0mV/A

R_AC_LL：- 7.0mV/A

Rmode		PS3	OSR
	100K Ohm	ON	ON
	150K Ohm	ON	OFF

BW-U 28W(1 phase)

Icc TDC PL2：19A

Icc Max：40A

OCP：47A

Fsw：800KHz

VCORE L/L：

R_DC_LL：- 2.0mV/A

R_AC_LL：- 7.0mV/A

For BW-U 28W 2 phase

Block 1.

BW-U 28W 1 phase	15W
Location	Value
PR63	CS22212FB11
PR191	CS32262FB15
PR67	CS45232FB00
PR95	CS24752FB12
PR70	CS35622FB10
PR79	CS44122FB00

BW-U 28W 2 phase			
Location	Value	Location	Value
PL7、PL8	0.24uH_7X7X4	PR75	56.2K/F_4
PR63	1.82K/F_4	PR95	2.37K/F_4
PR191、PR194	*22.6K/F_4	PR101	10K/F_4
PR182	2.67K/F_4	PR79	150K/F_4
PC144、PC148	0.15u/10V_4	PR84、PR87	*0_4
PR67	294K/F_4	PC142、PC145 PC147、PC149	*0.1u/25V_4
Block 1.	Stuff		

Quanta Computer Inc.

PROJECT : ZQX

+VCCIN(TPS51624)

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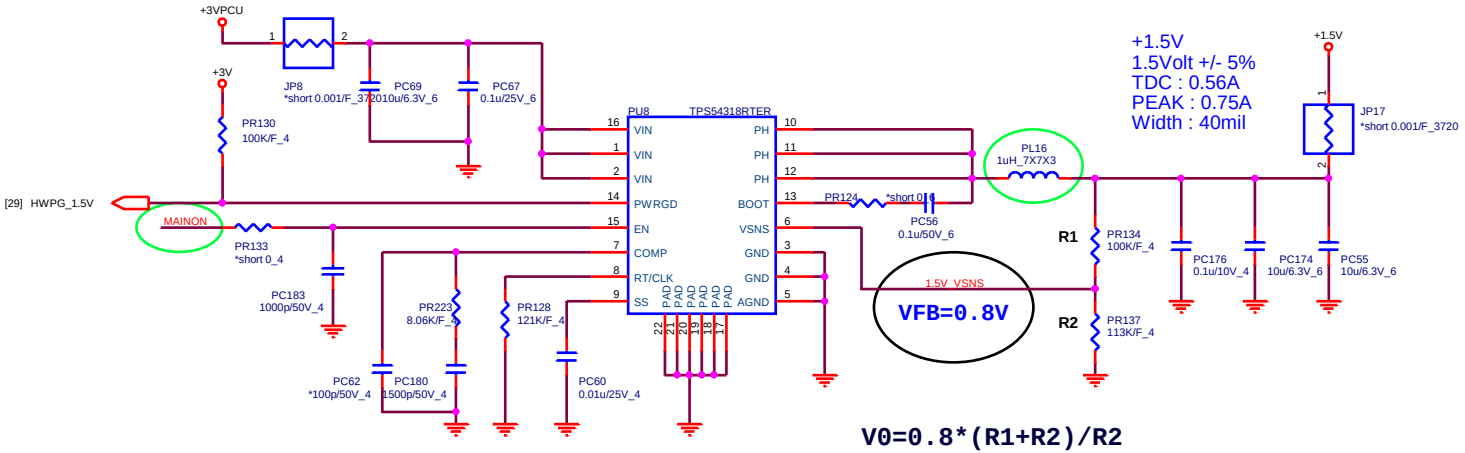
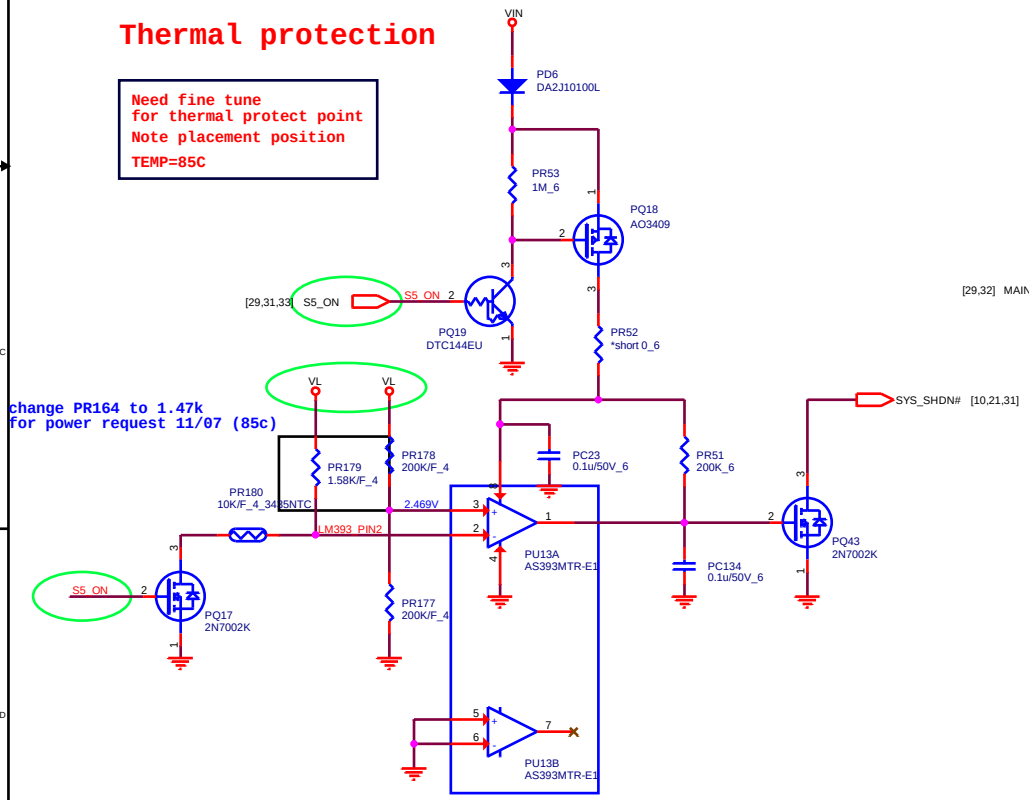


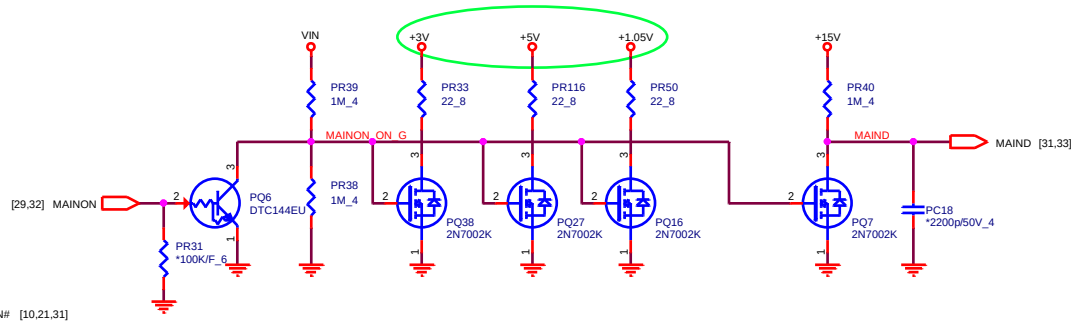
+1.5V
1.5Volt +/- 5%
TDC : 0.56A
PEAK : 0.75A
Width : 40mil

V0=0.8*(R1+R2)/R2

Thermal protection

Need fine tune
for thermal protect point
Note placement position
TEMP=85C





For EC control thermal protection (output 3.3V)

Quanta Computer Inc.
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	+1.5V/Thermal Protect	1B

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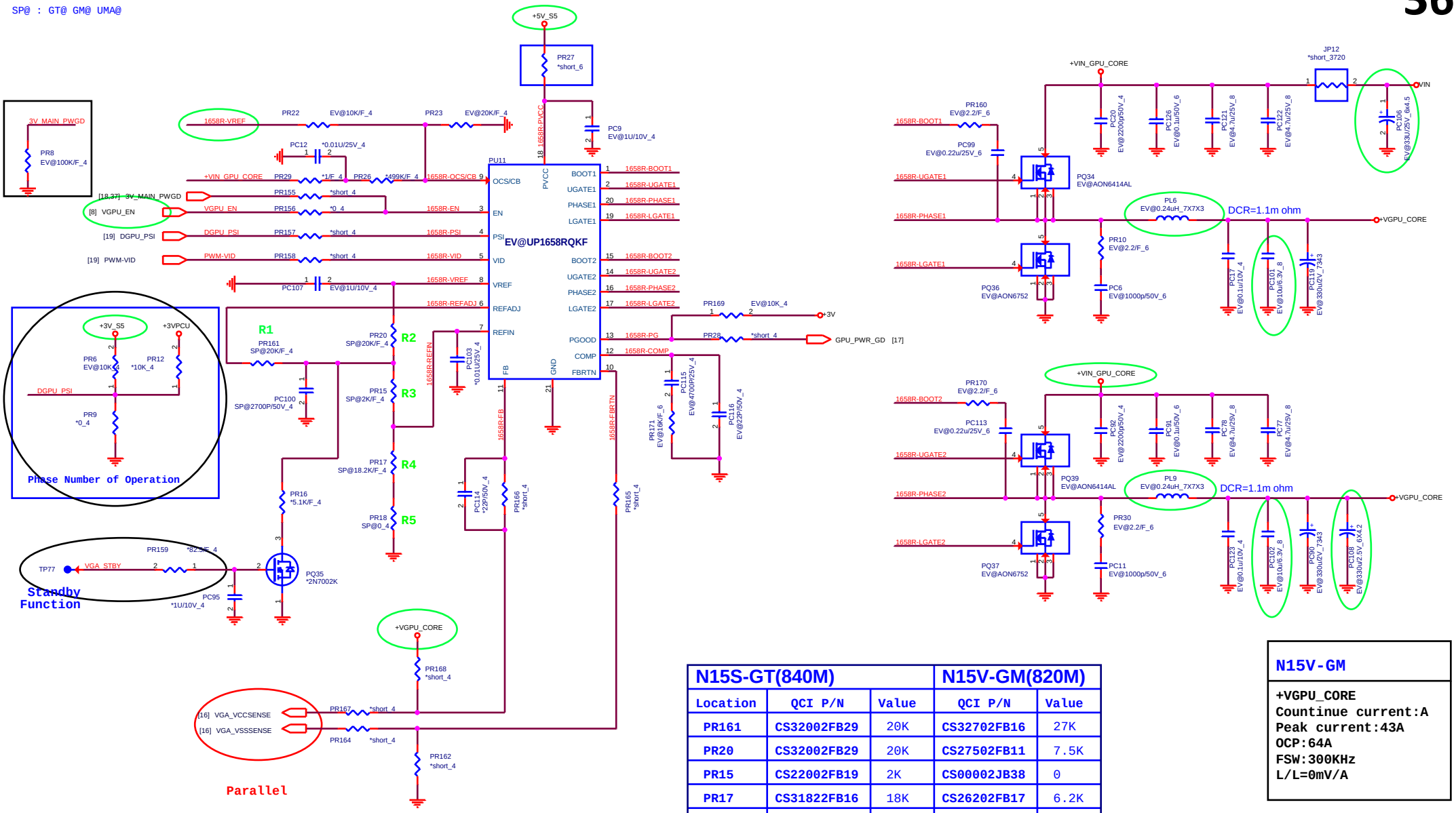
SP@ : GT@ GM@ UMA@



N15S-GT(840M)			N15V-GM(820M)	
Location	QCI P/N	Value	QCI P/N	Value
PR161	CS32002FB29	20K	CS32702FB16	27K
PR20	CS32002FB29	20K	CS27502FB11	7.5K
PR15	CS22002FB19	2K	CS00002JB38	0
PR17	CS31822FB16	18K	CS26202FB17	6.2K
PR18	CS00002JB38	0	CS21742FB00	1.74K
PC100	CH22706KB14	2.7N	CH25604KB18	5.6N

N15V-GM

+VGPU_CORE
Countinue current:A
Peak current:43A
OCP:64A
FSW:300KHz
L/L=0mV/A

Quanta Computer Inc.
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	+VGPU_CORE(UP1642PQAG)	1B

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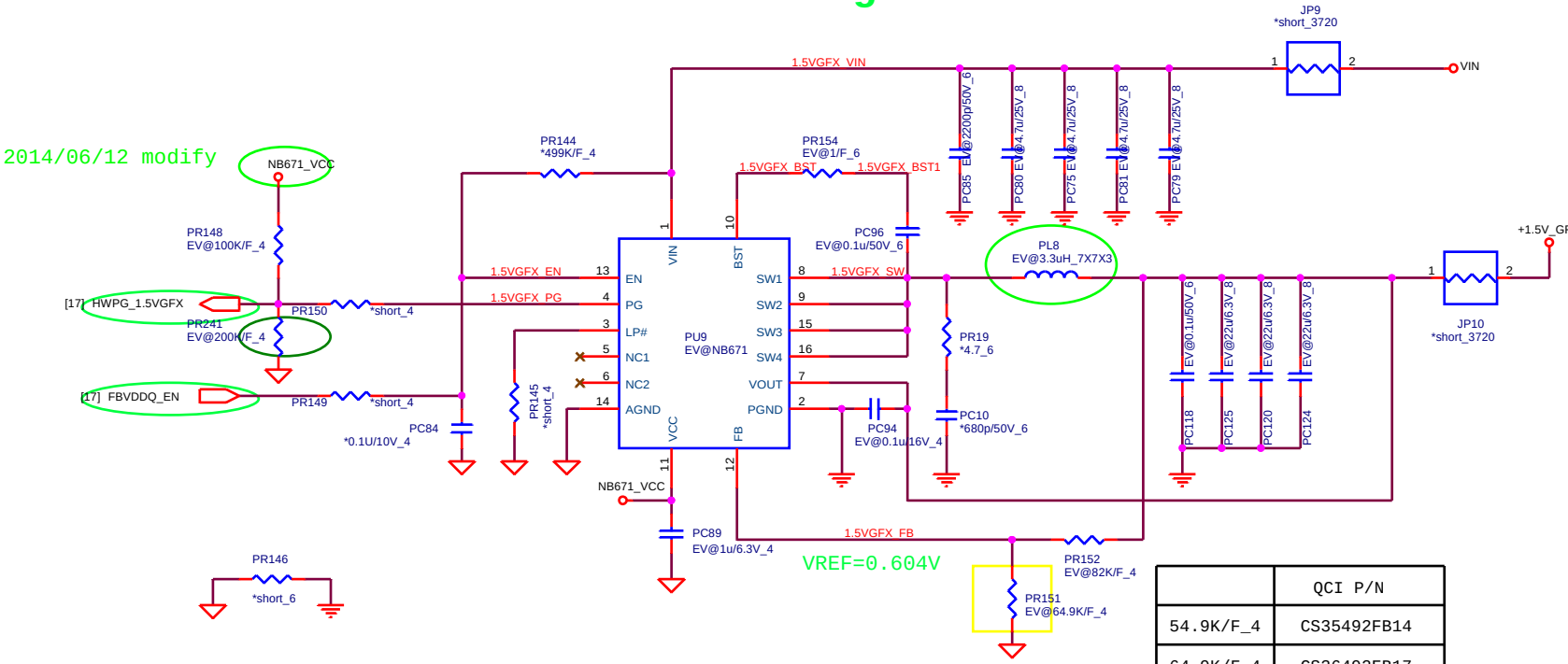
[16,17,18] +1.05V_GFX
[17,20] +1.5V_GFX
[16,17,18,19,29] +3V_GFX

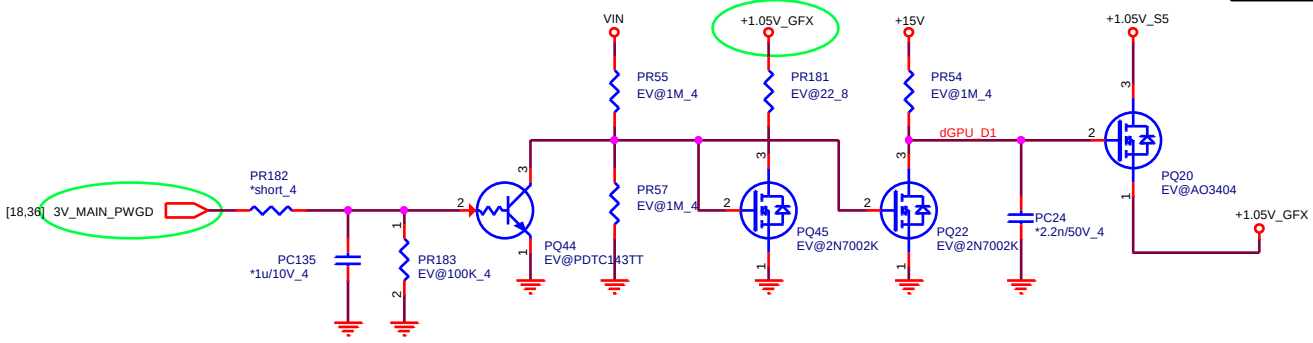
2013/12/19 Change to converter

2014/06/12 modify

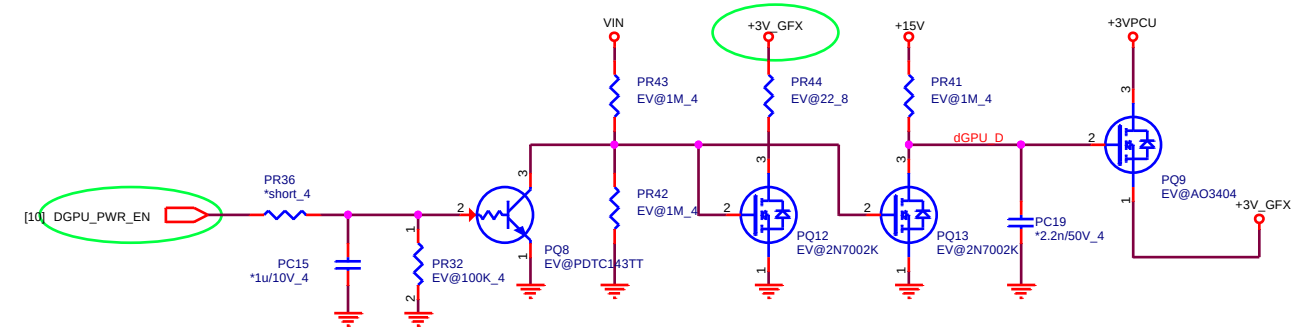


+1.5V_GFX
1.5 Volt +/- 5%
TDC : 3.2A
PEAK : 4.3A
Width : 130mil

	QCI P/N
54.9K/F_4	CS35492FB14
64.9K/F_4	CS36492FB17



+1.05V_GFX
TDC : 1.72A
PEAK : 2.29A
Width : 80mil



+3V_GFX
TDC : 0.26A
PEAK : 0.35A
Width : 20mil

Quanta Computer Inc.
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Size	Document Number	Rev
	+1.5V_GFX/+1.05V_GFX/+3V_GFX	1B
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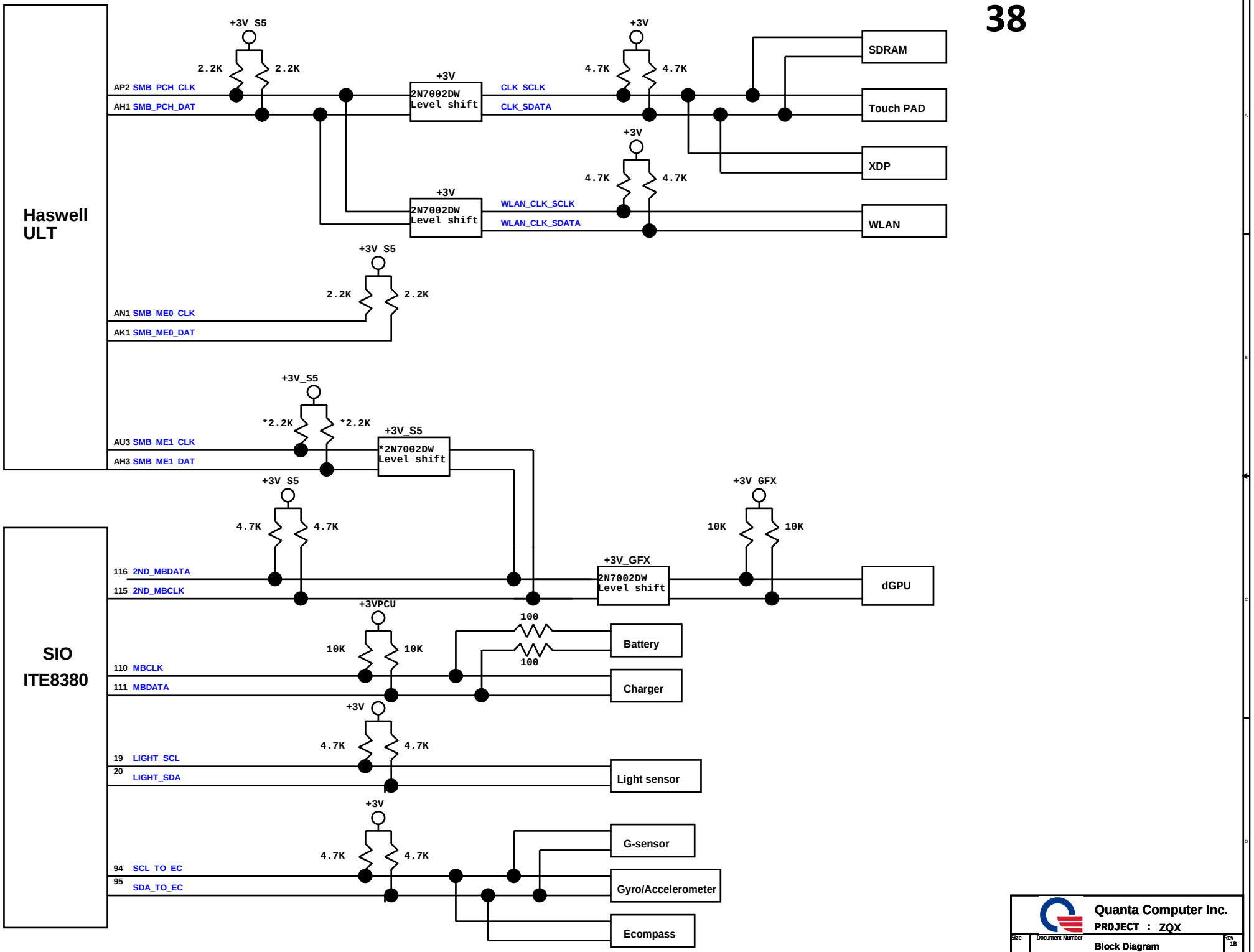

Quanta Computer Inc.
PROJECT : ZQX
Block Diagram
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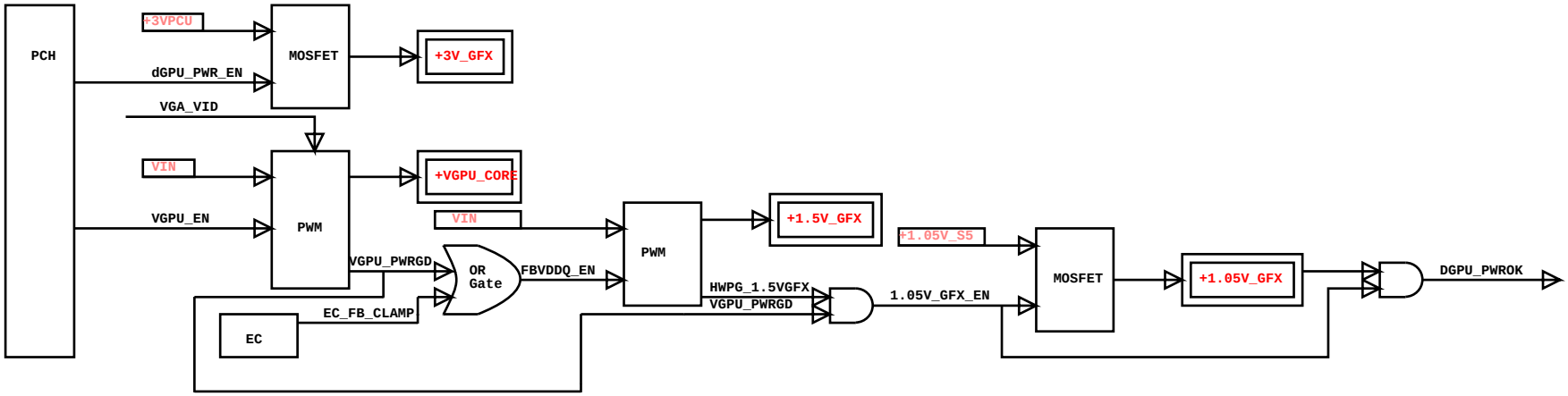
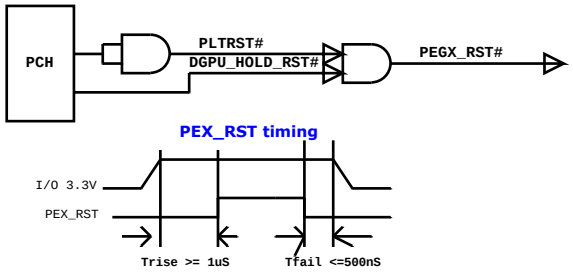
VGA power up sequence



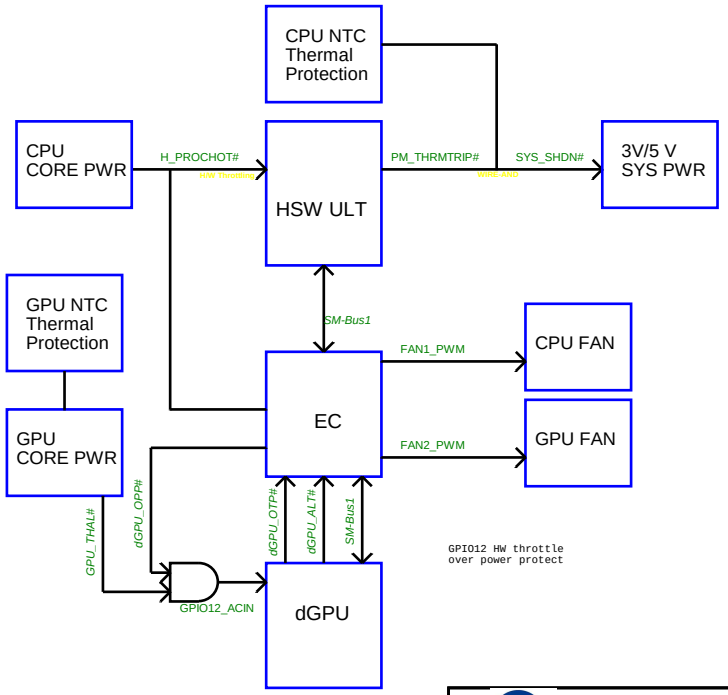
VGA Reset



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+3V_RTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	USB CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/SPK/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.35VSUS	+1.35V	CPU/SODIMM/MD POWER	SUSON	S0-S3
+DDR_VTT_RUN	+0.675V	SODIMM/MD Termination POWER	MAINON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE VCCST POWER	MAINON	S0
+VCCIN	variation	CPU CORE POWER	VRON	S0
+VGPU_CORE	variation	External GPU POWER	VGPU_EN	S0
+3V_GFX	+3.3V	External GPU POWER	dGPU_PWR_EN	S0
+1.5V_GFX	+1.5V	External GPU POWER	FBVDDQ_EN	S0
+1.05V_GFX	+1.05V	External GPU POWER	1.05V_GFX_EN	S0

Thermal Follow Chart



dGPU_OPP# EC notify HW throttle over power protect
dGPU_ALT# for ADPS circuit to infrom EC NV dGPU VPS Alert
dGPU_OTP# VGA thrmtrip# => inform EC over temperature protect

Quanta Computer Inc.
PROJECT : ZQX
Size | Document Number: PWR Status & GPU PWR CRL & THRM | Rev 1B
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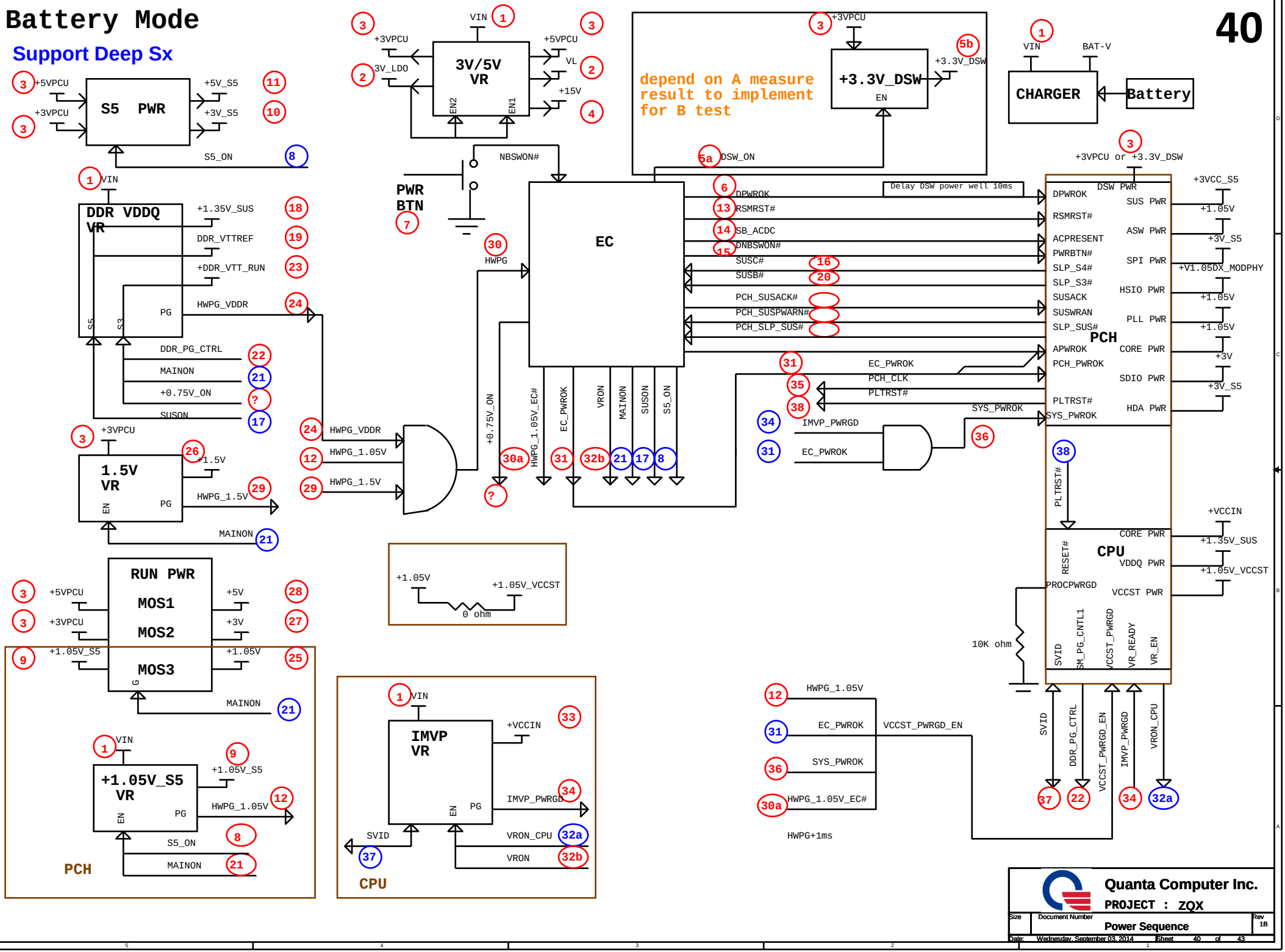
Battery Mode

Support Deep Sx



Quanta Computer Inc.

PROJECT : ZQX

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	Power Sequence	1B

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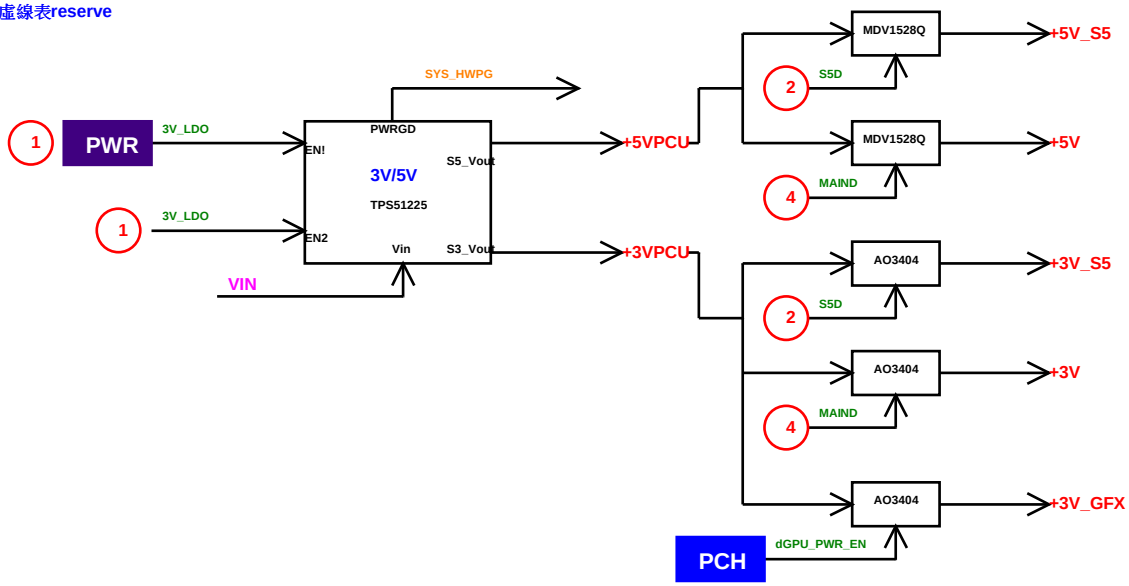
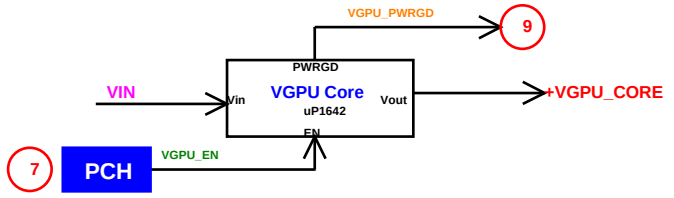
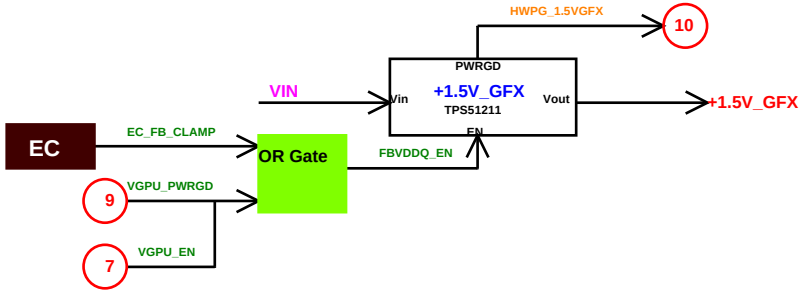
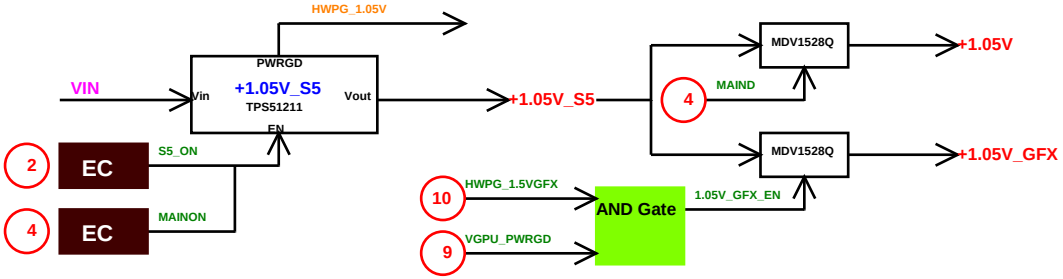
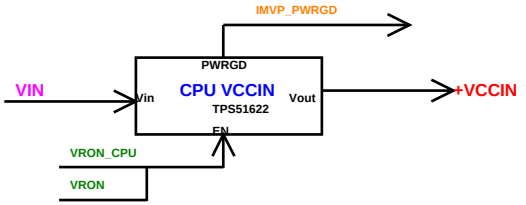
實線表defult
虛線表reserve

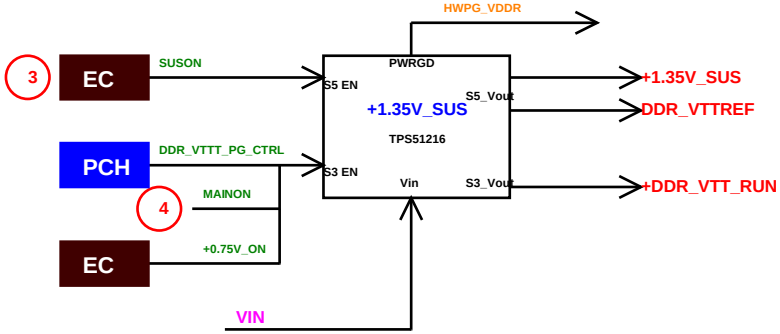


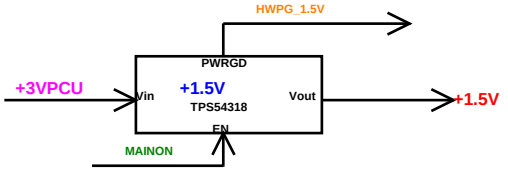












Quanta Computer Inc.
PROJECT : ZQX

Size	Document Number	Rev
	ULT PWR CONTROL	1B

Date: Wednesday, September 03, 2014 Sheet 41 of 43

Model	Version	CHANGE LIST
ZQX	1A	1. Add TPM function. (page26) 2. Modify Audio L/R connection. (page28) 3. Add 100k on MIC2-VREFO to AGND for FAE suggest (page22) 4. update CN31 footprint and PN (page29)
	10/24	5. Add 0805 0 ohm on +1.35V_SUS. (page5) 6. Modify VCCST_PWRGD_EN connection. (page5) 7. Add LPCPD# for TPM function (page7) 8. Change SPI damping R fform 15 to 0 ohm (page8) 9. change USB2.0 mapping port (page9) 10. change GPIO0~7 mapping port (page10) 11. Add pull high res for GPIO pin (page10) 12. unmount page13 debug itrm (page13) 13. Change +DDR_VTT_RUN res from 34.8 to 36 ohm 14. Change Q63 type (page19) 15. Reserve +3V for TP_PWR (page23) 16. Add 1.6P cap on USB3.0 for RF (page28) 17. reserver 0 ohm for Light_sensor I2C (page28)
	10/25	18. Modify M_A_CLK0,M_A_CLK1 connection. (page14) 19. Modify Block diagram (page1) 20. Change PC134,PC139 PN (page37) 21. Change TPM module to SLB9635 (page26) 22. Change G-sensor to BMA250E (page 29) 23. Add CN2 pin31 AGND 24. Add GPIO25 PU res (page10) 25. Change DGPU_SELECT# to PU10K (page2)
	10/28	26. Modify BMA250E CSB pin for FAE suggestion. (page29) 27. Change USB3.0 mapping for WHCK (page9) 28. Change HDD conn type to FFC (page26) 29. Change C301,C9089 to 3.3p (page14) 30. Change Q5045 SW power to +3v (page29)
	10/29	31. Modify LineL/R connection (page29) 32. Remove IOAC function (page24,page27,page30) 33. Add Mos for leakage (page27)
	10/30	34. Change to LANCC and add PU res for FAE suggest (page24) 35. Change MDI0~MDI3 Res form 1 ohm to shortpad for FAE suggest (page24) 36. Swap GND and HP_JD# for FAE suggest (page28) 37. Add 10u Cap on +5v codec for FAE suggest (page22) 38. Modify USB port mapping (page10)
	10/31	39. Swap DDR Data,DQS for layout request. (page14,15) 40. Swap Vram Data,DQS for layout request.(page21) 41. Add 100K on INT_AMIC-VREFO for FAE suggest (page22) 42. Reserve 0805 Res between +3V_MAIN and +3V_GFX for non GC6 function (page20) 43. SWAP PCH_SUSACK# and PCH_SUSPWARN# for EC request. (page30) 44. Change TP_INT_PCH port to GPIO83 (page10) 45. Add TPD_EN,TPD_INT# (page2,page29) 46. Modify EC_GPIO pin, detail please see page30 mark (page30) 47. Mount PR183,unmount PR184 for power request (page37) 48. Change +1.35_SUS o ohm 0805 to1206 49. Add TP_RST# PU RES (page23)
	11/01	50. Swap LSPK+,LSPK- 11/01 (page14,15) 51. Swap I2C port 0 and port1 (page10) 52. Swap USB2.3,7 +-for layout (page28) 53. Del TP_PWR 5V,Add pin31 connect to TP_PWR (page 23) 54 Change +3V to +WL_VDD Q5043 (page27) 55. Remove SMB_PCH_CLK and SMB_PCH_DAT (page30) 56. Reverse CN25 HDD(page26)
	11/04	57. Modify screw hole type (page29,31) 58. Swap Rin2,Sleeve,HPL_C,HPR_C (page28) 59. Modify surge sch follow ZQSA (page24) 60. Modify CN23 gnd and surge component PN.
	11/05	61. Delete shortpad for layout 11/05 (page24) 62. Use MOS replace U40, +1.05V_MODPHY (page11) 63. Delete SW6 for ACER request No system power cut off mechanism.(page31)
	11/06	64. Change CN6 PN for ME request (page26) 65. Add powe net name SP_PLLVDD (page18) 66. Add TP, update EC PN (page30) 67. Modify surge sch (page24) 68. Modify SMB_PCH_CLK/DAT for EC (page30) 69. Add sensor_INT (page10,30)
	11/07	70. Chage pr164 to 1.47k for power request (page36) 71. Change Hole2 type (page29) 72. Use GPIO46 to be G-sen_INT (page10,29)
	11/08	73. I2C0 connect to Sensor HUB,I2C1 connect touchpanle and touchpad for Acer request 11/08 (page10,30) 74. Modify on 11/08, add touchpad i2c PU RES(page29) 75. Change power cap 22u PN from CH6221M9A03 toCH6221M9A00 76. Reserve 0ohm on Sensor_PCH I2C (page10)
	11/11	77. Change L45,L46,L47 PN for EOL issue (page30) 78. Change D25,D49 to RB500V-40 (page22) 79. Change L15,L19 to CX300T10000, L20 to CX5PX101000 For EOD issue(page15,page17) 80. Change power net 3V_MAIN_PWGD PL 100k for power request (page37) 81. Mount Q26,R227 unmount R226 for leakage issue (page19) 82. Change PC79,PC147,PC132 PN for EOD issue (page35,page37)
	11/12	83. Change Hole7 type (page29) 84. Change L20 footprint (page18)
	11/14	85. update power +VCCIN(TPS51624) sch (page35) 86. Swap net for layout request (DDR Dim,keyboard and usb filter) (page9,page15,page23) 87. Delete Hole10 (page29) 88. Add 0ohm between LAND and GND (page24) 89. Add 0.1u cap on VIn (page31) 90. Delete 2 pcs 0.1u cap on VIN (page31) 91. Rename. 92. update titleblock; power description (page35)
	11/15	93. Change power discription (page38) 94. Change PU4 PN for +1.5V_GFX for peak current to 4.3A(page38) 95. Change Rnm PN to AKE3EFP0N07 (3.3V type) (page8)
	11/18	96. Modify GC6 mount part (page17,19,20) 97. change PU4 PN to AL0543180I0 (page38)

DOC NO.	PROJECT MODEL :	ZQX	APPROVED BY:		DATE:	
	PART NUMBER:		DRAWING BY:		REVISON:	

Quanta Computer Inc.
PROJECT : ZQX
Size: Document Number: Rev:
Change list-1
Date: Sheet of

Model	Version	CHANGE LIST	
ZQX	1B	Change Item	Reason for Change
		1. Add HDD protect function. example : U7 (page28) 2. Change Sensor board conn. (CN9) from 16 to 10 pin Remove Gyro/Accelerometer & eCompass function (page27) 3. Add DEVSLP0_R & HDD protect to CN13.4 (page21) 4. Add RTC charge circuit (page 8) 5. Q13.2 connect change from +3V+S5 to +3V (page26) 6. Q44.2 & 5 connect change from +3V to +TPVDD (page28) 7. R65 connect change from +3V to +3VPCU (page23) 8. R22 connect change from +3V to +5V (page23) 9. Connect SWAP PCIE CLKOUT 2 & 3 (page28) 10.TP_INT connect to CN7.5 & 6 (page23) 11. Add BLON pin (PCH_BLON_EC) to EC. (page23) 12. Change GPU from 29*29 to 23*23 Modify GPU circuit . Cahnge VRAM circuit.(page16 ~20)	1. Reserve for HDD protect in machine rotate condition 2. Remove sensors which aren't using on feature list 3. Reserve for HDD protect in machine rotate condition 4. Cause of placement and PE requirement, ZQX need to use small size of RTC(1220) with charging circuit 5. Remove IOAC function 6. Match touch pad support S5 power well 7. Ite load code time to long, cause backlight has flicker when AC in. 8. Touch screen voltgae change to 5V 9. PCIE clock request mapping issue 10. Reserve for touch screen interrupt control signal 11. Fn+F6 function 12. Acer feature change
	2A	1. Add C583 C585 C586 C588 C589 C692 C693 C694 C695 Modify C8 from 0.1UF to 1000PF for EMI request 2. Change TPM circuit Add. C584 C587 D35 R645 R646 R647 R649 R758 TP121 TP122 & R648 Remove T28 3. Modify TP circuit Add. L23 4. Change +3VSUS circuit Add PQ66 PQ65 PQ64 PQ67 PR238 PR237 PR236 PR239 PR240 & PC195 5. Add R644 for NV 6. R631 & R630 change from 56 to 47 ohm for vender request	
	2B	1. Add R651 & R645 for glitch of DDR_VTTT_PG_CTR Modify C8 from 0.1UF to 1000PF for EMI request 2. Change TPM circuit Add. C584 C587 D35 R645 R646 R647 R649 R758 TP121 TP122 & R648 Remove T28 3. Modify TP circuit Add. L23 4. Change +3VSUS circuit Add PQ66 PQ65 PQ64 PQ67 PR238 PR237 PR236 PR239 PR240 & PC195 5. Add R644 for NV 6. R631 & R630 change from 56 to 47 ohm for vender request	

DOC NO.	PROJECT MODEL :	ZRQ	APPROVED BY:		DATE:		Quanta Computer Inc. PROJECT : ZQX
	PART NUMBER:		DRAWING BY:		REVISON:		Change list-2