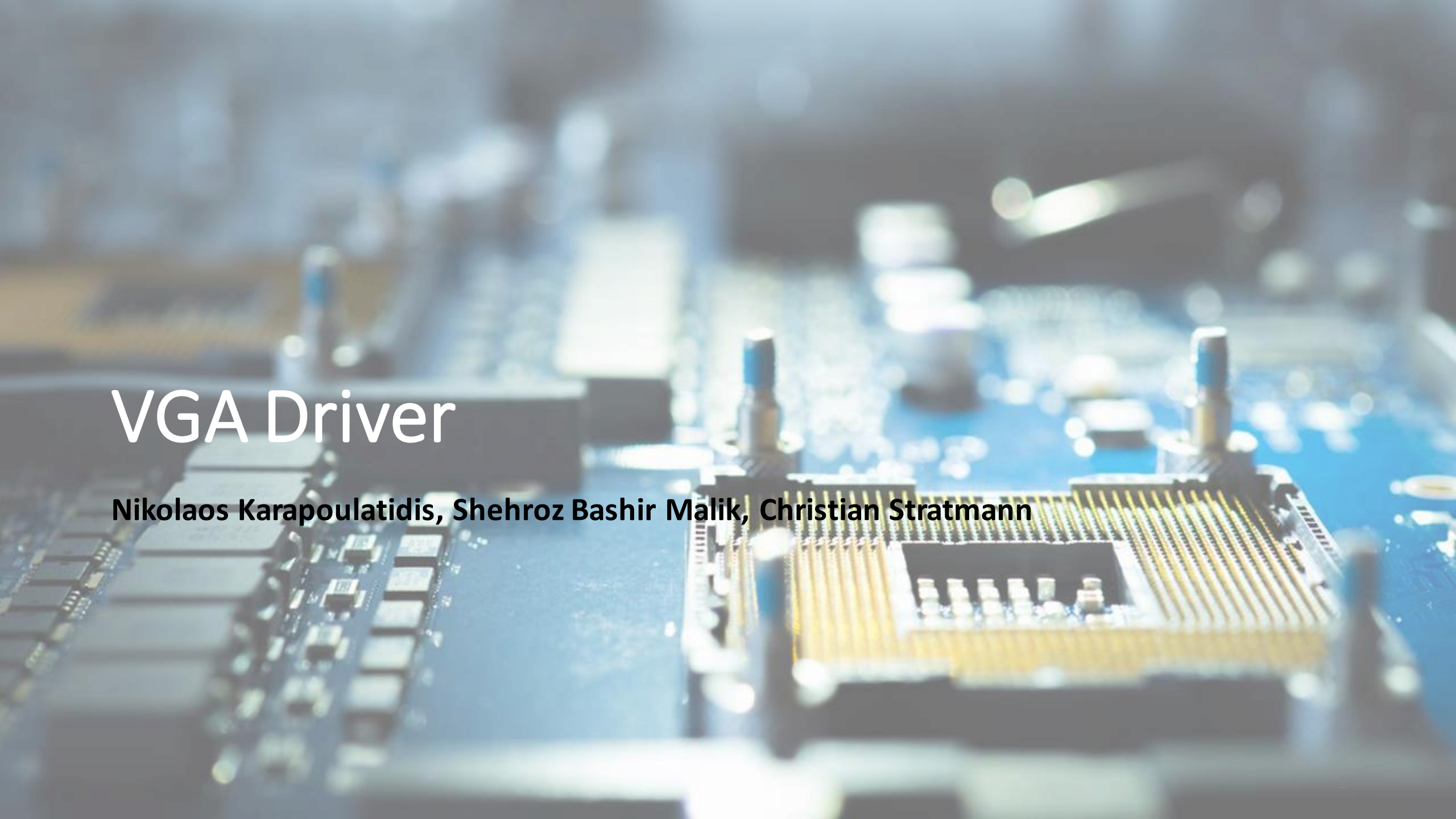
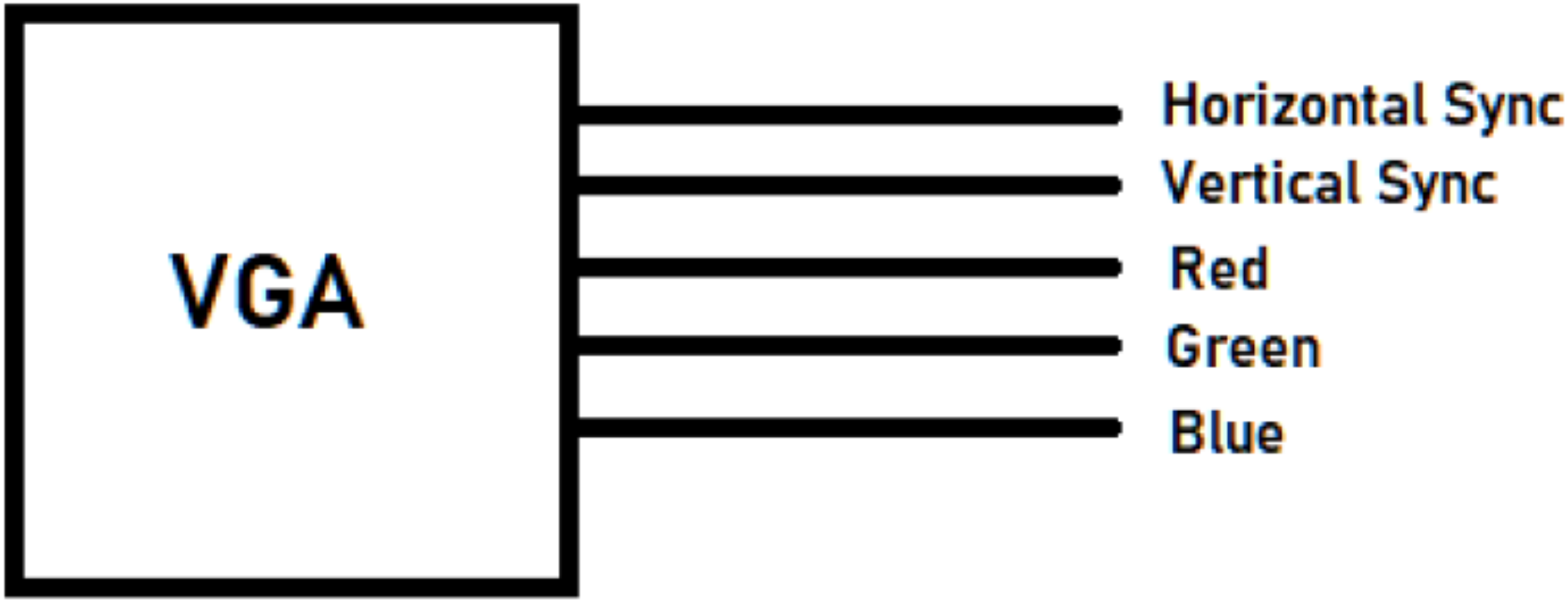


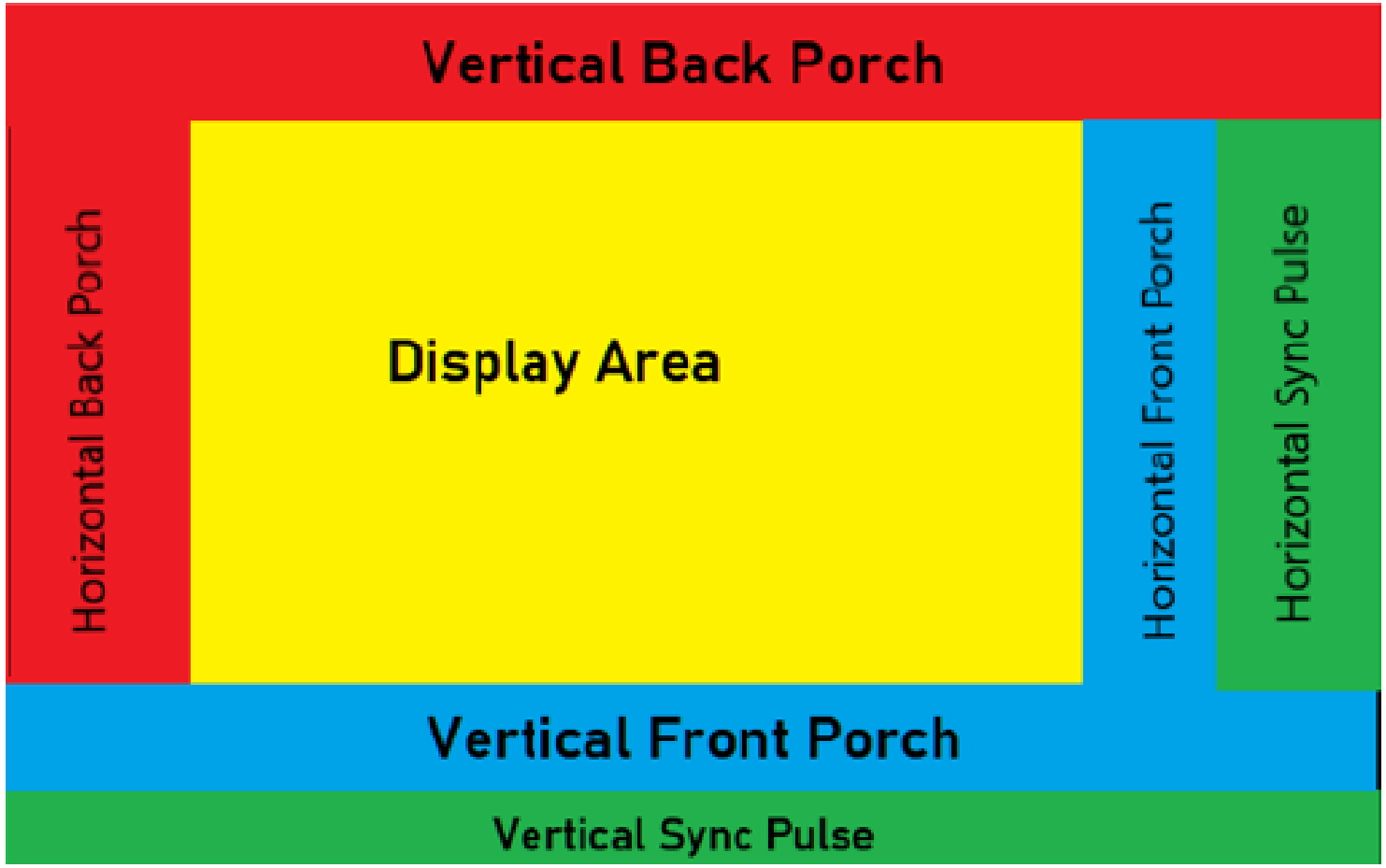
VGA Driver

Nikolaos Karapoulatidis, Shehroz Bashir Malik, Christian Stratmann

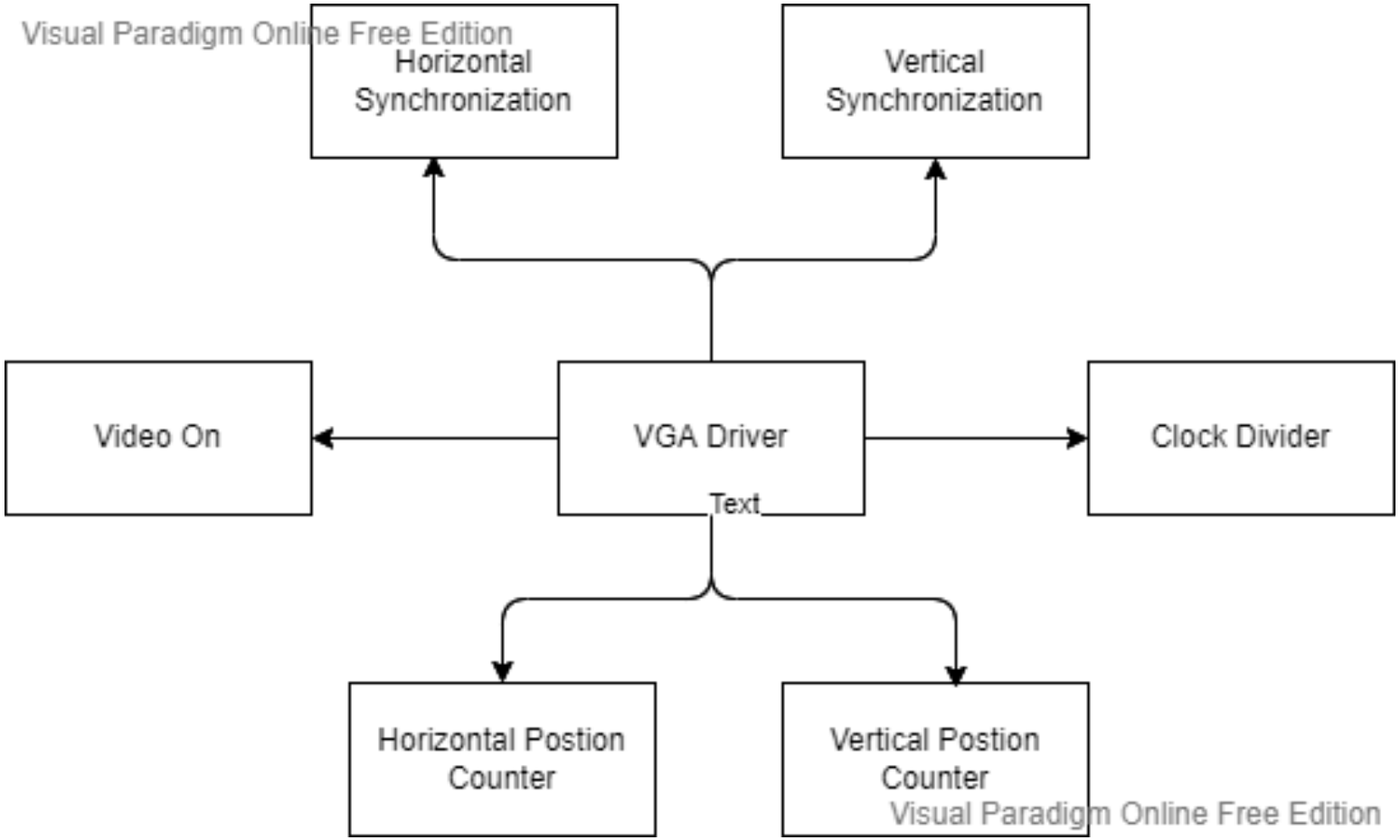
VGA Signals



Concept Design



Block Diagram



Entity

- **Input:** Clock and reset with type STD_logic

- **Output:** Horizontal Sync and Vertical Sync with type STD_logic, Red Green Blue with STD_Logic_Vector

Architecture

- **Signals:** Clock25, Horizontal Position, Vertical Position and VideoOn
- **Constants for Horizontal** (pixel number)**:** Display, front porch, back porch, sync pulse/retrace
- **Constants for Vertical** (line number)**:** Display, upper porch, lower porch, sync pulse/retrace

Processes I

- Every **process depends on the rising edge** of the clock
- **Clock Divider:** creates a clock of 25 mHz (default is 50mHz)
- **Horizontal Position Counter:** horizontal position = the total horizontal pixels? If true then start from left side, if not then counter++ and head to the next pixel
- **Vertical Position Counter:** If true when start from the top

Processes II

- **Horizontal Synchronization:** checks if the actual horizontal position is inside the horizontal front porch or back porch. If true then HSYNC set to 1
- **Vertical Synchronization:** checks for upper and lower porch
- **Video On Check:** ensures that the video is only on when the actual position is not inside a porch

Processes III

- **Draw Box:** set the output RGB to 111 if we are between 10 and 60 for the horizontal position and vertical position, outside those boundaries RGB is set to 000

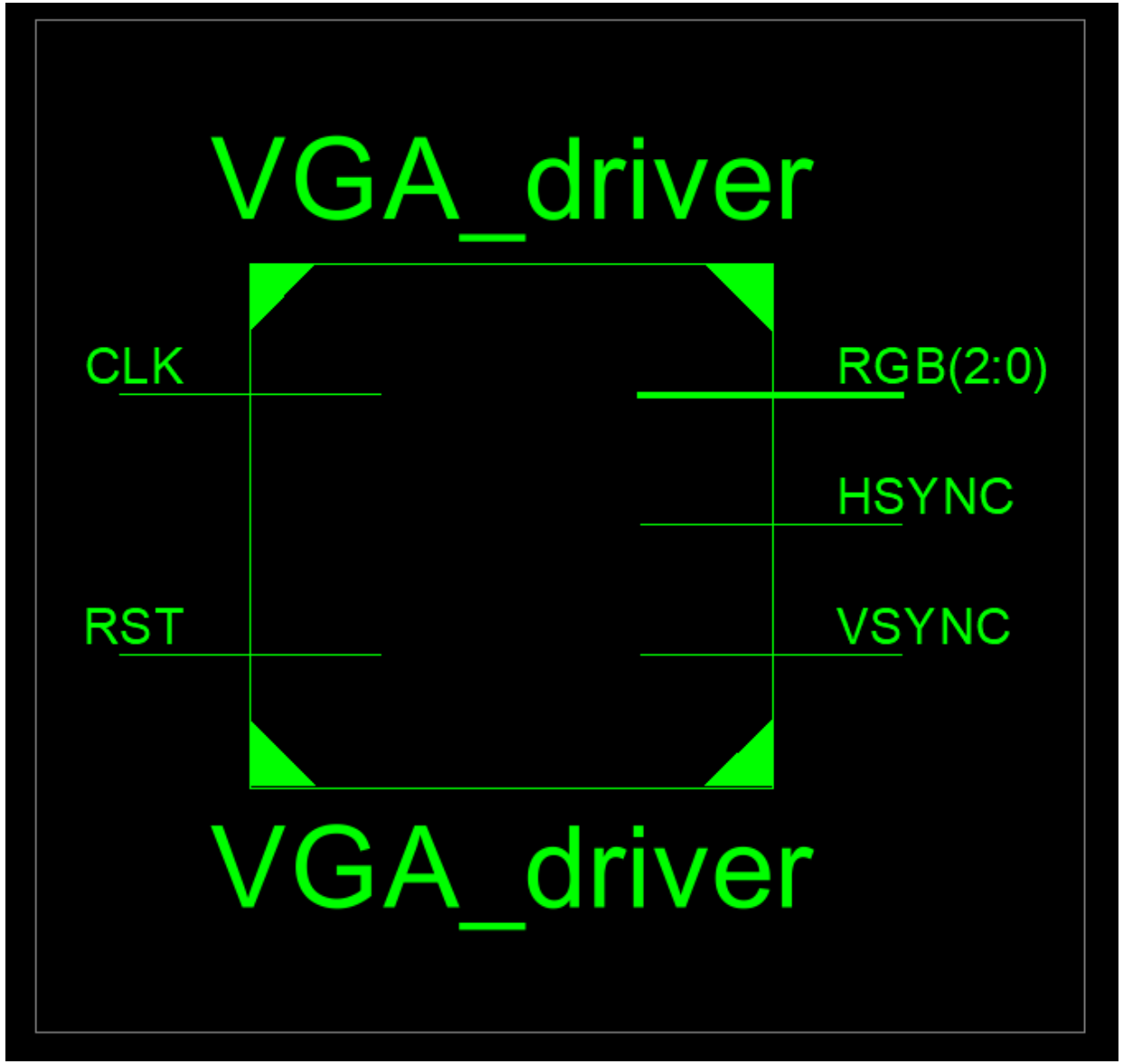
  -> white square appears on the VGA monitor

Testbench

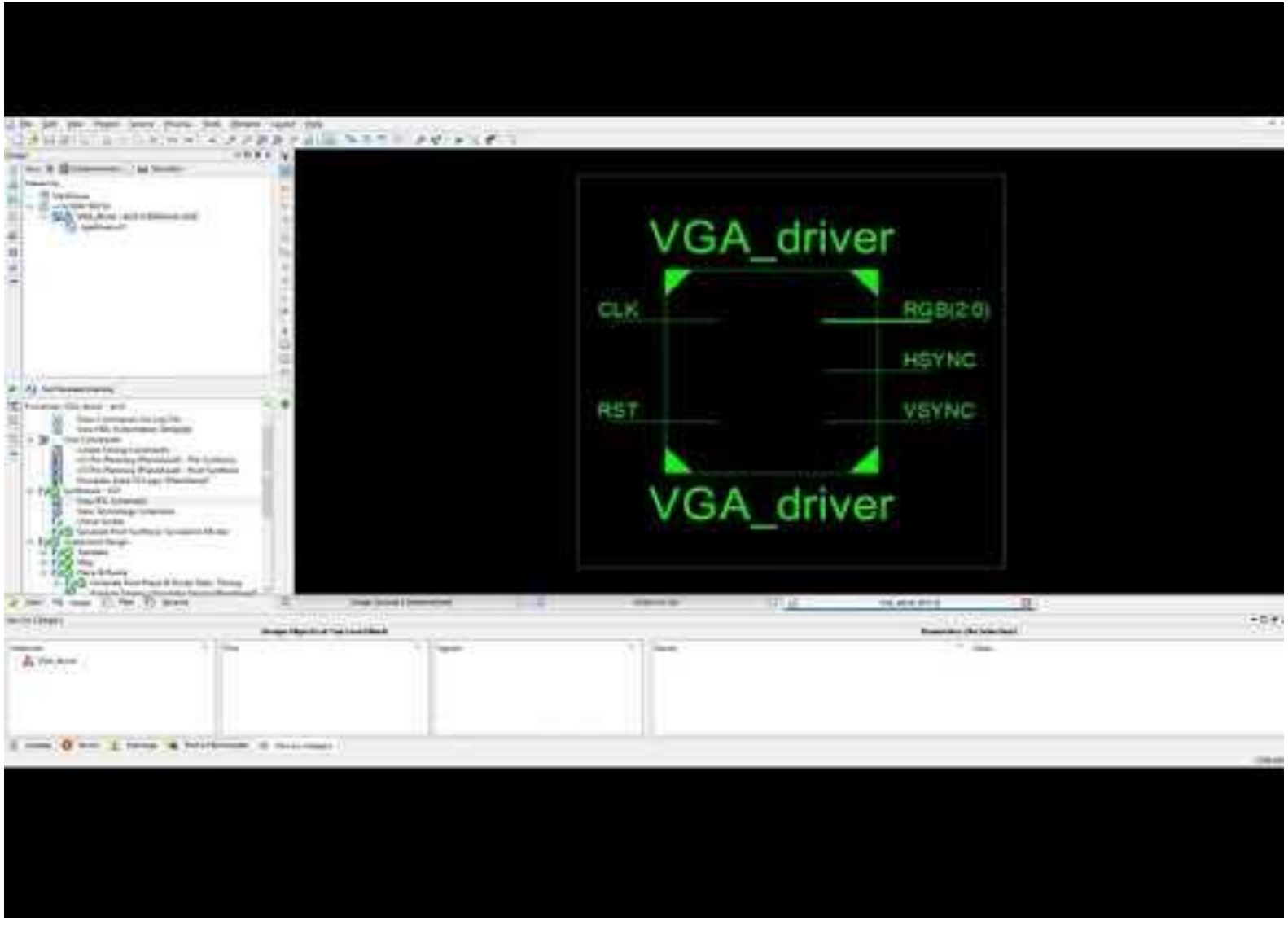
- testbench is toggling the clock every 5ns and the reset every 100ns

RTL Schematic I

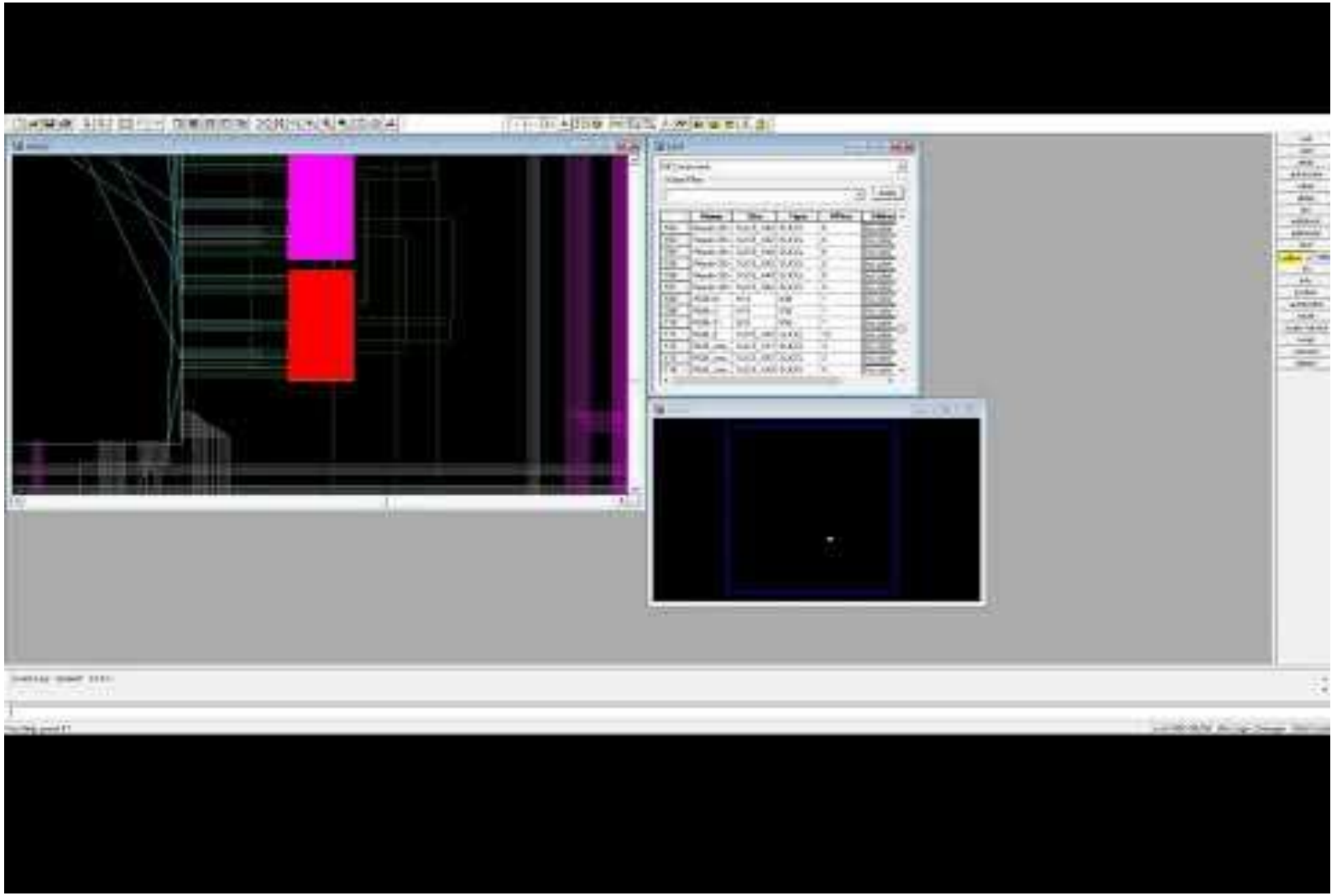
```
1  NET "CLK" LOC = "C9" |IOSTANDARD = LVCMOS33 ;
2  NET "RST" LOC = "P14" ;
3
4  NET "RGB<0>" LOC = "H14" |IOSTANDARD = LVTTL |DRIVE = 8 |SLEW = FAST ;
5  NET "RGB<1>" LOC = "H15" |IOSTANDARD = LVTTL |DRIVE = 8 |SLEW = FAST ;
6  NET "RGB<2>" LOC = "G15" |IOSTANDARD = LVTTL |DRIVE = 8 |SLEW = FAST ;
7  NET "HSYNC" LOC = "F15" |IOSTANDARD = LVTTL |DRIVE = 8 |SLEW = FAST ;
8  NET "VSYNC" LOC = "F14" |IOSTANDARD = LVTTL |DRIVE = 8 |SLEW = FAST ;
9
```



RTL Schematic II

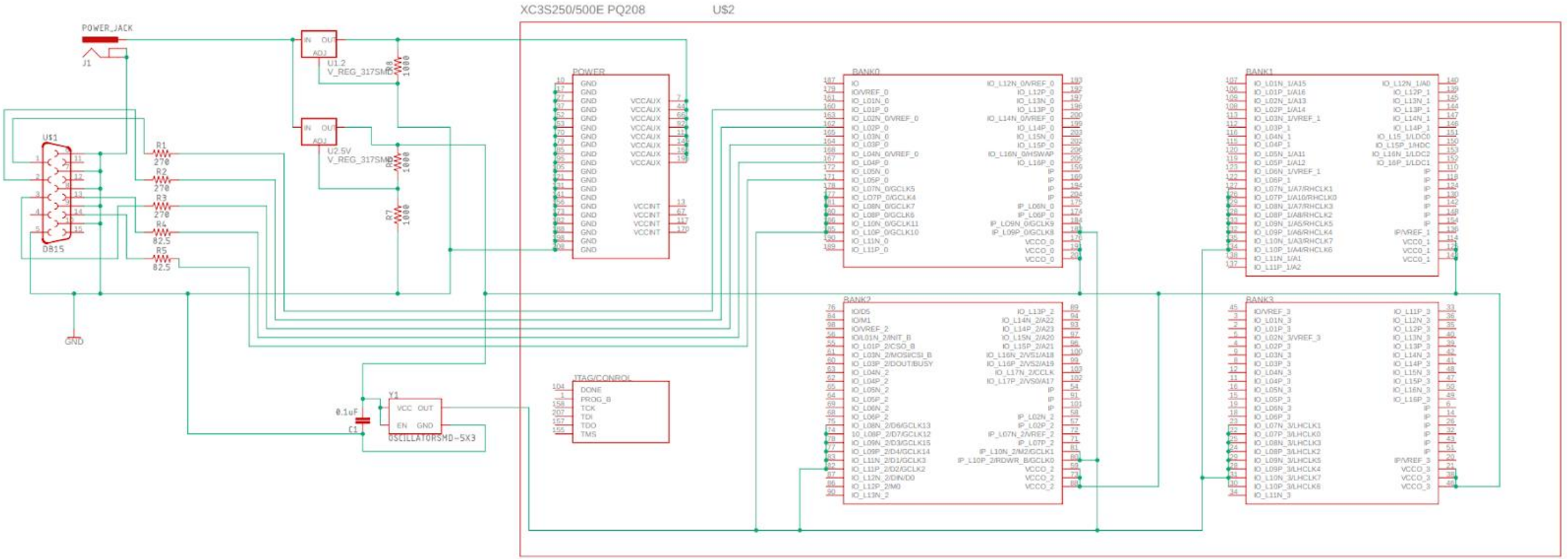


Routed Design



PCB schematic

- Spartan 3E from Xilinx
- Two 317 voltage regulators (2.5 and 1.2 volts)
- Oscillator is providing a 25 MHz clock signal

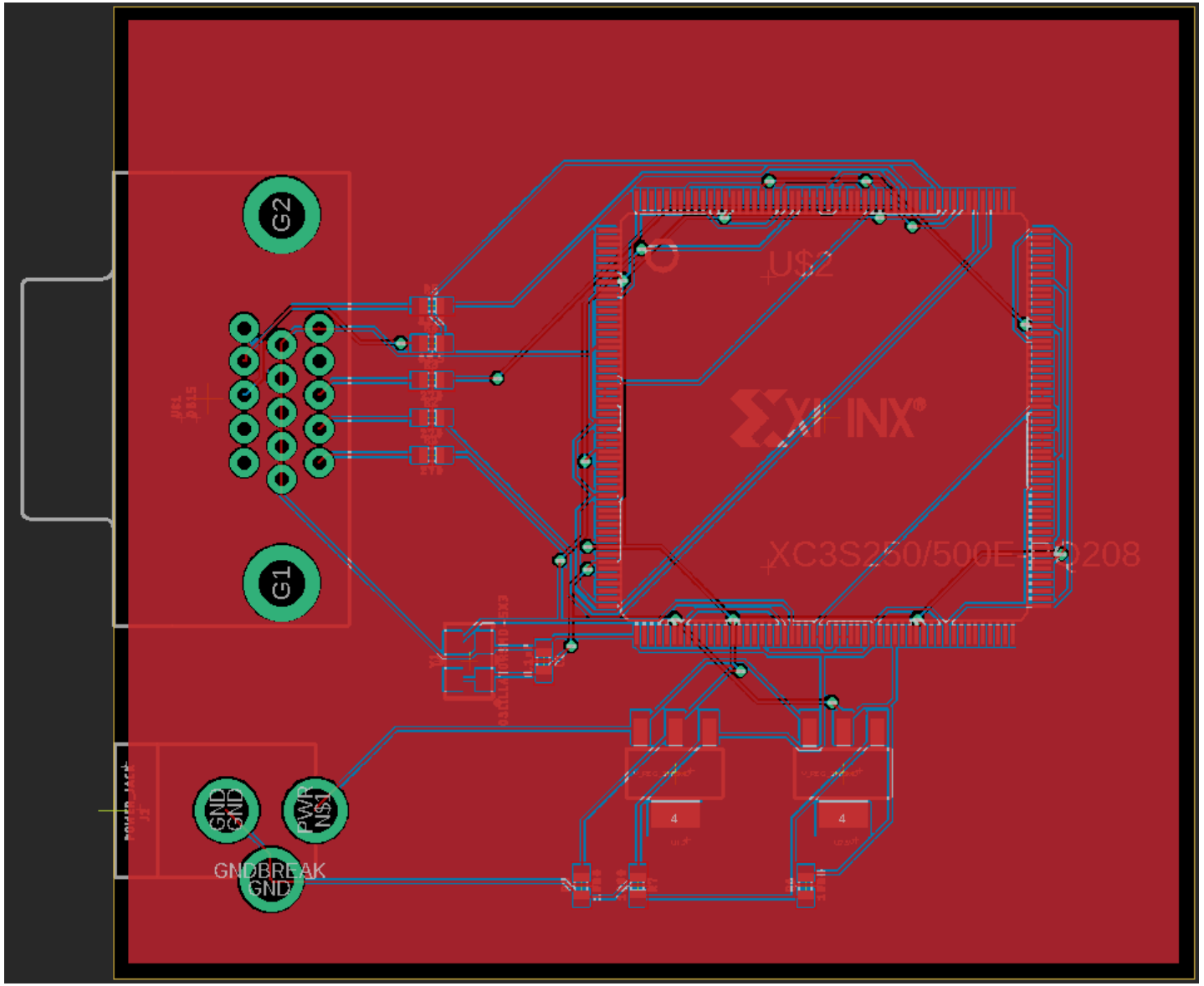


PCB layout

- Width: 80.1 mm
- Length: 67.5 mm

Part	Value	Package	Cost
C1	0.1 uF	0603	0.10€
J1	PW_Jack		0.62€
R1-3	270 Ohm	0603	0.55€ (10 pieces)
R4-5	82.5 Ohm	0603	0.50€ (5 pieces)
R6-8	1000 Ohm	0603	0.45€ (10 pieces)
U$2			22.07€
V_REG	317SMD	SOT223	1.30€ (2 pieces)
Y1			1.68€

Total cost for the components: €27.27
PCB: ~€4.74 (with shipping ~€25)



Conclusion

- VGA Concepts examined
- Succesfully implemented in VHDL
- PCB Schematic explored
- Ready for FPGA Implementation