

VGA_driver Project Status (06/23/2022 - 16:08:54)			
Project File:	VGADriver.xise	Parser Errors:	No Errors
Module Name:	VGA_driver	Implementation State:	Programming File Generated
Target Device:	xc3s1000-5ft256	• Errors:	No Errors
Product Version:	ISE 14.7	• Warnings:	No Warnings
Design Goal:	Balanced	• Routing Results:	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	All Constraints Met
Environment:	System Settings	• Final Timing Score:	0 (Timing Report)

Device Utilization Summary					[-]
Logic Utilization	Used	Available	Utilization	Note(s)	
Number of Slice Flip Flops	69	15,360	1%		
Number of 4 input LUTs	181	15,360	1%		
Number of occupied Slices	134	7,680	1%		
Number of Slices containing only related logic	134	134	100%		
Number of Slices containing unrelated logic	0	134	0%		
Total Number of 4 input LUTs	253	15,360	1%		
Number used as logic	181				
Number used as a route-thru	72				
Number of bonded IOBs	7	173	4%		
Number of BUFGMUXs	2	8	25%		
Average Fanout of Non-Clock Nets	3.28				

Performance Summary				[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	Pinout Data:	Pinout Report	
Routing Results:	All Signals Completely Routed	Clock Data:	Clock Report	
Timing Constraints:	All Constraints Met			

Detailed Reports						[-]
Report Name	Status	Generated	Errors	Warnings	Infos	
Synthesis Report	Current	Thu Jun 23 13:20:40 2022	0	0	1 Info (1 new)	
Translation Report	Current	Thu Jun 23 16:06:56 2022	0	0	0	
Map Report	Current	Thu Jun 23 16:07:02 2022	0	0	2 Infos (0 new)	
Place and Route Report	Current	Thu Jun 23 16:07:15 2022	0	0	2 Infos (0 new)	
Power Report						
Post-PAR Static Timing Report	Current	Thu Jun 23 16:07:20 2022	0	0	6 Infos (0 new)	
Bitgen Report	Current	Thu Jun 23 16:08:51 2022	0	0	1 Info (1 new)	

Secondary Reports			[-]
Report Name	Status	Generated	
Post-Synthesis Simulation Model Report	Current	Thu Jun 23 15:25:31 2022	
WebTalk Report	Current	Thu Jun 23 16:08:52 2022	
WebTalk Log File	Current	Thu Jun 23 16:08:54 2022	

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