# Work Package #5

1. Implement and simulate a 4-bit full adder using 1-bit half adders as components.
2. Research carry lookahead adder, implement and simulate an 8-bit carry lookahead adder (structural & behavioral).
3. Implement and simulate a circuit whose input is a decimal number and its output is the same number in negbinary.
4. Implement and simulate an 8-bit unsigned Arithmetic Logic Unit (in structural VHDL) capable of the following functions:
    a. Addition
    b. Subtraction
    c. Multiplication
    d. Comparison

# Work Package #6

1. What is the main difference between a level sensitive element and an edge sensitive element?
2. Implement and simulate an 8-bit SISO Shift Register with a clock enable signal.
3. Implement and simulate a 32-bit SISO Shift Register with asynchronous parallel load.
4. What are the main advantages and disadvantages of synchronous designs?
5. What are the main advantages and disadvantages of asynchronous designs?
6. Implement and simulate the 8-bit counter from the examples and pinpoint a potential problem with its functionality.
7. Implement and simulate the following FSMs: