VHDL Basics

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Work Package #1

1. Design a behavioral and a structural view model for a 4-bit full adder.
2. What is an even parity decision circuit and where do we use it?
3. What are the main differences between structural description and behavioral description in VHDL?
4. What is dataflow description in VHDL?
5. Which signals must be included at the sensitivity list of a process?

Work Package #2

1. Why do we use packages in VHDL descriptions?
2. What are the main differences between the std_logic_1164 and bit data types in VHDL?
3. Give a simple example explaining the functionality of the following operators: sll, sla, ror and rol.

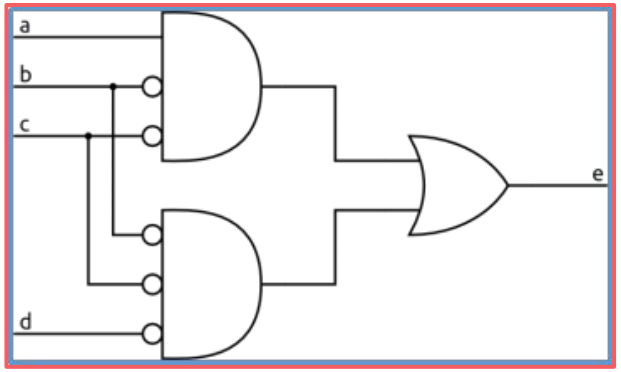
Work Package #3

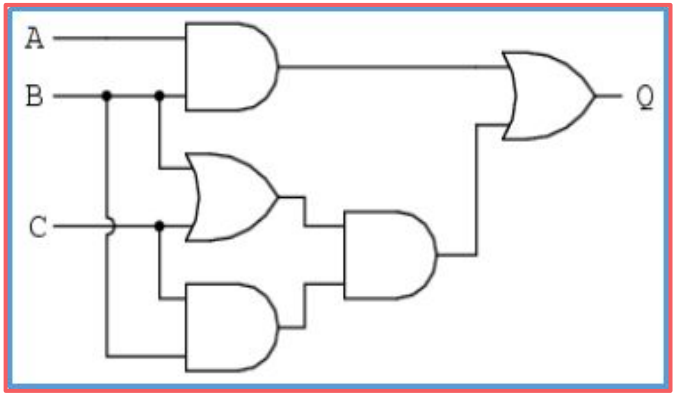
1. Research .do files in ModelSim.
2. What are they used for?
3. Write a .do file for a simple design and explain the simulation process using the .do file.

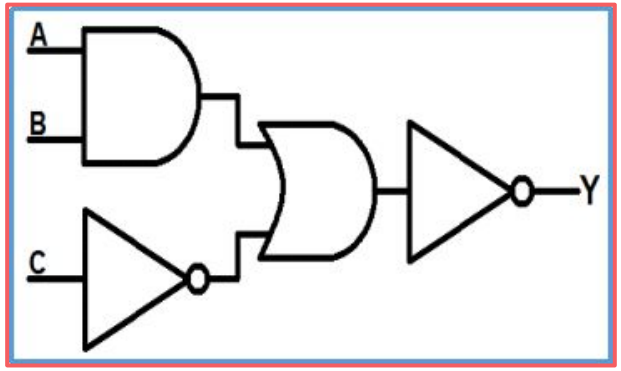
Work Package #4

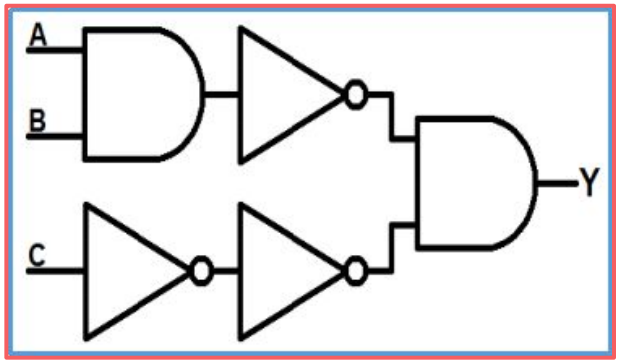
1. Implement and simulate the following designs (behavioral & dataflow):
    a. NAND2
    b. NOR3
    c. XNOR2
2. Implement and simulate the following designs (structural, behavioral, dataflow):

Work Package #4 (cont.)









Work Package #4 (cont.)