BER timing scans in SciFi

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Timing Scans

Aim: Tune the relative phases of various clocks in SciFi electronics to achieve low transmission error rates

- Scan range of time settings for a clock
- Send pseudo-random bit pattern
- Return bit error counters
- Calculate common error-free intervals

Analysis code on gitlab (with README)
Documentation: twiki, note

Timing Scans

Two types of timing scans:

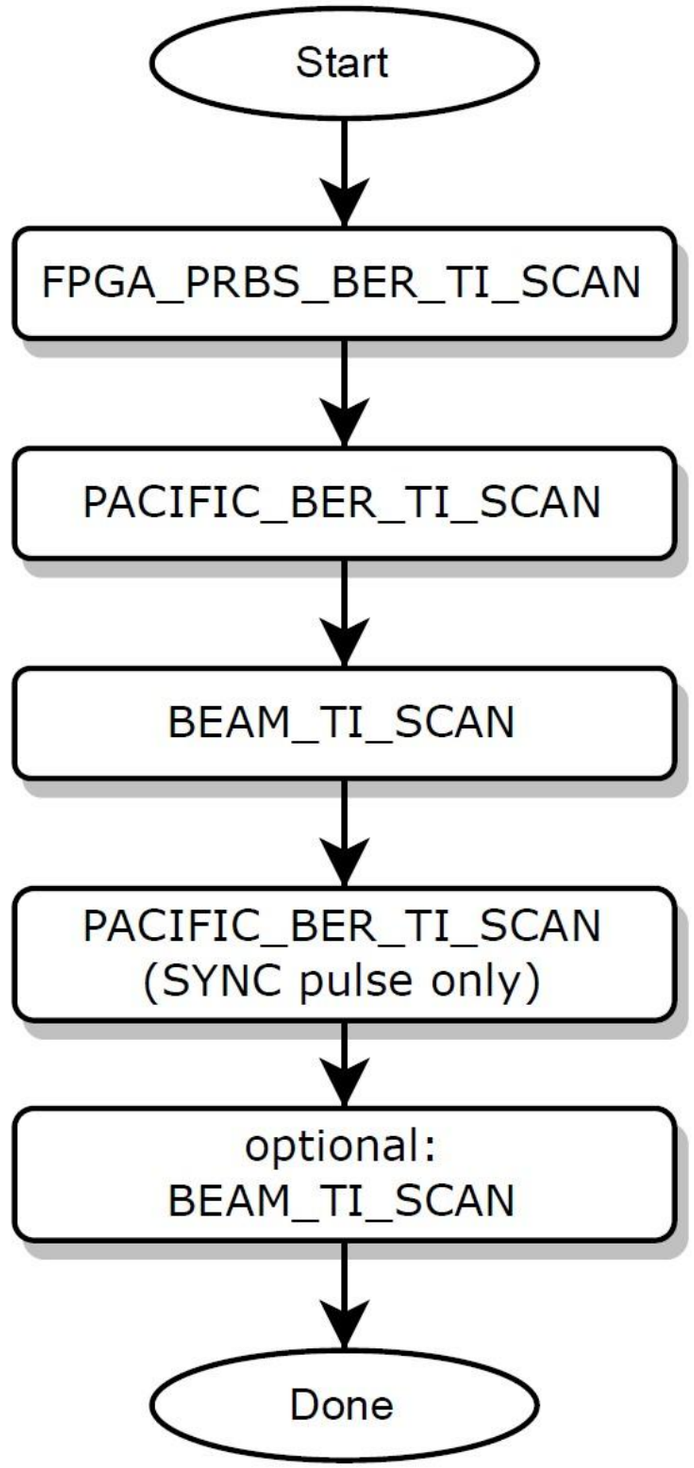
BER timing scans

internal data transmission in front-end electronics

This presentation

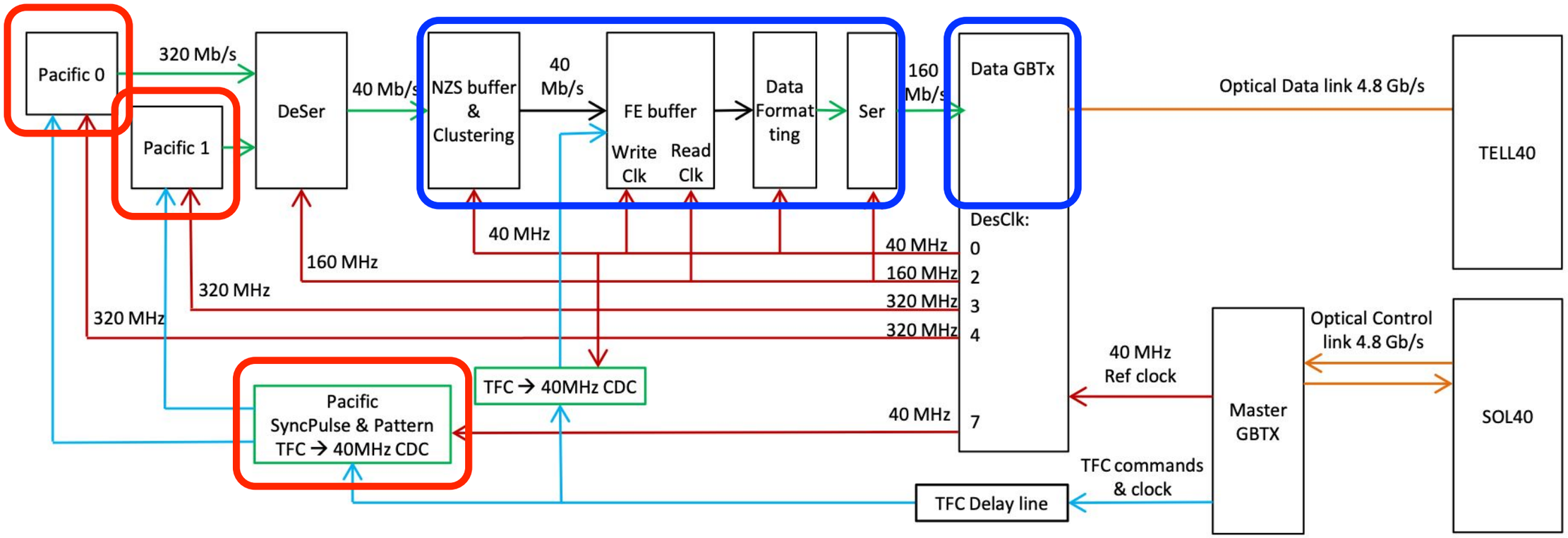
Beam timing scans

time align data taking and processing to LHC collision



Timing Scans

Tune the relative phases of various clocks in SciFi electronics to achieve low transmission error rates



FPGA_PRBS_BER_TI scan

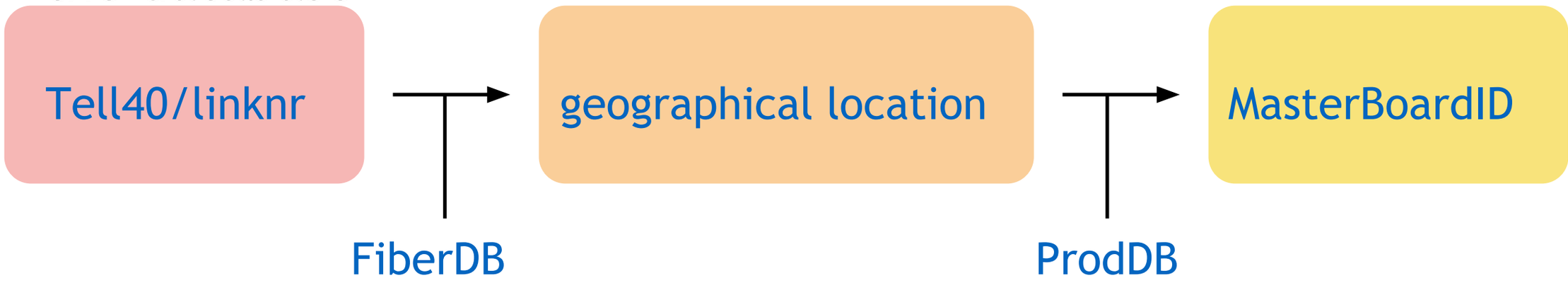
PACIFIC_BER_TI scan

Procedure

Per TELL40, a csv file with bit error rates is created by the scan.

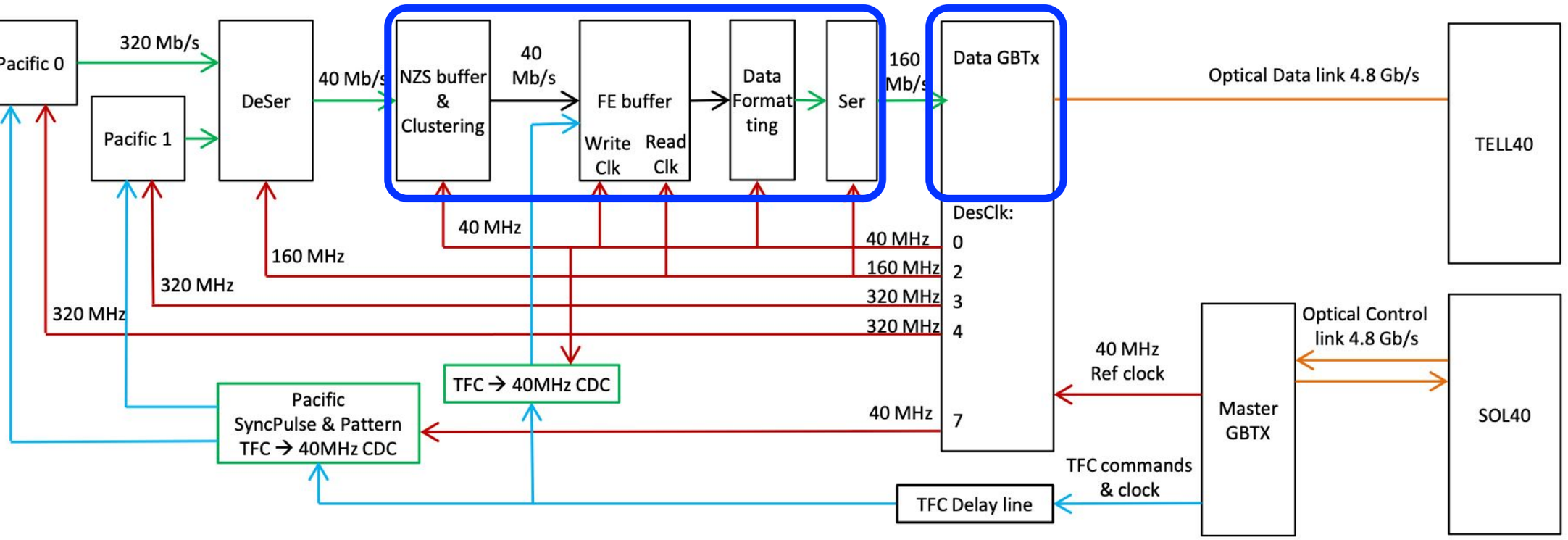
Want to find clock delay settings per GBT link.

- Find error-free step intervals and calculate the width and center
- Map TELL40 links to MasterBoard ID to enable importing results to the database



- Create XML file with scan results per TELL40.
  - If no common interval is found, create empty XML entry
  - Format according to twiki.

FPGA scans



FPGA_PRBS_BER_TI scan

BER and FPGA PRBS

- FPGA scan done by sending pseudorandom binary sequence (PRBS)
- 7-bits x 16
- Pseudorandom -> response predicted by TELL40 backend
  - Compare output with expectation
  - Count number of wrong bits
- Bit Error Rate (BER)
  - # bit errors / # total bits transmitted
  - In ideal situation, BER = 0

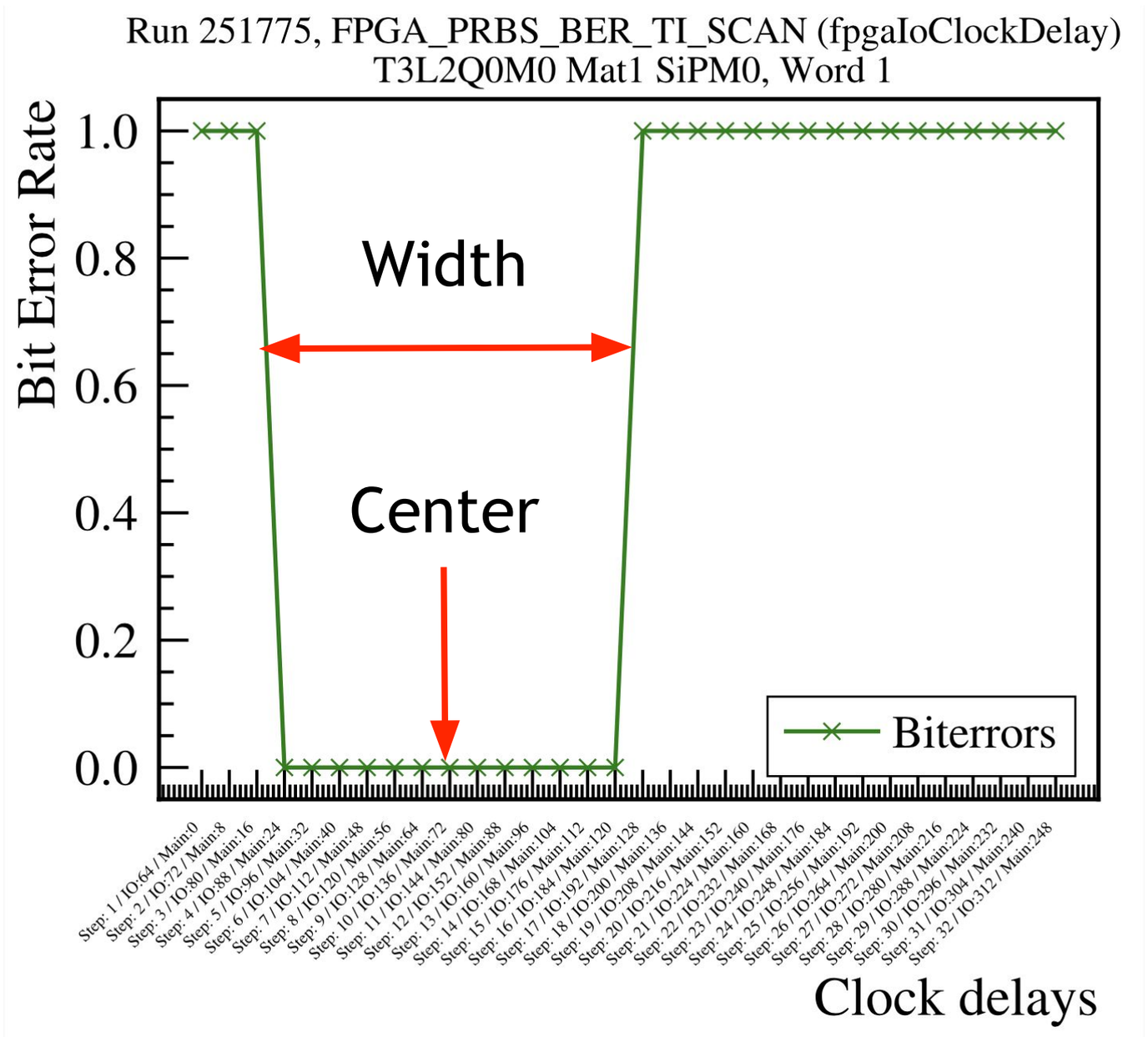
FPGA scans

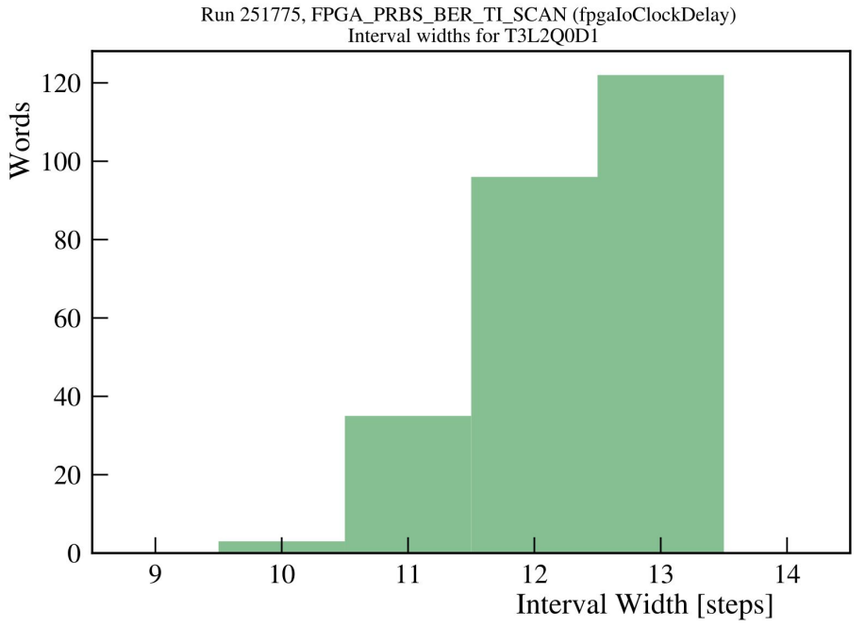
- Goal: find clock setting region with BER 0
  - Find center and width of the error-free region

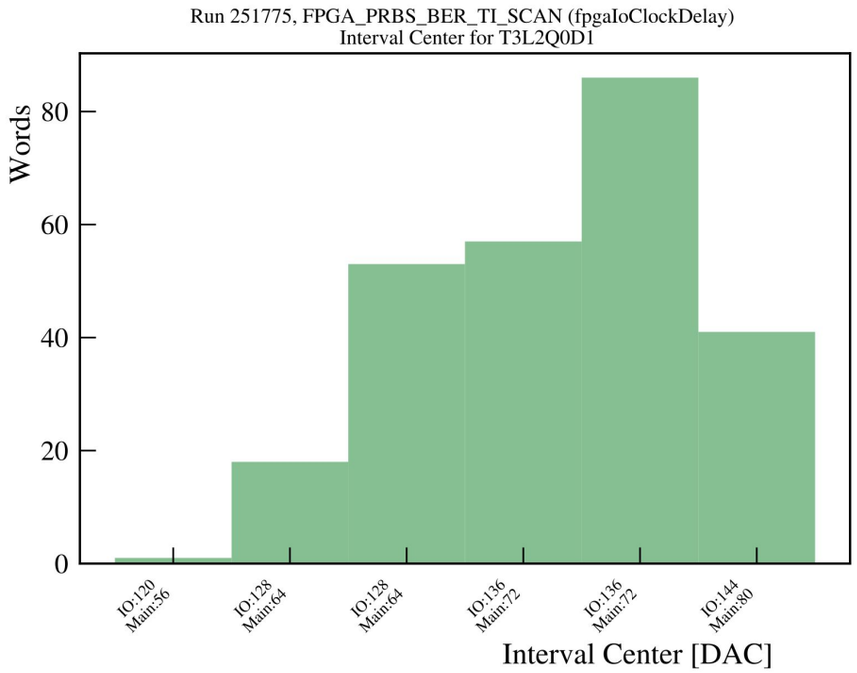
- Timing scan divided in 2 parts:
  1. fpgaIoClockDelay & fpgaMainClockDelay
     Phase between clocks kept constant
  2. fpgaMainClockDelay
     fpgaIoClockDelay fixed

- Compare fixed clock value from 2 with best value found in 1
  - Do they agree?

FPGA scans


Run 251775, FPGA_PRBS_BER_TI_SCAN (fpgaIoClockDelay)
T3L2Q0M0 Mat1 SiPM0, Word 1
Bit Error Rate
1.0
0.8
0.6
0.4
0.2
0.0
Width
Center
Biterrors
Step: 1 / IO:64 / Main:0
Step: 2 / IO:72 / Main:8
Step: 3 / IO:80 / Main:16
Step: 4 / IO:88 / Main:24
Step: 5 / IO:96 / Main:32
Step: 6 / IO:104 / Main:40
Step: 7 / IO:112 / Main:48
Step: 8 / IO:120 / Main:56
Step: 9 / IO:128 / Main:64
Step: 10 / IO:136 / Main:72
Step: 11 / IO:144 / Main:80
Step: 12 / IO:152 / Main:88
Step: 13 / IO:160 / Main:96
Step: 14 / IO:168 / Main:104
Step: 15 / IO:176 / Main:112
Step: 16 / IO:184 / Main:120
Step: 17 / IO:192 / Main:128
Step: 18 / IO:200 / Main:136
Step: 19 / IO:208 / Main:144
Step: 20 / IO:216 / Main:152
Step: 21 / IO:224 / Main:160
Step: 22 / IO:232 / Main:168
Step: 23 / IO:240 / Main:176
Step: 24 / IO:248 / Main:184
Step: 25 / IO:256 / Main:192
Step: 26 / IO:264 / Main:200
Step: 27 / IO:272 / Main:208
Step: 28 / IO:280 / Main:216
Step: 29 / IO:288 / Main:224
Step: 30 / IO:296 / Main:232
Step: 31 / IO:304 / Main:240
Step: 32 / IO:312 / Main:248
Clock delays

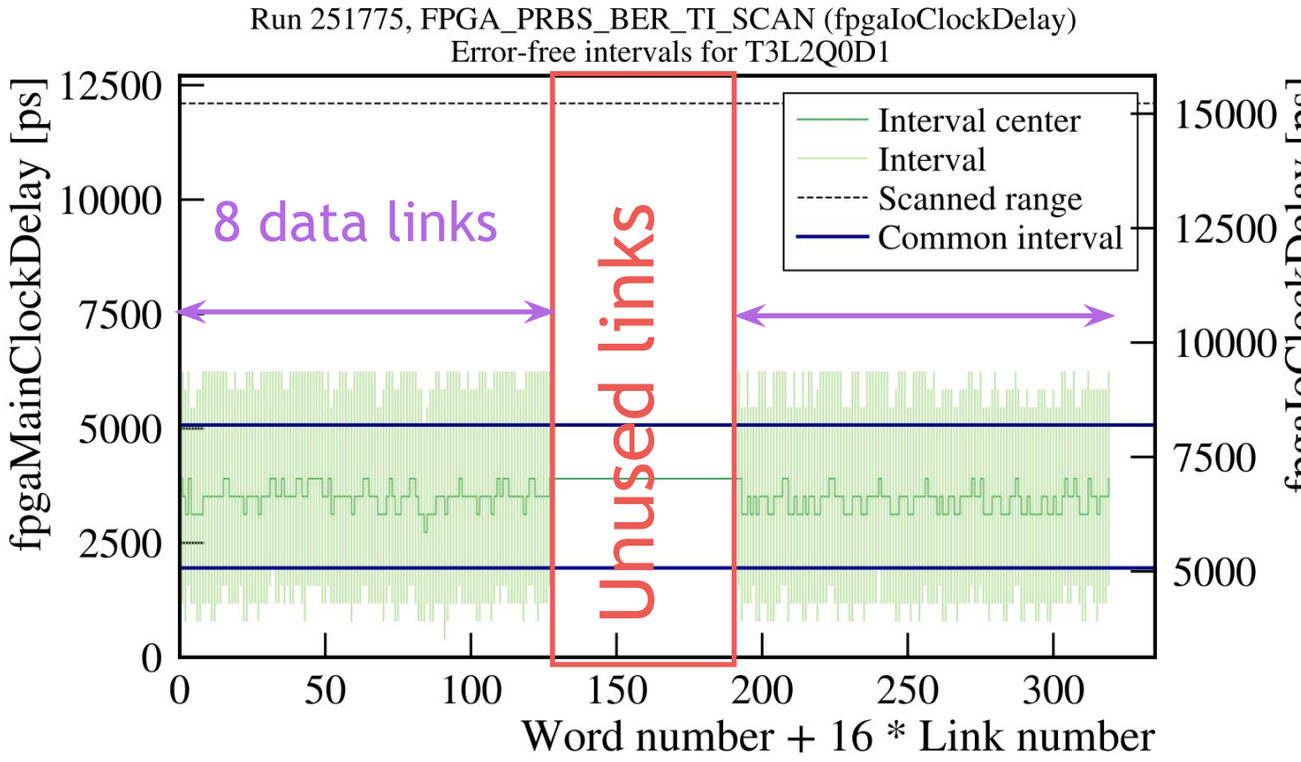

Run 251775, FPGA_PRBS_BER_TI_SCAN (fpgaIoClockDelay)
Interval widths for T3L2Q0D1
Words
120
100
80
60
40
20
0
9
10
11
12
13
14
Interval Width [steps]


Run 251775, FPGA_PRBS_BER_TI_SCAN (fpgaIoClockDelay)
Interval Center for T3L2Q0D1
Words
80
60
40
20
0
IO:120 Main:56
IO:128 Main:64
IO:128 Main:64
IO:136 Main:72
IO:136 Main:72
IO:144 Main:80
Interval Center [DAC]

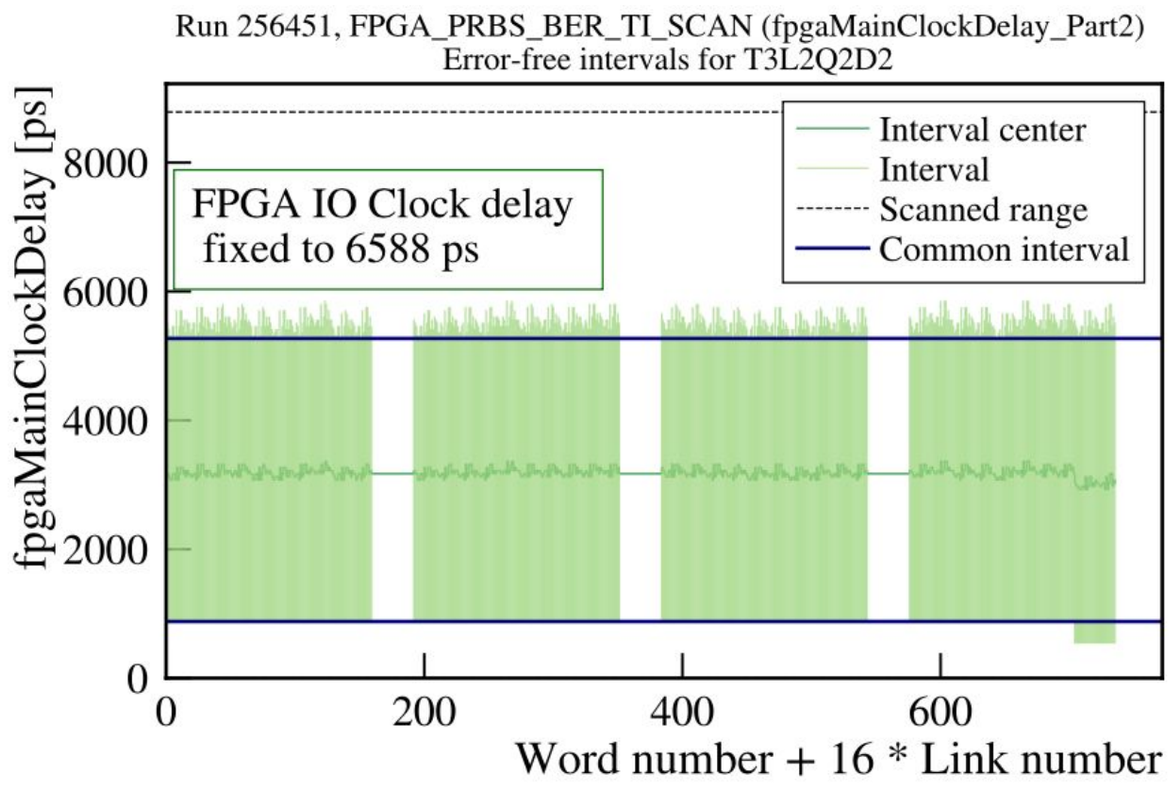
FPGA scans

Plots for one TELL40

Part 1: Find IO clock



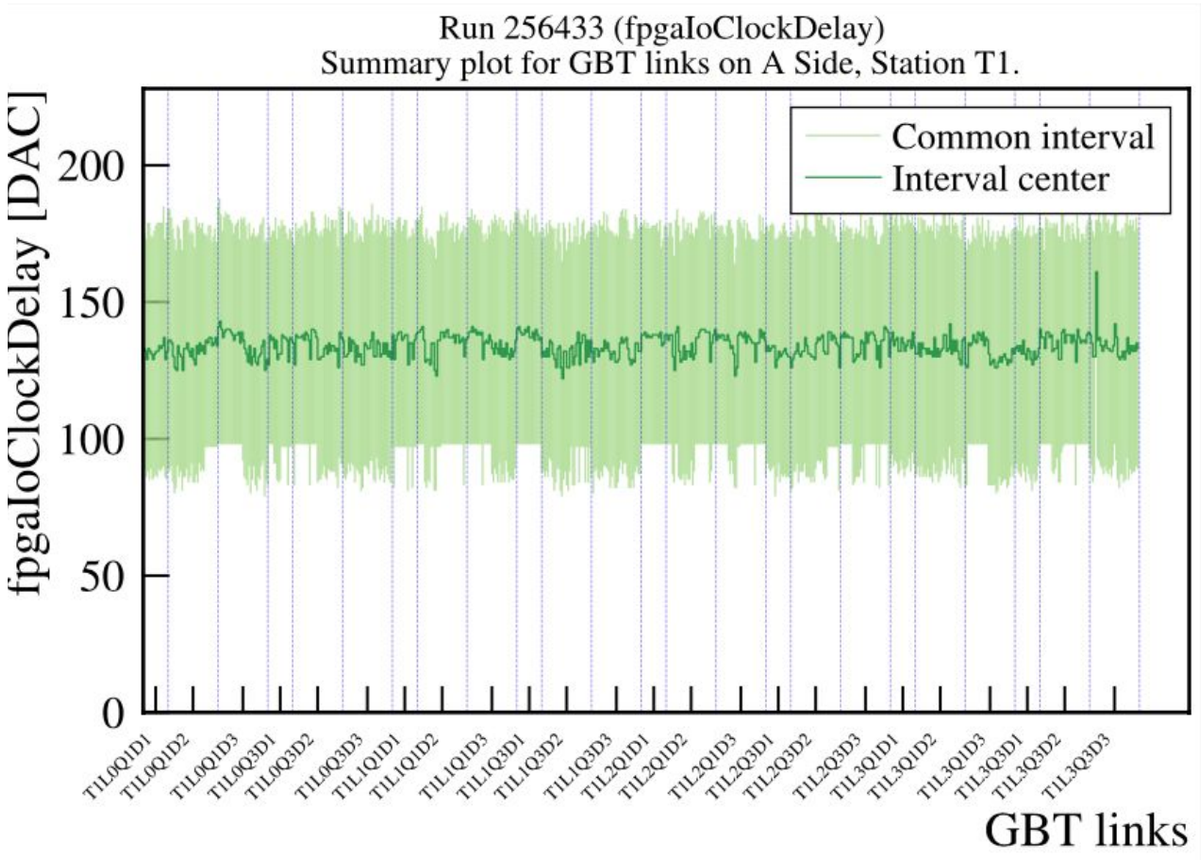
Part 2: Find Main clock using fixed IO

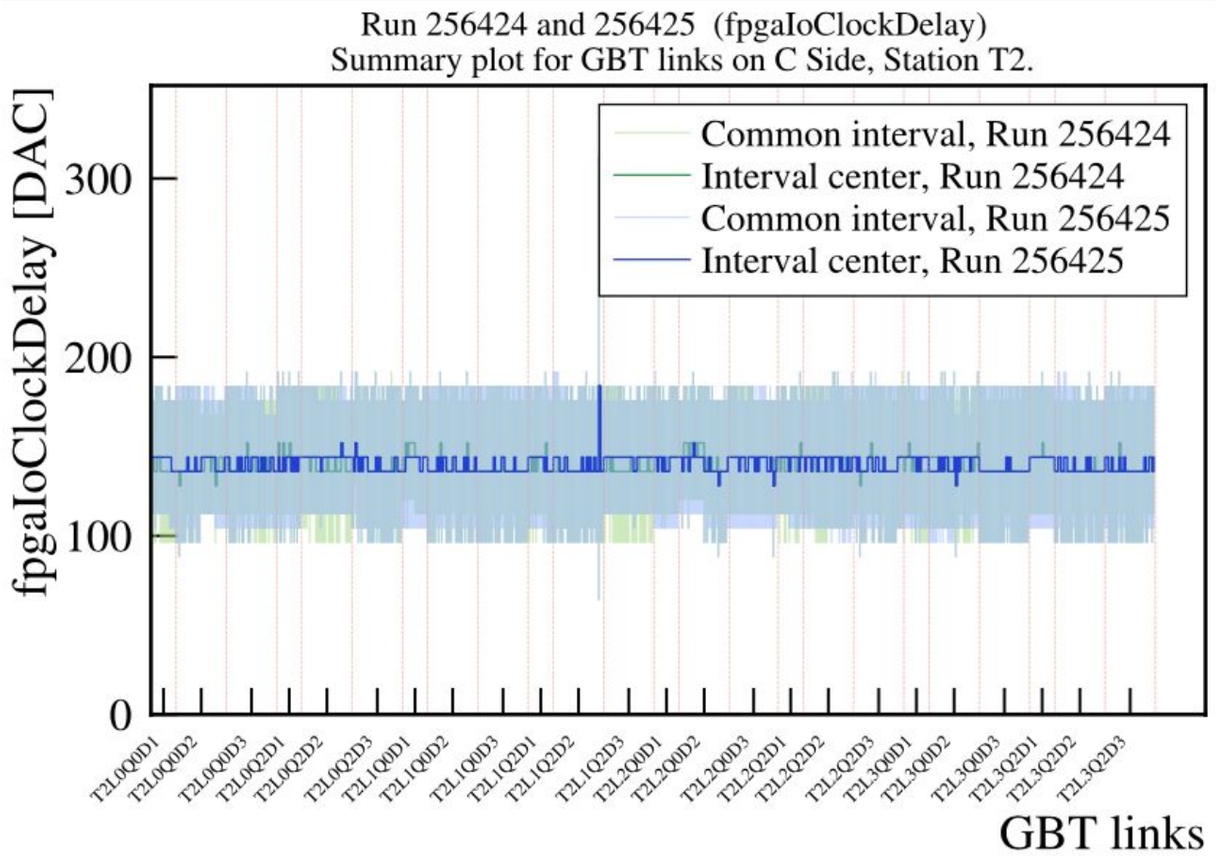


Part 3: Check if they match

Overview plots

- To check how stable timing settings are across the detector, create overview plots (6 plots, one per station and side)
- Also can be used to compare stability between runs.

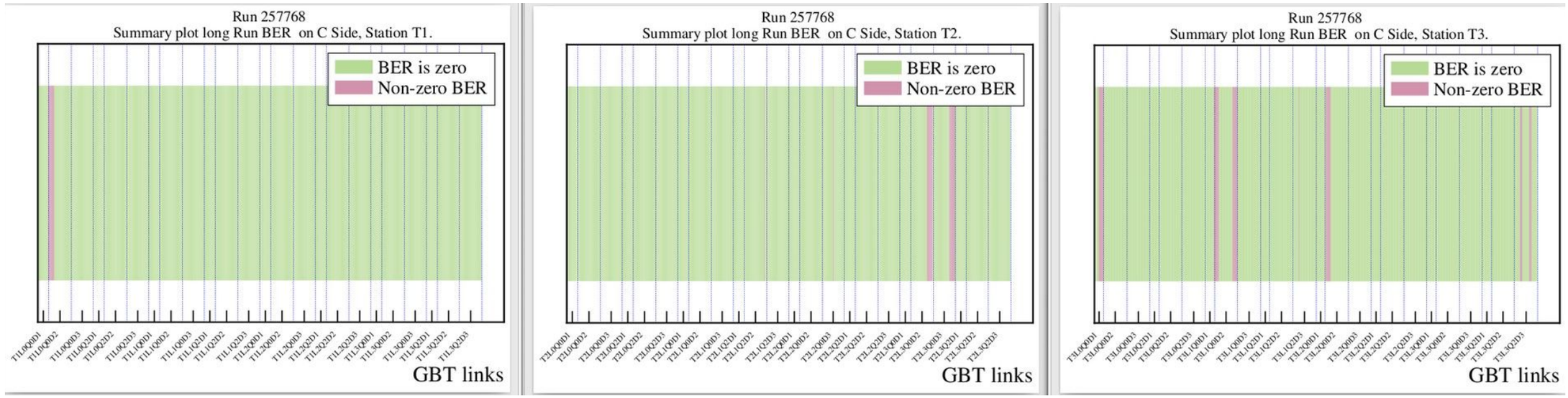




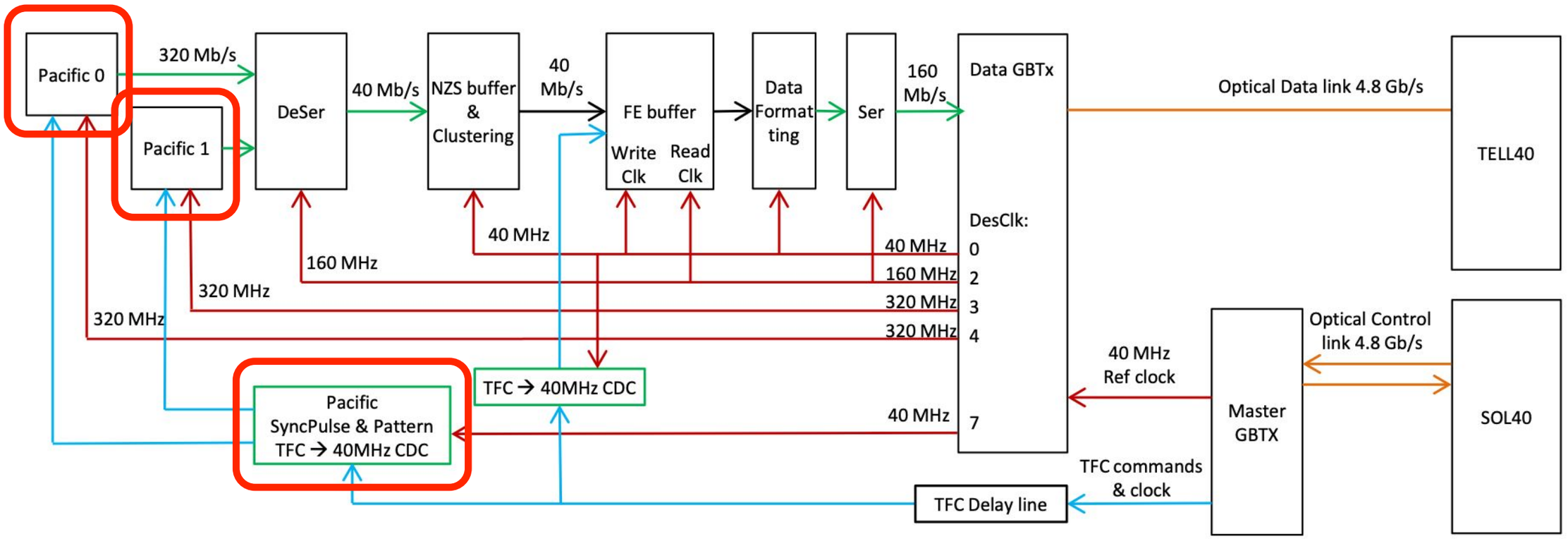
FPGA scans

- Find median and std. dev for whole detector
  - FPGA IO clock: 135 +- 4 [DAC]
  - FPGA main : 61 +- 2 [DAC]

- Check detector stability with long FPGA BER scan
  - Run overnight on "default" settings and best settings
  - First run last week with default settings
  - Analysis code in progress
  - Also look at SOL40 RX-ready



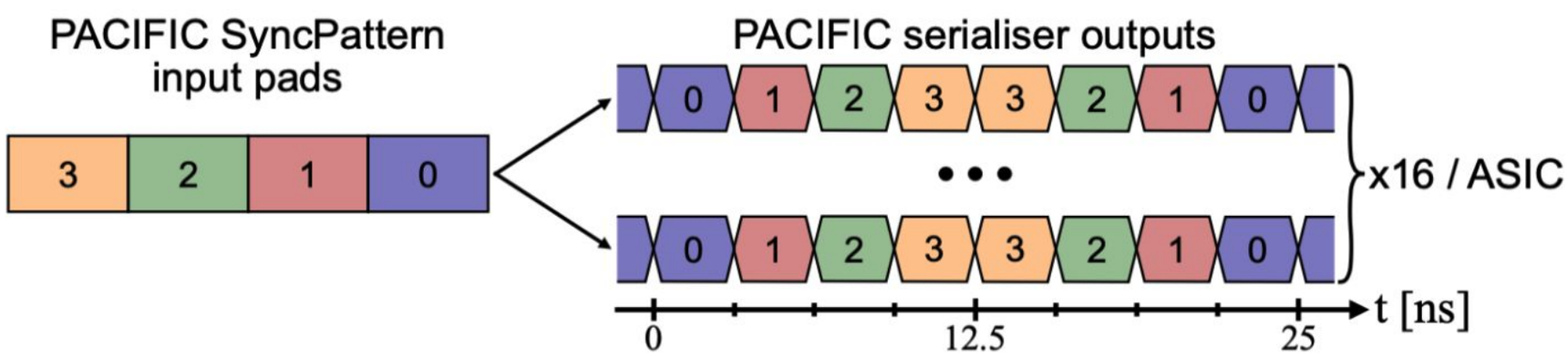
PACIFIC scans



PACIFIC_BER_TI scan

PACIFIC scans

- PACIFIC scan performed after FPGA scan
- FPGA delays fixed to best found values
- Two ASIC chips scanned simultaneously
- Also scan SyncPulse: align 320MHz clock with 40 MHz LHC clock
- Uses PACIFIC SyncPattern
  - 2 bits per channel -> 4 bits per PACIFIC output line
- Combined with itself -> detect 12.5 ns phase shifts
- Get a error count per SiPM channel



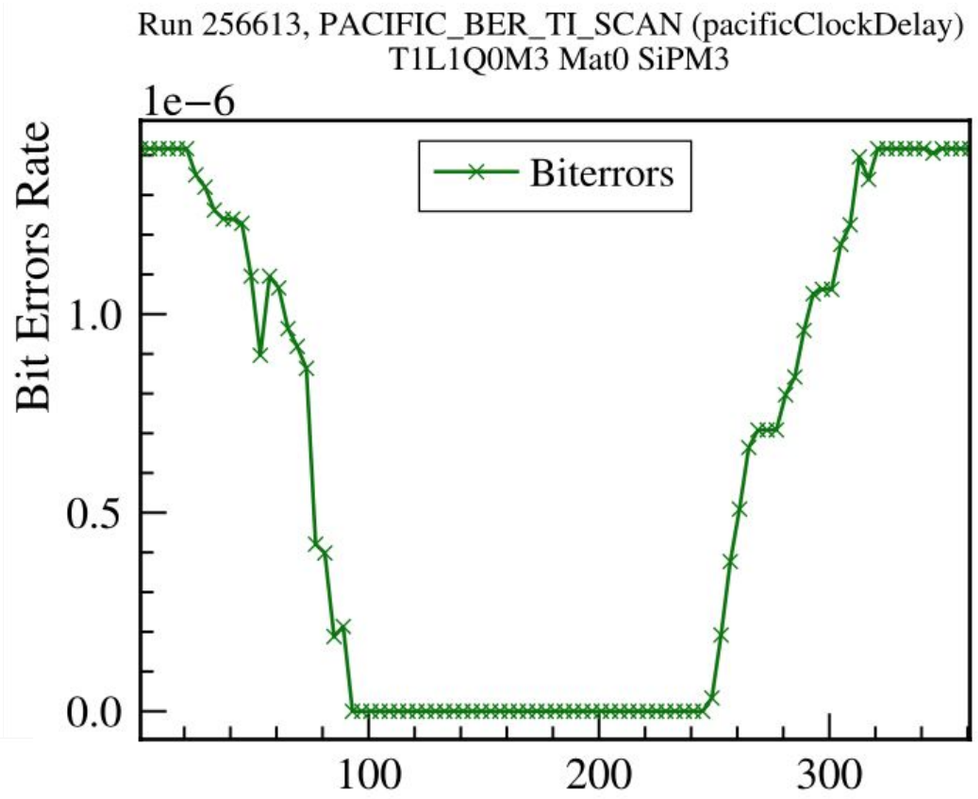
PACIFIC scans

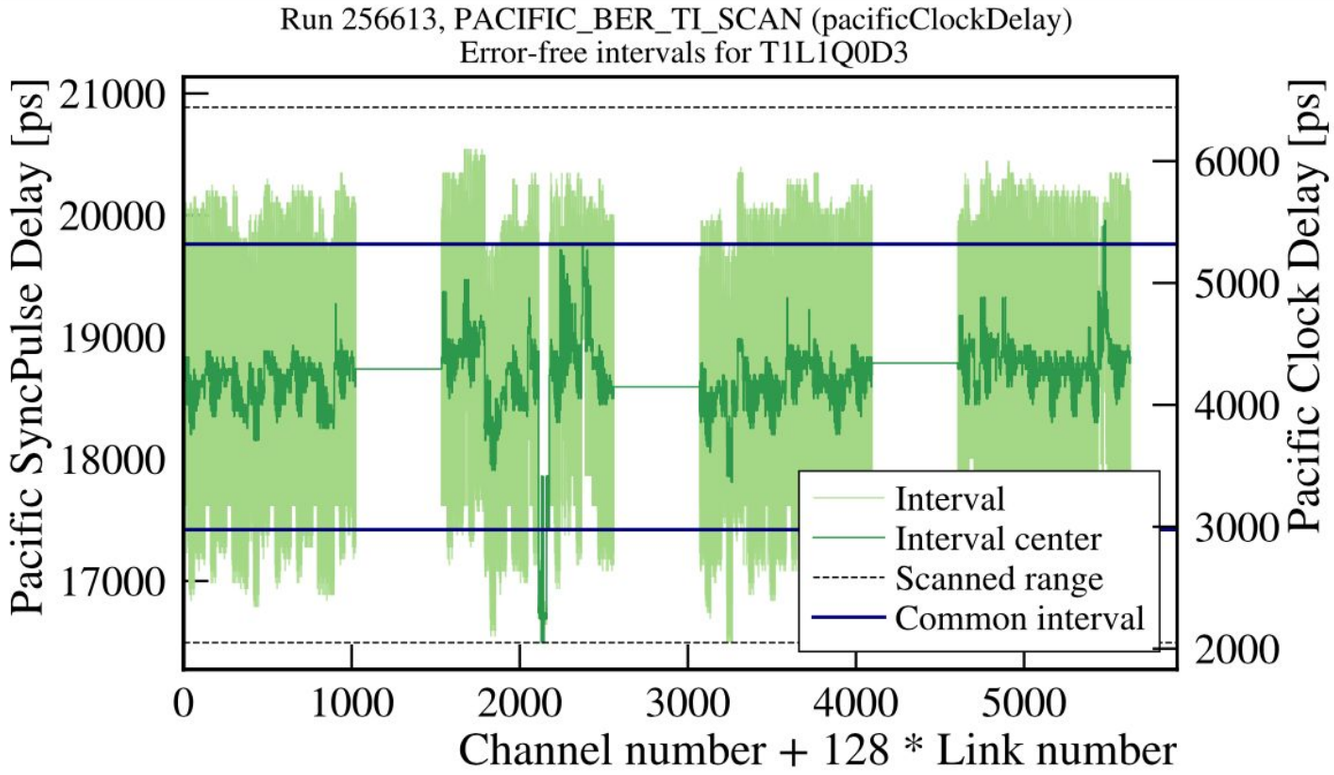
128 channels per data link.
Per counter we have

- Number of errors
- Is BER locked?
- Has BER lost lock?

0
Yes
No

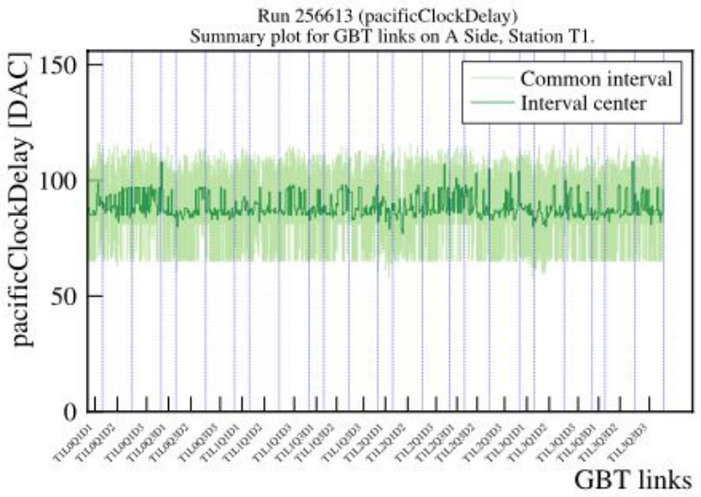
→ Error free counter!

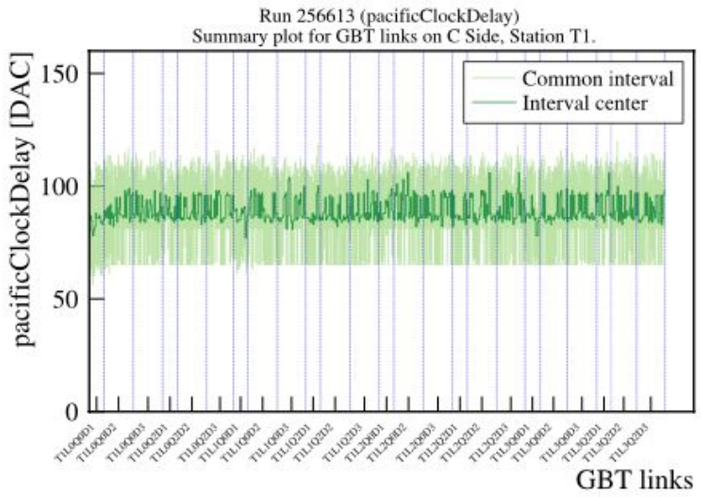


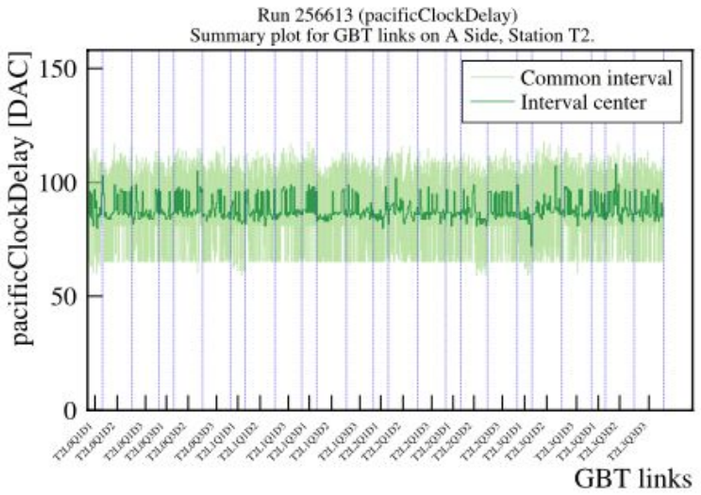


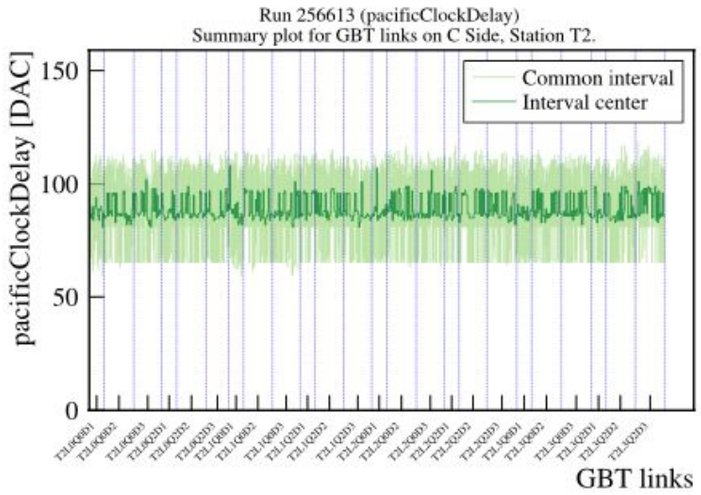
PACIFIC scans

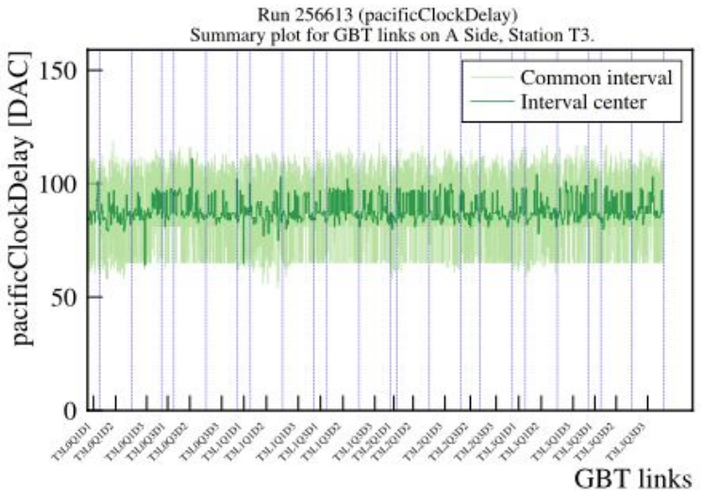
- Not as stable as FPGA clock scan
- Median: 87+-5 DAC

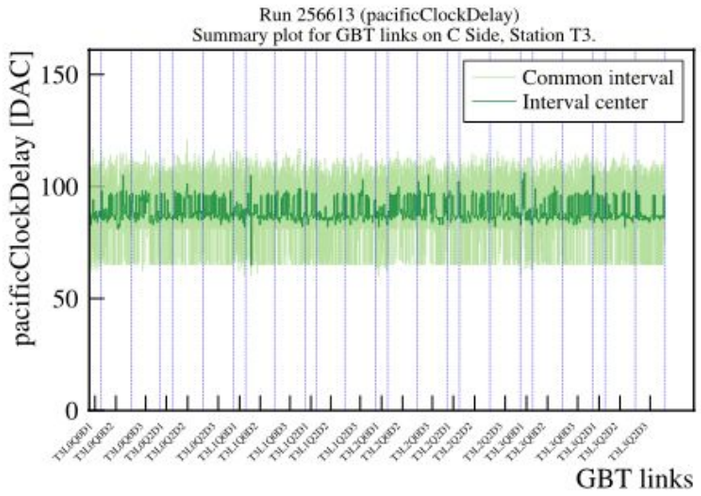








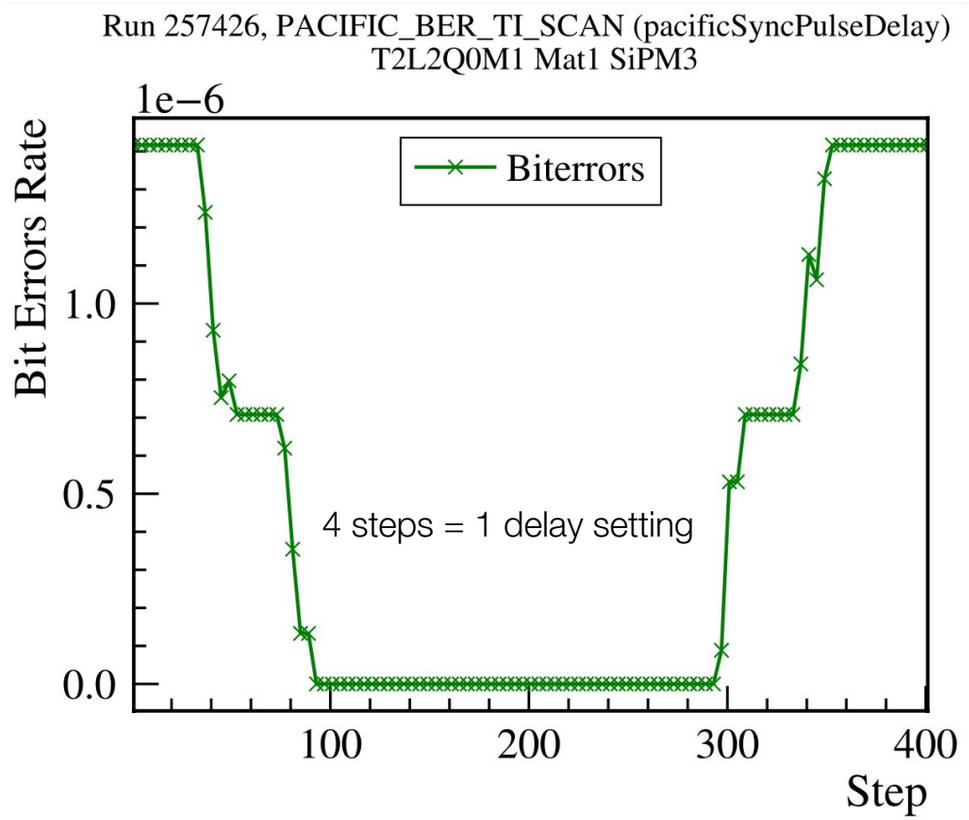




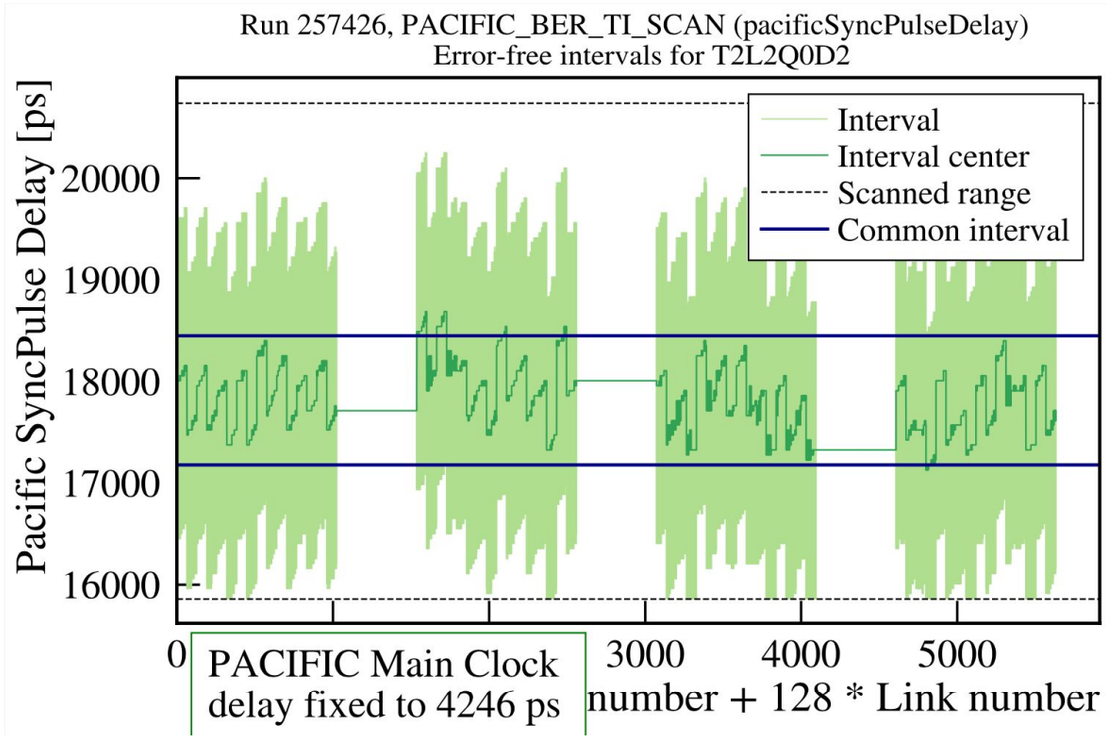
PACIFIC SyncPulse

Fix PACIFIC clock to best setting from last scan: 87+-5 DAC

Scan SyncPulse from 325 to 425 DAC
- Indicated error-free region from 4 DAC resolution scan on A side



- SyncPulse: 367 +- 6 [DAC]
- Zig-zag pattern in center of error-free region?



Conclusions

- All scans taken successfully.
  - Best settings for all clock delays found.
  - FPGA IO clock: 135 +- 4 [DAC]
  - FPGA main : 61 +- 2 [DAC]
  - PACIFIC clock : 87 +- 5 [DAC]
  - SyncPulse : 367 +- 6 [DAC]

- First stability check with long BER test taken last week. Analysis code for long tests in progress.

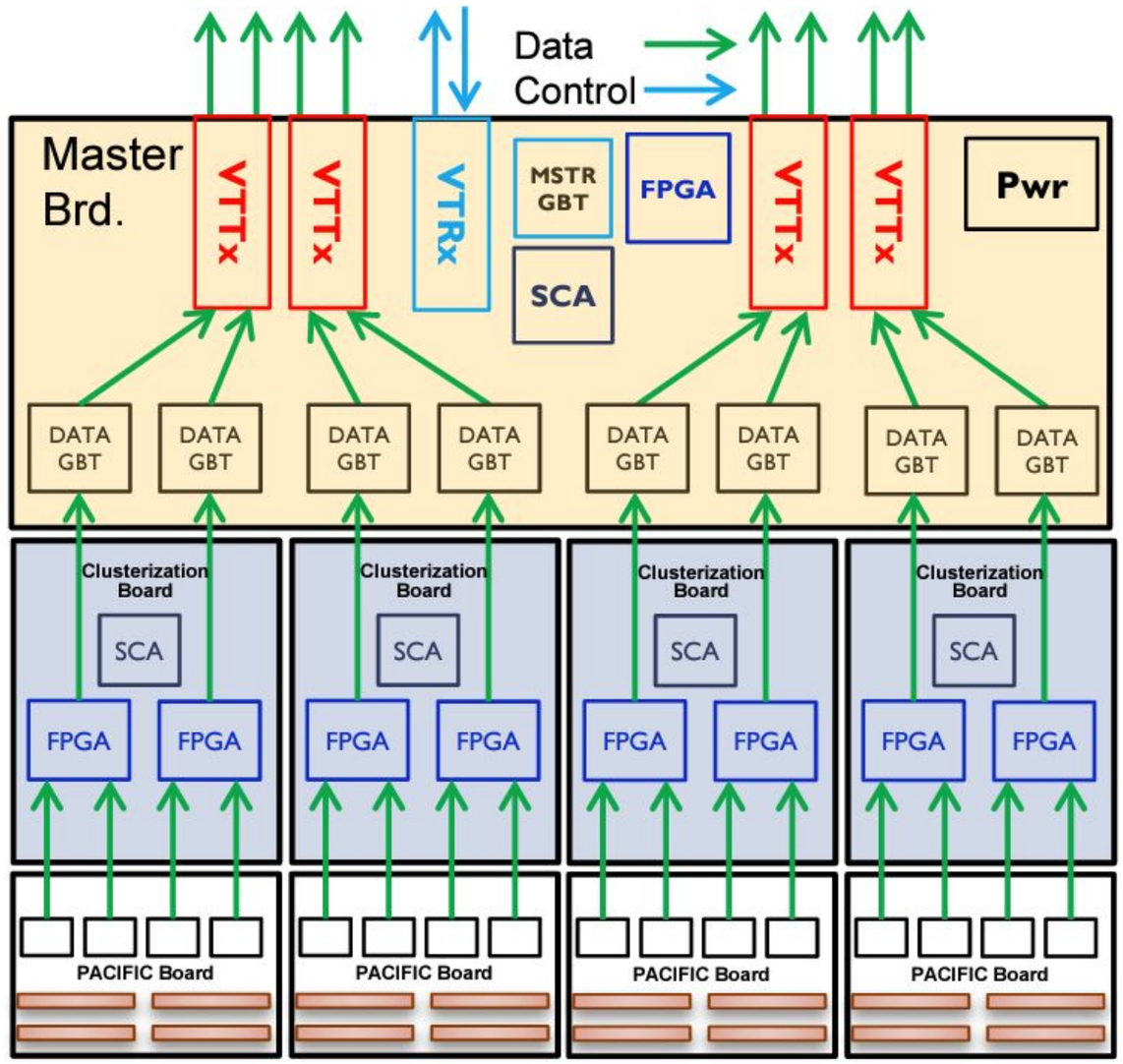
- To do:
  - Run PACIFIC SyncPulse scan for the entire detector
    - Check result compatibility
  - Further long BER runs

BACKUP

Dataflow and DAQ - Front End

Half-ROB instrumented with 8 SiPMs located on the top and bottom of SciFi modules:

- *4 PACIFIC Boards:* analog-to-digital conversion of SiPM signals
- *4 Cluster Boards:* FPGA's run the clusterisation algorithm
- *1 Master Board:* sends data to back-end DAQ system & sets clock values



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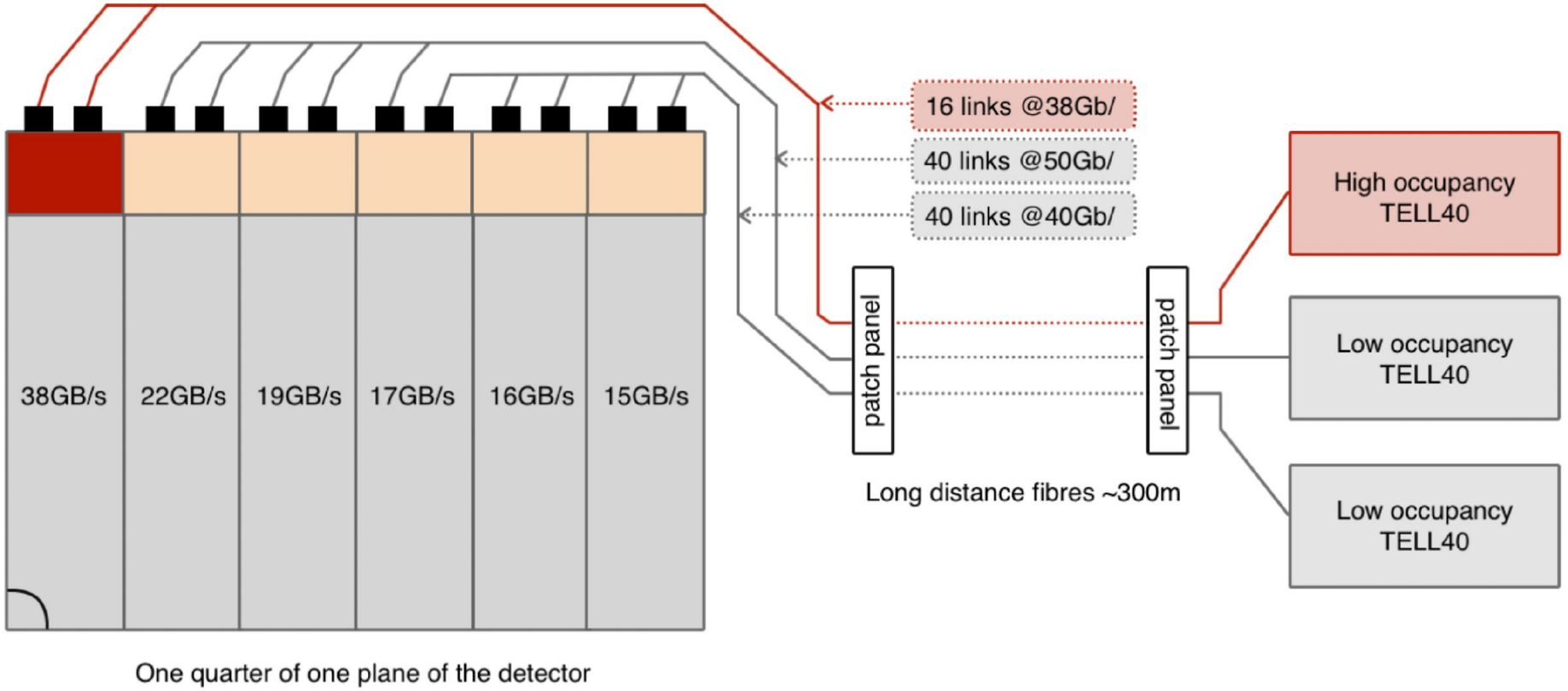
Dataflow and DAQ - Back End

- TELL40 boards read out data from the Front End
- Installed in data center, **not** downstairs

- *3 TELL40 boards per quarter:*
  1 *high* occ.
  2 *low* occ.

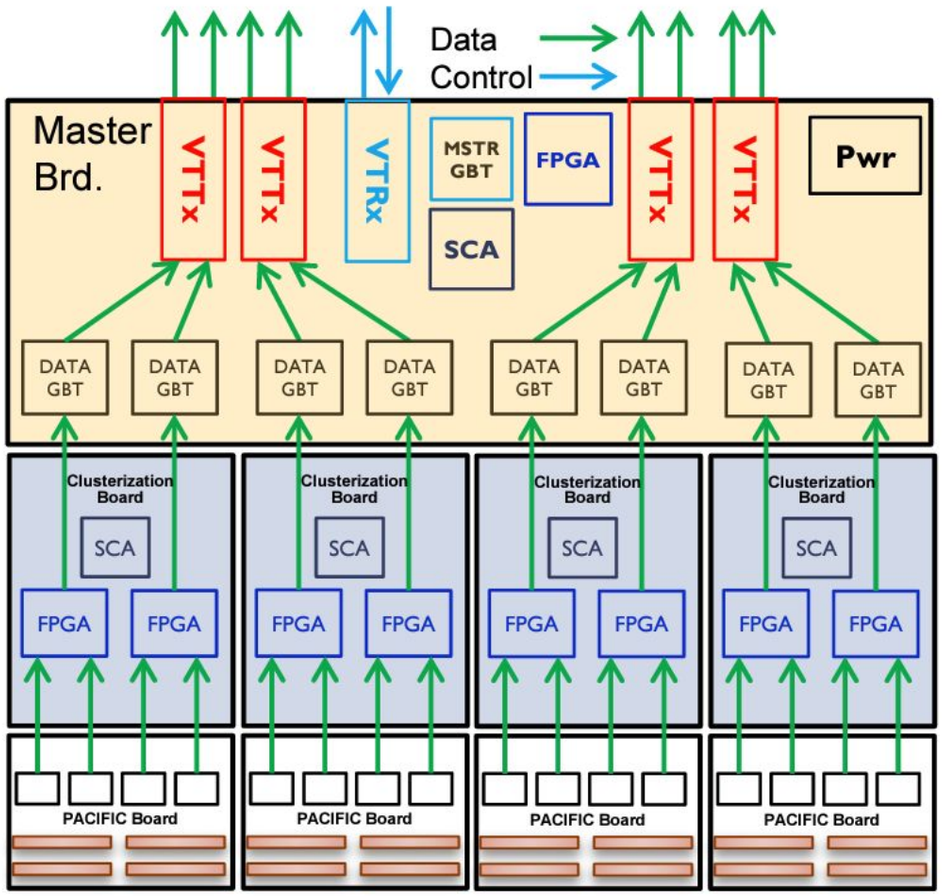


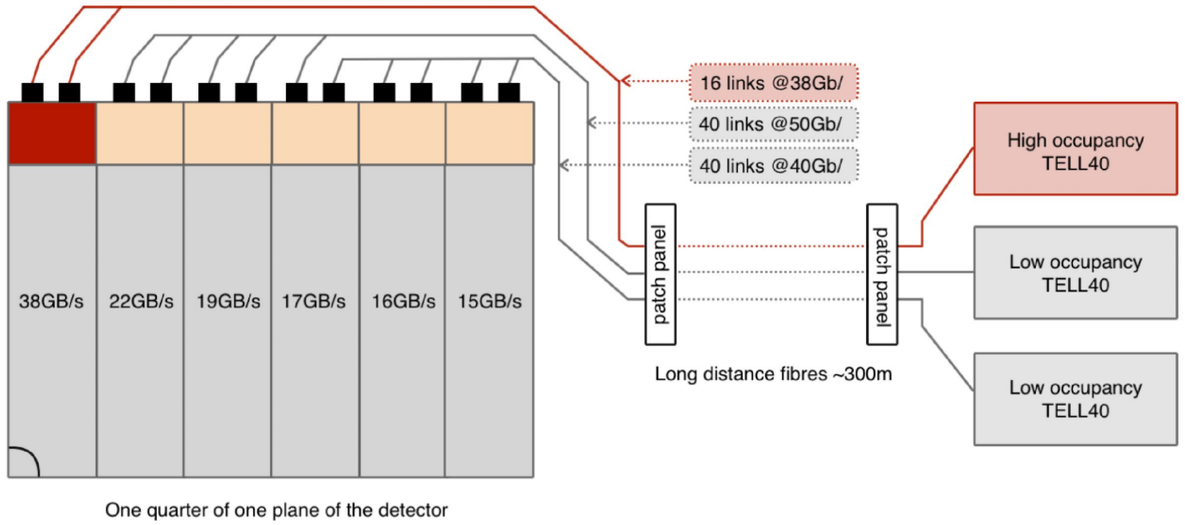
One quarter of one plane of the detector

Timing Scans

The clocks are set per GBT link (8 per Master Board) corresponding to:

- 8 SiPMs, each with a datalink to the back-end TELL40s
- Each TELL40 has *up to* 48 datalinks





One quarter of one plane of the detector

Each Q read-out by

- one 16-link TELL40
- two 40-link TELL40s

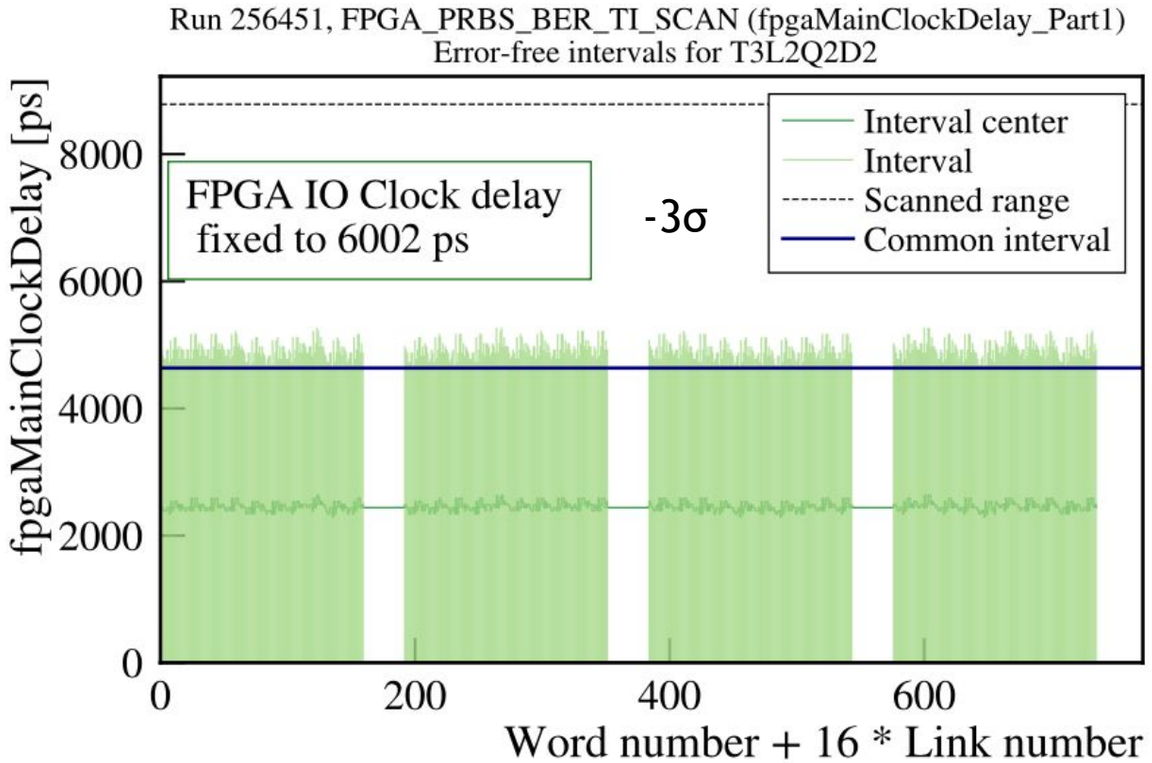
Front-end electronics

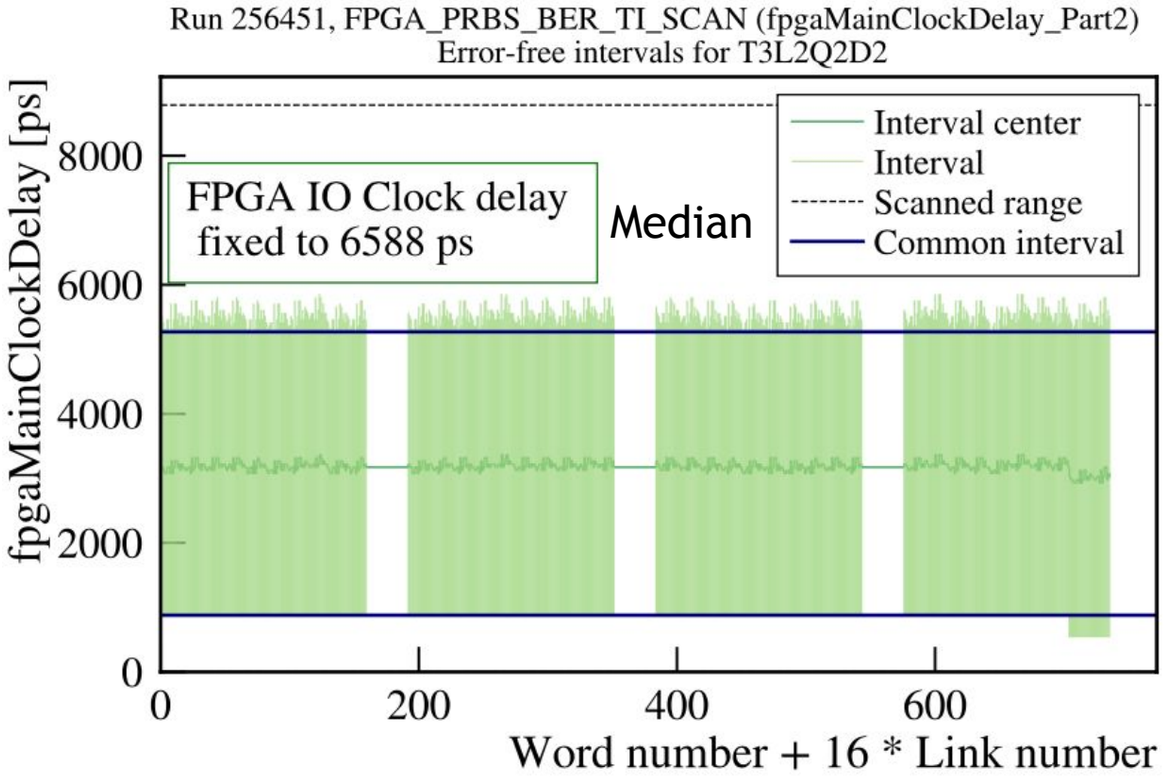
Back-end electronics

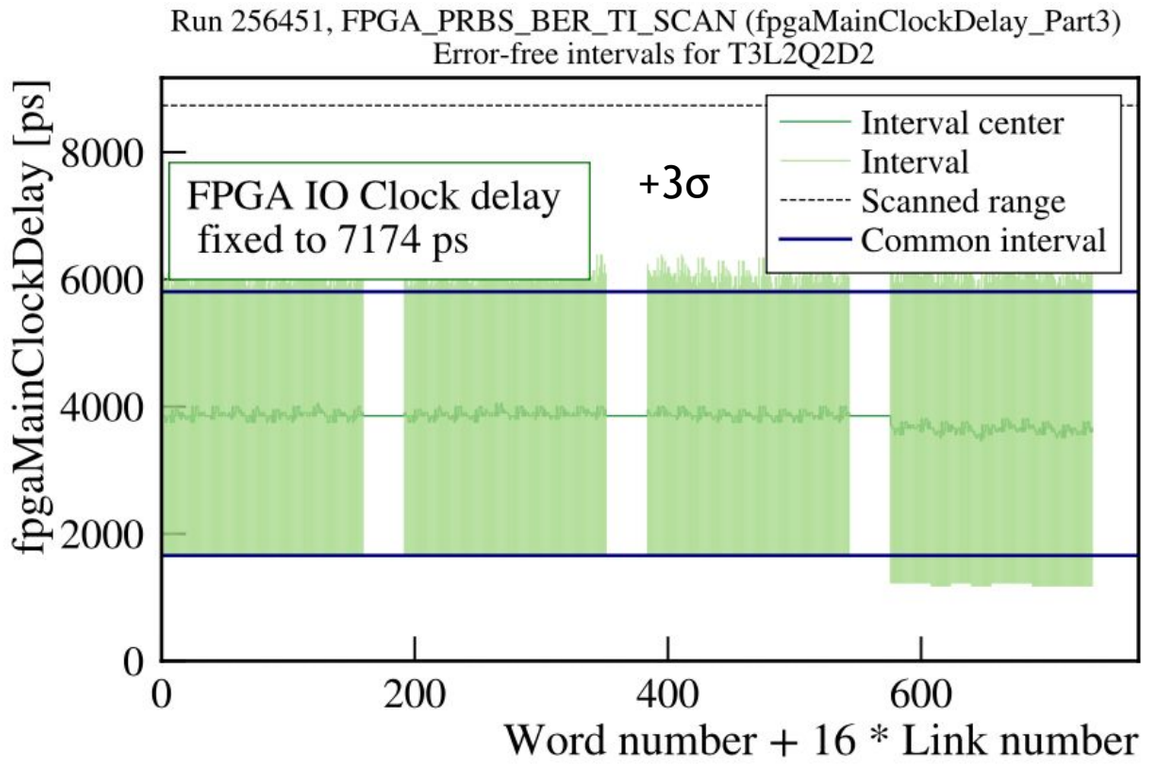
FPGA scans

Part 2: fix IO clock, scan Main clock

- Fix IO to median, +3σ, -3σ
- Median: FPGA main = 61 +- 2 [DAC]







Timing Scans

Front-end firmware update September for whole detector.

Latest timing scans can be found in
`/calib/sf/FPGA_PRBS_BER_TI_SCAN/`
`/calib/sf/PACIFIC_SIMPLE_TI_SCAN/`

We are running a simplified version of PACIFIC scans which only scans the *PacificClockDelay* and *PacificSyncPluseClockDelay*.

Results saved in:
`/calib/sf/CavernCommissioning/{scantype}/{runnumber}`

Output

The output of each scan is an xml file with only the clock delay settings resulting from the scan, per GBT link:

FPGA scan

```
<?xml version="1.0" encoding="UTF-8"?>

<TimeCalibrationTables>
    <RunType>FPGA_PRBS_BER_TI_SCAN</RunType>
    <RunNo>
        <NRuns>1</NRuns>
        <array desc="list_of_run_no">
            <item>251775</item>
        </array>
    </RunNo>
    <Entry>
        <Table>TIME_CALIB_MB_DATAGBT</Table>
        <ProdDBId>EMB00520</ProdDBId>
        <ScanResults>
            <GBTData>
                <GBT_N>0</GBT_N>
                <CLKDEL0 desc="FPGA Main" ScanName="fpgaMainClockDelay">0x48</CLKDEL0>
                <CLKDEL2 desc="FPGA I/O" ScanName="fpgaIoClockDelay">0x90</CLKDEL2>
            </GBTData>
            <GBTData>
                <GBT_N>1</GBT_N>
                <CLKDEL0 desc="FPGA Main" ScanName="fpgaMainClockDelay">0x48</CLKDEL0>
                <CLKDEL2 desc="FPGA I/O" ScanName="fpgaIoClockDelay">0x90</CLKDEL2>
            </GBTData>
            <GBTData>
                <GBT_N>2</GBT_N>
                <CLKDEL0 desc="FPGA Main" ScanName="fpgaMainClockDelay">0x48</CLKDEL0>
                <CLKDEL2 desc="FPGA I/O" ScanName="fpgaIoClockDelay">0x90</CLKDEL2>
            </GBTData>
```

PACIFIC scan

```
<?xml version="1.0" encoding="UTF-8"?>

<TimeCalibrationTables>
    <RunType>PACIFIC_BER_TI_SCAN</RunType>
    <RunNo>
        <NRuns>1</NRuns>
        <array desc="list_of_run_no">
            <item>245249</item>
        </array>
    </RunNo>
    <Entry>
        <Table>TIME_CALIB_MB_DATAGBT</Table>
        <ProdDBId>EMB00445</ProdDBId>
        <ScanResults>
            <GBTData>
                <GBT_N>0</GBT_N>
                <CLKDEL3 desc="PACIFIC Clk 0/2" ScanName="pacificClockDelay">0x2c</CLKDEL3>
                <CLKDEL4 desc="PACIFIC Clk 1/3" ScanName="pacificClockDelay">0x2c</CLKDEL4>
                <CLKDEL7 desc="PACIFIC Sync" ScanName="pacificSyncPulseDelay">0x154</CLKDEL7>
            </GBTData>
            <GBTData>
                <GBT_N>1</GBT_N>
                <CLKDEL3 desc="PACIFIC Clk 0/2" ScanName="pacificClockDelay">0x2c</CLKDEL3>
                <CLKDEL4 desc="PACIFIC Clk 1/3" ScanName="pacificClockDelay">0x2c</CLKDEL4>
                <CLKDEL7 desc="PACIFIC Sync" ScanName="pacificSyncPulseDelay">0x154</CLKDEL7>
            </GBTData>
```

One file created per TELL40
Files are combined after the full detector analysis is performed.

These parameters are currently defined in ‘TimeCalibrationTables’ in SciFi online DB. Separate software written by Karol to load results into this table.

PACIFIC: CDC phase