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Master of Science

**Data acquisition and diamond detector
pulse shape measurements for the
upgrade of the LHCb Beam Condition
Monitor**

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Kurzfassung

Das LHCb-Experiment ist eines der vier großen Experimente am Large Hadron Collider, einem Teilchenbeschleuniger am CERN, der Europäischen Organisation für Kernforschung. Protonenpakete werden dort auf eine Strahlenergie von 7 TeV beschleunigt und an vier Interaktionspunkten zur Kollision gebracht. Wegen ihrer Nähe zum Strahl sind einige Komponenten des LHCb-Detektors gefährdet, beschädigt zu werden. Als Sicherheitsmaßnahme misst der Beam Condition Monitor den Teilchenfluss nah am Strahlrohr mit zwei Ringen von Diamant-Strahlungsdetektoren. Wenn eine Flussschwelle überschritten wird, löst das System schnell einen Strahlabbruch aus, um die gefährdeten Bauteile zu schützen. Während des Long Shutdown 2 des Large Hadron Colliders, zwischen 2018 und 2022, wird ein Upgrade des Systems durchgeführt. Einerseits wird ein Datenerfassungssystem gemäß dem Stand der Technik eingeführt, zu dem die vorliegende Arbeit eine Firmwarekomponente beiträgt. Andererseits wird ein neuer Satz von Diamant-Strahlungssensoren eingebaut, da einige Sensoren am Ende der letzten Datennahmperiode ein problematisches Verhalten zeigten. Daher wird in dieser Arbeit ein alternativer Aufbau zur Charakterisierung mithilfe von Einzelpulsmessungen aufgebaut und benutzt, um die Ladungssammlungsentfernung von 18 Sensoren zu messen.

Abstract

The LHCb experiment is one of the four large experiments at the Large Hadron Collider, a particle accelerator located at the European Organization for Nuclear Research. There, proton bunches are circulating at a beam energy of 7 TeV and are brought into collision at four interaction points. Due to their proximity to the beam, some components of the LHCb detector are at risk of being damaged. As a safety measure, the Beam Condition Monitor measures the particle flux in the vicinity of the beam pipe using two rings of diamond radiation detectors. When a flux threshold is exceeded, a beam abort is initiated rapidly to protect the periled equipment. During the Long Shutdown 2 of the Large Hadron Collider, between 2018 and 2022, an upgrade of the system is conducted. On the one hand, a new state-of-the-art data acquisition system is being established, to which this thesis contributes a firmware component. On the other hand, a new set of diamond radiation sensors is being installed, as some sensors showed problematic behavior at the end of the last run. Therefore, in this thesis, an alternative diamond sensor characterization setup using a single-pulse measurement scheme is implemented and utilized to measure the charge collection distance of 18 sensors.

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Acronyms

- ADC** analog-to-digital converter. 16, 18
- ASIC** application-specific integrated circuit. 11
- BCM** Beam Condition Monitor. 1–10, 50
- CCD** charge collection distance. 29, 30, 45
- CCE** charge collection efficiency. 30, 45
- CDR** clock and data recovery. 14
- CERN** European Organization for Nuclear Research. 1, 50
- CFC** current-to-frequency converter. 6, 16–18, 20
- CIBU** Controls-Interlocks-Beam-User. 7, 9, 18
- CRC** cyclic redundancy check. 20
- DC** direct current. 32, 33, 36
- ECAL** electromagnetic calorimeter. 5
- FIFO** first in first out. 14, 15, 21
- FPGA** Field Programmable Gate Array. 6, 9, 11, 12, 14, 16, 50
- GPU** Graphics Processing Unit. 6
- HCAL** hadronic calorimeter. 5
- HDL** hardware description language. 12
- IP** intellectual property. 11, 14, 20

- LHC** Large Hadron Collider. 1, 2, 6, 7, 9, 18, 50
- LHCb** Large Hadron Collider beauty. 1–7, 9, 50
- LS2** Long Shutdown 2. 3, 6, 9
- LUT** look-up table. 11
- MIBAD** Machine Interface and Beam Abort Decision. 9, 16, 18–20, 22
- MIP** minimum ionizing particle. 23
- MMIC** monolithic microwave integrated circuit. 33
- PCB** printed circuit board. 34, 36, 38, 46
- PCS** physical coding sublayer. 14
- pCVD** polycrystalline chemical vapor deposition. 30, 31
- PLL** phase-locked loop. 15
- PMA** physical medium attachment. 14, 15
- PMT** post-mortem trigger. 18
- PSB** Proton Synchrotron Booster. 2
- PSRR** power supply rejection ratio. 33
- QCD** quantum chromodynamics. 1
- RF** radio frequency. 34, 51
- RICH** Ring Imaging Cherenkov Detector. 5
- RTL** register-transfer level. 12
- scCVD** single-crystal chemical vapor deposition. 30, 31
- SciFi** Scintillating Fiber. 4
- SM** Standard Model of Particle Physics. 1
- SNR** signal-to-noise ratio. 36
- UT** Upstream Tracker. 4
- VELO** Vertex Locator. 3, 4, 7

1 Introduction

The efforts of modern particle physics are concentrated on finding shortcomings in the Standard Model (SM), an extremely successful theory describing three of the four known fundamental forces [1, 2, 3]. These include the electromagnetic, the weak, and the strong interactions; gravity is not part of the Standard Model. Even though there are some results that show tension with the SM (e.g. [4]), it is not yet fundamentally falsified. The incompleteness of the model is obvious in other aspects: Gravity and neutrino masses are not included in the model, the CP violation in the model is not strong enough to explain the existence of matter in the universe and it has no explanation for the large amounts of Dark Matter observed throughout the cosmos. One of the experiments probing the SM is the Large Hadron Collider beauty (LHCb) experiment at European Organization for Nuclear Research (CERN). It is one of the major experiments located at the Large Hadron Collider (LHC), a synchrotron providing proton-proton collisions at a center-of-mass energy of up to $\sqrt{s} = 14 \text{ TeV}$ [5]. The LHC accelerator chain is described in [section 1.1](#). Although the LHCb experiment was originally designed for precision measurements of decays of beauty and charm hadrons, the physics program covers a broad range of other measurements from probing fundamental quantum chromodynamics (QCD) over the electroweak, top and Higgs sector up to fixed-target experiments with proton-gas collisions and can therefore be seen as a general-purpose detector in the forward region. The LHCb detector and its components are described in [section 1.2](#).

The circulating 7 TeV beams of the LHC pose an immediate risk to the LHCb detector itself – misaligned beams and showers from upstream collimators can deposit damaging doses of ionizing radiation in the experiment hardware, which is very close to the beam at some points. The beam parameters are monitored by the LHC, but as an additional safety measure, the Beam Condition Monitor (BCM) is employed to measure the particle flux in the close vicinity of the beam pipe on both sides of the interaction region. The BCM uses radiation-hard diamond particle detectors, whose currents are measured with an integration time of $40 \mu\text{s}$. This allows the detection of developing adverse beam conditions and to initiate a beam dump averting damage to the experiment. The BCM System is described in detail in [section 1.3](#). In this thesis, parts of a new data acquisition system for the BCM on the one hand, and a measurement setup for diamond detector efficiency is developed on the other hand. Those undertakings are done in the course of an upgrade

of the BCM system, which is part of a larger upgrade of the LHCb detector itself, preparing for the next run of the LHC at a fivefold instantaneous luminosity when compared to the previous runs.

1.1 Large Hadron Collider

The LHC is the highest-energy particle accelerator in the world, situated in the Geneva region, extending over the French-Swiss border region. Within the machine, two particle beams are being circulated in opposite directions and brought into collision in one of the four major experiments. Mainly protons are being accelerated, but the LHC can also be filled with other particles, such as lead and xenon nuclei. The LHC accelerator complex consists of a long chain of pre-accelerators up to the 26.7 km-measuring main rings, depicted in Figure 1.1: For the proton mode, the particles' path starts at the *LINAC 4*, a linear accelerator where H^- ions are accelerated to 160 MeV. Those are injected into the *Proton Synchrotron Booster (PSB)*, at the same time the two electrons are stripped off every ion leaving bare protons. In the PSB, an energy of 1.4 GeV is achieved, which is raised to 25 GeV in the next stage, the *Proton Synchrotron*. From this accelerator, the proton bunches are injected into the 6.9 km *Super Proton Synchrotron*, which is the last stage prior to the LHC. The particles are transferred to the LHC at an energy of 450 GeV and then brought to the final beam energy of up to 7 TeV. Every bunch is populated by around 10^{11} protons, with a bunch spacing of 25 ns. In the upcoming Run 3 of the machine, projected to start data-taking in 2022 [6], an instantaneous luminosity of up to $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ is planned [7], though the LHCb experiment will only run at $2 \times 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$ [8], limiting track multiplicity to improve reconstruction quality.

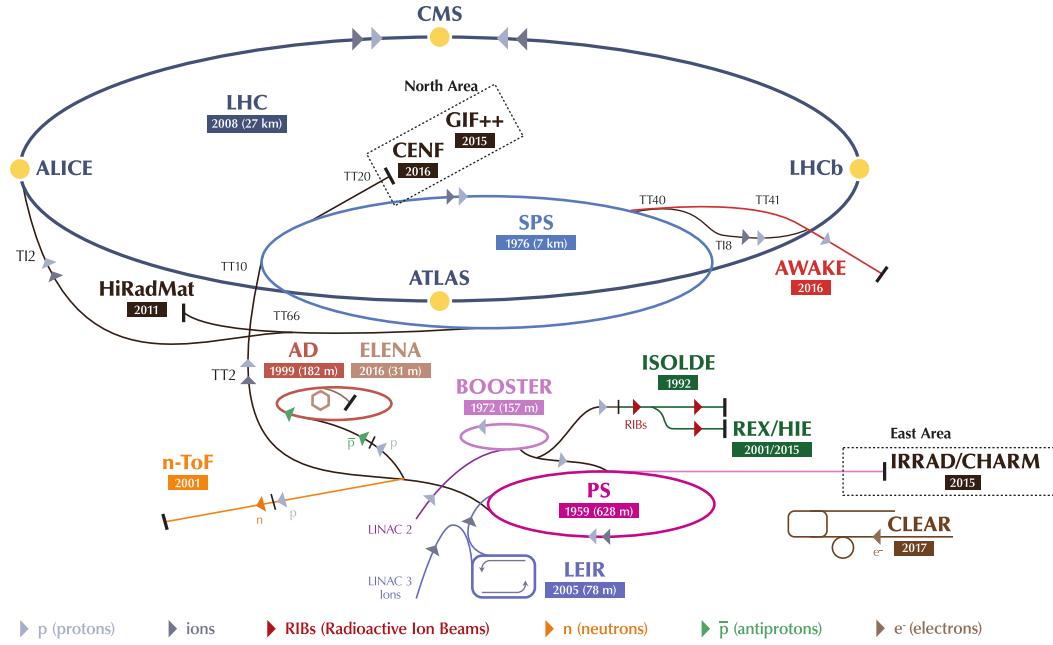


Figure 1.1: Overview of the CERN accelerator complex. [9]

1.2 LHCb experiment

The LHCb detector is a single-arm forward spectrometer with a pseudorapidity acceptance of 1.8 to 4.9. Currently, in the course of the LHC-wide *Long Shutdown 2* (*LS2*), all subdetectors are being upgraded. Only the new detector will be described here, except for the BCM, where the existing readout system will be briefly outlined. A description of the pre-upgrade LHCb detector can be found in [10]. As a single-arm spectrometer, LHCb has a defined “downstream” direction, which is to the right in Figure 1.2 and the positive z direction in the LHCb coordinate system. The y axis denominates up and down, positive being up, in the cavern. The x axis denominates left and right, positive being right, seen downstream from the interaction point. There are two systems, the subdetectors can be split into: Tracking and particle identification.

The tracking system detects the trajectories of charged particles to reconstruct vertices on the one hand and determine the particles’ momentum on the other. One part of the tracking system is the *Vertex Locator (VELO)*, a silicon pixel detector consisting of 52 detector modules surrounding the interaction point with a minimal distance to the beam of 5.1 mm. The two sides of the VELO are movable and are only brought close once stable beams are achieved. There are 41 million pixels and

1 Introduction

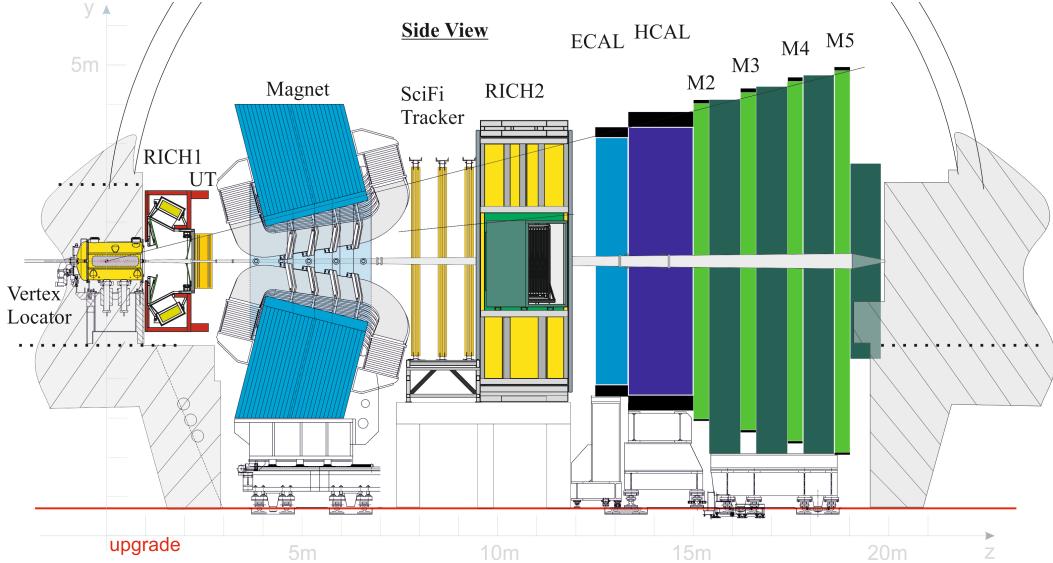


Figure 1.2: Layout of the LHCb detector for Run 3 of the LHC. [11]

the detector is read out at a rate of 40 MHz (as all subdetectors except the BCM). VELO achieves a spatial hit resolution of $12 \mu\text{m}$ [12]. The next part of the tracking system in the downstream direction is the *Upstream Tracker (UT)*, a silicon strip tracker with a $100 - 200 \mu\text{m}$ pitch, and four tracking planes. The planes are arranged in a so-called $x-u-v-x$ stereo pattern where the center two planes are rotated $\pm 5^\circ$ to achieve a two-dimensional spatial resolution while suppressing ghost hits in the reconstruction. To be able to measure momenta, there is a large normal-conducting reversible dipole magnet with an integrated field of 4 T m between the UT and the *Scintillating Fiber (SciFi) Tracker*, which is the last element of the tracking system. It is a large tracker consisting of twelve layers of scintillating fiber mats grouped in four stations, with a spatial resolution of better than $100 \mu\text{m}$ covering an area of 360 m^2 . SciFi also employs an $x-u-v-x$ pattern with a stereo angle of 5° but repeats this pattern for every station [11].

The particle identification system is used to distinguish various particles, as a track reconstruction alone can only tell the sign of a particle's charge and its momentum. Starting from the interaction point there are the *Ring Imaging Cherenkov Detectors* one and two, that have volumes filled with fluorocarbon gas in which traversing high-energy particles generate Cherenkov radiation. This radiation is emitted at a characteristic angle of

$$\cos \vartheta = \frac{1}{n\beta}, \quad (1.1)$$

with β being the fraction of the speed of light the particle is moving at and n the refractive index of the medium. A sophisticated optical system maps the Cherenkov cones to rings which are then detected by a large array of multi-anode photomultiplier tubes. It is then possible to reconstruct the speed of a particle which is in turn used to determine its mass and ultimately its identity. The distinction works especially well for pions, kaons, and protons. Ring Imaging Cherenkov Detector (RICH) 1 has a momentum range of 2–40 GeV/c, whereas RICH 2 covers 15–100 GeV/c and is placed further downstream, as higher-momentum particles are deflected less by the magnet [13]. The *electromagnetic calorimeter (ECAL)* and *hadronic calorimeter (HCAL)* are positioned downstream of RICH 2 and are designed to stop most particles (except muons and neutrinos, for example) and at the same time measure their deposited energy. The ECAL is a sampling calorimeter of the Shashlik type, consisting of alternating 4 mm thick scintillating tiles and 2 mm thick lead absorber tiles, stacked to a thickness of 40 cm and longitudinally spiked by scintillating fibers. The fibers guide the scintillation light to a photomultiplier tube for each of the 6066 cells. The HCAL is similar to the ECAL but much thicker (1.2 m). Iron is used as absorbing material and the cell count is lower at 1488 cells. The muon system is located at the very end of the experiment. It is used to identify those muons that, due to their minimally-ionizing properties, traversed the whole detector up to this point. They are of special interest, as many final states of relevant decays contain muons. The detection happens in the muon stations $M2 - M5$, $M1$ was removed in the course of the upgrade. A station is made up of 276 multi-wire proportional chambers and the stations are interleaved with 80 cm thick low-background iron absorbers to achieve an energy selectivity [13].

Not as a detector to take physics data, but as a safety measure, there is the Beam Condition Monitor, situated in two stations upstream of the magnet. The BCM system is the focus of this thesis and its details are described in [section 1.3](#).

As mentioned before, the time between two collisions, the so-called bunch spacing, is 25 ns. Therefore, to be able to capture the aftermath of every bunch interaction and to maximize the physics data collection, every single detector channel has to be read out at 40 MHz. Even though most of the data acquisition happens in a zero-suppressed way (i.e. only fired detector channels send their data) and for LHCb only at most three-quarters of the theoretical bunch crossings actually happen, this corresponds to a data rate of 32 Tbit s^{-1} . It is neither economical nor scientifically beneficial to permanently store data at this kind of rate, therefore it is necessary to filter out relevant data of physical interest.

Most of the experiments facing this problem (also the LHCb experiment prior to the LS2 upgrade) solve it by implementing a hardware trigger. There, some of the subdetectors are read out at the full rate and the data is fed into some form of

hardware logic (usually Field Programmable Gate Arrays (FPGAs), see [section 2.1](#)) that is hardwired to identify interesting signatures in those subdetectors. This allows a significant reduction of the data rate (a factor of 40 for the pre-upgrade LHCb experiment) before more sophisticated and complex methods are applied to reduce the rate to a storable value. The hardware trigger method has two major disadvantages: On the one hand, it is not very flexible, as changing an FPGA firmware is usually more complex than updating software on computer systems. On the other hand, complex algorithms like charged-particle tracking are very hard to implement in hardware but extremely useful in finding an efficient trigger decision. Today, extremely high throughput parallel data processing can be done on Graphics Processing Units (GPUs). This potential will be utilized by the LHCb experiment in the next LHC run, as the previous hardware trigger was removed entirely and a GPU-based software trigger will be fed the full experiment data rate [8].

1.3 LHCb Beam Condition Monitor

1.3.1 Previous system

This section describes the situation of the system prior to the LS2 upgrade, i.e. during the LHC runs 1–2, between 2009 and 2018. The Beam Condition Monitor of the LHCb experiment is a fast particle flux measurement system. It consists of two rings with 8 diamond sensors each, placed at two z positions closely around the beam pipe inside the LHCb detector. One station, BCM-U is placed upstream of the Vertex Locator at $z = 2131$ mm, the other station, BCM-D is placed downstream of the *Tracker Turicensis*, the predecessor of the UT described before, at $z = 2765$ mm. In [Figure 1.4](#), technical drawings of the two detector rings are shown, where in [Figure 1.5](#) the current state of the BCM-U station is visible. The centers of the sensors are placed at a radius of 50.5 mm for BCM-U and 37 mm for BCM-D. The stations differ as the downstream one is inside the LHCb acceptance, implying higher demands regarding the material budget. A bias voltage of 200 V is applied and the current through the diamonds is read out by current-to-frequency converter (CFC) cards, originally designed for the LHC Beam Loss Monitor. The whole readout scheme is presented in block diagram form in [Figure 1.3](#). The cards feature an integration time of 40 μ s and a measurement range between 2.5 pA and 1 mA, which is adequate for the BCM diamonds as they show a dark current in the picoampere range and dump thresholds in the microampere range. The digitized current data is sent with a rate of 125 kHz through redundant optical fibers to a *TELL1* readout board (which was the standard LHCb readout board until LS2), where it is processed and buffered [14].

The firmware of the TELL1 board applies a beam dump logic to determine whether the measured flux values are in a problematic range. To cover slow and fast error regimes, running sums over the last 2 and 32 samples are calculated. This is equivalent to the duration of approximately 1 and 14 LHC turns. For the longer running sum, lower thresholds are defined, as this measurement smooths out fluctuations more. As the false-positive rate needs to be kept extremely low, for the fast abort regime, the beam dump request is only initiated when the respective current threshold is exceeded in the short running sum on three adjacent sensors at the same time. For the slow regime, the threshold is applied to the sum of all sensors in a station, except the ones with the lowest and highest values. This abort logic has proven to be reliable during the operation of the system.

The TELL1 board is located in the so-called D3 rack behind the experiment's shielding wall in the LHCb cavern, as this is also where the interface to the LHC machine is available. This so-called Controls-Interlocks-Beam-User (CIBU) [15] interface has two purposes: First, the TELL1 board can, when the conditions described above are met, request a beam dump from the LHC through the interface. Second, it can inhibit the injection of further particle bunches into the LHC, if the system determines that is not in a ready and safe state. Additionally, there is, through the so-called post-mortem trigger, the possibility for the LHC to request a memory snapshot of the system's current data. This is done every time an LHC dump is initiated, regardless of the reason, and can provide valuable insight to the LHC operators when they are investigating a possible problem. The system also provides the so-called BCM_OK signal to the LHCb Vertex Locator. When the signal is withdrawn, the VELO immediately moves out of the closed position into a safe state. This happens when the BCM detects an internal malfunction and can therefore no longer protect the VELO, but a beam dump is not indicated because no above-threshold values were measured.

During the last months of LHC Run 2, problems with the BCM system emerged. Multiple diamonds started showing excessive currents during normal LHC conditions, some up to the power supply current limit. It is suspected that this may have been due to radiation damage because no other electrical fault was found. Though radiation damage occurs in diamonds as in any other semiconductor detector material, the extent of this problem is unexpected, as the usual failure mode would be a gradual increase in dark current, not sudden jumps. More on diamonds as a detector material can be found in subsection 3.1.4. It is worth noting that no erroneous beam dump was generated by the BCM system at any point. The affected sensor channels were masked in the firmware and the system was able to run the last months without those channels.

1 Introduction

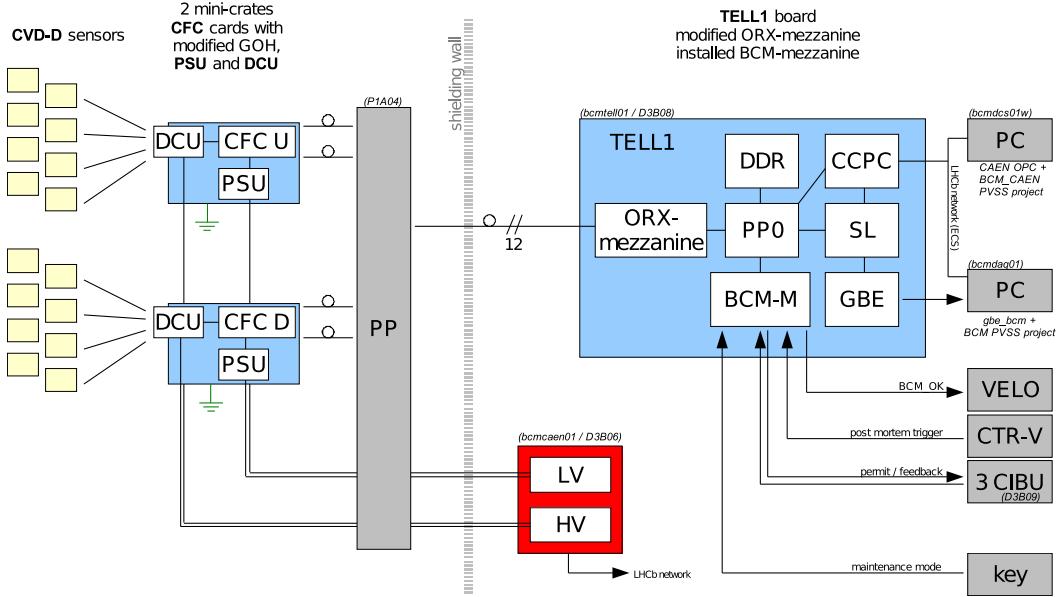


Figure 1.3: Block diagram of the previous BCM readout system. [16]

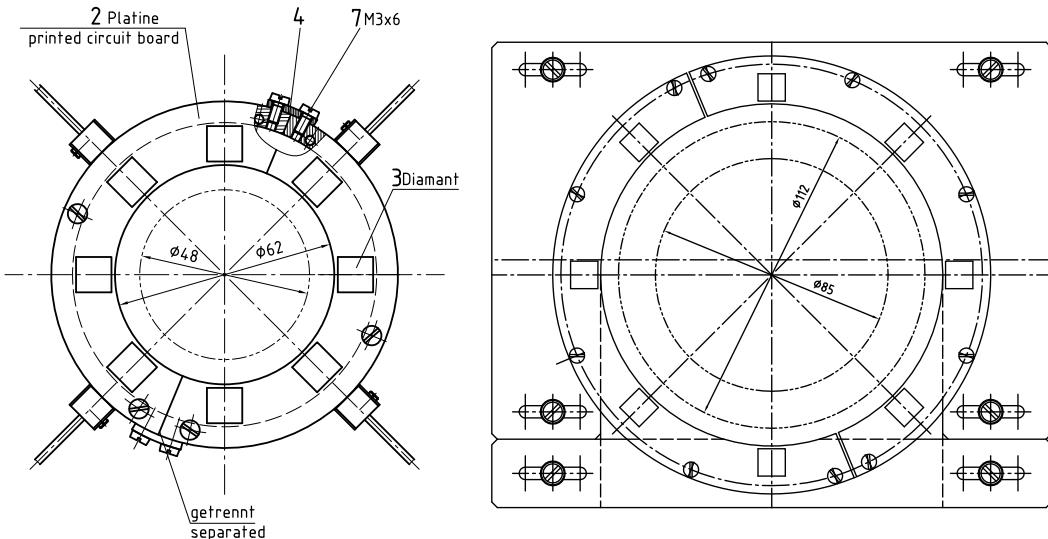


Figure 1.4: Technical drawings of the BCM-D (left) and BCM-U (right) station.
Not to scale. [17]

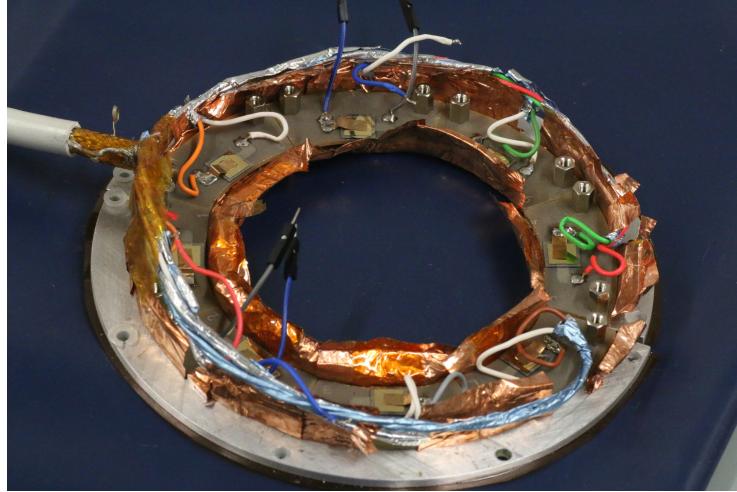


Figure 1.5: Photograph of the BCM-U station in its current state.

1.3.2 Upgraded system

During the LS2, between 2019 and 2022, many of the LHCb subdetectors are replaced and all of them are getting new readout hardware. The aforementioned TELL1 FPGA readout board is being deprecated in this process. As it would not be reasonable to use and maintain one single TELL1 board for the BCM, the system is changed over to the new LHCb-wide standard readout board called PCIe40 [18]. The BCM-specific variant of the board configuration is called BCM40. This board is implemented as an *PCI express* computer expansion card and will be operated inside a host node in the newly established data center above ground next to the LHCb cavern. As the aforementioned CIBU interface to the LHC machine will stay in the cavern, it is necessary to add another component to the system. The so-called Machine Interface and Beam Abort Decision (MIBAD) board, featuring an Intel Arria V FPGA, will be placed in the same rack as the TELL1 was previously and handles the low-level parts of the BCM system: Receiving the read-out data, implementing the beam dump logic, and interfacing to the machine. The acquired data is then forwarded through redundant “long-distance” fibers to the BCM40 in the surface data center. Using the BCM40 as an interface to the MIBAD board, the computer housing the BCM40 will run the monitoring software that allows observation and control of the whole system from the LHCb control room. In chapter 2 I describe my contributions to the readout system, specifically the MIBAD side of the high-speed data link between the two FPGA boards.

Another aspect of the BCM upgrade concerns the diamond detectors: Some of the

sensors failed in the last run. As radiation damage is the suspected cause, the whole setup will be replaced. It would be of scientific and operational value to understand the failure mode and how to avoid it in the future. In general, the characterization of diamond sensors is an important aspect of future BCM operations. One of the most fundamental characteristic figures is the charge collection efficiency, which can be measured in different ways. As a further part of this thesis, I implemented an existing measurement concept for a single-pulse sensor characterization setup in Dortmund and compared the results for some exemplary sensors to the legacy method. This is described in detail in [chapter 3](#).

2 Data acquisition for the Beam Condition Monitor

2.1 Field Programmable Gate Arrays

FPGAs are integrated digital circuits that feature a high number of reconfigurable logic blocks, allowing low-latency parallelized data processing. Unlike microprocessors, as commonly used in computers, they do not rely on a fixed set of instructions executed in a specific order with different operands. Rather, the configured internal connections determine its output's behavior as a result of a given set of input data. The basic building blocks of FPGAs are logic cells that contain a configurable look-up table (LUT) to map from input to output, as visualized in [Figure 2.1](#). The interconnection of a large number (currently a few million) of logic cells yields the processing power these devices can offer. The entirety of the logic cells and interconnections is sometimes called *fabric*. Besides logic cells, memory and input/output blocks are implemented in the chip, as well as so-called hard IP cores. Intellectual property (IP) designates circuits that are prefabricated by the vendor. This can be useful for functions like high-speed serial communication, which is, due to the high frequencies and analog circuits used, usually not possible to implement in the regular FPGA fabric. Furthermore, regularly used but resource-intensive functions like digital signal processing are often implemented as hard IP cores to be able to reduce logic cell occupancy. Besides hard IP cores there are also soft IP cores, which are sets of code that implement specific functionality, very similar to software libraries, but consume logic cells of the FPGA fabric. An FPGA can be considered a generalized device, as it is possible and common to implement a microprocessor inside it, allowing it to perform tasks otherwise hard to realize in the FPGA logic itself. Thanks to their reconfigurability, FPGAs are also often used as prototyping devices for application-specific integrated circuits (ASICs), which are hard-wired circuits for one task, thus less flexible, but also less expensive to mass-produce.

2.1.1 FPGA toolchain

An FPGA's configuration is expressed in a hardware description language, similar to a programming language a computer program can be written in. The most common

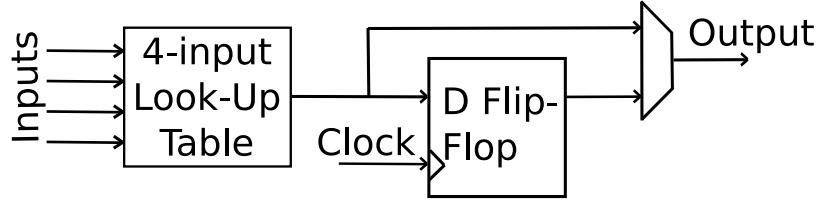


Figure 2.1: Block diagram of a basic FPGA logic cell, consisting of a 4-input look-up table and a (bypassable) flip-flop. [19]

hardware description languages (HDLs) are VHDL, Verilog, and SystemVerilog. They all have in common that they are human-readable, therefore it is necessary to transform the description into something the device can handle – the so-called bitstream. It contains an encoded representation of all the logic cells' (and other blocks') configurations and interconnections. To produce this bitstream, a hardware development toolchain is necessary. This encompasses every step needed to turn HDL code into a configuration, as shown in Figure 2.2. Starting from the *register-transfer level (RTL) HDL description* (written in VHDL or similar), the low-level logic realizing the described functions is synthesized. Register-transfer level refers to a level of abstraction where the logic circuit's state is modeled using registers and the data flow between them by combinatorial logic. This low-level logic is realized in the so-called *Netlist* that encodes all required logic elements and their connections and is not (directly) human-readable anymore. Recently it is also possible to start with a *Behavioral description* in a high-level language such as C or C++, which is then used to synthesize the RTL HDL description. This *High level synthesis* is not used in this thesis, as it does not provide significant benefits for very low-level functionality like interfacing high-speed serial transceivers explained in the next section. In the *Place and route* step, another program takes the Netlist and tries to realize it inside a given FPGA fabric, optimizing the fabric usage and path lengths. This results in the aforementioned bitstream, called *Configuration data* in the figure, that can then be downloaded to the device. Verification is necessary along the toolchain workflow. Every step up to the FPGA itself is usually verified by simulation, starting with *Behavioral level simulation* (if applicable) and *RTL simulation* verifying a correct logic behavior for all specified input situations. After the Place and route step, the generated layout is verified with regard to the skew introduced by non-negligible signal propagation delays using *Timing verification*. When the configuration is downloaded to the FPGA, tools like the Intel SignalTap Logic Analyzer can be utilized to verify correct in-device behaviour by essentially implementing a digital logic analyzer in the unused FPGA fabric.

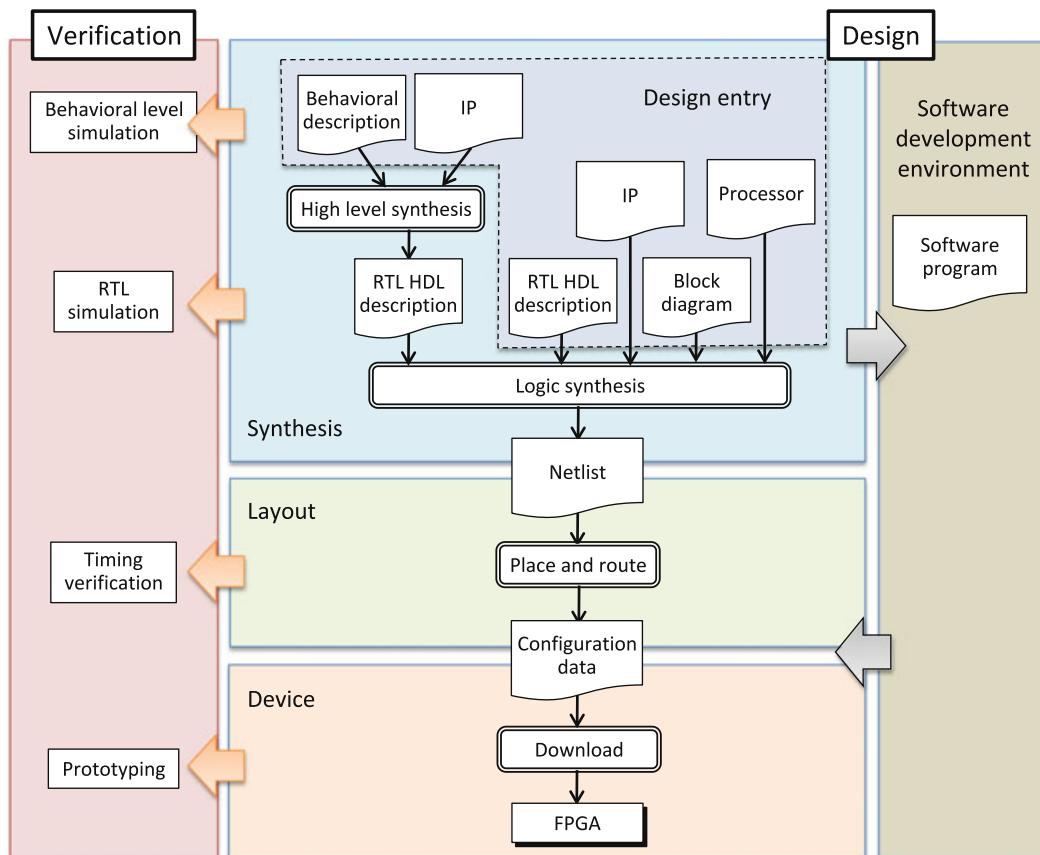


Figure 2.2: Hardware development toolchain flow chart. [20]

2.1.2 High-speed serial transceivers

Communication between different entities within the same subsystem (i.e. a printed circuit board) can be established through simple single-ended wire connections or differential signaling in case of higher data rates. Differential signaling refers to the method of carrying the same signal on two adjacent conductor paths, but with reversed polarity. Under the assumption that interfering signals affect both paths in the same way, the undisturbed signal can be recovered by evaluating the difference between the two lines. Due to transmission line effects, the maximum usable frequency and therefore data rate per line is limited, therefore often a parallel communication using multiple data lines is established. Often, another line additionally carries a clock signal, which indicates the moment at which the data should be read by the receiving side, e.g. synchronous to its falling edge. When communication between different devices over longer distances than approximately half a meter is needed, this approach becomes impractical. To save cost, less physical media are beneficial, furthermore, timing constraints between multiple transmission lines become harder to comply with for longer media. Therefore, for these applications, high-speed serial transceivers are used. They are implemented as hard IP blocks on many FPGAs and allow transmitting and receiving high data rates (sometimes more than 100 Gbit s^{-1}) through a single differential line while interfacing with the FPGA fabric through a parallel bus (e.g. 16 bit wide) to keep clock frequencies manageable. A key feature of serial transceivers is clock and data recovery (CDR) that allows omitting a separate clock signal. Using an encoding that guarantees frequent signal level transitions, the device is able to recover the clock from the data stream.

An exemplary hard IP serial transceiver block diagram from an Intel Arria V FPGA is shown in [Figure 2.3](#). The block can be split into the physical medium attachment (PMA) and the physical coding sublayer (PCS). The former is the low-level, fast interface that handles serialization and deserialization and clock recovery, while the latter handles higher-level parallel functions like line coding and byte ordering. On the transmit side, depicted in grey, the data path starts with the parallel data interface to the FPGA fabric, designated by the `tx_parallel_data` signal on the upper right of the block diagram. The data is transferred to the *TX Phase Compensation FIFO* that allows compensating for a phase difference between the parallel data and transceiver clocks. FIFO stands for *first in first out* and designates a memory block that allows buffering some words. The next stage is the *Byte Serializer* which optionally allows for a 16 bit instead of an 8 bit wide parallel interface. In the case of the wider interface, the 16 bit words are split into 8 bit words of the double clock frequency at this point. Subsequently follows the *8B/10B Encoder* that transforms the raw data into a line code, that is suited for signaling on a transmission line. The

key feature of this 8b/10b encoding is its so-called *DC-balance*, meaning that the ratio between low- and high-level bits is exactly $\frac{1}{2}$ when averaging over a longer term. This is equivalent to a nonexistent 0 Hz Fourier component (DC), which is important because many media cannot transmit a DC component reliably, often because an AC coupling is used to achieve galvanic isolation. DC-balance is achieved by the 8b/10b code through a running disparity, meaning that every non-neutral code word is defined in two opposing polarities and the appropriate word is chosen based on the history of used word disparity. Another feature of line codes is control words, that allow signaling non-data communication, like idle patterns (for when no data is ready to be transmitted) or synchronization words. As mentioned before, the line code needs to guarantee frequent enough state changes for the clock recovery to work, even if the same data is sent all the time. The requirement can be illustrated by an example without any measures to guarantee this: Sending only zero data would result in the transmitter signal always having the same state – of course, no clock could be recovered from this. To allow implementing these features, each 8 bit data word is now encapsulated in a 10 bit code word. The next pictured block is *TX Bit Slip* and allows inserting single bits to allow compensation of possible shifts. The data signal now traverses the boundary to the PMA side, where the *Serializer* converts the 10 bit parallel data to a single-bit serial signal with tenfold clock frequency and is sent out through a differential line driver.

On the receive side, depicted in light blue, the data arrives on the left side, designated by the `rx_serial_data` signal. The *CDR* block recovers the clock using a phase-locked loop (PLL). A PLL uses a phase detector and a voltage-controlled oscillator connected in feedback to generate a clock signal synchronized to the transmitter clock. The *Deserializer* block takes the fast-clocked 1 bit signal and converts it into a 10 bit word at a tenth of the serial clock frequency. Starting up at an arbitrary point in time, the deserialized 10 bit words are in general not aligned to the 10 bit words the transmitter sent, hence the need to use a *Word Aligner*. It compares the currently-received word to a predefined control word (e.g. the idle pattern) and introduces a bit slip until it finds a matching word and declares the receiver locked. Next, there is a *Rate Match FIFO* to allow for a slight difference in receiver and transmitter clock frequencies. When the FIFO runs empty, it inserts fill words, when it overflows, received words are discarded. In both cases, a status signal is asserted to allow the connected logic to react to this. The *8B/10B Decoder* undoes the previously described line code and forwards the decoded 8 bit words to the *Byte Serializer* that optionally assembles them to 16 bit words at half the clock frequency. When the Byte Serializer is used, it is required to also enable the *Byte Ordering* block to ensure the correct order of words in the output. It looks for a special control word that is always transmitted as the first 8 bit word within the assembled 16 bit word. If the control word is detected at the wrong position, the

Byte Ordering block inserts an 8 bit fill word to adjust this. Lastly, there is the *RX Phase Compensation FIFO*, another memory block, providing a buffer for phase differences between the transceiver and FPGA fabric clocks.

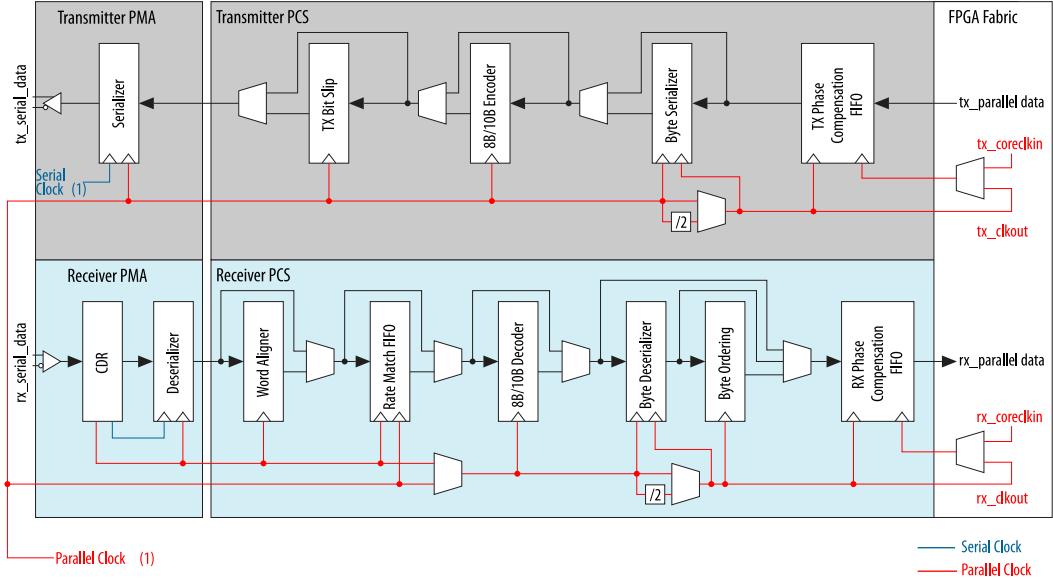


Figure 2.3: Block diagram of an Intel Arria V serial transceiver. [21]

2.2 Upgraded BCM data acquisition chain

In this section, the data acquisition of the upgraded BCM system is described in detail, starting from diamond currents at the detectors and ending at various interfaces to other systems. Figure 2.4 shows a block diagram overview of the whole system's data flow. As previously described, the diamond currents are read out by CFC cards at a rate of 125 kHz. Their data is transmitted through two redundant optical links at a rate of 800 Mbit s^{-1} to the MIBAD board. The transmission uses the aforementioned 8b10b line code, its data format is shown in Figure 2.5. Next to auxiliary data (identification numbers and status data), each of the eight current values is transmitted. Due to the way the CFC card works, each sensor channel is represented by two fields, a count and an analog-to-digital converter (ADC) value. The count represents the number of times an internal capacitor is charged during the integration time, the ADC value represents its final state of charge. One of these frames is sent by each CFC card every 40 μs to the MIBAD board, where it is received using high-speed serial transceivers. The internal logic of the MIBAD

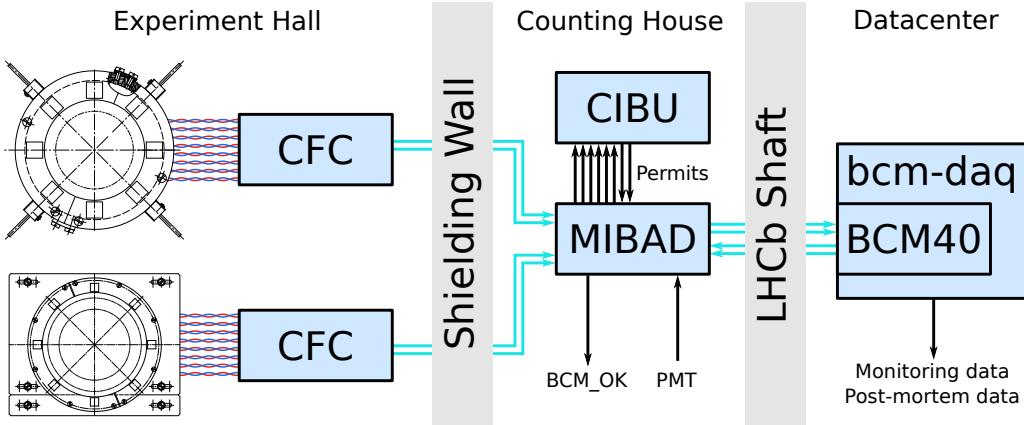


Figure 2.4: Data flow and topology of the upgraded LHCb BCM system. The twisted pair and black lines are copper connections, the aqua lines are optical fibers.

CID (card identity number)		
STATUS 1		
STATUS 2		
Count 1	ADC 1	
ADC 1	Count 2	ADC 2
ADC 2	Count 3	
ADC 3	Count 4	
Count 4	ADC 4	
Count 5	ADC 5	
ADC 5	Count 6	ADC 6
ADC 6	Count 7	
ADC 7	Count 8	
Count 8	ADC8	
FID (frame identity number)		
DAC1	DAC2	
DAC3	DAC4	
DAC5	DAC6	
DAC7	DAC8	
CRC		
CRC		

Figure 2.5: Data format of the CFC cards. The word length is 16 bit. [22]

board, described in the next paragraph, processes the data and makes a beam abort decision, which it communicates to the LHC machine using the so-called CIBU interface. The interface provides redundant inputs that allow dumping both beams and inhibiting injection to each beam if the BCM is not in a safe state for injection. The beam permit signal is returned through a channel for each beam to allow checking whether the permit signal was received correctly on the CIBU side. Next to the beam interlock interface, there is a redundant bidirectional optical connection to the LHCb surface datacenter, where the BCM40 board receives the data and status information. The current data is buffered and filtered by the *bcm-daq* host node that houses the BCM40. It is then forwarded to the monitoring system that allows the LHCb operators in the control room to oversee the BCM operation. As already described in the introduction, the LHC machine operators can request a memory dump of the BCM current value history by using the so-called *post-mortem trigger (PMT)*. The trigger arrives in the Counting House and is relayed by the MIBAD board through the status flags of the optical uplink to *bcm-daq*, where the current values are stored in a ring buffer. Upon request, the ring buffer is stopped and read out.

The internal logic of the MIBAD board is visualized in Figure 2.6. After receiving the CFC card raw data through high-speed serial transceivers (XCVRs on the left side), the data integrity is verified using checksums and comparison between the two redundant links. Running sums of two and 32 values are formed using current values calculated from the count and ADC value. Now the data path splits, on the one hand, it goes into the beam dump logic block that applies thresholds and sends permit signals to the CIBU interface. On the other hand, it goes into the frame builder block that assembles data frames according to the format specified in the next section for sending up to the BCM40 board in the data center for monitoring. Next to this, a controller block monitors the device's parameters, taking in status signals from all blocks exposing some. This status data is sent to the frame builder block as well and transmitted along with the measurement data. That way, the BCM system status can be monitored. The block also reacts to commands sent from the data center, e.g. for setting new thresholds or querying internal registers, that can be reported through the uplink as well.

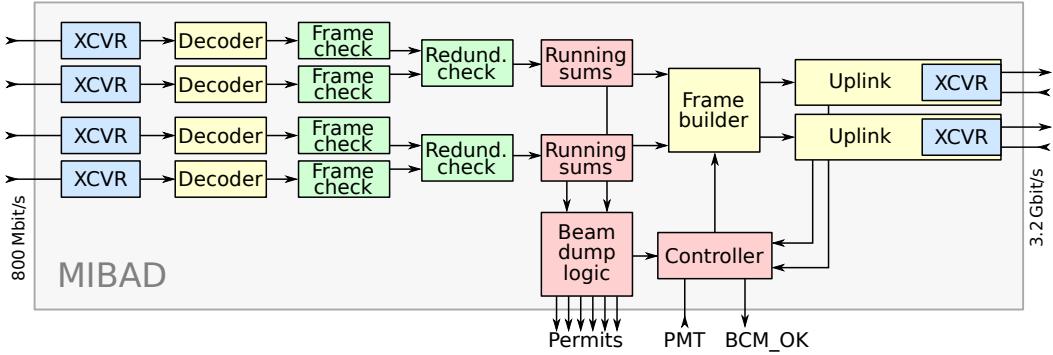


Figure 2.6: Internal block diagram of the MIBAD FPGA board. XCVR is short for transceiver.

2.3 MIBAD uplink block

In the course of this thesis, the uplink data format was specified and the firmware for the uplink logic block was developed. Both are described in this section.

2.3.1 Data format description

The data format is composed of sixty-four 64 bit wide words, where one block of these words is called a frame. As visible in the diagram in Figure 2.7, the focus for this format does not lie on optimal packing density, more on simplicity. In the diagram, the most significant bit is on the left side. Data fields are never split across multiple words which streamlines the encoding and decoding procedures. Bit-efficiency is not of concern for this format because the optical link is strongly oversized. Even with this rather inefficient arrangement of data, only

$$\eta = \frac{64 \cdot 64 \text{ bit}}{3.2 \text{ Gbit s}^{-1}} / 40 \mu\text{s} = 3.2 \% \quad (2.1)$$

of the link is saturated. The high data rate for this link was chosen because it matches an existing interface on the BCM40 side, which simplifies the implementation of the other side of communication.

The first word of each frame is used as a frame identification number that is monotonously increasing. Considering a $40 \mu\text{s}$ frame interval, this would suffice for 7.4×10^{14} seconds of continuous operation. Next, there are three blocks of 16 words containing the three running sums RS1, RS2, RS32 for each of the 16 diamond sensors, RS1 being the value of the last integration cycle. The longer running

sums obviously need $\log_2(2) = 1$ and $\log_2(32) = 5$ more bits not to truncate any binary places. At the 50th and 51st word-slots, status flags and a possible register readout reply is placed, if it was requested beforehand by the BCM40 board. If not, this word stays all-zero. Following this, the two CFC raw data frames are placed, to be able to verify the calculated running sums in the monitoring system, if necessary. Compared to the original raw data format (see Figure 2.5), the data is reordered slightly to fit in the 64 bit grid without fields splitting to multiple words. Finally, a cyclic redundancy check (CRC) [23] word is appended to verify the integrity of the whole frame.

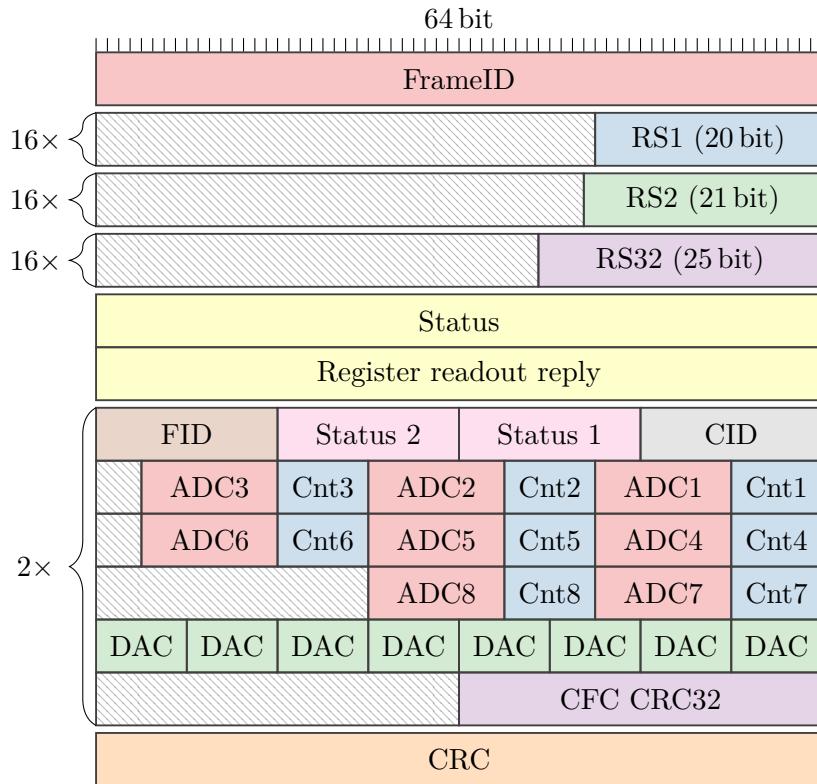


Figure 2.7: MIBAD to BCM40 uplink data format.

2.3.2 Block description and implementation

The task of the uplink block is taking in 64 bit words at 40 MHz to transmit them using a high-speed serial transceiver and vice-versa. An Intel Arria V *Transceiver Native PHY* hard IP block is used as transceiver. The internal structure of this

block is described in [subsection 2.1.2](#), where it is presented as a generic example. It is set to a data rate of 3.2 Gbit s^{-1} , this is equivalent to 16 bit words at a rate of 160 MHz when accounting for the 8b10b line code overhead of $\frac{2}{8}$. The Transceiver Native PHY is accompanied by a reset controller block that ensures the various reset signals for analog and digital circuitry, the transceiver exposes, are asserted in the correct sequence. Furthermore, it aggregates the transceiver's status signal for the control logic to interpret. As the word width on the FPGA side is 64 bit but 16 bit on the transceiver side, a kind of gearing has to be implemented. This is done through two FIFO blocks that, when configured in this way, allow reading and writing with a different word width. At the same time, they provide buffering at the clock domain crossing between the 160 MHz transceiver clock (`xcvr_clk`) and the regular 40 MHz FPGA fabric clock (`clk`). As the transmission occupancy is very small, no measures reacting to a full FIFO buffer are taken. The `rx` and `tx` signals are data out- and inputs, synchronous to `clk`. Sending data can be stopped by deasserting the `tx_enable` signal. The control logic assures that each 16 bit is aligned correctly by waiting for a "start of frame" control word before enabling writing to the Receive FIFO. Furthermore, it checks whether any of the received words are marked as erroneous by the transceiver and invalidates the whole 64 bit word, should this occur. This is communicated through the `rx_error` signal that is asserted in this case. If a valid received word is present at the `rx` signal vector, the `rx_valid` signal is asserted. `link_ready` is derived from reset controller signals and signalizes the transceiver status outward. The signals `serial_tx` and `serial_rx` represent the serial connection and ought to be connected to FPGA pins that interface the optical transceivers. Finally the `rst` signal allows to asynchronously reset the whole block, initiating the reset controller sequence, clearing FIFO memory, and resetting any control logic state.

To verify the function of the uplink block, simulation tests were conducted using the *Questa Advanced Simulator* by Mentor Graphics. In [Figure 2.9](#), the startup procedure of the block and the transceiver can be seen. For this test, the serial output and input are connected in a loopback manner. After the transceiver acquires a lock on the receiver side, the resulting output can be seen in [Figure 2.10](#). A hexadecimal header word (AFFE) and a counter is sent together with a counter. In the `rx` row this test pattern is visible and can be seen delayed with respect to the `tx` signal. This is on purpose, as a delay is part of the simulated fiber connection between serial output and input. Using this method, it would also be possible to introduce random bit errors and jitter into the data stream to test the resilience of the block. The simulation provides evidence that the uplink block works in the desired manner. Studies of the real-world behavior of the firmware as a whole are pending.

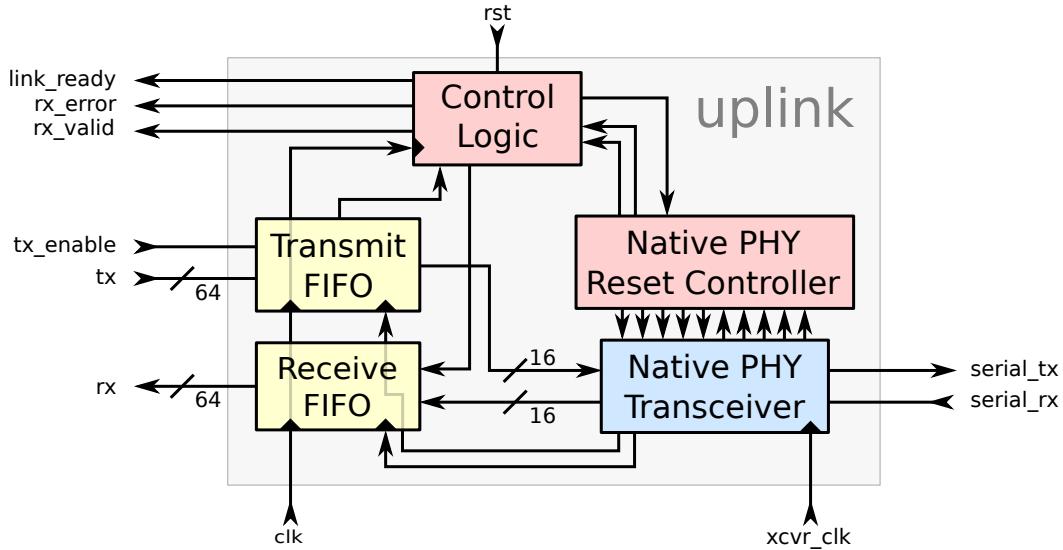


Figure 2.8: Internal block diagram of uplink block in the MIBAD firmware. Some signal paths are omitted for clarity.

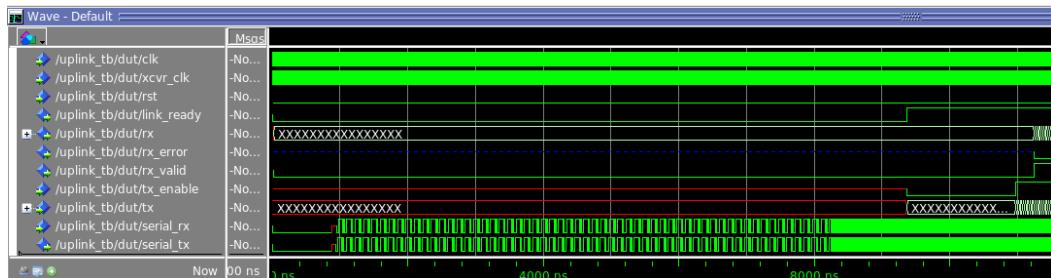


Figure 2.9: Questa Advanced Simulator screenshot of the startup sequence of the MIBAD uplink block signals.

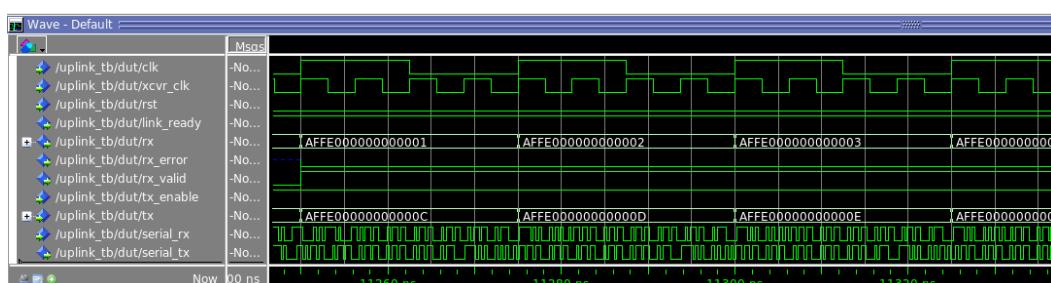


Figure 2.10: Questa Advanced Simulator screenshot of the MIBAD uplink block signals during operation.

3 Diamonds

3.1 Fundamentals

3.1.1 Interaction of particles with matter

The operating principle of particle detectors requires a form of energy deposition inside a sensitive volume. When particles with high kinetic energy traverse matter, they interact with the material. Several mechanisms occur in this case, all of which implying an energy loss of the penetrating particle to the medium. The dominant processes are determined by the energy of the particle. For the purposes of this thesis, it is sufficient to describe only the processes for charged particles. In [Figure 3.1](#) the mass stopping power, i.e. the energy loss per length in relation to the density, of copper is plotted for muons of different momenta. On the low-energy side, up to around 100 GeV/c, multiple approximations for ionization losses are visible. The stopping power shows a minimum, particles with energies around this value are called minimum ionizing particles (MIPs). Above 100 GeV/c, radiative losses (Bremsstrahlung) dominate the losses. For many purposes (in the region $0.1 \leq \beta\gamma \leq 1000$), the Bethe approximation can be used to obtain an appropriate estimate. For heavy particles it is described by the Bethe-Bloch formula

$$\left\langle -\frac{dE}{dx} \right\rangle = 4\pi N_A r_e^2 m_e c^2 z^2 \frac{Z}{A} \frac{1}{\beta^2} \left[\frac{1}{2} \ln \frac{2m_e c^2 \beta^2 \gamma^2 W_{\max}}{I^2} - \beta^2 - \frac{\delta(\beta\gamma)}{2} \right] \quad [24],$$

with the maximum single-collision energy transfer

$$W_{\max} = \frac{2m_e c^2 \beta^2 \gamma^2}{1 + 2\gamma m_e/M + (m_e/M)^2},$$

Avogadro number N_A , classical electron radius r_e , electron mass m_e , charge number of incident particle z , atomic number of material Z , atomic mass of material A , mean excitation energy I , density effect correction $\delta(\beta\gamma)$ (see [\[25\]](#), p. 538) and particle mass M . The ionization mechanisms depend strongly on the particles' mass, for light particles like electrons the above approximation is not valid. In addition to the mass aspect, it has to be considered that an electron is indistinguishable from

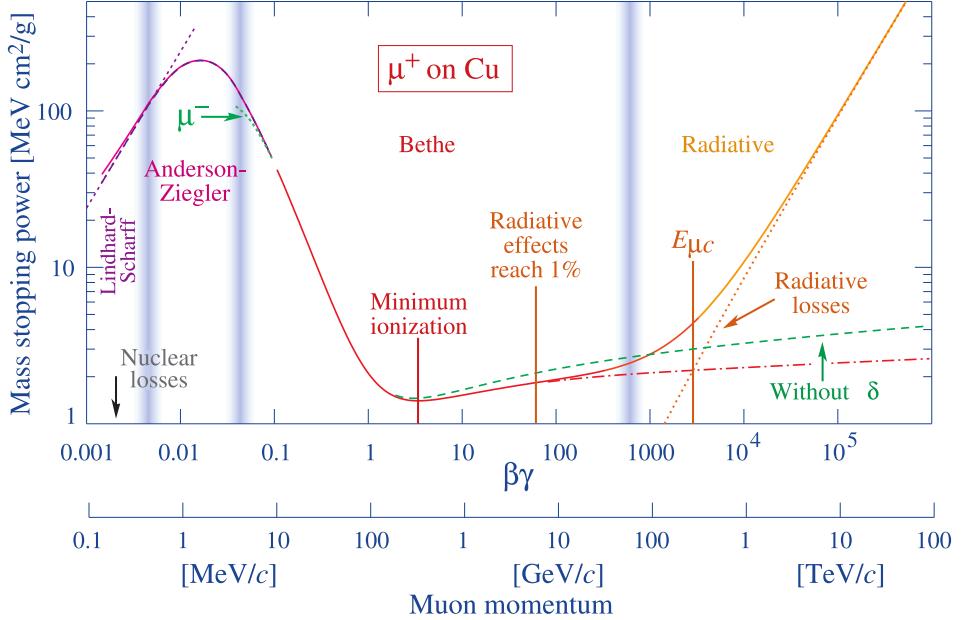


Figure 3.1: Mass stopping power for muons in copper as a function of muon momentum over 12 orders of magnitude. Vertical lines separate different approximations. [25]

the electrons excited in the material. These facts lead to the modified Bethe-Bloch formula for electrons, with a mean energy loss of

$$\left\langle -\frac{dE}{dx} \right\rangle = 2\pi N_A r_e^2 m_e c^2 \frac{Z}{A} \frac{1}{\beta^2} \left[\frac{1}{2} \ln \frac{m_e c^2 \beta^2 \gamma^2 \{m_e c^2 (\gamma - 1)/2\}}{I^2} + (1 - \beta^2) - \frac{2\gamma - 1}{\gamma^2} \ln 2 + \frac{1}{8} \left(\frac{\gamma - 1}{\gamma} \right)^2 \delta(\beta\gamma) \right] \quad [24].$$

For more precise estimates of mean energy loss, databases and simulations can be consulted. In Figure 3.2, the mean energy deposition for electrons in diamond and silicon is plotted over a wide energy range. This data is taken from the NIST EStar database [26].

Up to this point, only the mean energy loss per distance is considered. When measuring the signal of single particles, this is only partly helpful, as ionization is a statistical process. The energy loss for single particles is therefore not constant. It can be described by the Landau–Vavilov distribution [28, 29], which is shown in Figure 3.3 for 10 GeV muons traversing through 1.7 mm of silicon as the dot-dashed

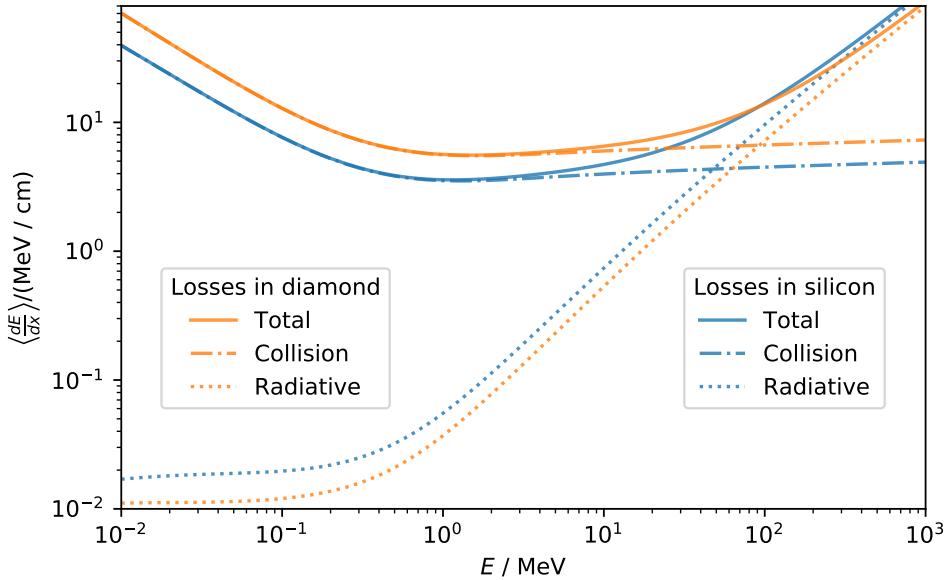


Figure 3.2: Mean energy deposition per length for electrons in diamond (orange) and silicon (blue). Bremsstrahlung (Radiative) and Ionization (Collision) contributions displayed separately. Data from [26], inspired by [27].

line. By adding the previously mentioned density correction to the Landau–Vavilov theory the distribution after Bichsel [30], shown in Figure 3.3 as a solid line, is obtained. As a property of a skewed distribution, the most probable value Δ_p and the mean $\langle \Delta \rangle$ differ significantly. For thicker detectors, the distribution's skewness decreases, as the number of interactions grows. This is due to the fact that the total loss is a sum of random variables (the loss per interaction) and according to the central limit theorem, the distribution of a sum of many random variables approaches a normal distribution, which is unskewed. To derive a loss spectrum in a given detector, single-particle simulations are often used, allowing precise estimates even for complex geometries.

3.1.2 Beta decay of Strontium-90

A simple way to gain a particle beam for the characterization of a detector in a laboratory is using a radionuclide source. ^{90}Sr is often chosen because the β^- electrons it generates have an energy spectrum that qualifies them as minimally-ionizing. Therefore, if a detector can detect ^{90}Sr electrons well, it will be able to detect other relevant particles and energies as well, because most of them have a larger energy loss per distance. Strontium-90 decays into Yttrium-90 with a half-life

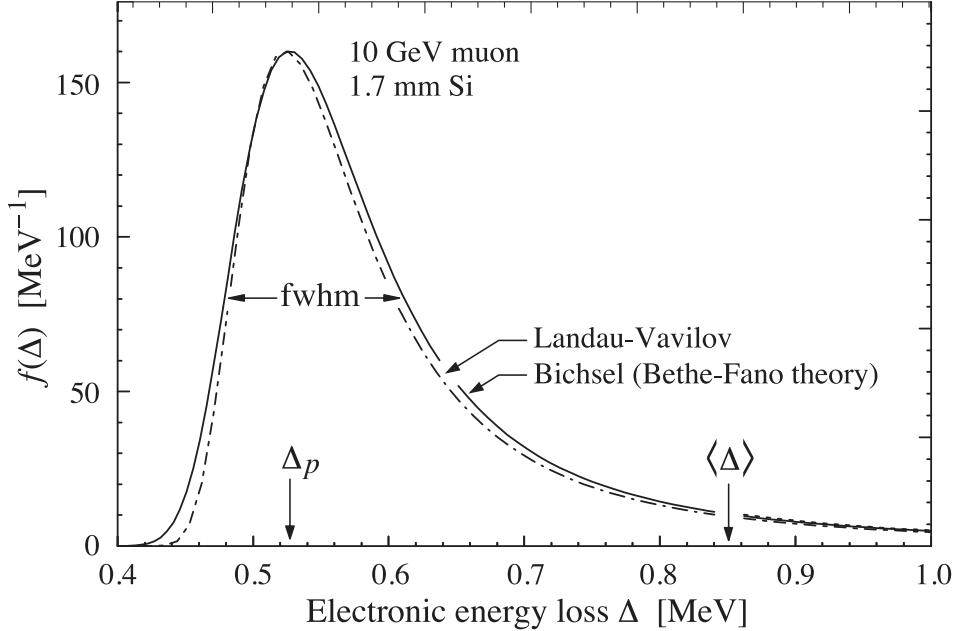


Figure 3.3: Energy loss distribution for 10 GeV muons propagating through 1.7 mm of silicon. Adapted from [25].

of 28.8 a



that further decays, with a half-life of 64 h, into Zirconium-90



which is stable. In the first decay, a total of 545.9 keV is split across the electron and the neutrino, in the second decay, the decay energy is 2278 keV [31, 32]. Due to the presence of two nuclides and the nature of the beta decay, it is necessary to use a simulation to derive the precise electron energy spectrum. In [33] this was done using Geant4 [34, 35, 36], resulting in a spectrum shown in Figure 3.4.

3.1.3 Current induction by moving charges

Electronic particle detectors rely on the detection of current signals stemming from the dynamics of freed charge carriers. As they drift in an electric field, they influence a displacement current in nearby electrodes electrostatically. This current is the measurable detector signal. The electric field is in this case generated either by an

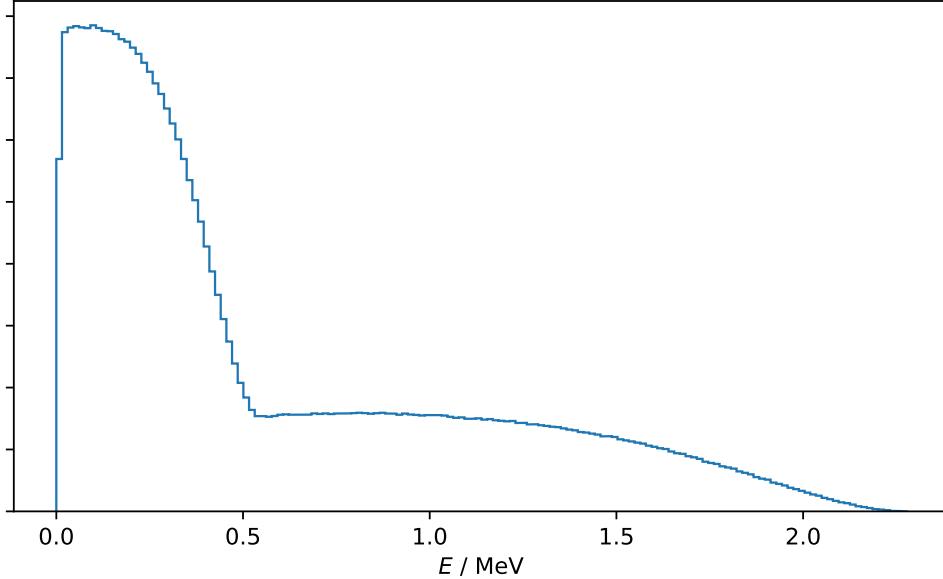


Figure 3.4: Total electron energy spectrum of a ^{90}Sr radiation source. [33]

external bias voltage or some intrinsic space-charge region like a p–n junction in the detector volume. In Figure 3.5, the mechanism is visualized: A positive charge q moves towards an isolated, conducting electrometer (analogous to a particle detector electrode) from infinity, attracting negative charges towards the upper part of the device while the atomic cores stay stationary. The apparatus reacts to the positive charge excess in the lower part by repelling the pivoted needle. When the lower part is then grounded through an ammeter, electrons attracted by the positively charged lower part flow into the electrometer and the resulting current can be measured.

This mechanism is quantitatively described by the *Shockley–Ramo theorem* [38, 39]. It states that for an arbitrary number of electrodes, the current influenced in electrode k is

$$i_k = q \vec{E}_{w,k} \vec{v} \quad (3.3)$$

with the particle velocity \vec{v} and the so-called weighting field $\vec{E}_{w,k}$ at the position of the particle. The weighting field is an auxiliary quantity defined as the electric field of only the electrode k with all other electrodes grounded and the moving charge removed.

Obviously, a current can only be measured as long the drift velocity is nonzero – i.e. the particle has not yet arrived at an electrode. For a thin (around 0.5 mm) detector

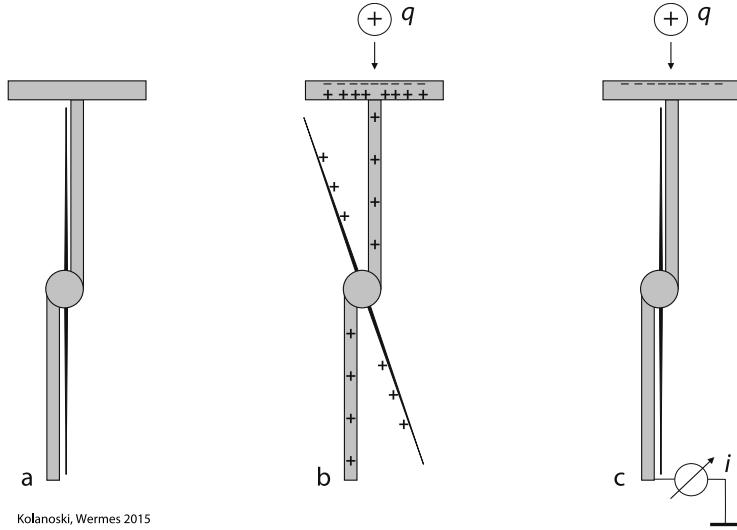


Figure 3.5: Electrometer visualization of displacement current signal generation through electrostatic influence. [37]

and common charge carrier mobilities of more than $1000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ in diamond [40] for example, this results in rather short pulse durations of few nanoseconds.

3.1.4 Diamond as a detector material

Diamond is a variant of crystalline carbon in the form of the crystal structure *diamond cubic*. This structure comprises two displaced face-centered-cubic lattices [41] and is shown in Figure 3.6. Each atom has four sp^3 bonds with their neighbors, leading to a high displacement threshold energy, i.e. the energy needed to remove an atom from the lattice, of 43 eV. That implies the very high mechanical hardness diamond is known for. Though diamond is, with a band gap of 5.47 eV [41], usually classified as an insulator, it can be considered a semiconductor as well. Due to the large band gap, its intrinsic charge carrier density is low, leading to very low dark currents (e.g. below 1 pA in our measurements). The general principle of semiconductor detectors is that traversing particles excite electrons from the valence band to the conduction band along their tracks, leaving behind holes in the valence band. Both, quasiparticle holes, and excited electrons can then drift in an applied or intrinsic electric field. Diamond's relatively high density of 3515 kg m^{-3} [42] counteracts its high mean energy for electron-hole pair creation of 13.19 eV [43] slightly with respect to charge carrier yield. In diamond, electrons exhibit a mobility of $1800 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, holes of $1600 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [40]. The moving charge carriers

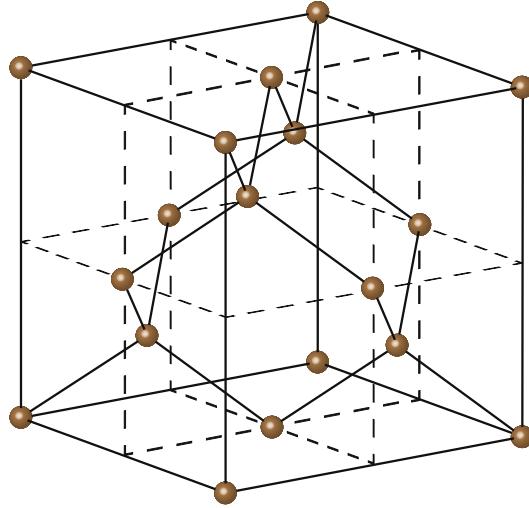


Figure 3.6: Diamond cubic crystal structure. [37]

influence a signal in affixed electrodes as described in the last chapter. Thanks to its extremely low intrinsic charge carrier density, diamond is used without any doping or p-n junction, as opposed to most other semiconductor detectors.

All semiconductor detector materials exhibit an aging process when exposed to radiation because of induced lattice defects and impurities. This leads to increasing leakage currents, dropping charge collection efficiencies, and, for doped semiconductors, even to a change of the doping structure. Its large band gap together with the high displacement threshold energy is the reason why diamond is considered very radiation hard. To determine detector efficiency and radiation hardness, one has to consider the average lifetime of the charge carriers, as a longer lifetime inside the material leads to a larger signal at the electrodes. The lifetime is limited by recombination processes, where electrons and holes merge again. Those occur for example at impurities or lattice defects. This is often done quantified by defining the charge collection distance (CCD)

$$d_{\text{sep}} = (\mu_e \tau_e + \mu_h \tau_h) E \quad [40] \quad (3.4)$$

where $\mu_{e,h}$ are the mobilities, $\tau_{e,h}$ the average lifetimes, and E the electric field strength. d_{sep} can then be interpreted as the sum of the mean free path of electrons and holes. For simple detector geometries with parallel electrode plates, the CCD can be approximated as

$$d_{\text{sep}} \approx \frac{Q_{\text{det}}}{Q_{\text{ion}}} \cdot d, \quad (3.5)$$

i.e. the so-called charge collection efficiency (CCE) multiplied by the detector depth d . In Figure 3.7, diamond and silicon are compared with respect to their CCD for different states of irradiation. It is apparent that diamond shows a better performance.

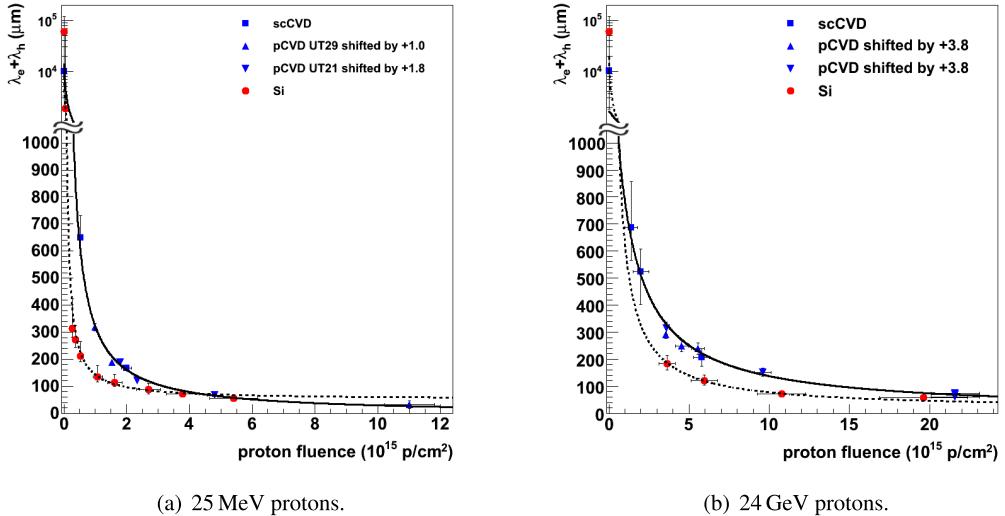


Figure 3.7: Charge collection distances of different detector materials (diamond in blue, silicon in red) after irradiation. [44]

Manufacturing process

In Figure 3.7, two kinds of diamond are mentioned, that differ in their manufacturing process: Polycrystalline chemical vapor deposition (pCVD) and single-crystal chemical vapor deposition (scCVD). Both have the basic method in common, illustrated in Figure 3.8. Inside a radio frequency cavity, a plasma is formed by feeding high-intensity microwaves into a gas volume. The gas has to provide carbon and hydrogen atoms, therefore a mix of methane (CH_4) and hydrogen gas is often used. The growth substrate, either a crystalline material for single-crystal growth or diamond powder for polycrystalline growth, is heated to $600\text{--}800^\circ\text{C}$. On the growth surface, carbon is deposited, partly in graphite and partly in diamond form. The atomic hydrogen contained in the plasma etches away the graphite depositions, leaving only diamond to grow. When diamond powder is used as the substrate, the resulting structure is polycrystalline, i.e. small monocrystalline grains are formed with boundaries between them. At these boundaries, the recombination of electrons and holes is possible, therefore polycrystalline diamond generally has a lower charge

carrier lifetime and thus charge collection depth than monocrystalline diamond. On the other hand, pCVD diamond is simpler to produce and therefore less expensive. Wafers up to a diameter of 140 mm are possible, while with the scCVD, dimensions are limited to around 8 mm [42].

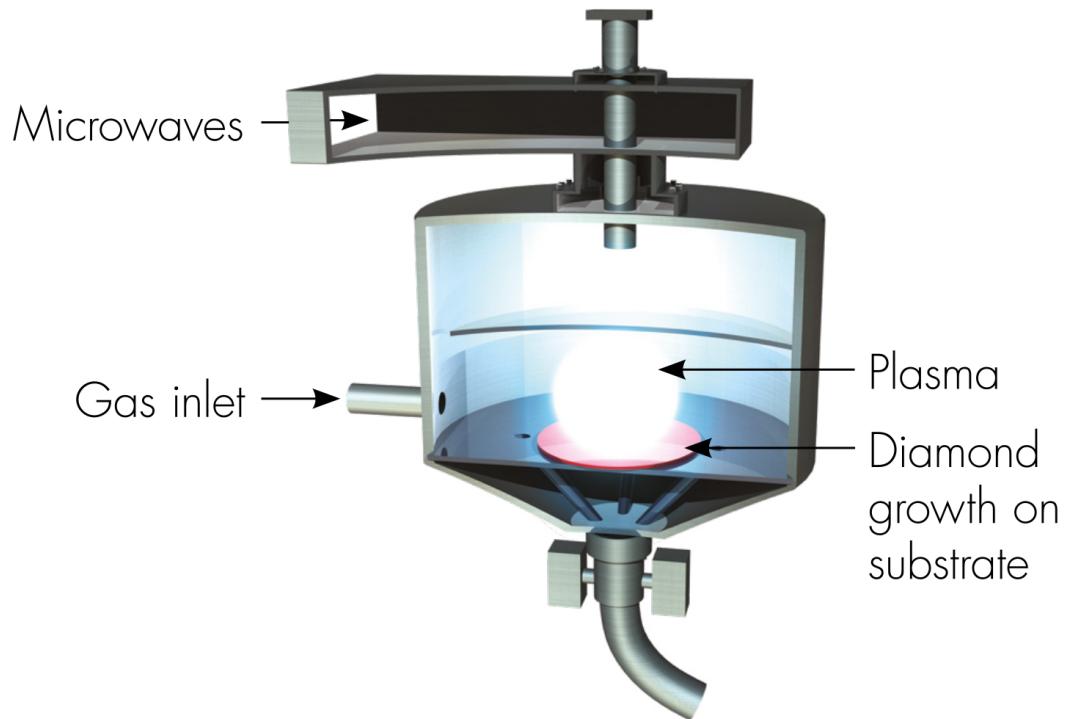


Figure 3.8: Apparatus for chemical vapor deposition to produce synthetic diamond [42].

Surface finish implications

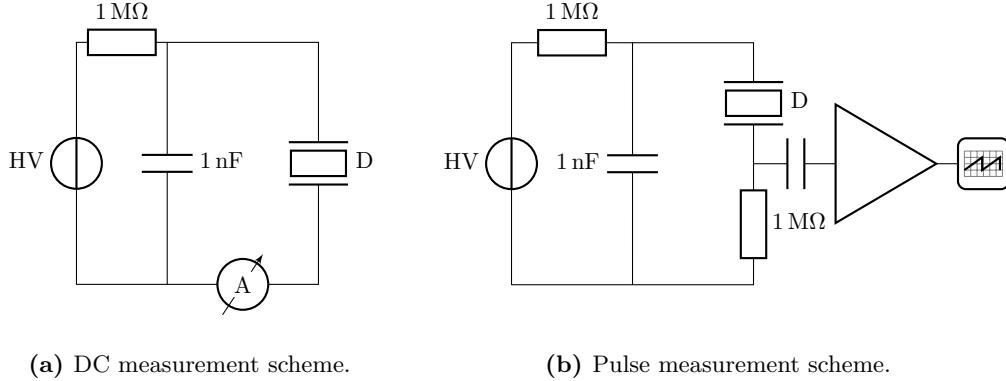
To obtain a signal from a diamond detector, it is necessary to create contact electrodes on both sides of the diamond. This is usually done by vapor deposition of a nonreactive metal like platinum or gold. At the interface between diamond and the electrode, a metal-semiconductor junction is formed. This junction can have either rectifying (*Schottky contact*) or non-rectifying properties (*ohmic contact*). A Schottky contact can be considered analogous to a p-n junction, as a space-charge region forms. For detector purposes, this is an unwanted effect, as the region features a high field strength (around 1 V nm^{-1}), partly trapping freed electrons below

it. This inhibits the electrons draining, leading to a polarization effect, as the electrons' field superposes the bias field. That in turn reduces the field present in the detector bulk and thereby the charge collection.

Another aspect is mechanical adhesion, as very flat diamond surfaces offer very little adhesion to most metals. Therefore, interface materials like tungsten are needed that form a chemical bond to the diamond surface. Another alternative that also provides good contact properties is layers of diamond-like carbon (an amorphous carbon variant), platinum, and gold [45]. The diamonds characterized in this thesis use this variant.

Measuring diamond performance

When using diamonds as detectors, the employed sensors need to be well-characterized, especially when utilized as a safety system. The key performance figure is the above-mentioned charge collection distance. There are two common methods to determine it for a given sensor: Direct current (DC) measurement with a well-known particle beam and single-pulse measurements. For the former, the detector is exposed to a beam of known flux and energy distribution. A bias voltage is applied and the current through the diamond is measured using an ammeter. In [Figure 3.9a](#), a simplified circuit diagram for this method is presented. The particle beam is often generated by a radioactive source, whose radiation field must be known well. Furthermore, the placement of the sensor relative to the radiation field must be kept constant for consistent results. Those requirements can be remedied by employing a single-pulse measurement scheme. As outlined in [Figure 3.9b](#), pulses of single traversing particles are amplified by a high-gain low-noise amplifier and are resolved temporally by an oscilloscope. The resulting pulse area distribution is compared to the expected ionization charge distribution and the charge collection efficiency is derived. The scheme is insensitive to flux variations and only relies on the knowledge of the beam energy distribution, as flux is only reflected in the pulse rate. On the downside, this scheme introduces difficulties, such as constructing an adequate amplifier and calibrating it. Even if unknown systematic uncertainties would not allow absolute charge collection efficiency determination, a relative comparison of multiple diamond sensors is possible in both schemes.



(a) DC measurement scheme.

(b) Pulse measurement scheme.

Figure 3.9: Conceptual circuit diagrams for measuring charge collection distance using two methods. The diamond under test is designated as D .

3.2 DONNA board design

The amplifier board designed in the course of this thesis is called DONNA. It is inspired by the amplifier circuit in [46] and a simplified circuit diagram is provided in Figure 3.10. The main functional elements are three GALI-39+ monolithic microwave integrated circuit (MMIC) amplifiers manufactured by Mini-Circuits. Internally, these are InGaP Darlington stages providing an amplification bandwidth of 7 GHz and a gain of around 20 dB in the relevant frequency range [47]. They are biased through their output port. Integrated bias tees of the type Mini-Circuits TCBT-14R+ [48] are used to provide the supply current. In the schematic, the bias tees are drawn in their discrete representation, consisting of an inductor and a capacitor, allowing DC current to flow through the inductor to the amplifier, but not into the input of the next stage. Then again, the high-frequency signal from the amplifier can traverse the capacitor but is blocked by the inductor. Also, there is an Analog Devices LT3042 voltage regulator [49] with a power supply rejection ratio (PSRR) of 79 dB integrated on the board to suppress any noise coming from the voltage supply.

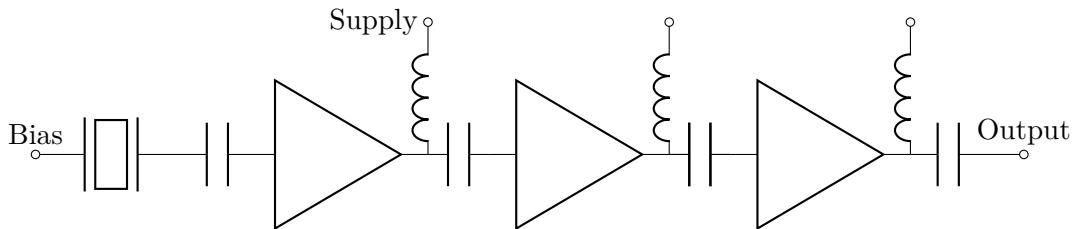


Figure 3.10: Simplified internal circuit diagram of the DONNA amplifier board.

Another vital component, the calibration circuit, is included on the board as well. It allows generating calibration pulses that are in the same order of magnitude as the expected detector pulses. To achieve this, the circuit consists of a high-ratio voltage divider feeding into a capacitor. It replicates the calibrator in [50]. A step signal of known height is injected, reduced by the divider, and then differentiated by the capacitor, yielding a known-charge pulse through

$$Q = CU \quad (3.6)$$

with a calibrator capacity C of 3.3 pF. The voltage divider is set up as a Π attenuator to match the input and output impedance. A circuit diagram is shown in [Figure 3.11](#). The circuit is connected to the amplifier input by a solder jumper, designated in the figure by a switch. In appendix [A.1](#), the complete schematics for of the DONNA board are presented.

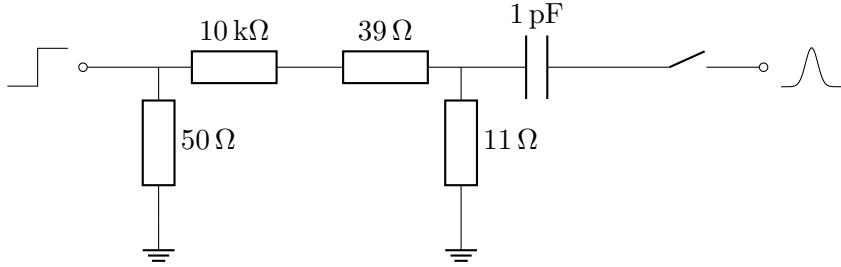


Figure 3.11: Schematic of the calibration circuit.

From these schematics, a printed circuit board (PCB) was designed. At the high signal frequencies, the impedance of traces on the PCB potentially needs to be taken into account to avoid reflections and distortions. To do this, the geometry of conductors and dielectrics has to be adjusted. In practice, that means for a standard two-layer PCB the track width needs to be around 3 mm to achieve a standard 50 Ω characteristic impedance. To circumvent this, usually four or more layer boards are used for radio frequency (RF) applications. They allow having a much thinner dielectric between the outer and inner layers, as mechanical strength is provided by a thicker dielectric between the two inner layers. A thinner dielectric between the first and second (ground) layer allows for narrower matched-impedance traces on the first layer. For the DONNA PCB, a two-layer board was used, because the length of all RF traces is shorter than $\lambda/10$, the rule-of-thumb limit up to which impedance matching is not required [51]. [Figure 3.12](#) depicts the final manufactured circuit board before soldering any components to it. For more detailed PCB design drawings, see [Appendix A.2](#). The large golden area on the center-right side is the diamond pad, where the detectors will be placed. The bias voltage is applied to the top of the diamond through a spring soldered to the SPRING1 pad just below.

3.2 DONNA board design

The slimmer right side separated by a slot is another approach to connect the calibration circuit but proved unsuitable and is therefore not expanded on. The board was subsequently assembled by the scientific electronics workshop at TU Dortmund. In Figure 3.13, the board can be seen with the components soldered to it.

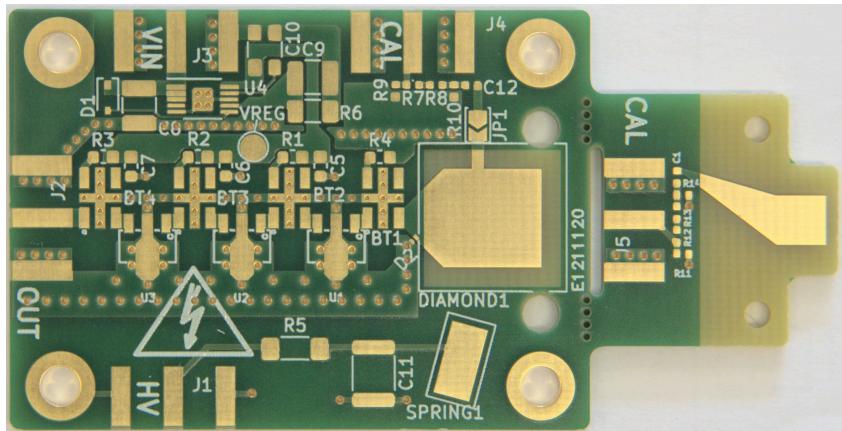


Figure 3.12: The bare DONNA printed circuit board.

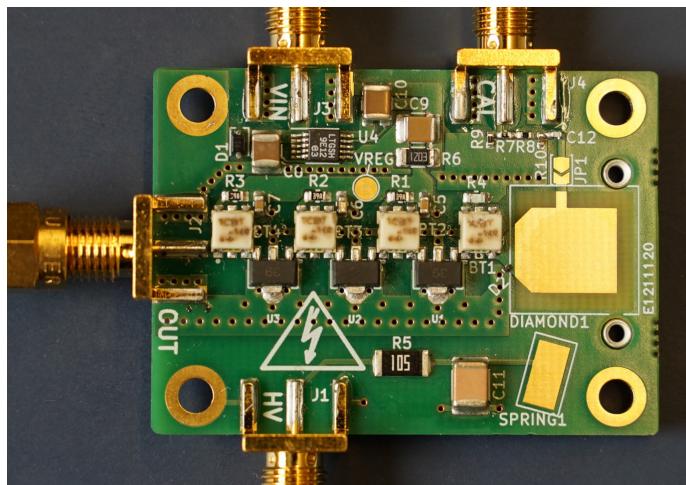


Figure 3.13: The assembled DONNA printed circuit board, still missing the high-voltage spring.

3.2.1 Initial operation

When starting up the board without any input connected, it showed very strong oscillatory behavior, also called amplifier instability. The resulting output signal showed the largest peak at about 8 GHz and varied wildly when the surroundings of the board were changed, e.g. by bringing pieces of metal in its vicinity. It is suspected that this instability is due to feedback from the amplifier outputs to amplifier inputs. Multiple approaches to reduce the feedback were tested. Two different microwave-absorbing materials, 3M AB7050HF [52] and Laird Eccosorb LS-30 [53] were applied to the board in various positions. Finally, a metal box internally clad with Eccosorb LS-30 and some absorber patches directly on the board showed a slight improvement. The final setup can be seen in [Figure 3.14](#). Still, a strong resonance could be observed, therefore other measures had to be taken. By reducing the amplifier current, the gain can be reduced. This in turn reduces the feedback instability. Unfortunately, a method of reducing the amplifier current was not implemented on the board – the voltage regulator output voltage is set by a fixed resistor. Reducing the board input voltage and driving the voltage regulator below its programmed output voltage is non-optimal for noise performance but proved to be working. A spectral analysis of the remaining noise is plotted in [Figure 3.15](#). The remnants of the resonance at 8 GHz are clearly visible, next to various other peaks at lower frequencies. Overall, the noise floor, while definitely suboptimal, later proved small enough for measurements. The input voltage for a maximal signal-to-noise ratio (SNR) had to be determined by a series of measurements with test pulses and was found to be 7.5 V in [33].

Another difficulty was the contact quality at the interface between diamond and PCB. For the first test measurements, pulses could not be seen reproducibly. Preceding DC measurements were done using a clamp with fine tips, resulting in a relatively high contact pressure – the large contacting pad can not provide this. A remedy was found in using a thin foil of indium between the diamond and the board pad. Being a very soft metal, it allowed for a better contact quality without exerting large pressure.

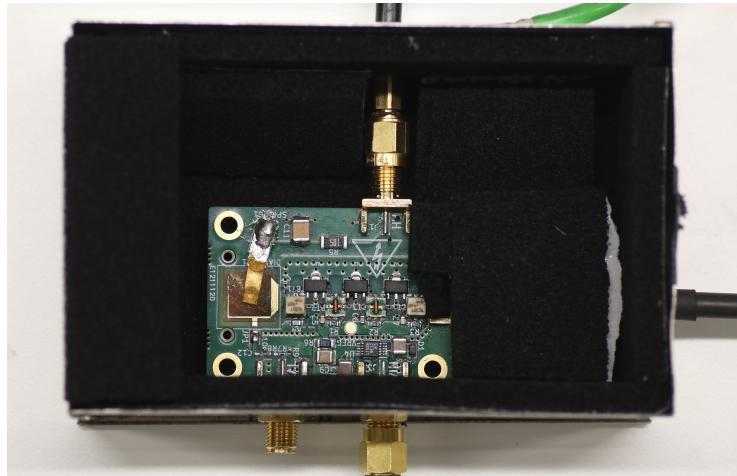


Figure 3.14: The DONNA board in its final microwave absorber-clad enclosure.

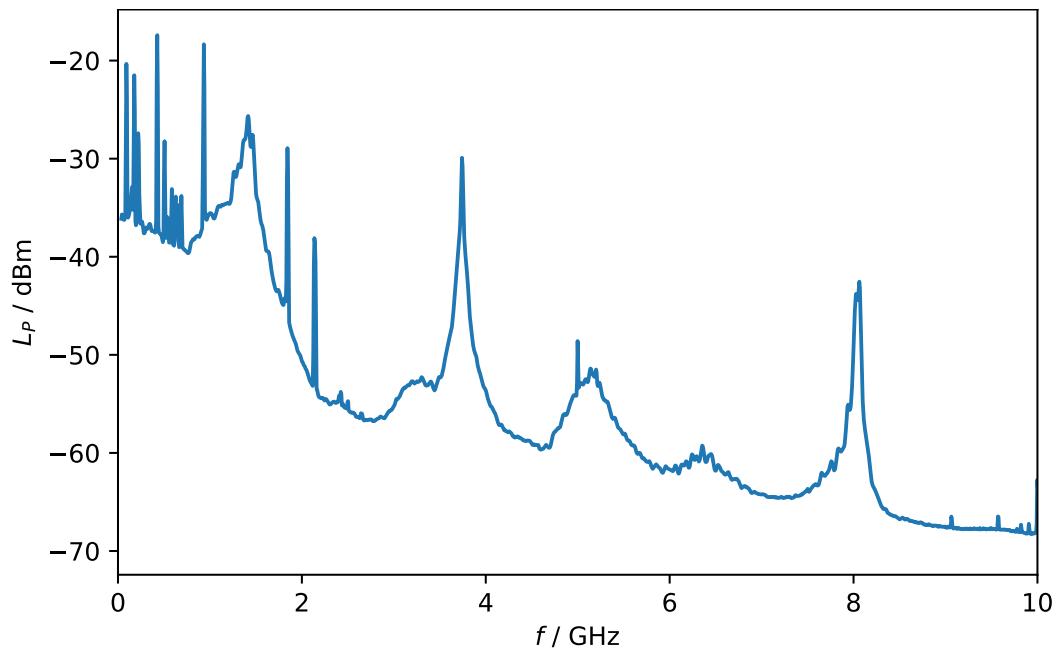


Figure 3.15: Noise power level spectrum of the DONNA board at 7.5 V input voltage from 0–10 GHz.

3.3 Pulse measurement setup

Next to the DONNA board, some other devices are needed for the diamond characterization setup, shown in [Figure 3.16](#). The nanosecond pulses amplified by the board are digitized by a LeCroy 825Zi-A oscilloscope [54], providing an analog bandwidth of 20 GHz and a sample rate of 40 GSamples/s on the used input. A pulse-width trigger in steps of 100 ps can be applied for filtering waveforms that are likely to be noise, which will be discussed later. The acquired waveforms are then saved to disk in a binary format. To feed in voltage steps for the calibration circuit, a Hewlett-Packard 81110A pattern generator [55] is used. It provides a rise time of 800 ps, which is sufficiently similar to the expected pulse rise time. The high voltage for the diamond bias is generated by a Keithley 6487 picoammeter [56] with an integrated voltage source. A particle beam is provided by the KV1 ^{90}Sr source, with an activity of around 13 MBq at the moment of the experiments.

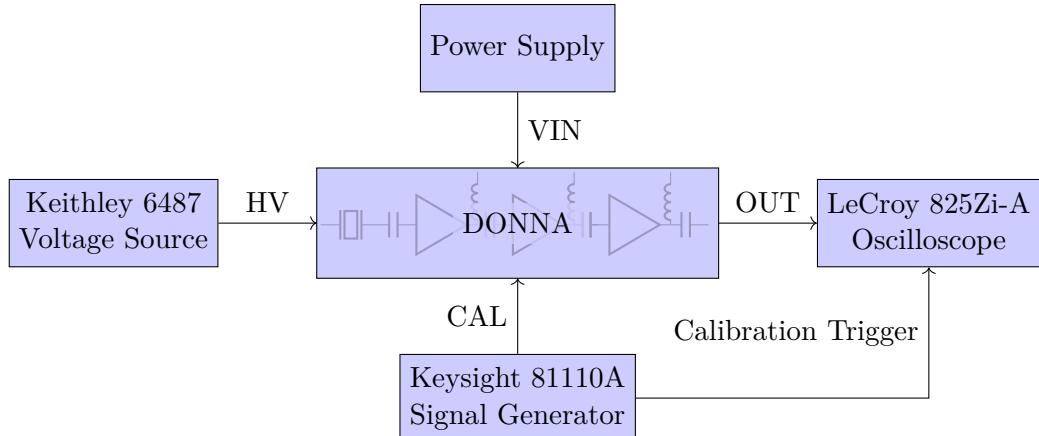


Figure 3.16: Block diagram of the single-pulse measurement setup.

3.4 DC measurement setup

The previously established DC current measurement setup consists of the Keithley 6487 picoammeter with integrated voltage source and some way of connecting the diamond, either a clamp or a small PCB with a pad and a spring, similar to the DONNA board contacts. In the case of the clamp contacting, external circuitry provides the RC filtering mentioned above. This circuitry is called mini-DCU (diamond connection unit). Consequently, the PCB variant, integrating the components on a small board, is called μ DCU. It is shown in [Figure 3.17](#).

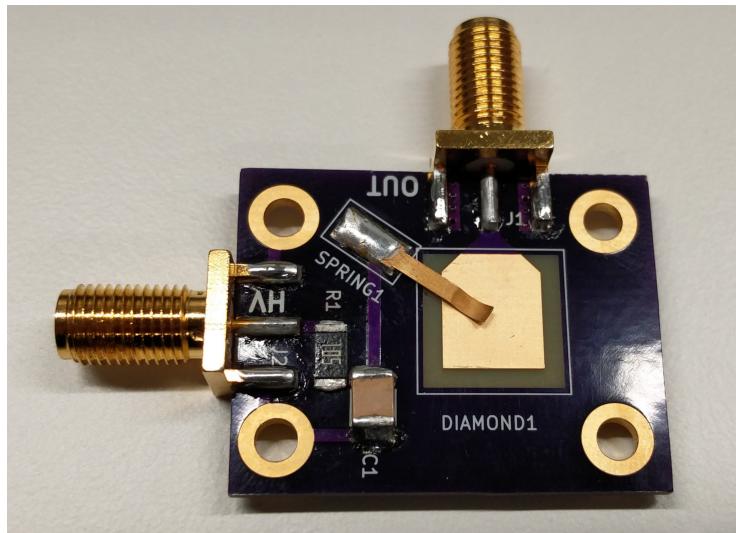


Figure 3.17: The μ DCU, used to connect to the diamond in the DC current measurement setup.

There are two ways to use this setup: On the one hand, it can be used together with either a vertical linear stage and the ^{90}Sr source to control flux by varying the distance. On the other hand, it can be placed in an accelerator-generated particle beam, a horizontal linear stage is used to vary the diamond position relative to the possibly wide beam.

3.5 Results

After adjusting the amplifier and contacting, it is possible to observe single-particle pulses with the DONNA board. An exemplary large pulse is shown in [Figure 3.18](#). To gain insight into the sensor performance, many of these pulses have to be acquired and the collected charge needs to be determined. To map from a pulse waveform to a pulse charge, a calibration using test pulses of known charge is carried out. This is described in detail in the next section.

3.5.1 Calibration

The calibration circuit consists of a voltage divider that feeds an external voltage step into a small capacitor to inject a known charge into the amplifier input. As a

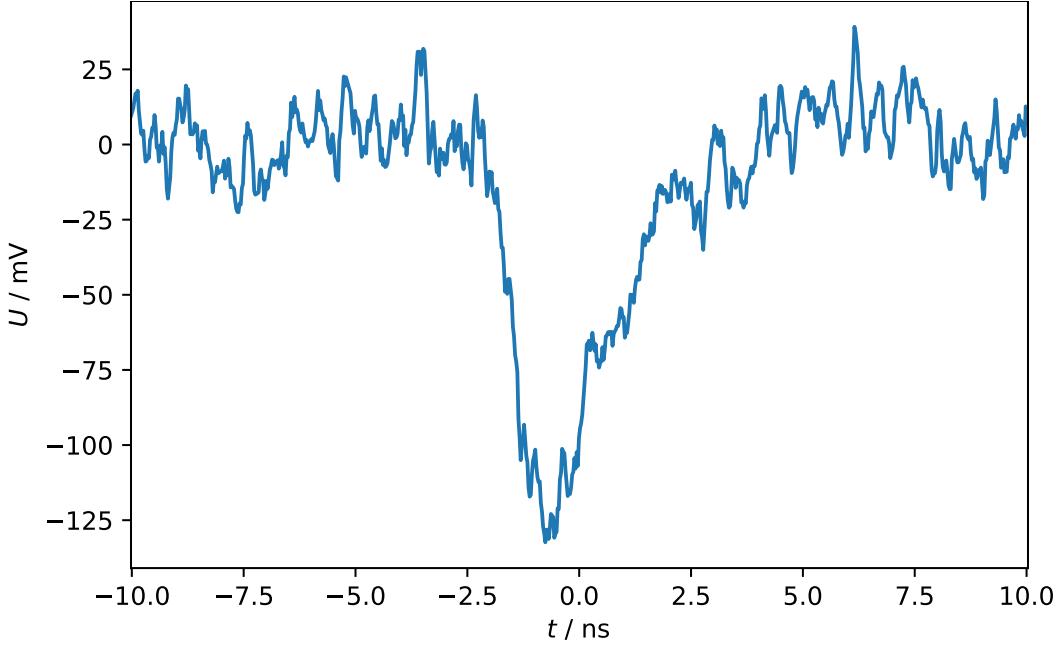


Figure 3.18: Exemplary single-particle diamond detector pulse.

first step, the calibrator voltage divider ratio is measured, as the component tolerances are rather high. This is done, in accordance with [50], with a comparatively high constant voltage, as directly measuring a very small voltage step is nontrivial. In [33] the voltage divider ratio is determined as

$$\frac{U_{\text{in}}}{U_{\text{out}}} = 905.3 \pm 1.3. \quad (3.7)$$

Now the relation between the fed calibration voltage step size and the charge injected into the amplifier chain is known, therefore the whole setup can be calibrated. The pulse generator is used to generate steps of different sizes and triggers the oscilloscope, where the pulses are stored. An exemplary pulse is plotted in Figure 3.19. Around one thousand pulses per voltage step are analyzed with respect to their pulse area, i.e. their time-integrated voltage signal. This data was taken in [33] as well. In Figure 3.20, the pulse area averages for every calibration voltage step are depicted. A ordinary least squares linear regression constrained to zero intercept is used to determine a calibration constant of

$$\kappa = (30.2 \pm 0.4) \text{ fC nV}^{-1} \text{ s}^{-1} \quad (3.8)$$

that is henceforth used to convert pulse areas into pulse charges.

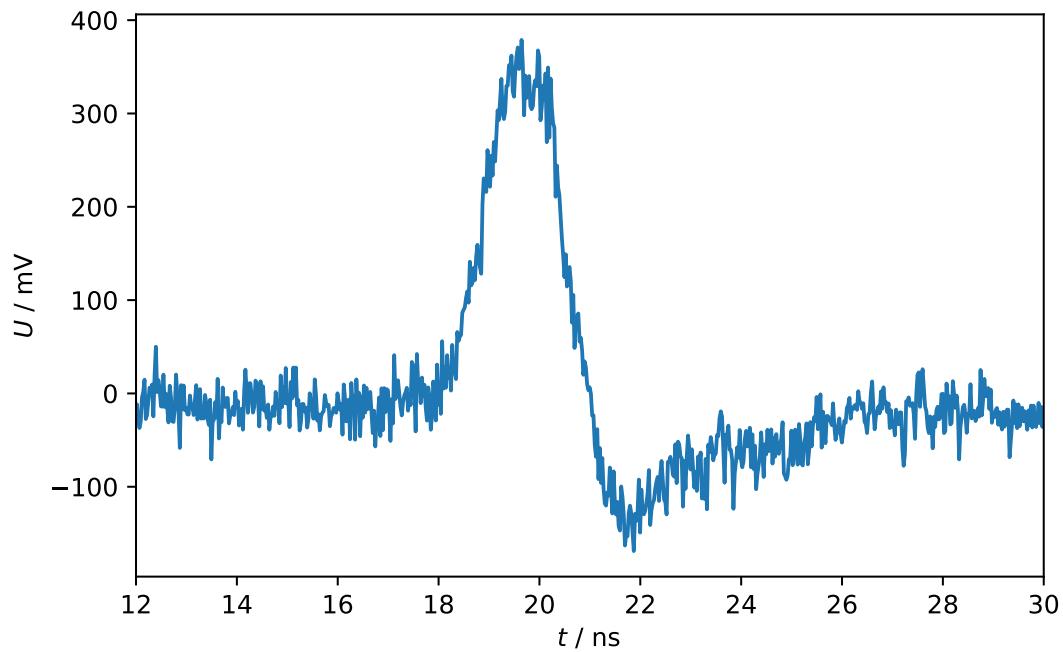


Figure 3.19: Exemplary calibration pulse waveform.

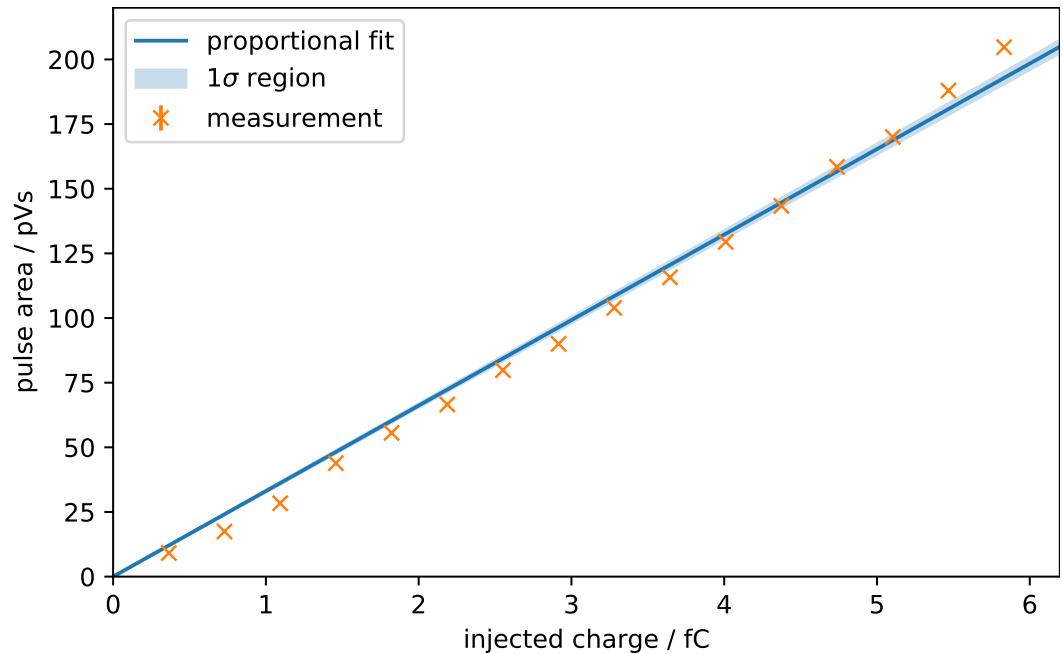


Figure 3.20: Calibration curve for the DONNA amplifier chain.

Another setting that needs tuning is the pulse-width trigger setting. Under the assumption that noise trigger events are shorter than signal pulses, noise can be rejected by requiring the voltage to stay above the trigger level for a defined time span. The assumption is validated by comparing the signal that can be seen without a radiation source present to the signal under irradiation. In Figure 3.21, pulse charge spectra for different width trigger settings between 200 ps and 700 ps are presented. These spectra are taken at a bias voltage of 500 V using the diamond called *CERN-873640-35* and at a delay of one hour after switching on the bias voltage and exposing the sensor to the ^{90}Sr source. This delay is chosen because there is a time dependence in diamond detector properties, which is of exponential nature. For our setup this has been investigated in [57], hinting that one hour would be an appropriate delay. An explanation for the behavior can be found in the so-called *pumping effect* [50], that occurs due to the fact that impurity atoms contained in the diamond lattice create charge traps that capture electrons, reducing the collected charge. When the traps are filled, the full pulse charge can be measured. For the low width trigger settings, a charge spectrum with two peaks is visible, the lower peak being noise. A setting of 500 ps is chosen to suppress this lower peak while rejecting signal pulses minimally.

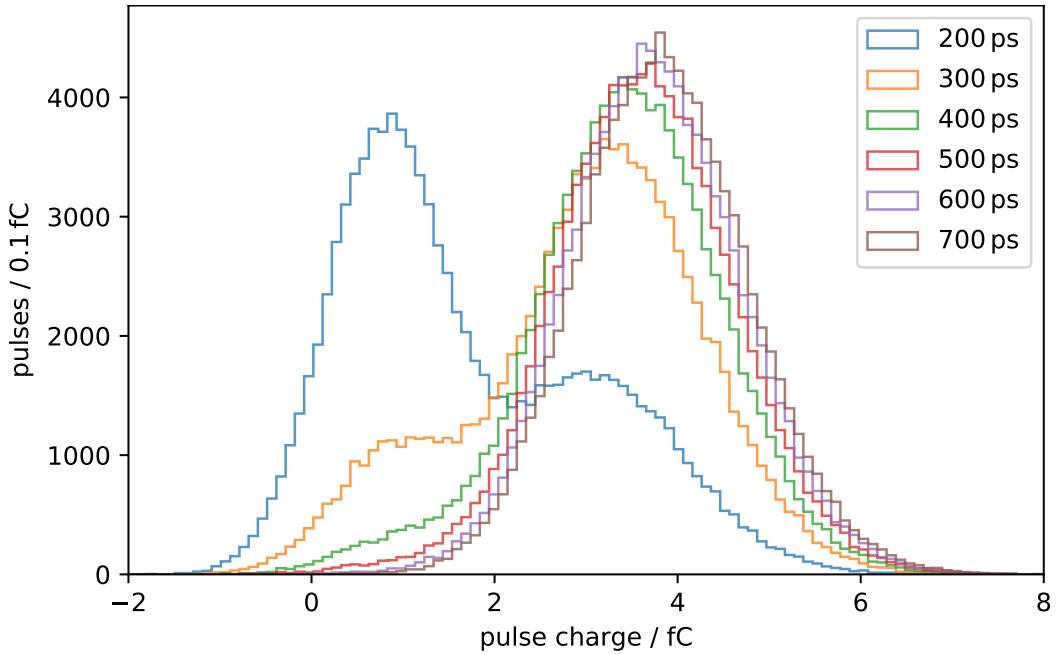


Figure 3.21: Pulse spectra for different pulse-width trigger settings.

3.5.2 Spectra

When 100000 pulses are captured, their area calculated, and the calibration constant applied, the charge spectrum presented in orange in [Figure 3.22](#) is the result. The bias voltage is 500 V – the same as for the previous trigger width measurements. As a comparison, a simulated charge spectrum for the same experimental setup from [33] is presented in blue. This represents an upper limit; the spectra would be identical if the sensor and the characterization setup would be ideal. It is visible that the spectra agree roughly, but the measured spectrum is missing the long Landau–Vavilov tail to high deposited charges.

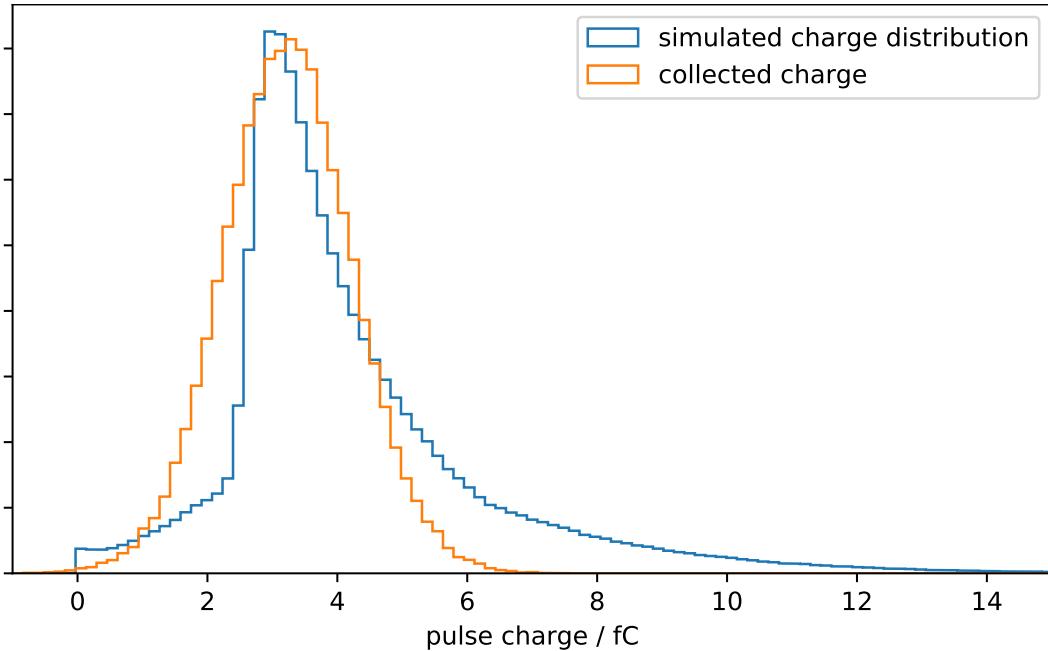


Figure 3.22: Measured charge spectrum of diamond *SO-202-D02* and simulated spectrum from [33]. The histograms are normalized to the same integrated area, as the measured spectrum contains 100000 pulses, where the simulated data contains around 2.2 million.

When this same measurement is repeated for all available diamond sensors, the spectra shown in [Figure 3.23](#) result. They appear to be in agreement with each other. A histogram of the mean charge for every diamond sensor is shown in [Figure 3.24](#). In this plot, the simulated deposited charged is marked with an orange line.

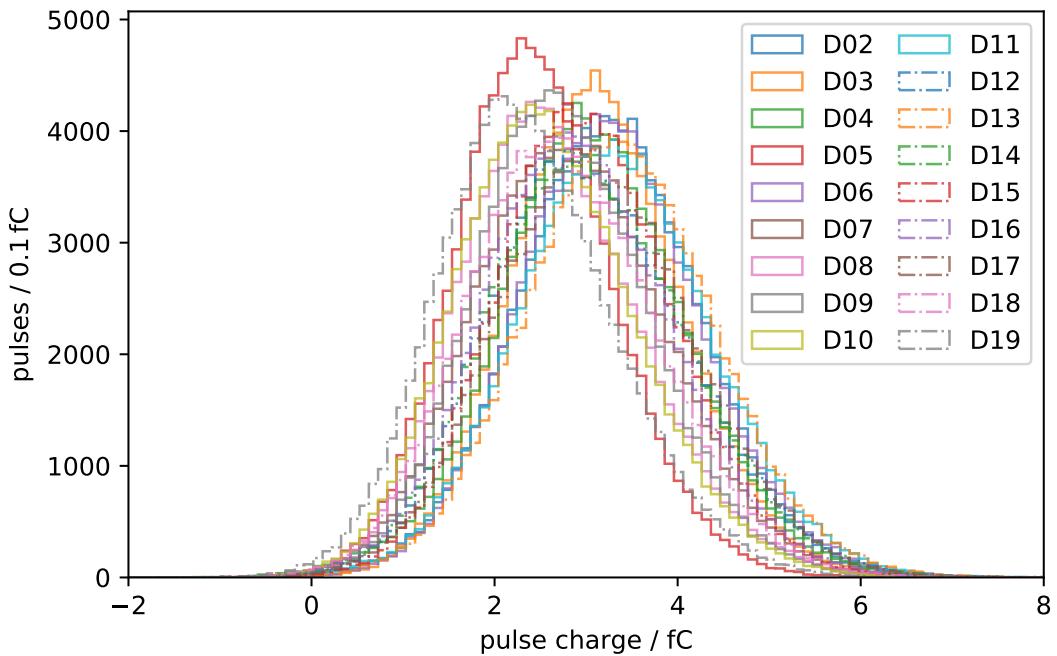


Figure 3.23: Pulse charge spectra for all measured diamond sensors.

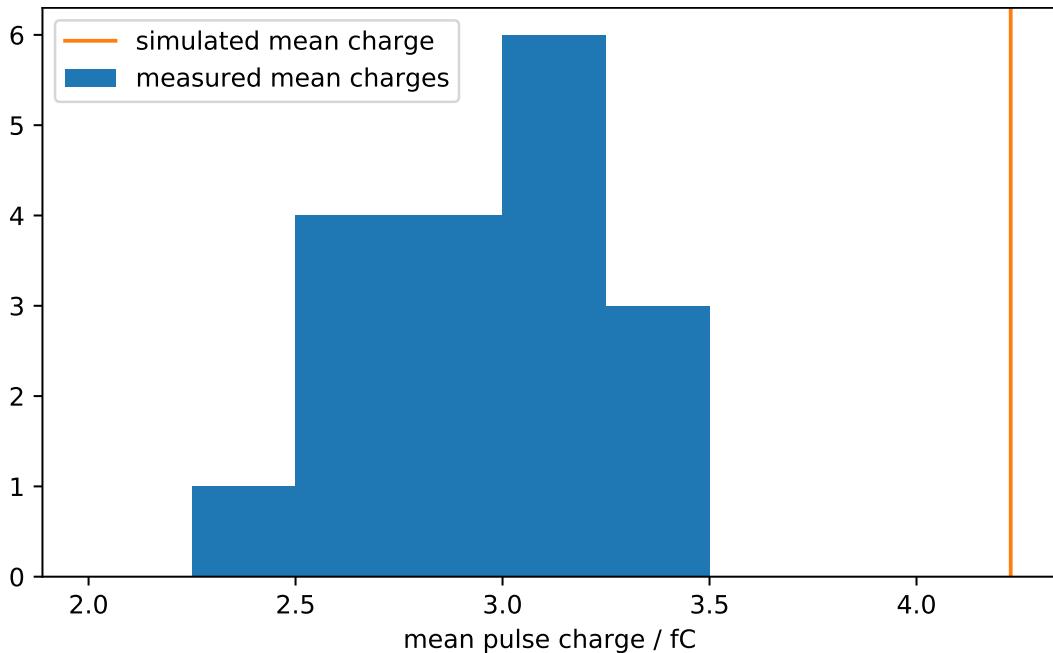


Figure 3.24: Histogram of all measured mean collected charges. For comparison the simulated freed charge is shown with an orange line.

3.5.3 Charge Collection Efficiency

For all measured diamonds, the mean charge, charge collection efficiency, and charge collection distance are given in [Table 3.1](#). These values are calculated from the charge spectra. The given uncertainty represents the standard error of mean for each measurement and the calibration uncertainty, but does not include other systematic uncertainties. Latter are expected to be large, possible causes are outlined in the next section.

Table 3.1: Charge collection efficiency and distance results for all measured diamonds.

Diamond	mean charge / fC	CCE / %	CCD / μm
SO-202-D02	3.24 ± 0.04	76.7 ± 1.0	384 ± 5
SO-202-D03	3.12 ± 0.04	73.7 ± 1.0	369 ± 5
SO-202-D04	3.07 ± 0.04	72.5 ± 1.0	363 ± 5
SO-202-D05	2.44 ± 0.03	57.8 ± 0.8	289 ± 4
SO-202-D06	3.27 ± 0.04	77.3 ± 1.0	387 ± 5
SO-202-D07	2.85 ± 0.04	67.3 ± 0.9	336 ± 4
SO-202-D08	2.68 ± 0.04	63.4 ± 0.8	317 ± 4
SO-202-D09	2.75 ± 0.04	64.9 ± 0.9	325 ± 4
SO-202-D10	2.58 ± 0.03	61.1 ± 0.8	305 ± 4
SO-202-D11	3.31 ± 0.04	78.3 ± 1.0	392 ± 5
SO-202-D12	3.11 ± 0.04	73.5 ± 1.0	367 ± 5
SO-202-D13	3.37 ± 0.04	79.6 ± 1.1	398 ± 5
SO-202-D14	3.05 ± 0.04	72.2 ± 1.0	361 ± 5
SO-202-D15	3.00 ± 0.04	70.9 ± 0.9	354 ± 5
SO-202-D16	2.92 ± 0.04	69.0 ± 0.9	345 ± 5
SO-202-D17	3.16 ± 0.04	74.7 ± 1.0	373 ± 5
SO-202-D18	2.76 ± 0.04	65.4 ± 0.9	327 ± 4
SO-202-D19	2.55 ± 0.03	60.3 ± 0.8	302 ± 4

3.5.4 Sources of systematic uncertainty

It is beyond the scope of this thesis to achieve a full analysis of the setup's systematic uncertainties. Some possible sources should be discussed anyway, in the order of the suspected magnitude: First and foremost, it has been observed that the contact quality between diamond and board has a large influence on the resulting measurements. As the sensors are placed on the board by hand, it is hard to achieve

the exact same conditions for every measurement. Second, the trigger efficiency has not been evaluated and is therefore unknown. A method to work around this would be to use another particle detector (e.g. a scintillator or silicon detector) placed below the diamond as an external trigger. In the case of the DONNA setup with ^{90}Sr , the additional material below the diamond (the PCB) needs to be considered when evaluating the feasibility of this approach. It is expected for the lower-charge end of the spectrum to be cut off, which interestingly is not observed in a significant amount (cf. [Figure 3.22](#)). On the contrary, the higher-charge end of the spectrum seems suppressed, which may be due to signal distortion along the amplifier chain. The used amplifiers are specified to be relatively linear in their frequency response [47], but this has not been validated. Furthermore, the amplifiers are operated below their specified optimal supply current to reduce gain and suppress instabilities. There is no data in the datasheet on the properties of the devices in this state of operation.

3.5.5 Pumping measurement

As discussed before, the detector properties show a time dependence on a scale of hours. In order to study this in detail, a long-term measurement with the ^{90}Sr source at 500 V bias voltage was done with one diamond (*SO-202-D08*). Before the start of the measurement, the diamond is irradiated with ultraviolet light to empty charged particle traps [50]. A 2D histogram of this measurement with charge spectra for many time bins is shown in [Figure 3.25](#). It is visible that the previously-made assumption of a one-hour delay between starting beta irradiation and the measurement may not be enough. Note that the trigger rate varies significantly with time, this may hint at unknown trigger inefficiencies, as the rate of penetrating particles does not vary on this time scale. The mean collected charge trend seems to be roughly consistent with literature [50]. It can be explained by assuming that in the beginning, charge traps are capturing electrons on their way to the electrodes, effectively lowering the mean lifetime τ and therefore reducing the signal. As traps fill up, they cannot capture more electrons and the mean collected charge increases to the maximum.

3.5.6 Comparison to test beam results

To evaluate the measurement principle, it is possible to compare the results of the single-pulse measurements to existing (but unpublished) DC measurements. In [Figure 3.26](#), a scatter plot of all measured diamond sensors is shown with the single-pulse mean pulse charge on the abscissa and the DC current for a source distance

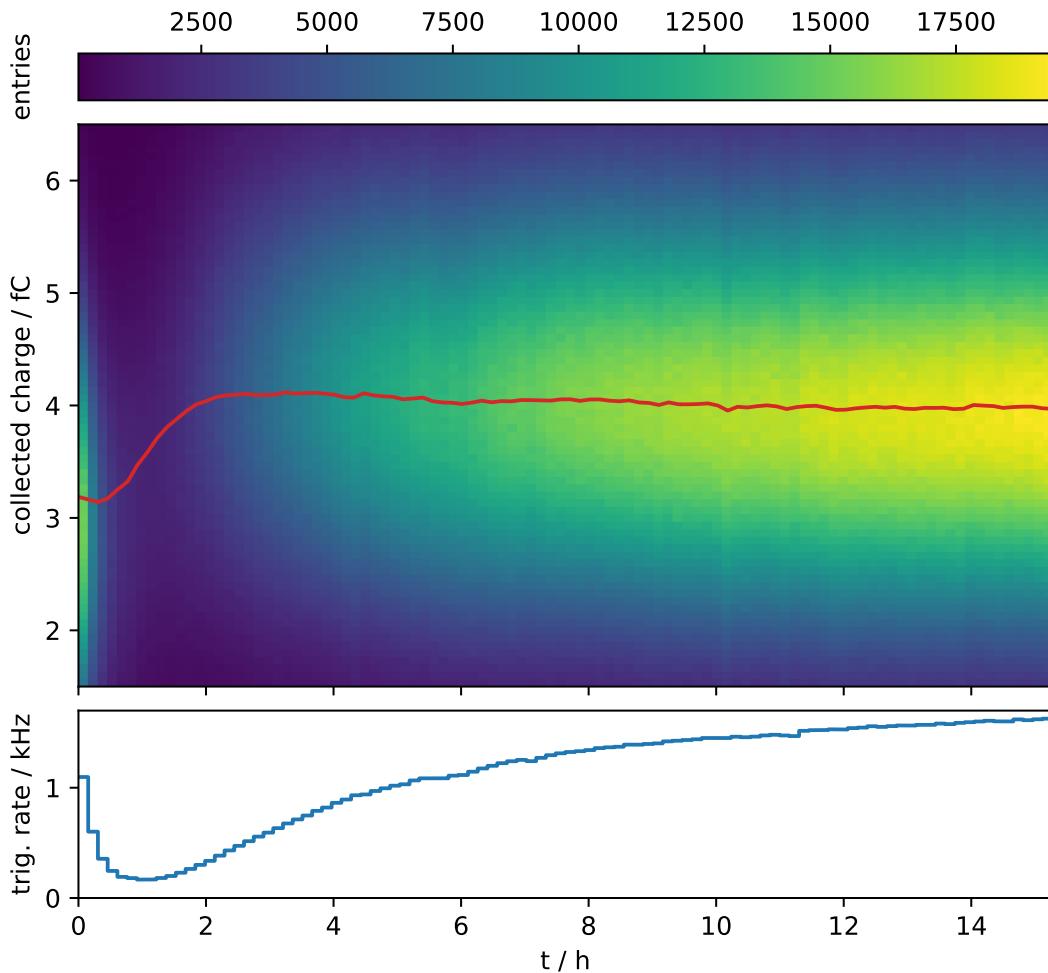


Figure 3.25: Long-term collected charge spectrum evolution of diamond *SO-202-D08*. A total of 66591000 pulses was captured. The red line denotes the average charge for every time bin. The trigger rate shown in the lower part is equivalent to the number of entries in one time bin divided by bin width.

of 10 mm on the ordinate. Ideally, the points would form a line. This is obviously not the case, leading to the conclusion that the systematic uncertainty of at least one of the measurement methods is too large to come to a meaningful result. In [Figure 3.27](#) this analysis is repeated for DC measurements that were taken using a 100 MeV proton testbeam and are unpublished as well. The conclusions are the same as above.

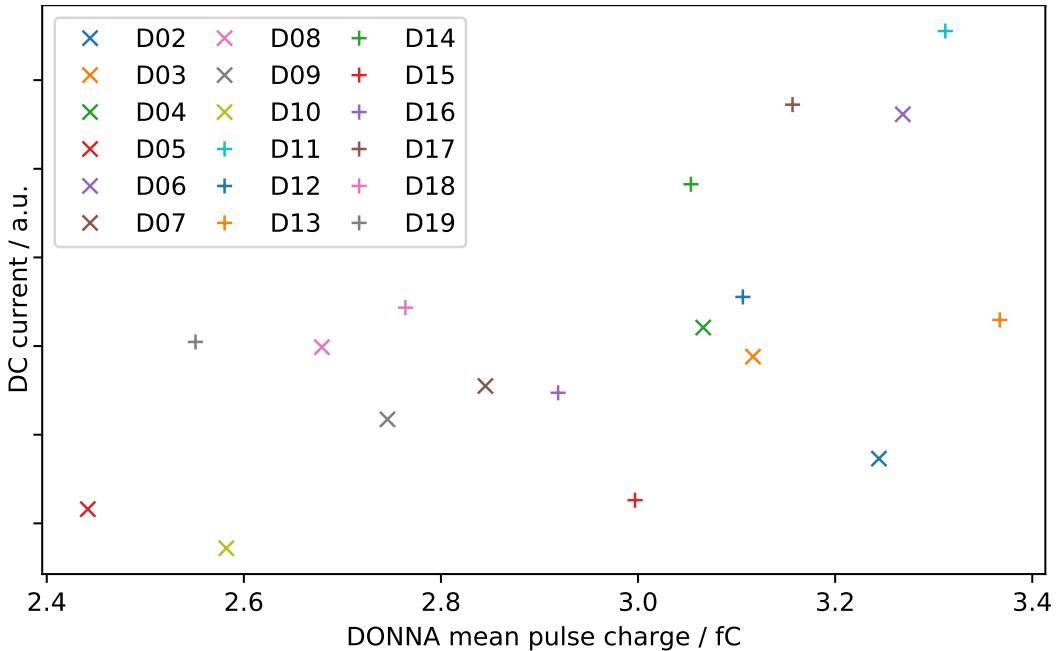


Figure 3.26: Comparison between ^{90}Sr DC and single-pulse measurement for every measured diamond. Error bars are omitted because the statistical uncertainties are very small and the systematic uncertainties are unknown.

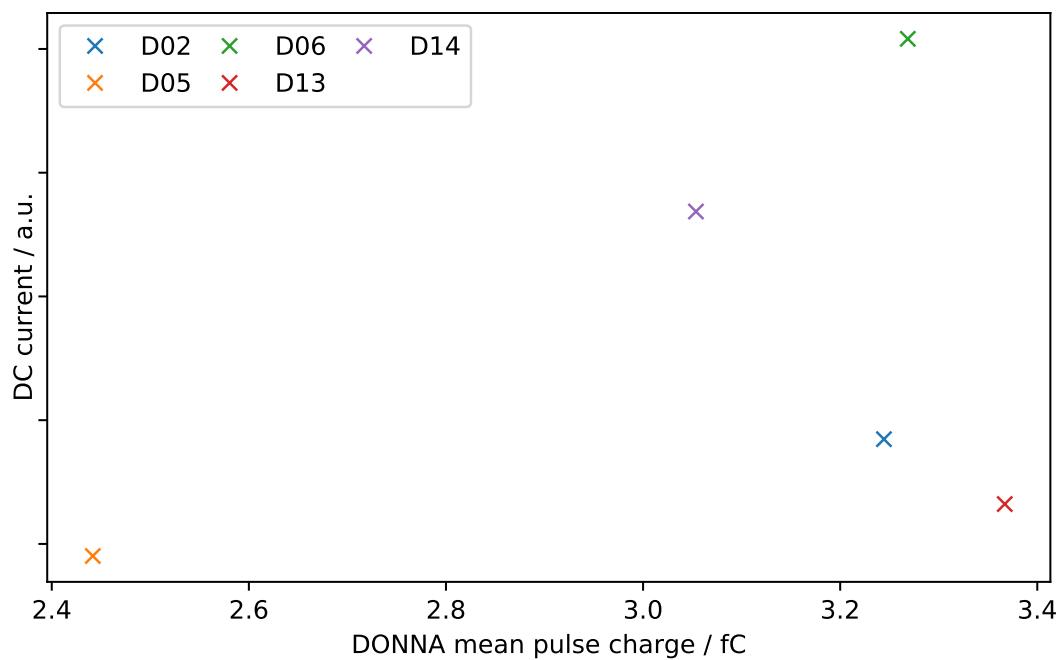


Figure 3.27: Comparison between testbeam DC and ^{90}Sr single-pulse measurement for every measured diamond. Error bars are omitted because the statistical uncertainties are very small and the systematic uncertainties are unknown.

4 Conclusion and outlook

Sensitive components of the LHCb experiment at CERN are placed so close to the damaging beams of the LHC that it needs to be continuously monitored for adverse conditions. To achieve this, a safety system called the Beam Condition Monitor has been keeping the detector safe since the beginning of the first LHC run in 2008. Two rings of eight diamond particle detectors each are placed around the beam pipe and their currents are measured regularly. As the system has been in operation for twelve years, the technologies powering it have progressed. Therefore and because some of the sensors started failing at the end of the last run, for the next LHC run a new readout system and new diamond sensors are planned to be installed. In the course of this thesis, contributions to the readout system were made. Namely, an FPGA firmware block responsible for the communication between two parts of the readout system was implemented using a hardware description language. The implemented block was tested in simulation. As a next step, this firmware block needs verification in the actual hardware setup. When a running system has been established, bit error rate tests need to be conducted to verify the long-term stability of the connection, which is very important for a safety system. Furthermore, a data format for the back channel needs to be specified in addition to the data format specified in this thesis, which is only suited for the other direction of communication.

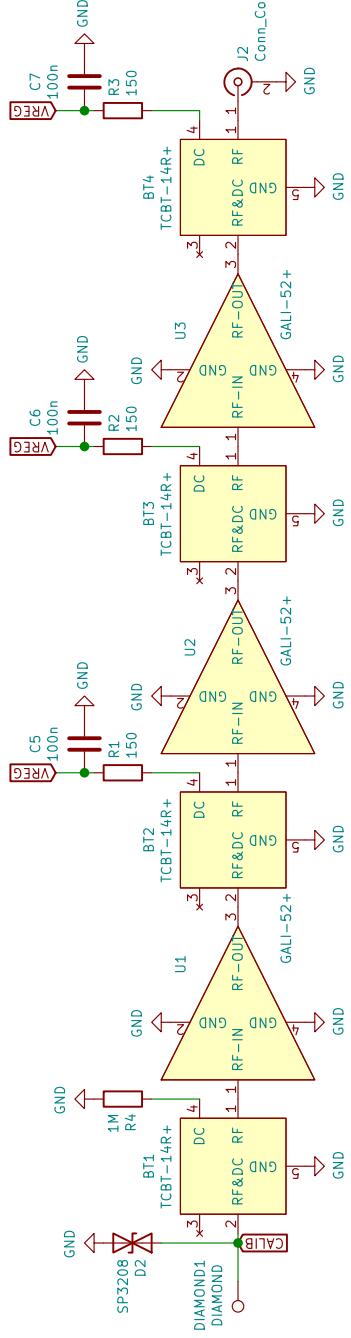
As the other large part of the BCM upgrade project is characterizing new diamond sensors, reliable measurement setups for detector efficiency need to be established. As an alternative to the legacy DC current measurement approach, a single-pulse measurement setup has been realized. An amplifier circuit board was designed, manufactured, and incorporated in a new measurement setup, and commissioned. The setup was characterized, calibrated, and pulse measurements were taken for all available diamond sensors. Charge collection efficiencies and distances were calculated respectively. The time dependence of the single-pulse charge spectrum was investigated for one sensor, showing partly expected results due to pumping of the diamond detector, but revealed deficiencies in the triggering scheme as the trigger rate varied wildly throughout the measurement. Finally, the concluded charge collection was compared to DC measurement data, yielding results that show room for improvement regarding the systematic uncertainties. Looking forward, other approaches of contacting the diamonds should be evaluated as the setup using only

a pad and a spring did not prove to deliver well-reproducible results. Furthermore, a better amplifier signal-to-noise ratio could improve the trigger efficiency, reducing systematic uncertainties stemming from this. This could be achieved by simulation-aided RF design or by using a commercially available amplifier solution. Ultimately it would be beneficial to determine all contributions of systematic uncertainty to the measurement. While being a complex endeavor, it would allow for having larger confidence in the sensor efficiency results, especially in view of safety-critical or even medical applications.

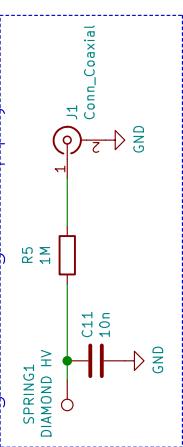
A Appendix

A.1 DONNA Schematics

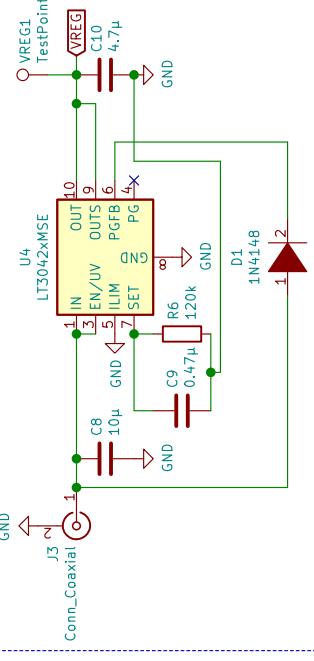
Amplification



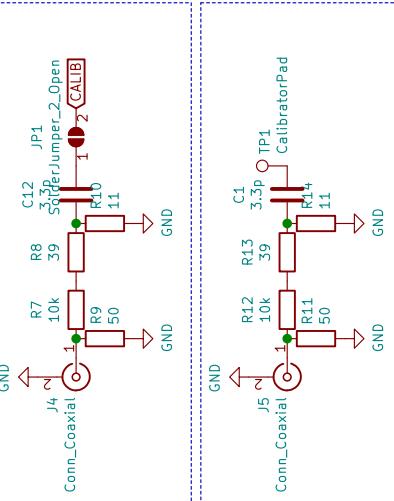
High Voltage Supply



Amplifier Voltage Regulator



Calibration Circuits



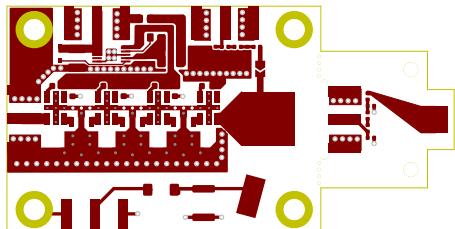
Lars Funke
Technische Universität Dortmund, Lehrstuhl für Experimentelle Physik 5
Sheet: /
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Title: **DONNA Diamond Amplifier Board**
Size: A4
Date: 2020-05-12
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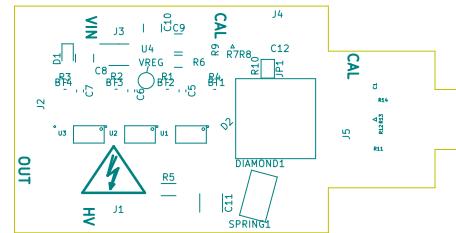
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A.2 DONNA PCB Layers

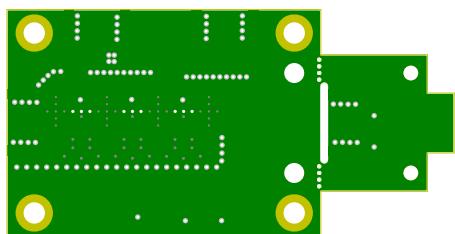
Front Copper



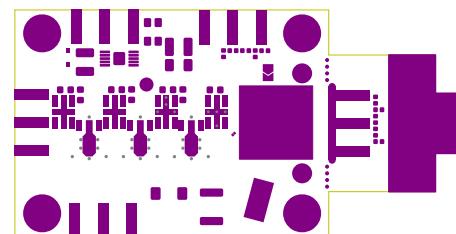
Front Silkscreen



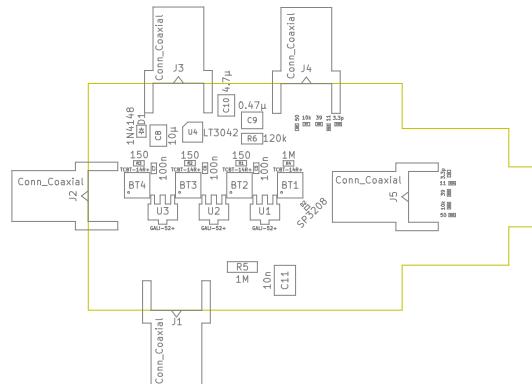
Back Copper



Front Solder Mask



Assembly Diagram



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