IIITB COMET FOUNDATION

BATCH-COMETFWC003

GATE 2018, EE, Q14

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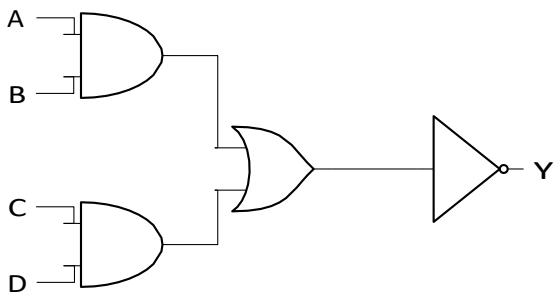
14 Question

Q.14 In the logic circuit shown in the figure, Y is given by:



Options:

(A) $Y = ABCD$

(B) $Y = (A + B)(C + D)$

(C) $Y = A + B + C + D$

(D) $Y = AB + CD$

1 Solution

1.1 Boolean Expression

The given circuit consists of:

- Two AND gates producing AB and CD.
- An OR gate combining them: $AB + CD$.
- A NOT gate complementing the result.

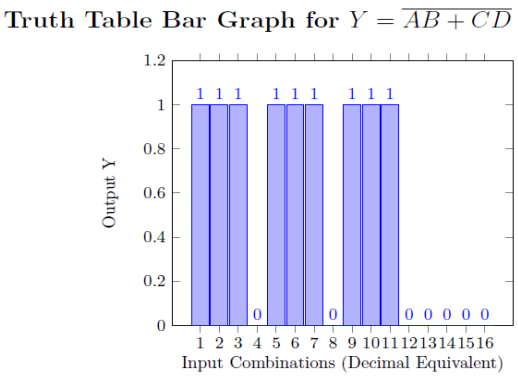
Thus, the Boolean expression for Y is:

$$Y = \overline{AB + CD}$$

1.2 Truth Table

A	B	C	D	AB	CD	AB+CD	$Y = \overline{AB + CD}$
0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	1
0	0	1	0	0	0	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	0	1
0	1	1	0	0	0	0	1
0	1	1	1	0	1	1	0
1	0	0	0	0	0	0	1
1	0	0	1	0	0	0	1
1	0	1	0	0	0	0	1
1	0	1	1	0	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	0
1	1	1	0	1	0	1	0
1	1	1	1	1	1	1	0

1.3 Graph Representation



2 Final Answer

From the analysis, the correct answer is:

$$Y = \overline{AB + CD}$$

None of the provided options exactly match this form, but if the

negation were removed, option (D) $AB + CD$ **would be the closest incorrect match.**