SVADS Assignment 3
ASIC Flow with Synopsis Tools

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March 2025

1. DC synthesis of RTL

Modified the following sections in the run_dc.tcl code: working directory and top module name.

```
# set the working directory path
set working_dir /evprj156/projects/nilakna/assignment

# check if the provided working_dir path exists
if {![file exists $working_dir]} {
    puts "Error: $working_dir does not exists"
    exit 1
}

#/* Top-level Module  - MODIFY as required           */
# set top_module full_adder; # set the variable top_module to hold the string "full_adder"
set top_module mvm_uart_system;
```

```
# MODIFY as required - aedc4 might need to change
set PDKDIR $working_dir/../../tsmc_32nm/SAED32_EDK
set SAED32_EDK $working_dir/../../tsmc_32nm/SAED32_EDK/lib
```

Since there were many SLACK violations, set my_period to 14 in run_dc.tcl.

```
# Default SDC Constraints (can be an sdc file)
set my_period 14
```

The final report of the commands ran were clear with no violated constraints and outputs saved to the respective files and folders.

```
Report : constraint
         -all_violators
Design : mvm_uart_system
Version: W-2024.09-SP2
Date   : Sun Mar 30 00:34:57 2025
****************************************

This design has no violated constraints.

Current design is 'mvm_uart_system'.
Writing verilog file '/evprj156/projects/nilakna/assignment/output/mvm_uart_system.out.v'.
Writing ddc file '/evprj156/projects/nilakna/assignment/output/mvm_uart_system.out.ddc'.
Current design is 'mvm_uart_system'.
```

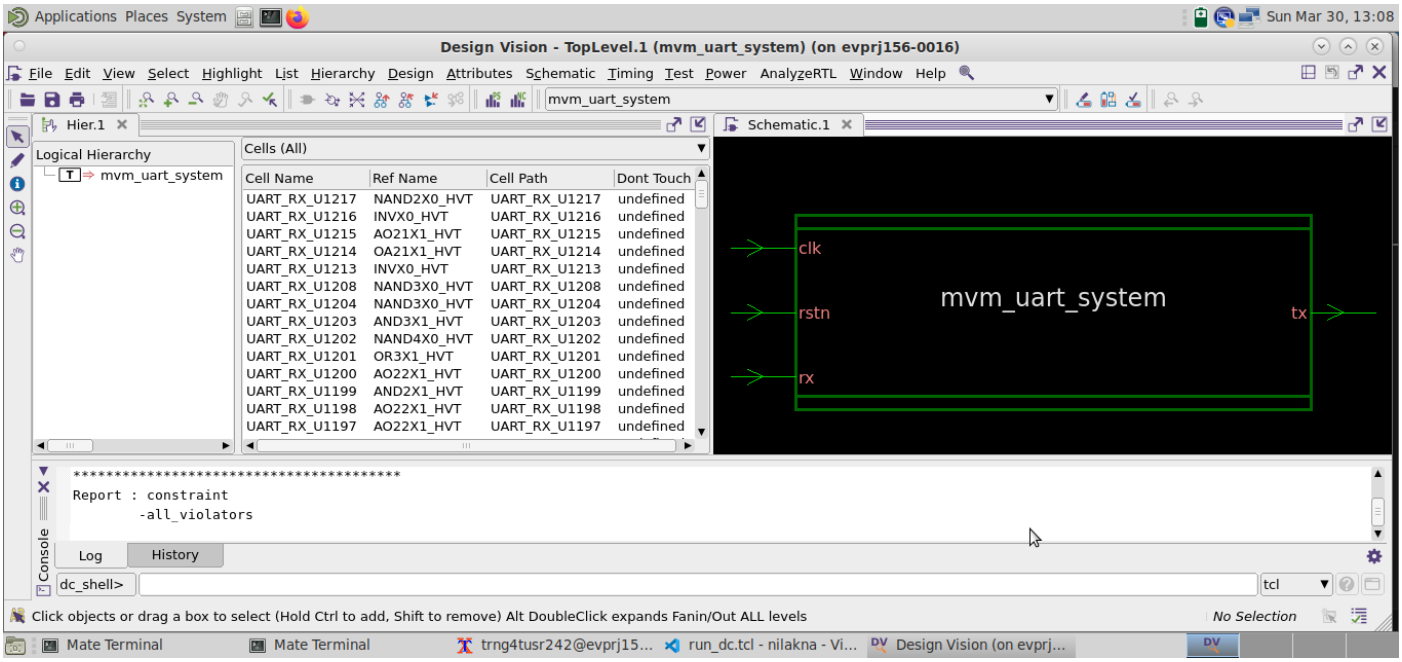
Compiled netlist is saved in the out.v file:

assignment > output > mvm_uart_system.out.v

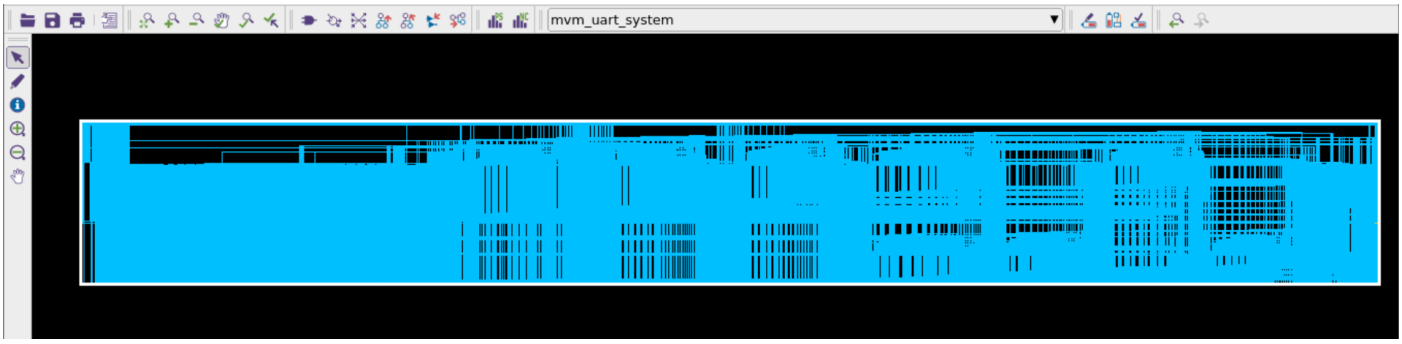
```
1  ////////////////////////////////////////////////////////////
2  // Created by: Synopsys DC Expert(TM) in wire load mode
3  // Version   : W-2024.09-SP2
4  // Date      : Sun Mar 30 01:07:08 2025
5  ////////////////////////////////////////////////////////////
6
7
8  module mvm_uart_system ( clk, rstn, rx, tx );
9    input clk, rstn, rx;
10   output tx;
11   wire   s_valid, s_data_kx_0_, s_ready, m_ready, m_valid, UART_RX_n1848,
12          UART_RX_n1847, UART_RX_n1846, UART_RX_n1845, UART_RX_n1844,
13          UART_RX_n1843, UART_RX_n1842, UART_RX_n1841, UART_RX_n1840,
14          UART_RX_n1839, UART_RX_n1838, UART_RX_n1837, UART_RX_n1836,
15          UART_RX_n1835, UART_RX_n1834, UART_RX_n1833, UART_RX_n1832,
16          UART_RX_n1831, UART_RX_n1830, UART_RX_n1829, UART_RX_n1828,
17          UART_RX_n1827, UART_RX_n1826, UART_RX_n1825, UART_RX_n1824,
18          UART_RX_n1823, UART_RX_n1822, UART_RX_n1821, UART_RX_n1820,
19          UART_RX_n1819, UART_RX_n1818, UART_RX_n1817, UART_RX_n1816,
20          UART_RX_n1815, UART_RX_n1814, UART_RX_n1813, UART_RX_n1812,
21          UART_RX_n1811, UART_RX_n1810, UART_RX_n1809, UART_RX_n1808,
22          UART_RX_n1807, UART_RX_n1806, UART_RX_n1805, UART_RX_n1804,
23          UART_RX_n1803, UART_RX_n1802, UART_RX_n1801, UART_RX_n1800,
24          UART_RX_n1799, UART_RX_n1798, UART_RX_n1797, UART_RX_n1796,
```

Design vision of DC – output of dc_shell GUI.

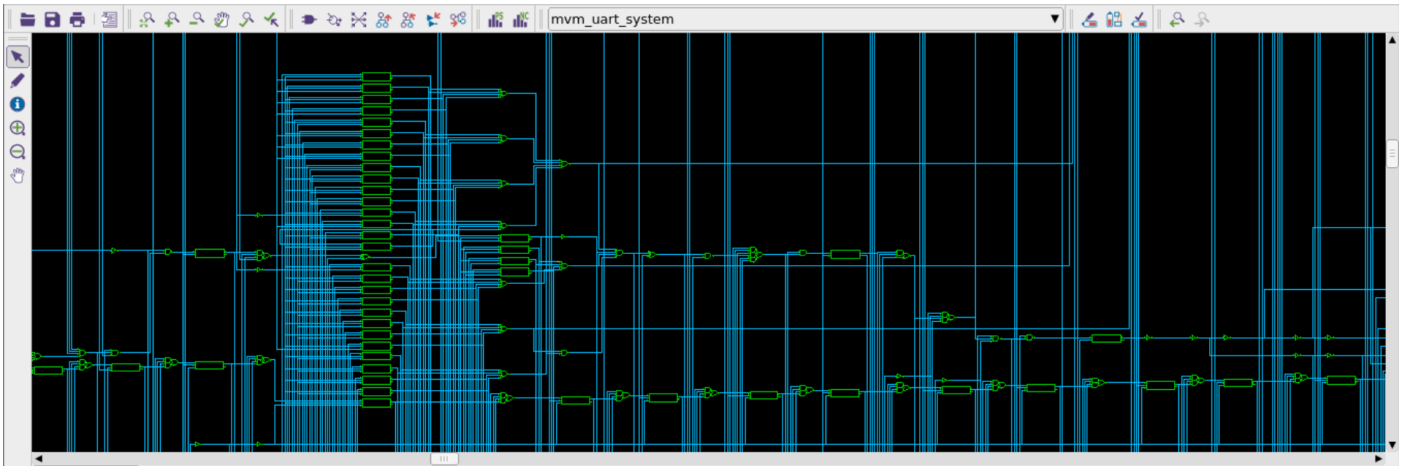
Created the schematic of the compiled netlist. Then selected mvm_uart_system in Logical hierarchy and Cells (All) in the dropdown to view details. Schematic was generated from the GUI and it is as follows.



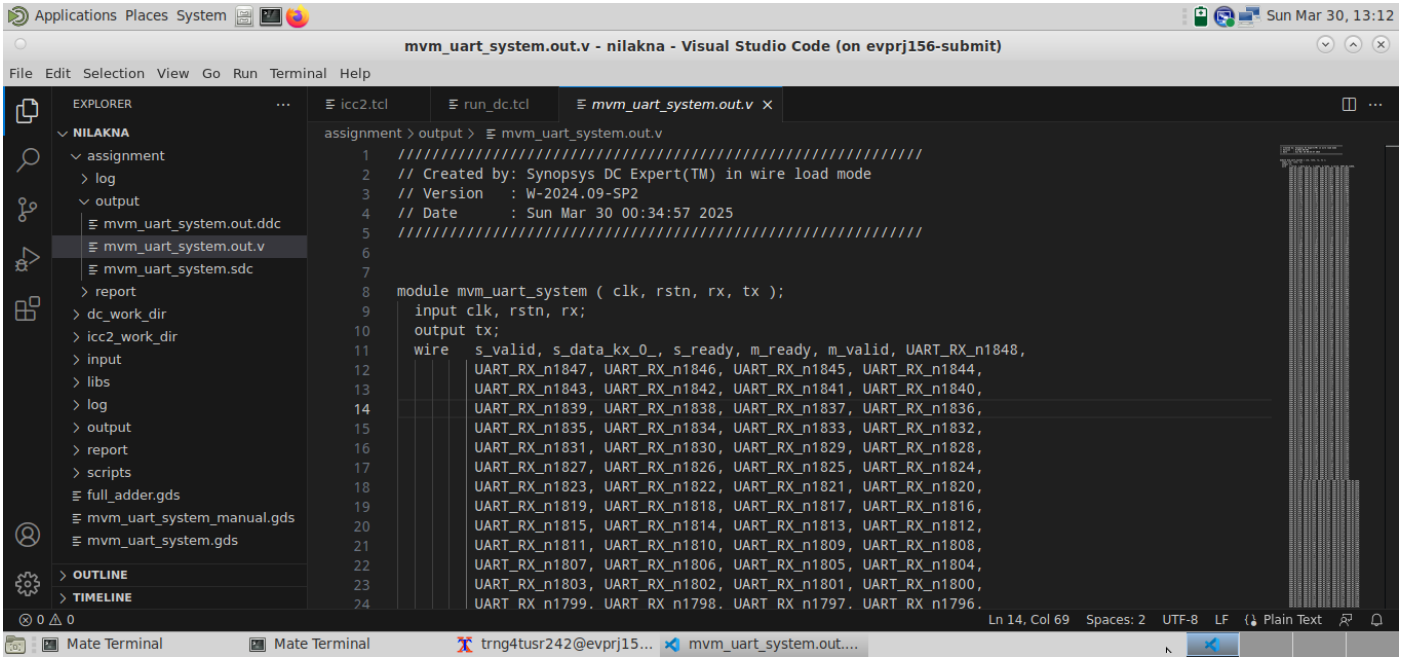
Double clicked the schematic top module to view the blocks inside.



A closer look of part of the design:



The generated netlist is saved in the mvm_uart_system.out.v file in the output folder.



2. Reports of DC synthesis

These reports are generated for the dc synthesis of the mvm_uart_system module for the values of R=8, C=8, W_X=8, W_K=8.

2.1. Ports

Ports information is recorded in mvm_uart_system_port.rpt file inside reports folder.

```
****************************************
Report : port
Design : mvm_uart_system
Version: W-2024.09-SP2
Date   : Sun Mar 30 00:34:58 2025
****************************************


                                  Pin      Wire     Max     Max     Connection
Port           Dir     Load     Load     Trans   Cap     Class       Attrs
--------------------------------------------------------------------------------
clk            in      0.0000   0.0000   --      --      --
rstn           in      0.0000   0.0000   --      --      --
rx             in      0.0000   0.0000   --      --      --
tx             out     0.0000   0.0000   --      --      --

1
```

2.2. Area

Area information is recorded in mvm_uart_system_area.rpt and mvm_uart_system_area_reference.rpt file inside reports folder.

```
*************************************
Report : area
Design : mvm_uart_system
Version: W-2024.09-SP2
Date   : Sun Mar 30 00:34:58 2025
*************************************

Library(s) Used:

    saed32hvt_ss0p7v125c (File: /evprj156/projects/tsmc_32nm/SAED32_EDK/lib/stdcell_hvt/db_nldm/saed32hvt_ss0p7v125c.db)

Number of ports:                          4
Number of nets:                       22499
Number of cells:                      17955
Number of combinational cells:        14227
Number of sequential cells:            3728
Number of macros/black boxes:             0
Number of buf/inv:                     1200
Number of references:                    39

Combinational area:              46278.351464
Buf/Inv area:                     5528.394523
Noncombinational area:           25197.870017
Macro/Black Box area:                0.000000
Net Interconnect area:           27935.836767

Total cell area:                 71476.221481
Total area:                      99412.058248
1
```

Total cell area is 71476.221481 and the Total area is 99412.058248

2.3. Power

Power information is recorded in mvm_uart_system_power.rpt file inside reports folder.

```
****************************************
Report : power
        -analysis_effort low
Design : mvm_uart_system
Version: W-2024.09-SP2
Date   : Sun Mar 30 00:35:00 2025
****************************************


Library(s) Used:

    saed32hvt_ss0p7v125c (File: /evprj156/projects/tsmc_32nm/SAED32_EDK/lib/stdcell_hvt/db_nldm/saed32hvt_ss0p7v125c.db)


Operating Conditions: ss0p7v125c   Library: saed32hvt_ss0p7v125c
Wire Load Model Mode: enclosed

Design        Wire Load Model            Library
------------------------------------------------
mvm_uart_system        140000            saed32hvt_ss0p7v125c


Global Operating Voltage = 0.7
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW
```

```
Attributes
----------
i - Including register clock pin internal power


  Cell Internal Power  = 827.9991 uW   (98%)
  Net Switching Power  =  13.9623 uW    (2%)
                         ---------
Total Dynamic Power    = 841.9614 uW  (100%)

Cell Leakage Power     = 434.2425 uW


                  Internal         Switching           Leakage            Total
Power Group       Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad              0.0000           0.0000              0.0000             0.0000  (   0.00%)
memory              0.0000           0.0000              0.0000             0.0000  (   0.00%)
black_box           0.0000           0.0000              0.0000             0.0000  (   0.00%)
clock_network     820.0468           0.0000              0.0000           820.0468  (  64.26%)  i
register            0.1713       4.1756e-02          1.3281e+08           133.0214  (  10.42%)
sequential          0.0000           0.0000              0.0000             0.0000  (   0.00%)
combinational       7.7496          13.9205          3.0144e+08           323.1066  (  25.32%)
--------------------------------------------------------------------------------------------------
Total             827.9677 uW        13.9622 uW       4.3424e+08 pW      1.2762e+03 uW
1
```

Total power consumption is 1276.2 uW.

2.4. Timing

Timing information is recorded in mvm_uart_system_timing.rpt file inside reports folder.

```
****************************************
Report : timing
        -path full
        -delay max
        -nets
        -max_paths 100
        -transition_time
        -capacitance
Design : mvm_uart_system
Version: W-2024.09-SP2
Date   : Sun Mar 30 00:35:00 2025
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

 Operating Conditions: ss0p7v125c   Library: saed32hvt_ss0p7v125c
Wire Load Model Mode: enclosed

  Startpoint: AXIS_MVM_MATVEC_tree_reg_7__2__1__0_
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: AXIS_MVM_MATVEC_tree_reg_7__3__0__18_
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  mvm_uart_system    140000                saed32hvt_ss0p7v125c
```

Point	Fanout	Cap	Trans	Incr	Path
clock clk (rise edge)				0.000	0.000
clock network delay (ideal)				0.000	0.000
AXIS_MVM_MATVEC_tree_reg_7__2__1__0_/CLK (DFFX1_HVT)			0.000	0.000 #	0.000 r
AXIS_MVM_MATVEC_tree_reg_7__2__1__0_/Q (DFFX1_HVT)			0.142	0.652	0.652 r
AXIS_MVM_MATVEC_tree_7__2__1__0_ (net)	3	2.306		0.000	0.652 r
U1220/Y (AND2X1_HVT)			0.117	0.314	0.967 r
AXIS_MVM_MATVEC_add_31_S2_G3_G8_carry[1] (net)	1	1.339		0.000	0.967 r
AXIS_MVM_MATVEC_add_31_S2_G3_G8_U1_1/CO (FADDX1_HVT)			0.220	0.460	1.427 r
AXIS_MVM_MATVEC_add_31_S2_G3_G8_carry[2] (net)	1	1.339		0.000	1.427 r
AXIS_MVM_MATVEC_add_31_S2_G3_G8_U1_2/CO (FADDX1_HVT)			0.220	0.512	1.938 r
AXIS_MVM_MATVEC_add_31_S2_G3_G8_carry[3] (net)	1	1.339		0.000	1.938 r
AXIS_MVM_MATVEC_add_31_S2_G3_G8_U1_3/CO (FADDX1_HVT)			0.220	0.512	2.451 r
AXIS_MVM_MATVEC_add_31_S2_G3_G8_carry[4] (net)	1	1.339		0.000	2.451 r
AXIS_MVM_MATVEC_add_31_S2_G3_G8_U1_4/CO (FADDX1_HVT)			0.220	0.512	2.963 r
AXIS_MVM_MATVEC_add_31_S2_G3_G8_carry[5] (net)	1	1.339		0.000	2.963 r
AXIS_MVM_MATVEC_add_31_S2_G3_G8_U1_5/CO (FADDX1_HVT)			0.220	0.512	3.475 r
AXIS_MVM_MATVEC_add_31_S2_G3_G8_carry[6] (net)	1	1.339		0.000	3.475 r
AXIS_MVM_MATVEC_add_31_S2_G3_G8_U1_6/CO (FADDX1_HVT)			0.220	0.512	3.987 r
AXIS_MVM_MATVEC_add_31_S2_G3_G8_carry[7] (net)	1	1.339		0.000	3.987 r
AXIS_MVM_MATVEC_add_31_S2_G3_G8_U1_7/CO (FADDX1_HVT)			0.220	0.512	4.499 r
AXIS_MVM_MATVEC_add_31_S2_G3_G8_carry[8] (net)	1	1.339		0.000	4.499 r
AXIS_MVM_MATVEC_add_31_S2_G3_G8_U1_8/CO (FADDX1_HVT)			0.220	0.512	5.011 r
AXIS_MVM_MATVEC_add_31_S2_G3_G8_carry[9] (net)	1	1.339		0.000	5.011 r
AXIS_MVM_MATVEC_add_31_S2_G3_G8_U1_9/CO (FADDX1_HVT)			0.220	0.512	5.523 r
AXIS_MVM_MATVEC_add_31_S2_G3_G8_carry[10] (net)	1	1.339		0.000	5.523 r
AXIS_MVM_MATVEC_add_31_S2_G3_G8_U1_10/CO (FADDX1_HVT)			0.220	0.512	6.035 r
AXIS_MVM_MATVEC_add_31_S2_G3_G8_carry[11] (net)	1	1.339		0.000	6.035 r
AXIS_MVM_MATVEC_add_31_S2_G3_G8_U1_11/CO (FADDX1_HVT)			0.220	0.512	6.547 r
AXIS_MVM_MATVEC_add_31_S2_G3_G8_carry[12] (net)	1	1.339		0.000	6.547 r

```
AXIS_MVM_MATVEC_add_31_S2_G3_G8_U1_12/CO (FADDX1_HVT)              0.220     0.512      7.059 r
AXIS_MVM_MATVEC_add_31_S2_G3_G8_carry[13] (net)     1     1.339              0.000      7.059 r
AXIS_MVM_MATVEC_add_31_S2_G3_G8_U1_13/CO (FADDX1_HVT)              0.220     0.512      7.571 r
AXIS_MVM_MATVEC_add_31_S2_G3_G8_carry[14] (net)     1     1.339              0.000      7.571 r
AXIS_MVM_MATVEC_add_31_S2_G3_G8_U1_14/CO (FADDX1_HVT)              0.220     0.512      8.084 r
AXIS_MVM_MATVEC_add_31_S2_G3_G8_carry[15] (net)     1     1.339              0.000      8.084 r
AXIS_MVM_MATVEC_add_31_S2_G3_G8_U1_15/CO (FADDX1_HVT)              0.220     0.512      8.596 r
AXIS_MVM_MATVEC_add_31_S2_G3_G8_carry[16] (net)     1     1.339              0.000      8.596 r
AXIS_MVM_MATVEC_add_31_S2_G3_G8_U1_16/CO (FADDX1_HVT)              0.220     0.512      9.108 r
AXIS_MVM_MATVEC_add_31_S2_G3_G8_carry[17] (net)     1     1.339              0.000      9.108 r
AXIS_MVM_MATVEC_add_31_S2_G3_G8_U1_17/CO (FADDX1_HVT)              0.220     0.512      9.620 r
AXIS_MVM_MATVEC_add_31_S2_G3_G8_carry[18] (net)     1     1.339              0.000      9.620 r
AXIS_MVM_MATVEC_add_31_S2_G3_G8_U1_18/S (FADDX1_HVT)               0.148     0.743     10.363 f
AXIS_MVM_MATVEC_N2087 (net)                         1     0.501              0.000     10.363 f
AXIS_MVM_MATVEC_U20/Y (AO22X1_HVT)                                 0.097     0.259     10.622 f
AXIS_MVM_MATVEC_n84 (net)                           1     0.508              0.000     10.622 f
AXIS_MVM_MATVEC_tree_reg_7__3__0__18_/D (DFFX1_HVT)                0.097     0.000     10.622 f
data arrival time                                                                      10.622

clock clk (rise edge)                                                 14.000     14.000
clock network delay (ideal)                                            0.000     14.000
AXIS_MVM_MATVEC_tree_reg_7__3__0__18_/CLK (DFFX1_HVT)                  0.000     14.000 r
library setup time                                                    -0.294     13.706
data required time                                                               13.706
-----------------------------------------------------------------------------------------
data required time                                                               13.706
data arrival time                                                               -10.622
-----------------------------------------------------------------------------------------
slack (MET)                                                                      3.084
```

Timing report has about 7200 lines. Hence, the screenshots of only first part are added to compact this report.

2.5. No of Cells

This information is recorded in mvm_uart_system_cell.rpt file inside reports folder.

Total no of cells is 17955 cells.

```
****************************************
Report : cell
Design : mvm_uart_system
Version: W-2024.09-SP2
Date   : Sun Mar 30 00:34:58 2025
****************************************

Attributes:
    b - black box (unknown)
    d - dont_touch
    h - hierarchical
   mo - map_only
    n - noncombinational
    r - removable
    u - contains unmapped logic

Cell                    Reference       Library            Area  Attributes
-------------------------------------------------------------------------------
AXIS_MVM_MATVEC_U2      AO22X1_HVT      saed32hvt_ss0p7v125c
                                                       2.541440
AXIS_MVM_MATVEC_U3      AO22X1_HVT      saed32hvt_ss0p7v125c
                                                       2.541440
AXIS_MVM_MATVEC_U4      AO22X1_HVT      saed32hvt_ss0p7v125c
                                                       2.541440
AXIS_MVM_MATVEC_U5      AO22X1_HVT      saed32hvt_ss0p7v125c
                                                       2.541440
AXIS_MVM_MATVEC_U6      AO22X1_HVT      saed32hvt_ss0p7v125c
                                                       2.541440
AXIS_MVM_MATVEC_U7      AO22X1_HVT      saed32hvt_ss0p7v125c
```

```
UART_TX_state_reg_30_     DFFARX1_HVT     saed32hvt_ss0p7v125c
                                                       7.116032  n
UART_TX_state_reg_31_     DFFARX1_HVT     saed32hvt_ss0p7v125c
                                                       7.116032  n
-------------------------------------------------------------------------------
Total 17955 cells                                   71476.221481
1
```

Cell report has 44000 lines and only the first and last parts are added as screenshots.

3. Comparison of DC synthesis for different combinations of matrix vector sizes and word lengths.

Test No	R	C	W_X	W_K	Total cell area	Total area	Internal power uW	Switching power uW	Leakage power uW	Total Power uW
1	8	8	8	8	71476.221481	99412.058248	827.9677 uW	13.9622 uW	4.3424e+08 pW	1.2762e+03 uW
2	4	4	8	8	21136.648381	27138.368484	265.0083 uW	5.8870 uW	1.4776e+08 pW	418.6560 uW
3	8	8	4	4	35525.011185	48000.615748	531.0989 uW	8.9981 uW	2.3467e+08 pW	774.7648 uW
4	4	4	4	4	11953.154912	14778.077071	185.4664 uW	4.6675 uW	9.7290e+07 pW	287.4242 uW

1- Original
2- Quarter the matrix size
3- Half the word size
4- Quarter the matrix size and half the word size

There is a slight variation in the current DC reports for the first combination since it has to be repeated after running the other combinations and repeating it again may have resulted in slightly different values. IC compiler report was generated on the current DC report which is from the second iteration.

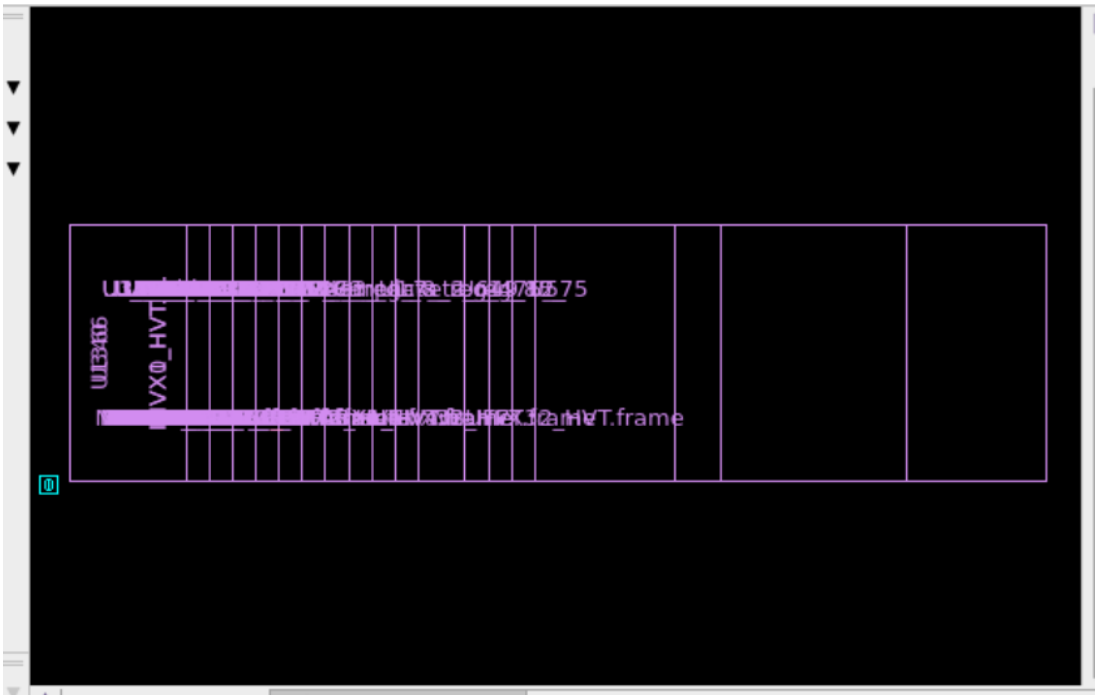
4. IC Compiler II Report

Modified the icc2.tcl file to have the assignment folder as the working directory as below.

```
#  MODIFY as required

# set the working directory path
set working_dir /evprj156/projects/nilakna/assignment

# check if the provided working_dir path exists
if {![file exists $working_dir]} {
   puts "Error: $working_dir does not exists"
   exit 1
}

#/* Top-level Module                                    */
# set top_module full_adder
set top_module mvm_uart_system

#/* Library Name                                        */
set library_name saed32_edk

set PDKDIR $working_dir/../../tsmc_32nm/SAED32_EDK
set SAED32_EDK $working_dir/../../tsmc_32nm/SAED32_EDK/lib
set synopsys /global/etc/modules/files/eda/syn/2024.09-SP2
```

Ran all commands in the icc2.tcl file

After creating the block and linking:

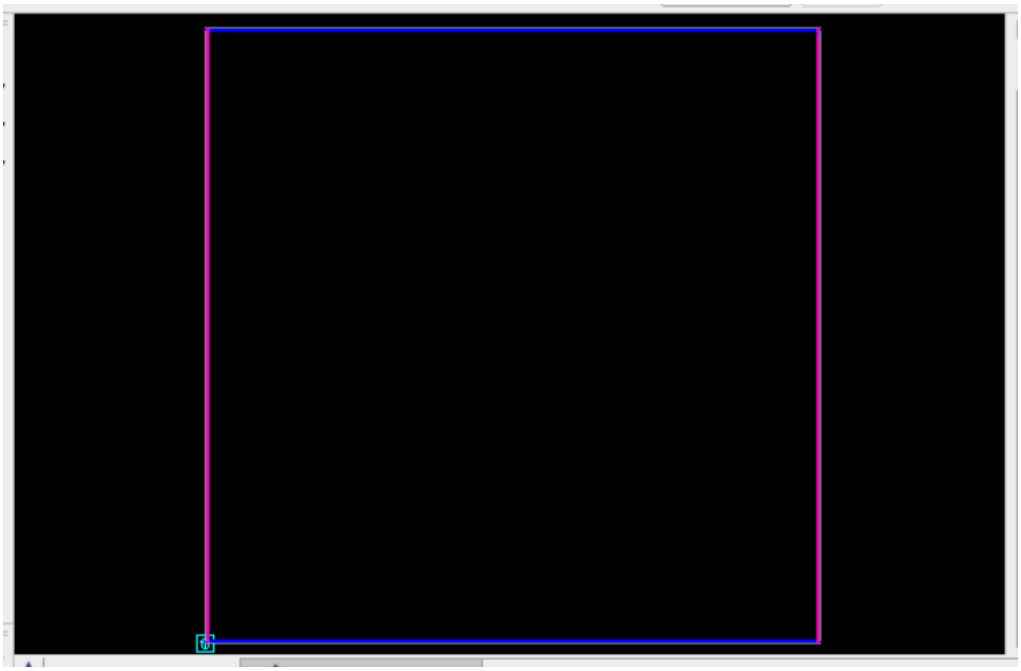


```
Design 'mvm_uart_system' was successfully linked.
1
icc2_shell> link_block
Warning: Block 'saed32_edk:mvm_uart_system.design' is already linked. (LNK-067)
0
icc2_shell> save_block $library_name:$top_module
Information: Saving block 'saed32_edk:mvm_uart_system.design'
1
icc2_shell> save_lib -all
Saving all libraries...
1
```

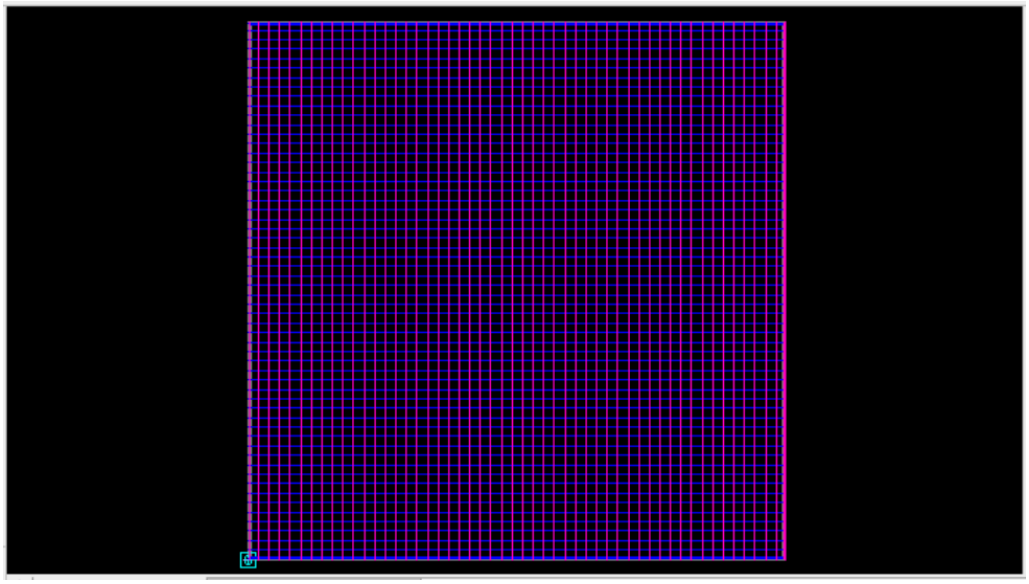
Floor plan initialization:

```
icc2_shell> connect_pg_net -automatic
Information: Connecting to PG and tie pins in automatic mode. (MV-396)
****************************************
Report : Power/Ground Connection Summary
Design : mvm_uart_system
Version: W-2024.09-SP2
Date   : Sun Mar 30 01:23:31 2025
****************************************
P/G net name                  P/G pin count(previous/current)
--------------------------------------------------------------------------------
Power net VDD                 0/17957
Ground net VSS                0/17957
--------------------------------------------------------------------------------
Information: connections of 35914 power/ground pin(s) are created or changed. (MV-382)
```

Connecting the power rings:



After adding mesh pattern and cell pattern:

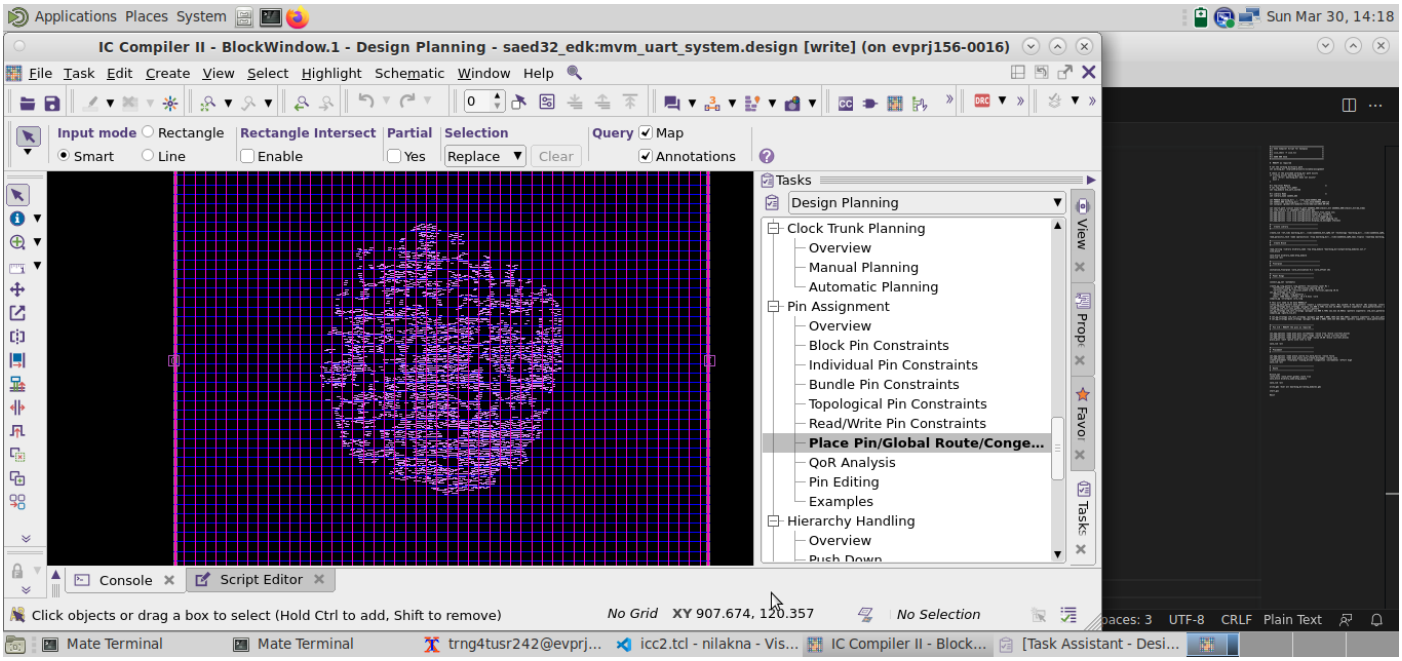


Place pins:

```
icc2_shell> place_pins -self -ports {clk rstn rx tx}
Information: Starting 'place_pins' (FLW-8000)
Information: Time: 2025-03-30 01:45:45 / Session:  00:32:02 / Command:  00:00:00 / CPU:  00:00:00 / Memory: 638 MB (FLW-8100)
Load DB...
CPU Time for load db: 00:00:00.01u 00:00:00.00s 00:00:00.01e:

Printing app options for 'plan.pins*':
plan.pins.incremental                 :  true
plan.pins.pin_range                   :  10
plan.pins.layer_range                 :  5

Min routing layer: M1
Max routing layer: MRDL


CPU Time for Top Level Pre-Route Processing: 00:00:00.02u 00:00:00.00s 00:00:00.02e:
CPU Time for Leaf Level Pre-Route Processing: 00:00:00.00u 00:00:00.00s 00:00:00.00e:
Number of block ports: 4
Number of block pin locations assigned from router: 0
CPU Time for Pin Preparation: 00:00:00.00u 00:00:00.00s 00:00:00.00e:
Number of PG ports on blocks: 0
Number of pins created: 4
CPU Time for Pin Creation: 00:00:00.00u 00:00:00.00s 00:00:00.00e:
Total Pin Placement CPU Time: 00:00:00.05u 00:00:00.01s 00:00:00.06e:
Information: Ending   'place_pins' (FLW-8001)
Information: Time: 2025-03-30 01:45:45 / Session:  00:32:02 / Command:  00:00:00 / CPU:  00:00:00 / Memory: 641 MB (FLW-8100)
1
icc2_shell> save_lib -all
Saving all libraries...
1
```

After placement:

```
****************************************
Report : report_placement
Design : mvm_uart_system
Version: W-2024.09-SP2
Date   : Sun Mar 30 01:47:20 2025
****************************************
  ==================
  Note: Ignoring violations of fixed cells or between fixed pairs of cells.
        To include violations of / between fixed cells, disable -ignore_fixed.
  ==================

  Wire length report (all)
  ==================
  wire length in design mvm_uart_system: 428756.358 microns.
  wire length in design mvm_uart_system (see through blk pins): 428756.358 microns.
  ------------------
```



After routing: