**SVADS Assignment 3**

**ASIC Flow with Synopsis Tools**

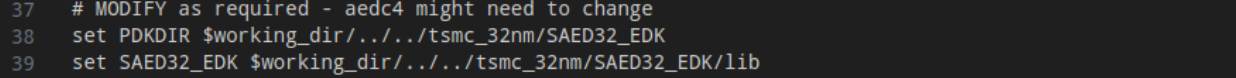
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1. **DC synthesis of RTL**

Modified the following sections in the run\_dc.tcl code: working directory and top module name.

A computer screen shot of white text

Description automatically generated

Since there were many SLACK violations, set my\_period to 14 in run\_dc.tcl.



The final report of the commands ran were clear with no violated constraints and outputs saved to the respective files and folders.

A screenshot of a computer code

Description automatically generated

Compiled netlist is saved in the out.v file:

A screenshot of a computer

Description automatically generated

**Design vision of DC – output of dc\_shell GUI.**

Created the schematic of the compiled netlist. Then selected mvm\_uart\_system in Logical hierarchy and Cells (All) in the dropdown to view details. Schematic was generated from the GUI and it is as follows.

A screenshot of a computer

Description automatically generated

Double clicked the schematic top module to view the blocks inside.

A screenshot of a computer

Description automatically generated

A closer look of part of the design:

A screenshot of a computer

Description automatically generated

The generated netlist is saved in the mvm\_uart\_system.out.v file in the output folder.

A screenshot of a computer

Description automatically generated

1. **Reports of DC synthesis**

These reports are generated for the dc synthesis of the mvm\_uart\_system module for the values of R=8, C=8, W\_X=8, W\_K=8.

* 1. **Ports**

Ports information is recorded in mvm\_uart\_system\_port.rpt file inside reports folder.

A screenshot of a computer program

Description automatically generated

* 1. **Area**

Area information is recorded in mvm\_uart\_system\_area.rpt and mvm\_uart\_system\_area\_reference.rpt file inside reports folder.

A screenshot of a computer

Description automatically generated

Total cell area is 71476.221481 and the Total area is 99412.058248

* 1. **Power**

Power information is recorded in mvm\_uart\_system\_power.rpt file inside reports folder.

A screenshot of a computer program

Description automatically generated

A screenshot of a computer

Description automatically generated

Total power consumption is 1276.2 uW.

* 1. **Timing**

Timing information is recorded in mvm\_uart\_system\_timing.rpt file inside reports folder.

A screenshot of a computer program

Description automatically generated

A screenshot of a computer screen

Description automatically generated

A screenshot of a computer screen

Description automatically generated

Timing report has about 7200 lines. Hence, the screenshots of only first part are added to compact this report.

* 1. **No of Cells**

This information is recorded in mvm\_uart\_system\_cell.rpt file inside reports folder.

Total no of cells is 17955 cells.

A screenshot of a computer

Description automatically generated A screenshot of a computer

Description automatically generated

Cell report has 44000 lines and only the first and last parts are added as screenshots.

1. **Comparison of DC synthesis for different combinations of matrix vector sizes and word lengths.**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Test No | R | C | W\_X | W\_K | Total cell area | Total area | Internal power uW | Switching power uW | Leakage power uW | Total Power uW |
| 1 | 8 | 8 | 8 | 8 | 71476.221481 | 99412.058248 | 827.9677 uW | 13.9622 uW | 4.3424e+08 pW | 1.2762e+03 uW |
| 2 | 4 | 4 | 8 | 8 | 21136.648381 | 27138.368484 | 265.0083 uW | 5.8870 uW | 1.4776e+08 pW | 418.6560 uW |
| 3 | 8 | 8 | 4 | 4 | 35525.011185 | 48000.615748 | 531.0989 uW | 8.9981 uW | 2.3467e+08 pW | 774.7648 uW |
| 4 | 4 | 4 | 4 | 4 | 11953.154912 | 14778.077071 | 185.4664 uW | 4.6675 uW | 9.7290e+07 pW | 287.4242 uW |

1. Original
2. Quarter the matrix size
3. Half the word size
4. Quarter the matrix size and half the word size

There is a slight variation in the current DC reports for the first combination since it has to be repeated after running the other combinations and repeating it again may have resulted in slightly different values. IC compiler report was generated on the current DC report which is from the second iteration.

1. **IC Compiler II Report**

Modified the icc2.tcl file to have the assignment folder as the working directory as below.

A screenshot of a computer

Description automatically generated

Ran all commands in the icc2.tcl file

After creating the block and linking:

A screenshot of a computer

Description automatically generated

A screenshot of a computer code

Description automatically generated

Floor plan initialization:

A screenshot of a computer

Description automatically generated

A screenshot of a computer

Description automatically generated

Connecting the power rings:

A black screen with a purple and pink border

Description automatically generated

After adding mesh pattern and cell pattern:

A grid with blue and purple squares

Description automatically generated

Place pins:

icc2\_shell> place\_pins -self -ports {clk rstn rx tx}

Information: Starting 'place\_pins' (FLW-8000)

Information: Time: 2025-03-30 01:45:45 / Session: 00:32:02 / Command: 00:00:00 / CPU: 00:00:00 / Memory: 638 MB (FLW-8100)

Load DB...

CPU Time for load db: 00:00:00.01u 00:00:00.00s 00:00:00.01e:

Printing app options for 'plan.pins\*':

plan.pins.incremental : true

plan.pins.pin\_range : 10

plan.pins.layer\_range : 5

Min routing layer: M1

Max routing layer: MRDL

CPU Time for Top Level Pre-Route Processing: 00:00:00.02u 00:00:00.00s 00:00:00.02e:

CPU Time for Leaf Level Pre-Route Processing: 00:00:00.00u 00:00:00.00s 00:00:00.00e:

Number of block ports: 4

Number of block pin locations assigned from router: 0

CPU Time for Pin Preparation: 00:00:00.00u 00:00:00.00s 00:00:00.00e:

Number of PG ports on blocks: 0

Number of pins created: 4

CPU Time for Pin Creation: 00:00:00.00u 00:00:00.00s 00:00:00.00e:

Total Pin Placement CPU Time: 00:00:00.05u 00:00:00.01s 00:00:00.06e:

Information: Ending 'place\_pins' (FLW-8001)

Information: Time: 2025-03-30 01:45:45 / Session: 00:32:02 / Command: 00:00:00 / CPU: 00:00:00 / Memory: 641 MB (FLW-8100)

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icc2\_shell> save\_lib -all

Saving all libraries...

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After placement:

A computer screen shot of a computer

Description automatically generated

A screenshot of a computer

Description automatically generated

After routing:

A screenshot of a computer

Description automatically generated