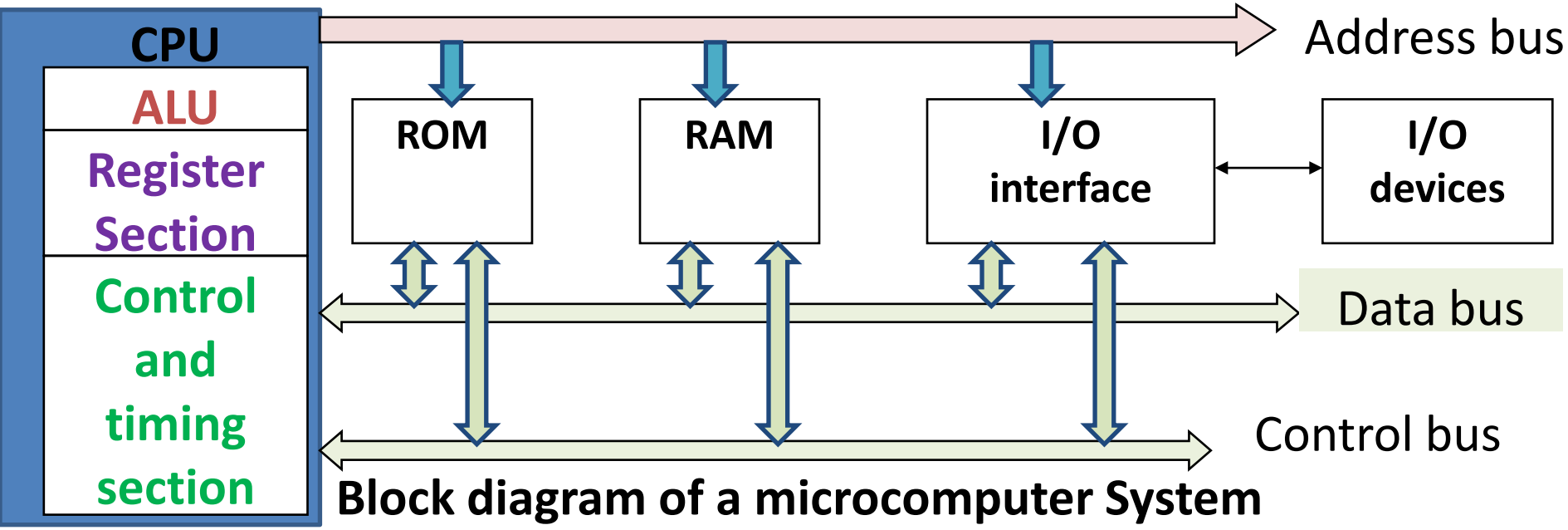
- A processor do some processing on some data or array of data.
- The type of processing is indicated by a program
- Program is a set of (sequence of) instructions, stored in consecutive memory locations), nomally to be executed sequentially.
- Both the program and Data are stored in Memory.
- A number of programs are stored in memory.

- Microprocessor is interfaced with Memory and Input and Output devices through External
- 1) Address bus, (Unidirectional, initiated by Processor only)
- 2) Data bus and (Bidirectional)
- 3) Control bus (RD, WR, and IO/M, Interrupts), (Bidirectional)

------to build up a microcomputer system.

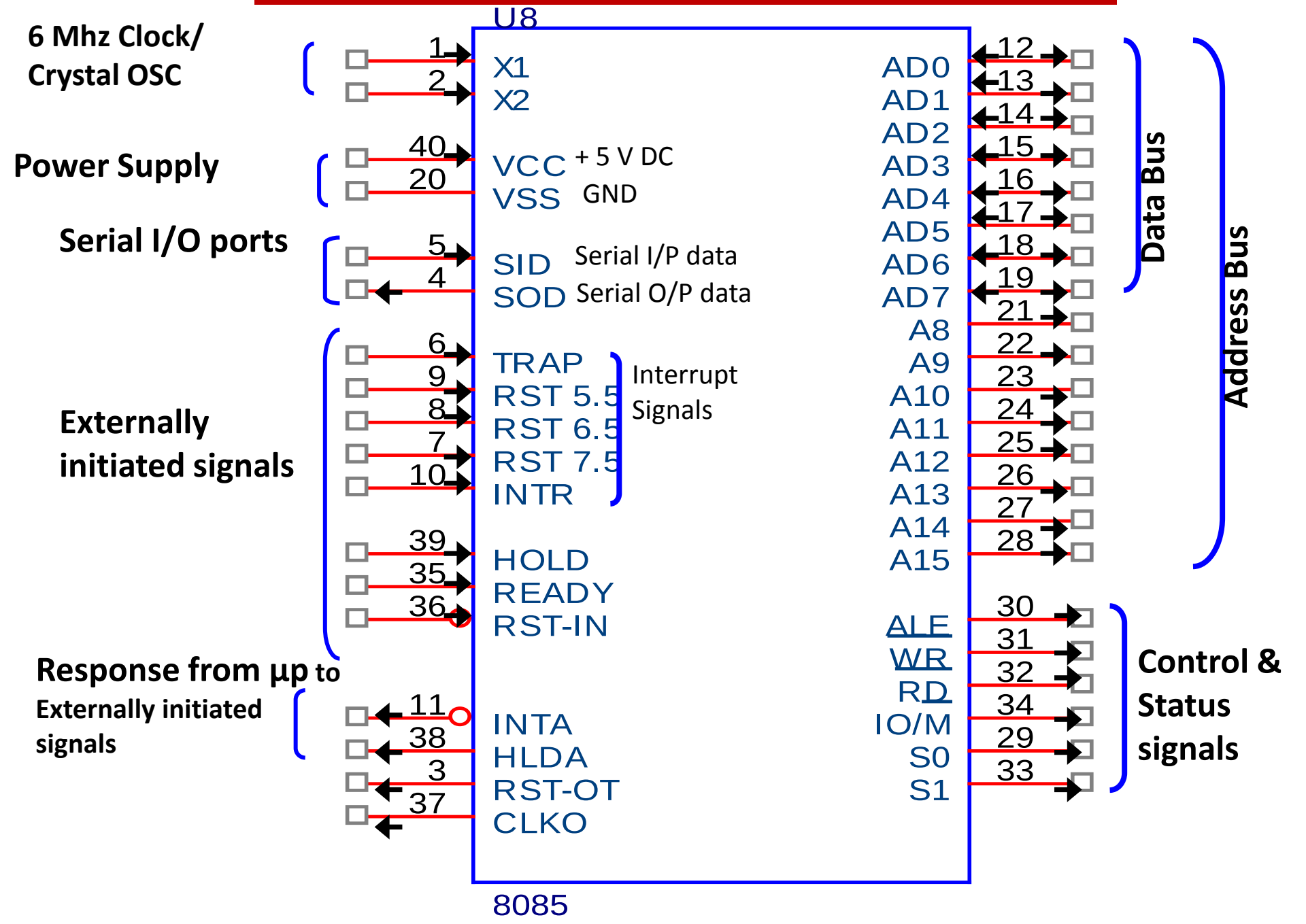


Block diagram of a microcomputer System

- **Basic Elements that contitute the CPU (Central Processing Unit)**
- ***1) ALU*** (Arithmatic & Logic Unit) (for performing Arithmatic (addition, subtraction,…), Logical operations(AND,OR..) & shift (left/right) operations), 8085 µP has 8 bit ALU that means at a time it can perform arithmatic or logical operation on 2, 8 bit operands.
- ***2) A register array*** (for temporary storage of information, during execution of an instruction)
- ***3) Control unit*** supervises the flow of information between various units, generates different control signals and synchronizes every operation with respect to a system clock,

- These elements are connected through one or more internal Bus. (Bus: A group of wires)

Interfaces/ Pinout of 8085 µP



- 8085 is a 40 pin, 8 bit Microprocessor (as it has 8 bit ALU & its data bus width is 8 bit)chip and uses +5V for power. It can run at a maximum frequency of 3 MHz (a clock running at 6 MHz should be connected to the X0 and X1 pins(The frequency is internally divided by 2)). Its I/P O/P pins can be grouped into 6 groups:
- Address Bus.(16 bit (AD0-AD7 & A8-A15))
- Data Bus. (8 bit (AD0-AD7) [multiplexed with Low order Address Bus]
- Control and Status Signals. (RD, WR, IO/$\overline{M}$, So,S1, ALE)
- Power supply and frequency. (VCC(5Volt), GND, Reset in, Reset out, Clock out, X1, X2)
- Externally Initiated Signals. (Trap, RST 7.5, RST 7.5, RST 7.5, INTR, HOLD) & their responses from CPU (INTA, HLDA)
- Serial I/O ports. (SOD(Serial Output Data), SID (Serial Output Data)

The Control and Status Signals

- There are 4 main control and status signals. These are:
- ALE: Address Latch Enable. This signal is a pulse that become 1 when the AD0 – AD7 lines have an address on them. It becomes 0 after that. This signal can be used to enable a latch to save the address bits from the AD lines.
- $\overline{RD}$: Read. Active low.
- $\overline{WR}$: Write. Active low.
- IO/$\overline{M}$: = 0 for memory operation (M-read / M-write)
- = 1 for Input/output (I/O) operation (I/O -read / I/O -write).
- S1 and S0 (In accordance with IO/$\overline{M}$:): Status signals to specify the kind of operation (Machine Cycle) currently being performed by CPU .
- [3 binary bits, hence can identify 8 different Machine cycles 8085.]

- When µP wills to get data from a memory location, **(1)** µp places the address of the memory location (16 bit) in A bus, **(2)** & asserts $\overline{RD}$ (active low)($\overline{RD}$ is made 0, $\overline{WR}$ =1 (deactivated)), **(3)** IO/ $\overline{M}$ is reseted to 0. **(4)** Then memory chip place the content of addressed memory location into data bus, & µp reads the data from data bus.

- When µP wills to send data to a memory location, **(1)** µp places the address of the memory location (16 bit) in A bus, ***places the data into Data bus*** & **(2)** activate $\overline{WR}$ (active low) ($\overline{WR}$ = 0, $\overline{RD}$ = 1), **(3)** IO/ $\overline{M}$ is made to 0. **(4)** Then addressed memory location content gets modified by the data from the data bus.

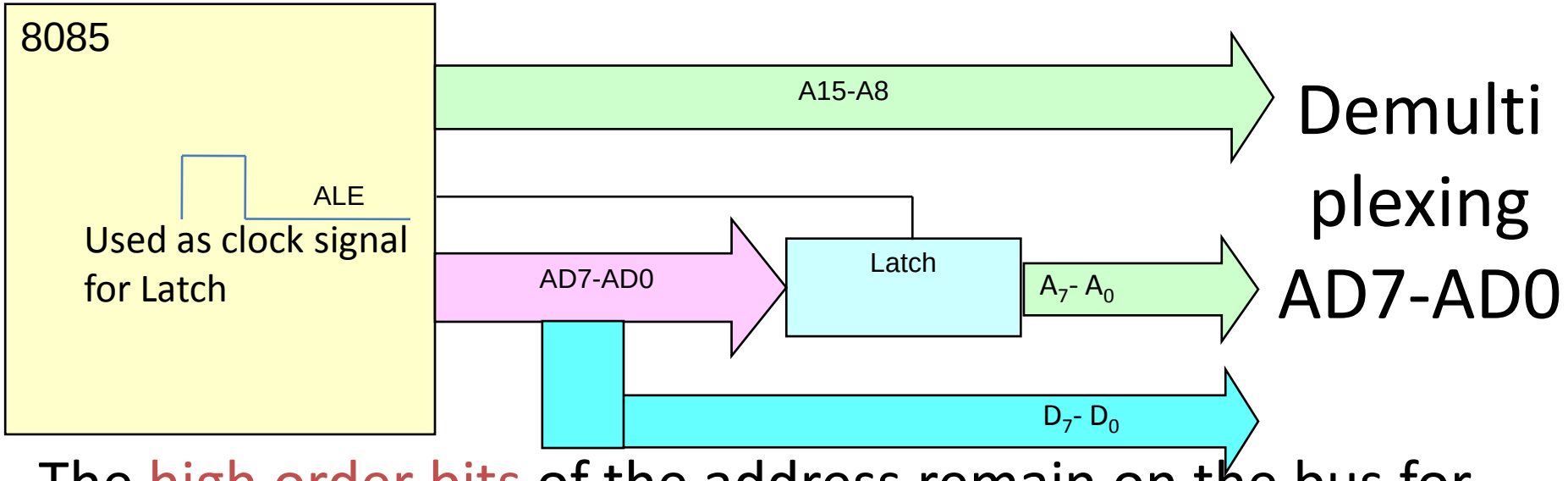
- When µP wills to get data from an input (I/P) device, µp places the address of the device in Address(A) bus, & asserts $\overline{RD}$ (active low) ($\overline{RD}$=0) , IO/ $\overline{M}$ is seted to 1. Then I/P device place the data into data(D) bus, & µp reads the data from data bus.
- When µP wills to send data to an output (O/P) device, µp places the address of the device in A bus, places the data into Data bus & asserts $\overline{WR}$ (active low)($\overline{WR}$=0), IO/ $\overline{M}$ is seted to 1. Then O/P device read the data from the data bus.
- Generally I/O device address is of 8 bit (for 8085). Te same 8 bit device address is duplicated in low as well in high order address bus.

CONTROL / STATUS SIGNALS-

8085 Machine Cycle

IO/M (Active Low)	S1	S2	8085 Machine Cycle
0	0	0	Halt
0	0	1	Memory WRITE
0	1	0	Memory READ
1	0	1	IO WRITE
1	1	0	IO READ
0	1	1	Opcode fetch
1	1	1	Interrupt acknowledge

When ALE=1, AD0-AD7 contain Low Order Address, When ALE=0, AD0-AD7 used as bidirectional Data Bus. ALE goes high only during 1st clock cycle of any 8085 Machine cycle



– The high order bits of the address remain on the bus for three clock periods. However, the low order Address bits remain for only 1st clock period (T1 T state) of a Machine cycle and they would be lost if they are not saved externally. When ALE goes low, the low order address is saved Externally from AD7– AD0 lines and the AD7– AD0 lines can be used as bi-directional data lines.