



EN4430 Analog IC Design

Assignment 03

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1 Introduction to Phase-Locked Loops

A Phase-Locked Loop (PLL) is a critical control system in analog and mixed-signal circuits, widely used for clock generation and frequency synthesis in system-on-chip (SoC) designs. PLLs ensure precise timing for digital circuits, wireline transceivers, and wireless systems by aligning the phase and frequency of an output signal with a reference signal.

A Phase-Locked Loop (PLL) consists of key blocks, each serving a distinct purpose. The phase/frequency detector (PFD) compares the phase of the reference and feedback signals, generating an error signal. The charge pump (CP) converts this error into a current to drive the loop. The charging or discharging of the low-pass filter (LPF) is decided by the positivity or negativity of the current pulse generated by the charge pump (CP). The voltage-controlled oscillator (VCO) generates an output signal, and its oscillation frequency is decided by the control voltage which comes from the Charge Pump and Loop Filter. The frequency divider adjusts the VCO output to match the reference, enabling integer or fractional multiplication.

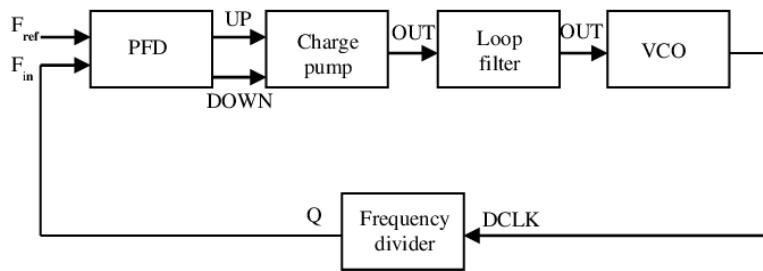


Figure 1: Block diagram of a phase-locked loop

1.1 Design Constraints

Table 1: Desired Project Performance Specifications

Parameter	Project Specification
Technology [Min. length of transistors (L_{min})]	45 nm CMOS
Supply voltage V_{DD}	1 V
Nominal input common-mode voltage $V_{DD}/2$	0.5 V
Reference frequency f_{REF}	200 MHz
Fractional division ratio N	$2 \leq N \leq 16$
Output frequency range f_{OUT}	$f_{OUT,min}$ GHz - $f_{OUT,max}$ GHz
PLL lock time t_{lock}	$t_{lock,min}$ ps - $t_{lock,max}$ ps
Overall average DC power consumption $P_{total,avg}$? μ W

2 Phase/Frequency Detector (PFD)

In a phase-locked loop (PLL), the phase detector compares the reference frequency (f_{ref}) with the feedback frequency (f_{feed}). When f_{ref} leads f_{feed} , indicating a positive phase error, the UP signal is extended. This drives the charge pump and loop filter to increase the voltage-controlled oscillator (VCO) frequency. Conversely, when f_{ref} lags f_{feed} , the DOWN signal dominates, reducing the VCO frequency to align the phases.

All PMOS and NMOS components inside the phase-frequency detector (PFD) are sized at a 45nm length, with a 1 μ m width for NMOS and a 2 μ m width for PMOS.

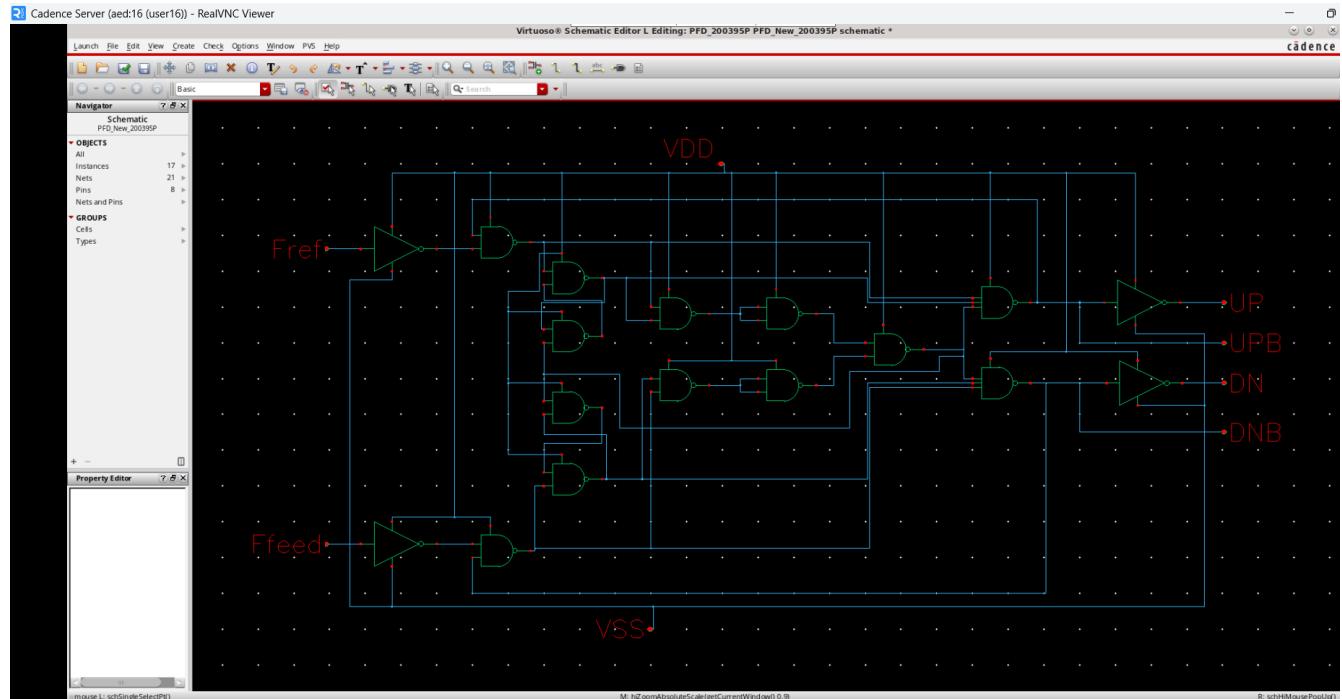


Figure 2: Schematic of the Phase/Frequency Detector (PFD).

Signal	Voltage 1	Voltage 2	Period	Delay	Rise/Fall Time	Pulse Width
fref	0 V	1 V	2 ns	—	50 ps	1 ns
ffeed	0 V	1 V	6 ns	1 ns	50 ps	3 ns

Table 2: Testbench parameters for the PFD signals fref and ffeed.

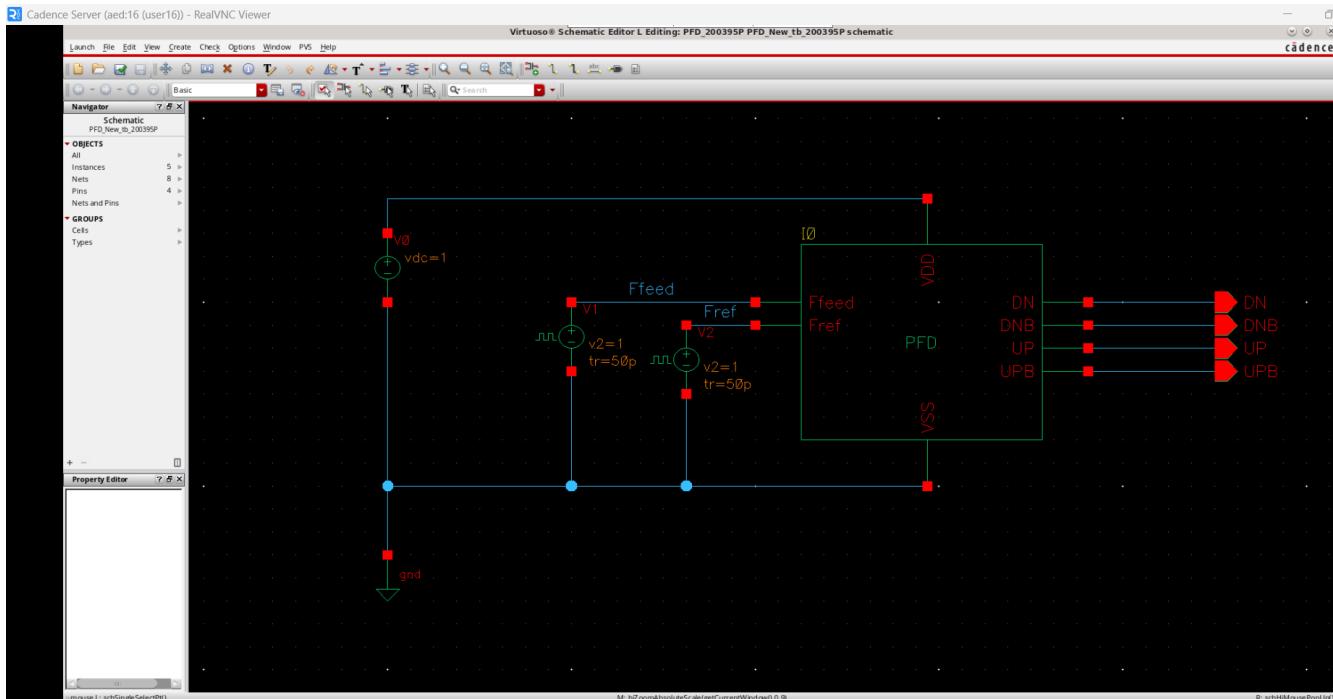


Figure 3: Testbench setup for the Phase/Frequency Detector (PFD).

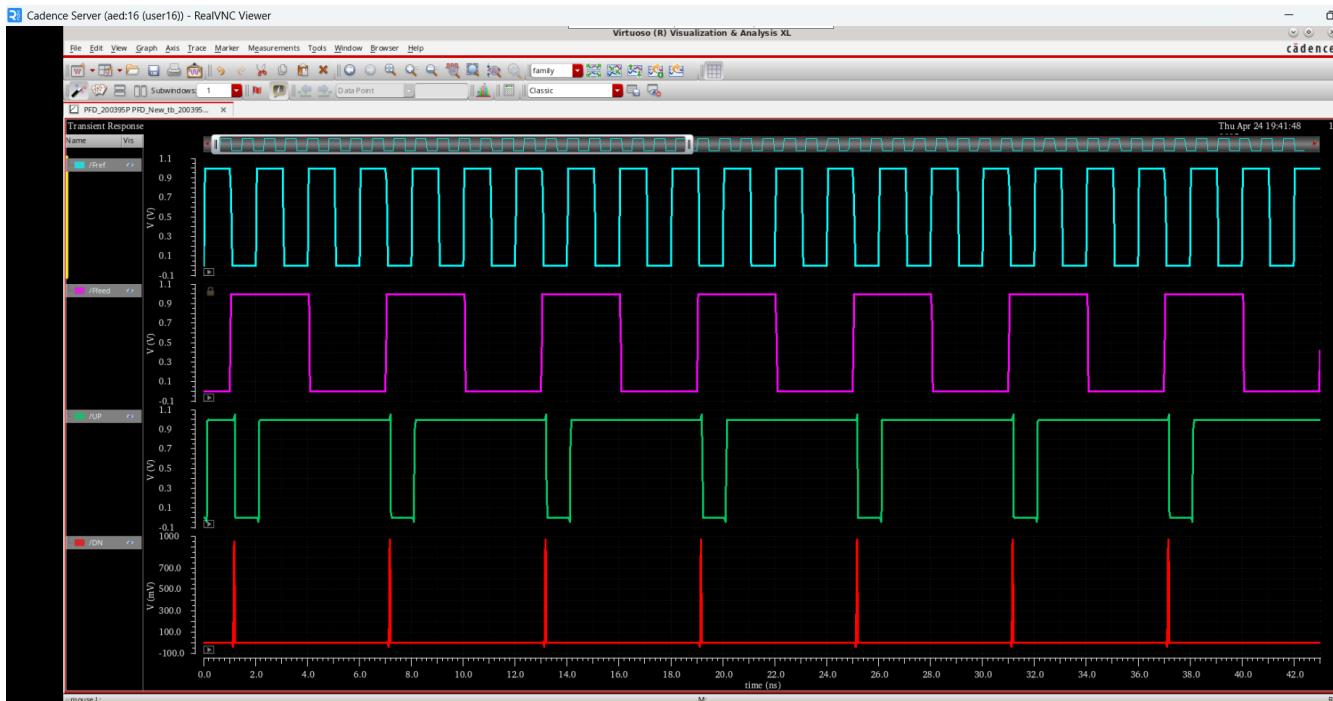


Figure 4: Transient Simulation results of the Phase/Frequency Detector (PFD).

3 Charge Pump(CP) & Loop Filter

The NMOS-switch high-swing cascode charge pump employs two high-swing cascode current mirrors: a p-channel mirror (MP1–MP5) for the charge-up current (I_{UP}) and an n-channel mirror (MN1, MN8–MN11) for the discharge current (I_{DN}), both with an output resistance proportional to $g_m r_o^2$, significantly enhancing current matching. A pull-up mirror (MN4, MP8, MP9) accelerates MP3 turn-off for I_{UP} , and a pull-down mechanism (MN7 connected to MN9's gate) remedies slow-node issues for I_{DN} , enabling fast charging and discharging of the output voltage V_{ctrl} . The operation principle of Charge Pump(CP) & Loop Filter can be described as follows where Φ_{IN} is the phase error between f_{REF} and f_{FEED} .

- When the PLL is unlocked and Φ_{IN} is positive(f_{REF} is leading to f_{FEED}), Φ_{IN} is detected by the PFD and CP generates a positive current pulse I_{CP} to charge the LPF so as to increase f_{VCO} to reduce Φ_{IN} .
- When the PLL is unlocked and Φ_{IN} is negative(f_{REF} is lagging to f_{FEED}), CP generates a negative current pulse I_{CP} to discharge the LPF so as to decrease f_{VCO} to reduce $|\Phi_{IN}|$.
- At the locking state, Φ_{IN} keeps zero so that the VCO tuning voltage V_C keeps stable. As a result, $f_{VCO} = N \cdot f_{REF}$.

Table 3: Transistor Sizes for NMOS-Switch High-Swing Cascode Charge Pump

Transistor	W/L Ratio	W/L (nm)
MP1	4/0.5	4000/500
MP2, MP3, MP4, MP5	11/0.2	11 000/200
MP6, MP7	20/0.12	20 000/120
MP8, MP9	0.5/0.2	500/200
MN1, MN2, MN3	2/0.2	2000/200
MN4, MN5, MN6, MN7	2/0.12	2000/120
MN8, MN9, MN10, MN11	10/0.2	10 000/200

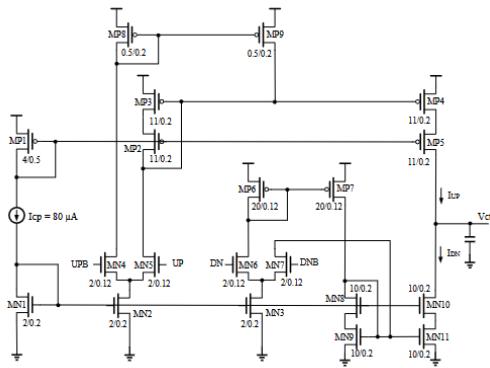


Figure 5: NMOS-switch high-swing cascode charge pump (W/L transistor dimensions in microns)

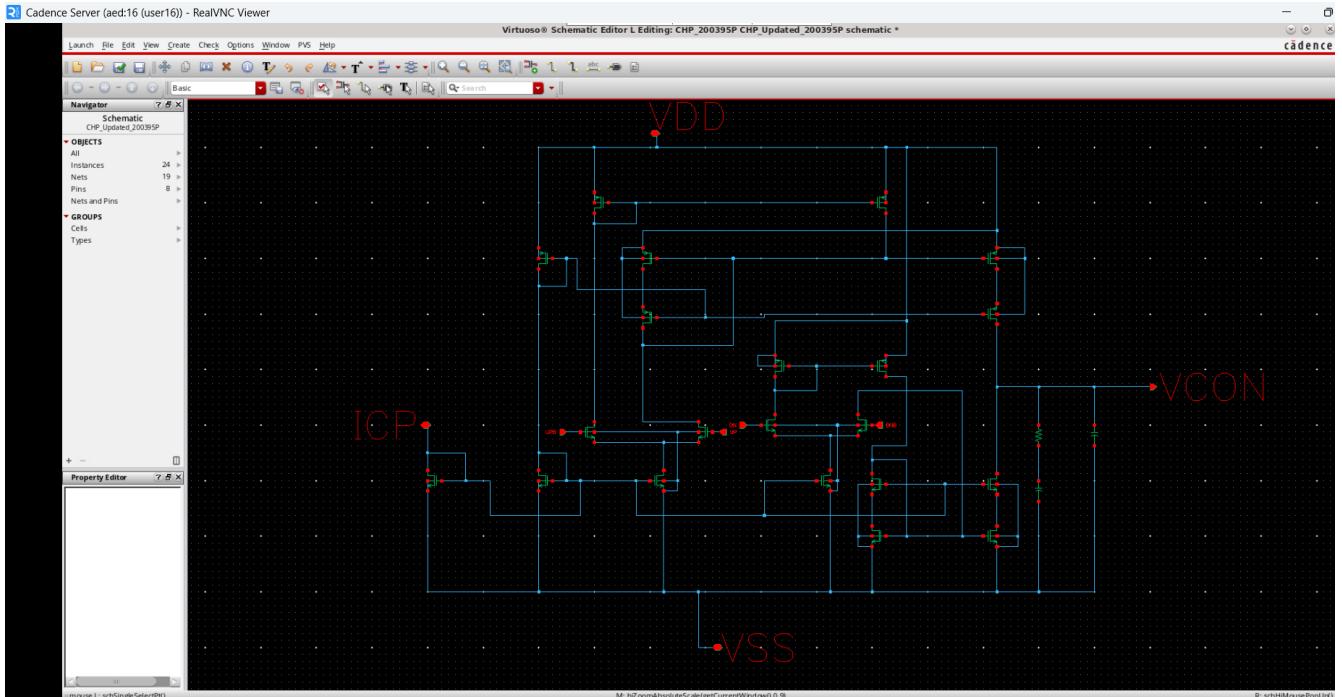


Figure 6: Schematic of the Charge Pump (CP) and Loop Filter (LPF).

The loop filter consists of a $1\text{k}\Omega$ resistor in series with a 5pF capacitor, with an additional 1pF capacitor connected in parallel to the resistor-capacitor series combination.

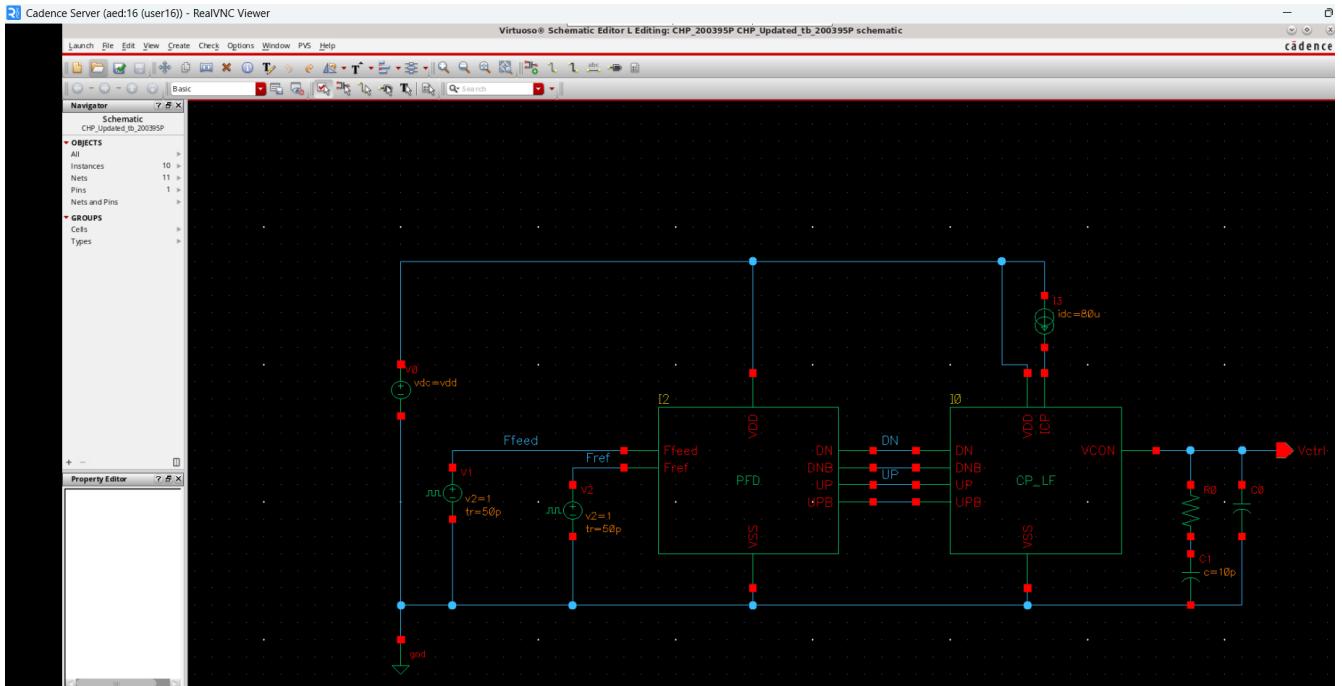


Figure 7: Testbench setup for the Charge Pump (CP) and Loop Filter (LPF).

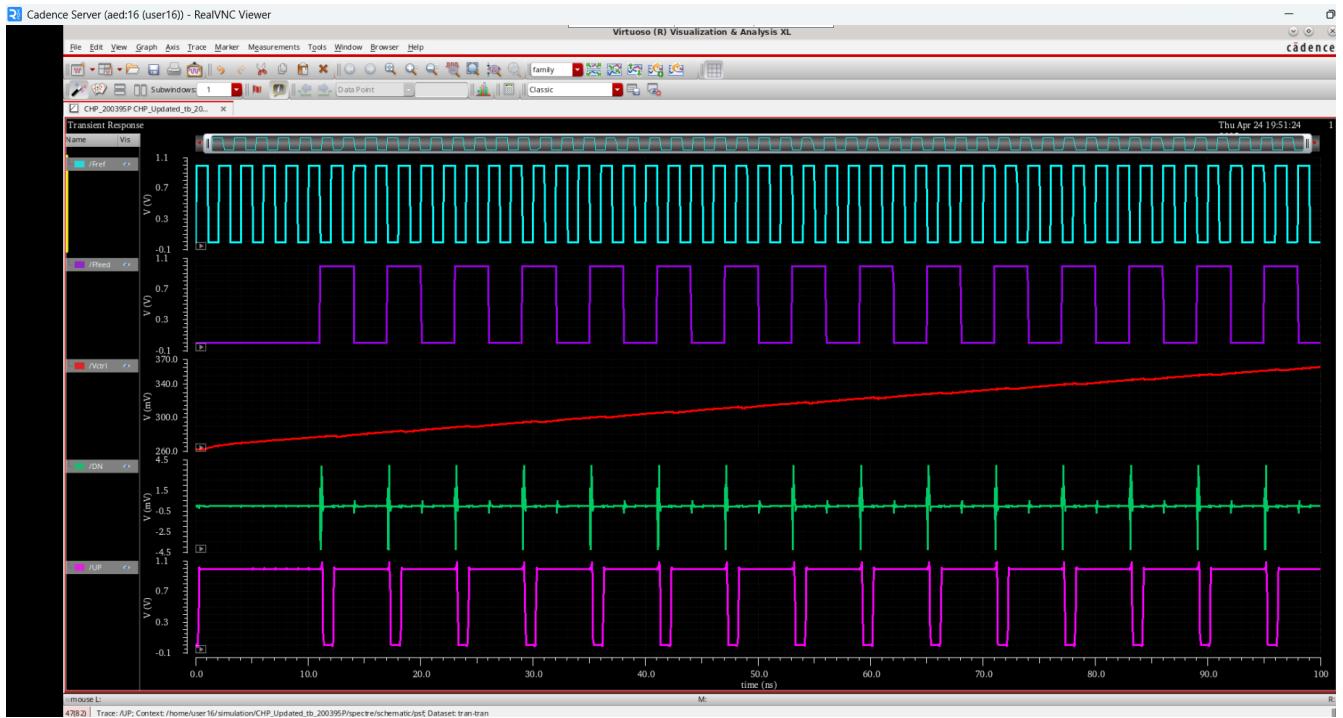


Figure 8: Transient Simulation results of the Charge Pump (CP) and Loop Filter (LPF).

4 Three-Stage Ring VCO

The three-stage ring voltage-controlled oscillator (VCO) designed for this project generates the output frequency for the Phase-Locked Loop (PLL). The PMOS transistors have a width of $2\text{ }\mu\text{m}$ and the NMOS transistors have a width of $1\text{ }\mu\text{m}$, both with a length of 45 nm. The frequency is tuned by adjusting the control voltage (V_{IN}), provided by the charge pump and loop filter. Compared to LC VCOs, which rely on inductors and capacitors for resonance and require a larger silicon area, this ring VCO design offers a more compact footprint and a wider frequency tuning range, making it well-suited for the fractional-N PLL's requirements.

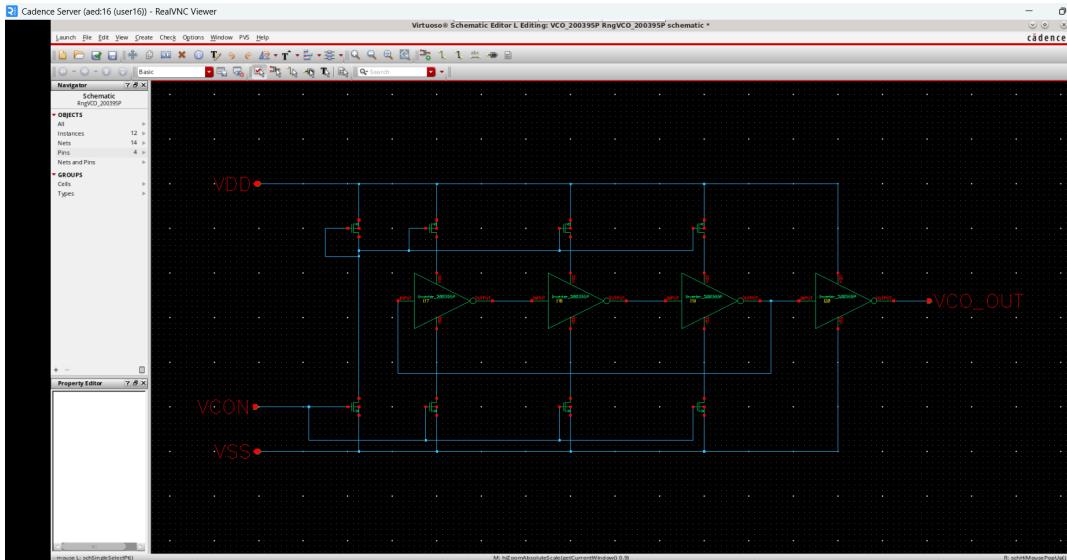


Figure 9: Schematic of the Three-Stage Ring VCO.

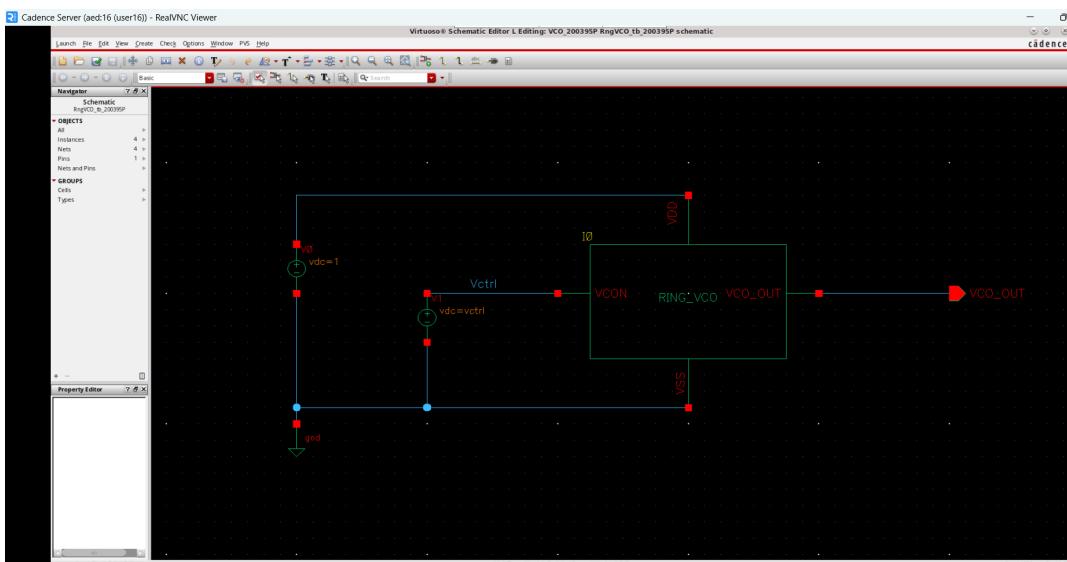


Figure 10: Testbench setup for the Three-Stage Ring VCO.



Figure 11: Transient Simulation & FFT Results for Vctrl range from 0V to 1V

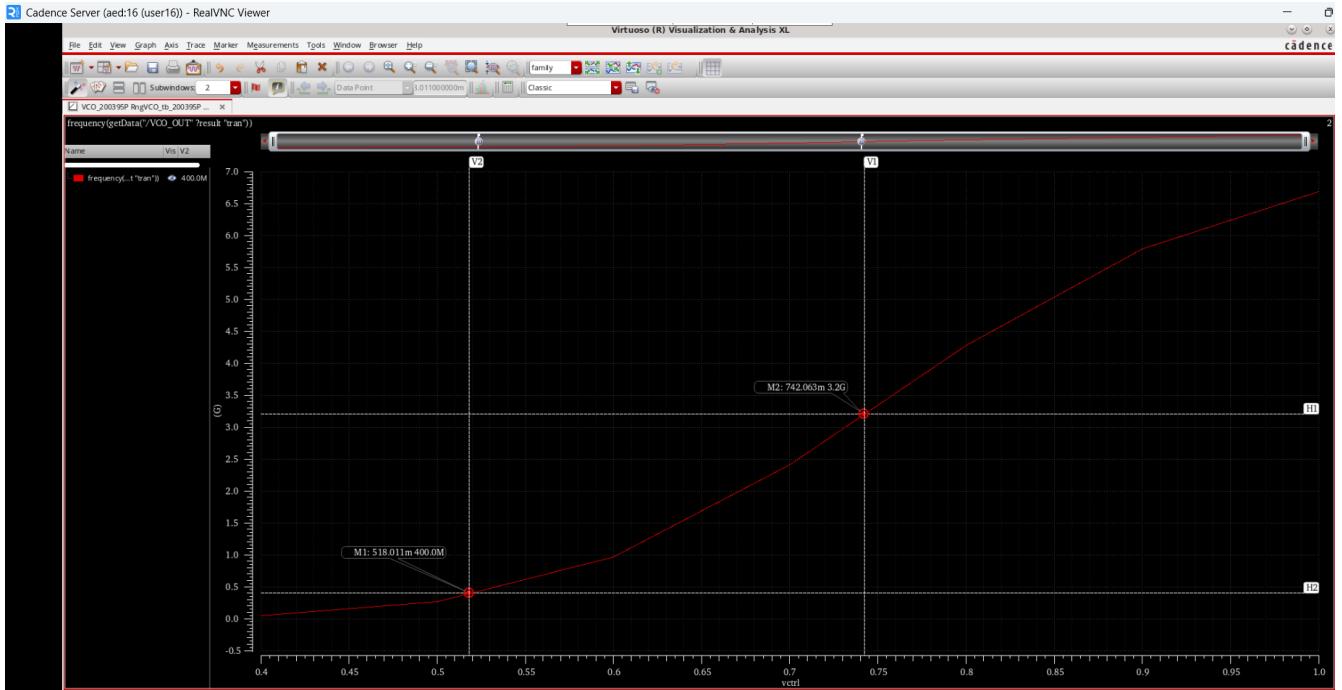


Figure 12: Control Voltage (Vctrl) vs. Output Frequency (Fout) for the Three-Stage Ring VCO

The PLL design should operate for $N = 2$ to $N = 16$, with $f_{ref} = 200 \text{ MHz}$. $F_{vco} = N \cdot f_{ref}$, yielding F_{vco} range from 400 MHz to 3.2 GHz; referring to the Vctrl vs. Fout plot for the Three-Stage Ring VCO, a wider tuning range of output frequency is achieved by varying Vctrl from 0 to 1. According to the simulation plot, to achieve the frequency range of 400 MHz to 3.2 GHz, Vctrl must be varied from 518.011 mV to 742.063 mV.

5 Multiple Frequency Divider

The multiple frequency divider is designed to divide the output frequency of the Voltage-Controlled Oscillator (VCO) by factors of 2, 3, 4, 5, 6, 8, 9, 10, 12, 15, and 16, making it a versatile component in the integer-N Phase-Locked Loop (PLL). This divider is implemented by cascading sub-frequency dividers to achieve the desired division ratios. For example, to divide by 15, the divide-by-3 and divide-by-5 dividers are cascaded. The schematic shows a series of flip-flop-based stages, with inputs CLK_IN and outputs CLK_OUT.

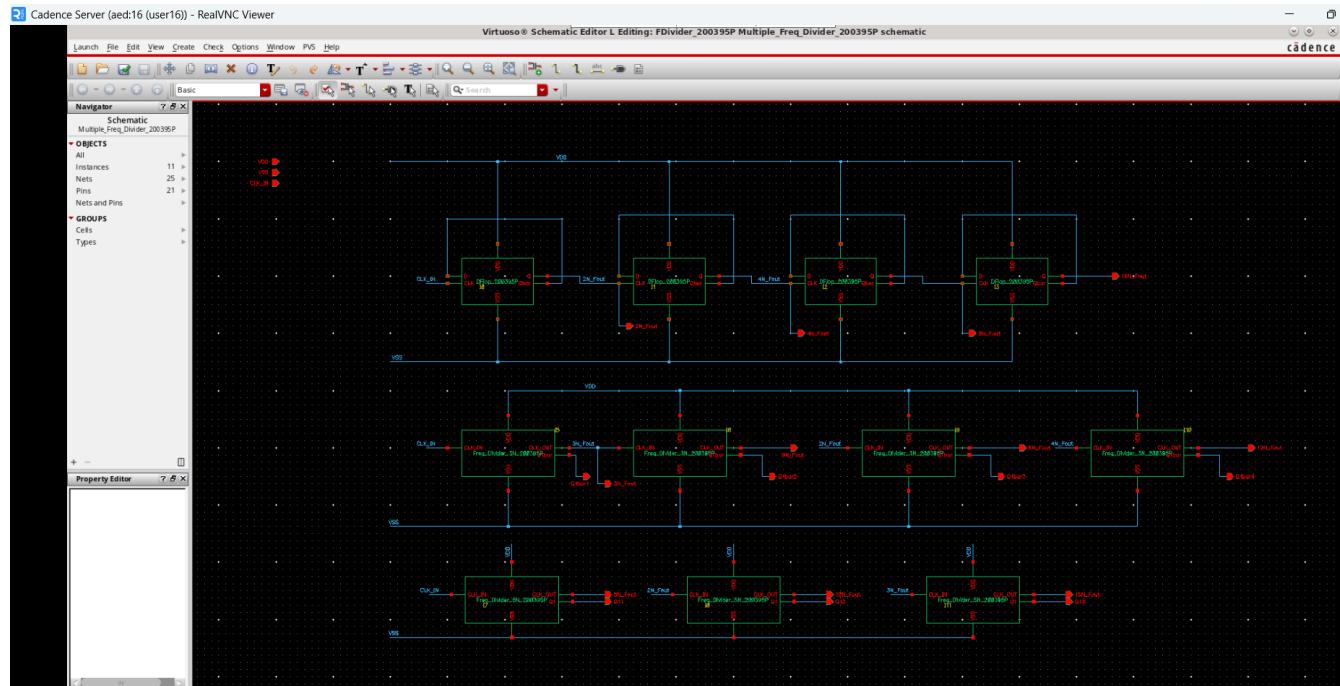


Figure 13: Schematic of the Multiple Frequency Divider.

Sub-Frequency Divider Schematics

The design includes sub-frequency dividers, such as divide-by-3 and divide-by-5, which are cascaded to form the multiple frequency divider. Below are the schematics for these sub-dividers.

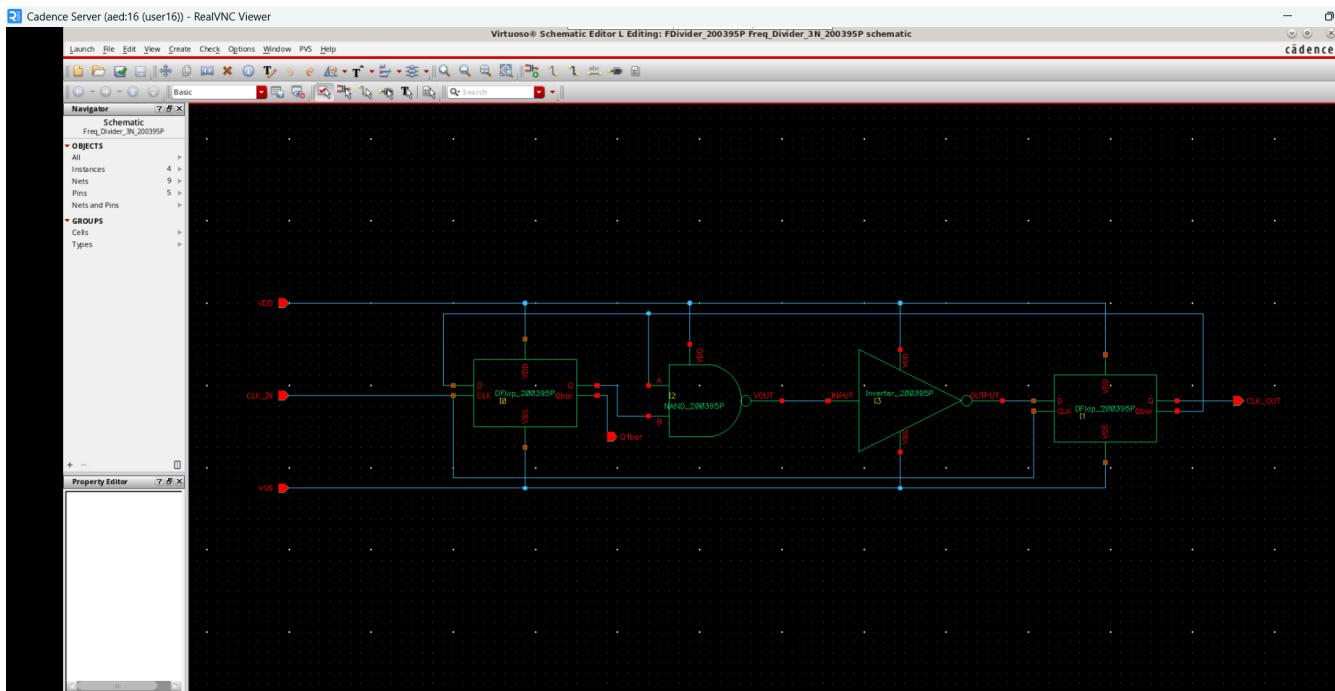


Figure 14: Schematic of the Divide-by-3 Frequency Divider.



Figure 15: Schematic of the Divide-by-5 Frequency Divider.

6 PFD-CP Based Integer-N Phase-Locked Loop Design

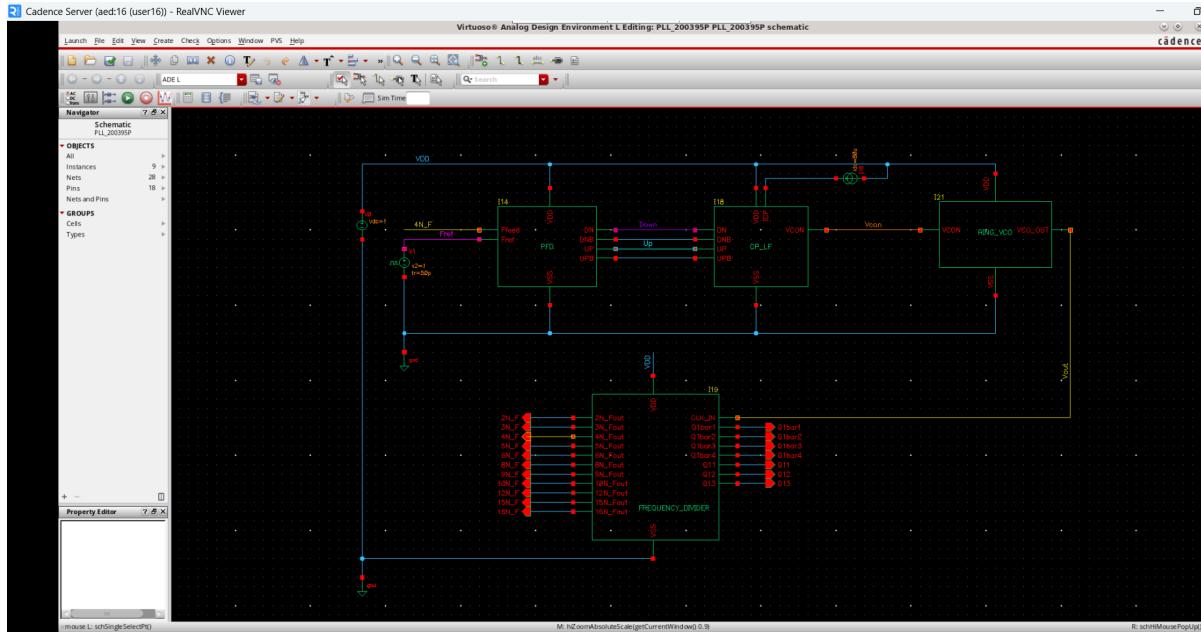


Figure 16: Testbench setup for the PFD-CP Fractional-N Phase-Locked Loop.

6.1 PLL's performance in a divide-by-2 configuration



Figure 17: Transient simulation results of the PLL with a divider ratio of $N = 2$, showing the locking behavior over time with a lock time of $\approx 70\text{ns}$.



Figure 18: FFT simulation results of the PLL with a divider ratio of $N = 2$, displaying the frequency spectrum with the oscillation frequency ($f_0 \approx 400MHz$ MHz).

6.2 PLL's performance in a divide-by-3 configuration

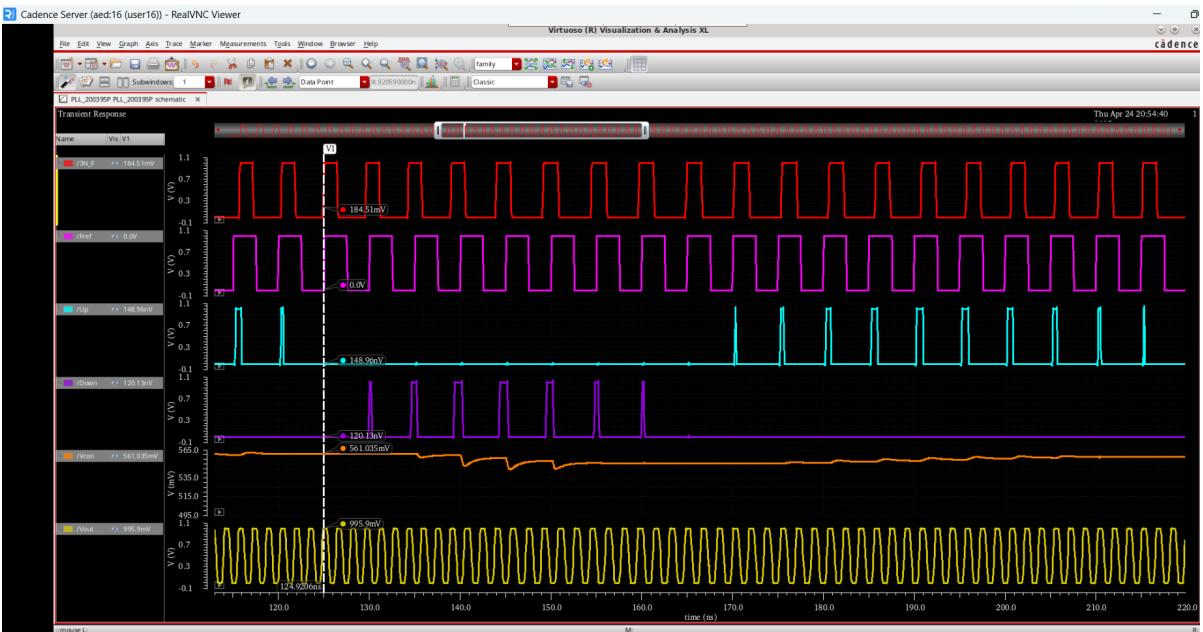


Figure 19: Transient simulation results of the PLL with a divider ratio of $N = 3$, showing the locking behavior over time with a lock time of $\approx 124.9206ns$.

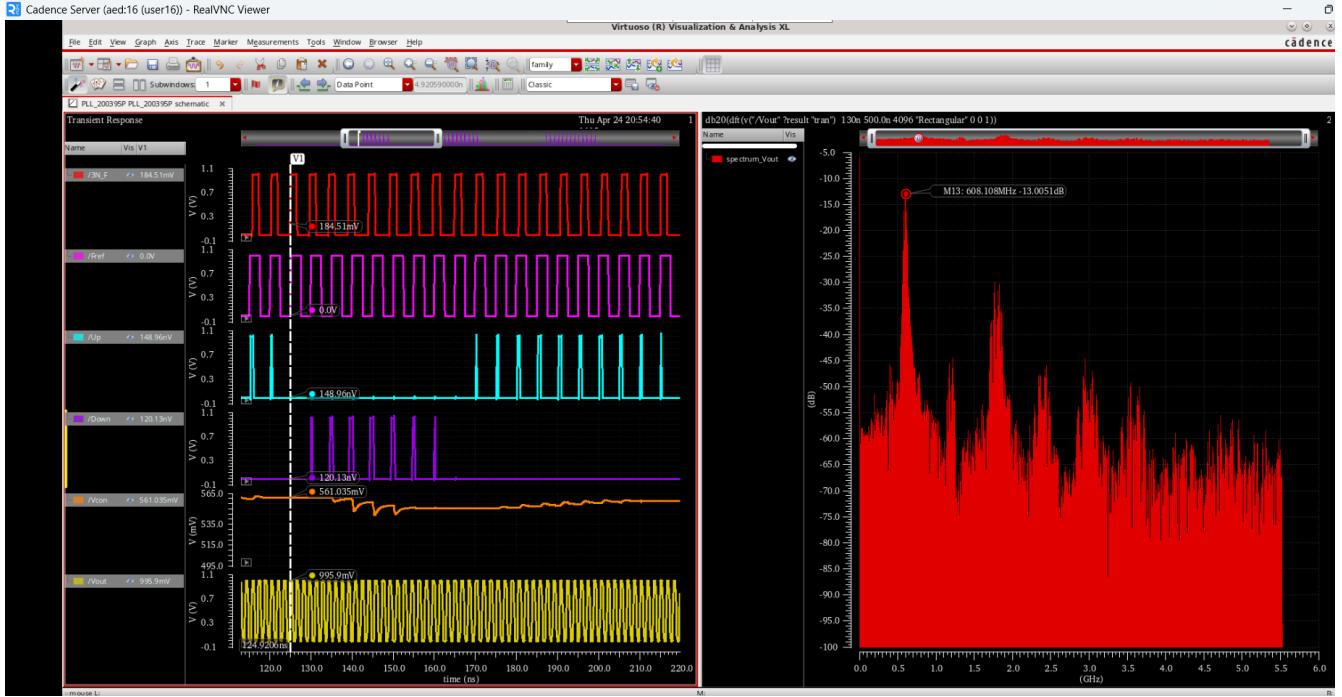


Figure 20: FFT simulation results of the PLL with a divider ratio of $N = 3$, displaying the frequency spectrum with the oscillation frequency ($f_0 \approx 608.108\text{MHz}$).

6.3 PLL's performance in a divide-by-4 configuration

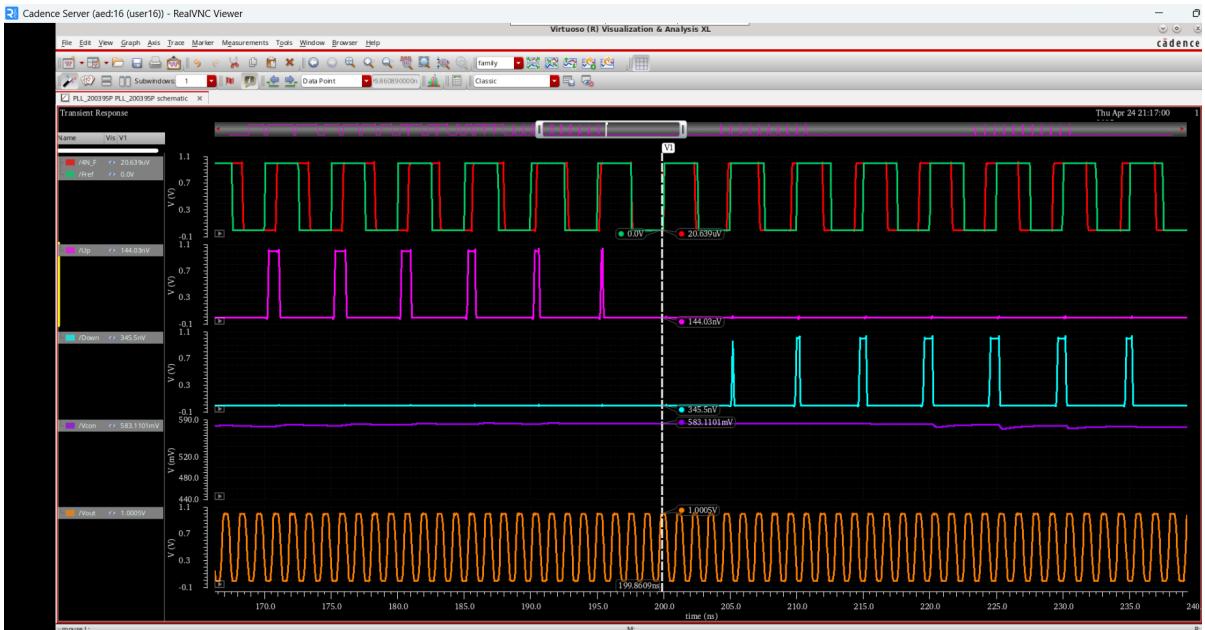


Figure 21: Transient simulation results of the PLL with a divider ratio of $N = 4$, showing the locking behavior over time with a lock time of $\approx 199.8609\text{ns}$.

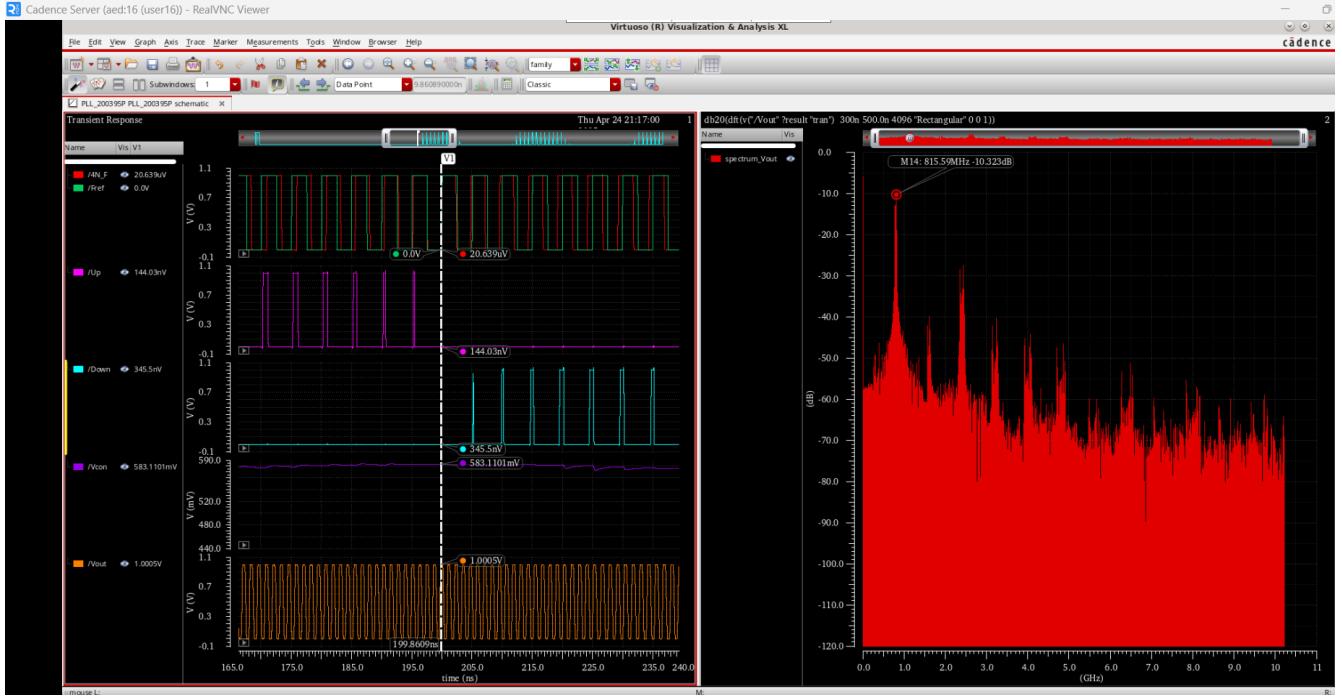


Figure 22: FFT simulation results of the PLL with a divider ratio of $N = 4$, displaying the frequency spectrum with the oscillation frequency ($f_0 \approx 815.59\text{MHz}$).

6.4 PLL's performance in a divide-by-5 configuration

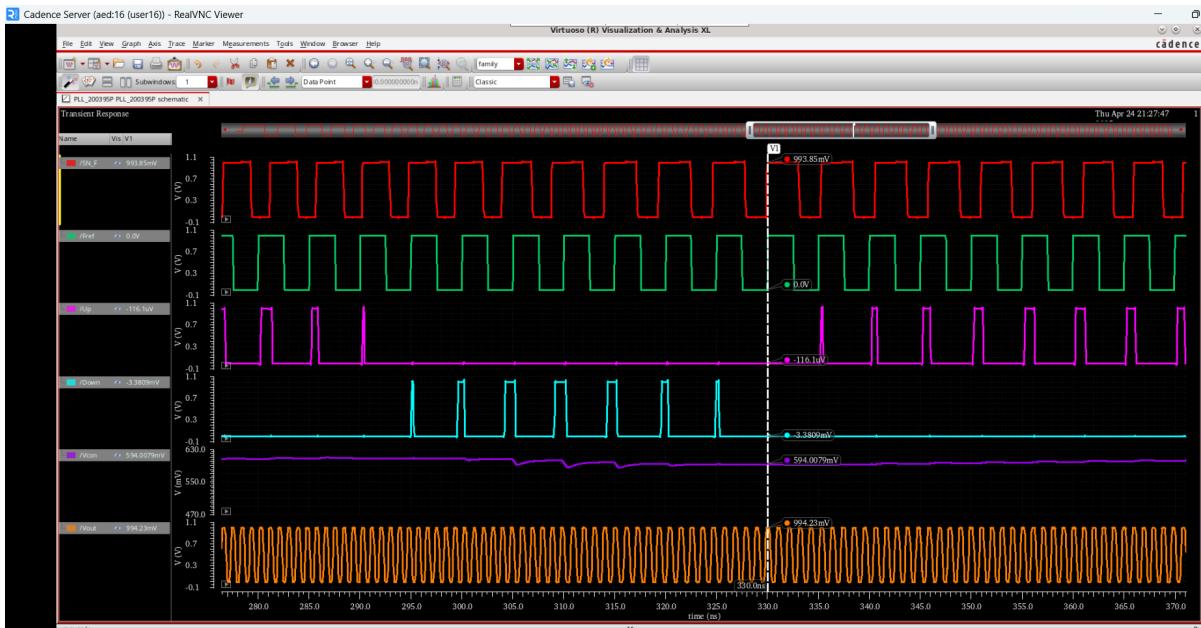


Figure 23: Transient simulation results of the PLL with a divider ratio of $N = 5$, showing the locking behavior over time with a lock time of $\approx 330\text{ns}$.

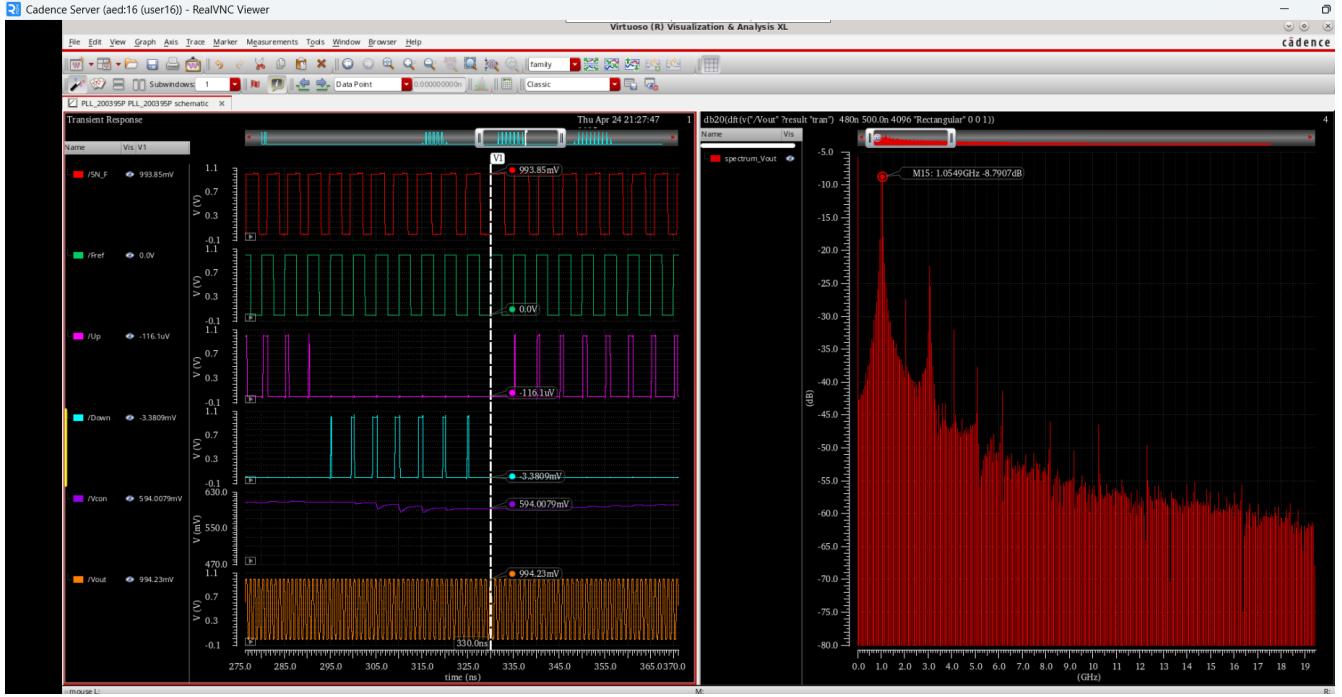


Figure 24: FFT simulation results of the PLL with a divider ratio of $N = 5$, displaying the frequency spectrum with the oscillation frequency ($f_0 \approx 1.0549\text{GHz}$ MHz).

6.5 PLL's performance in a divide-by-6 configuration



Figure 25: Transient simulation results of the PLL with a divider ratio of $N = 6$, showing the locking behavior over time with a lock time of $\approx 320\text{ns}$.

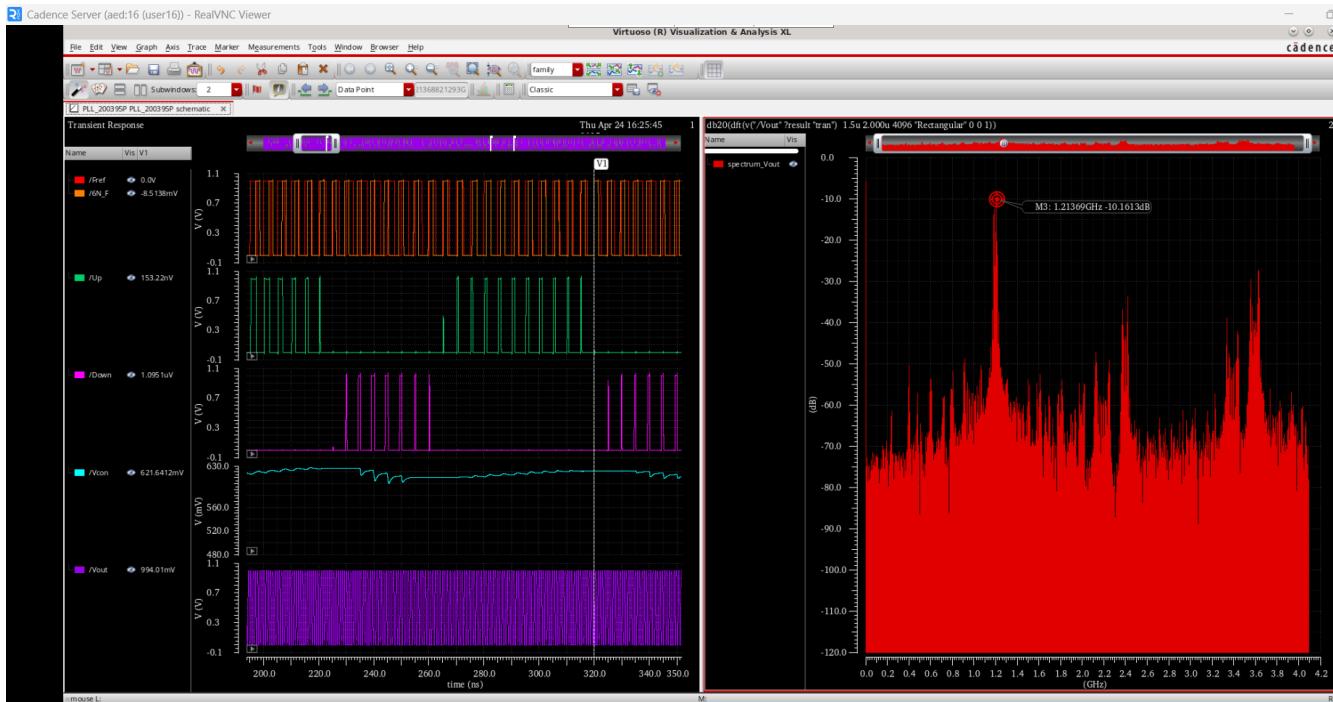


Figure 26: FFT simulation results of the PLL with a divider ratio of $N = 6$, displaying the frequency spectrum with the oscillation frequency ($f_0 \approx 1.21369\text{GHz}$ MHz).

6.6 PLL's performance in a divide-by-8 configuration

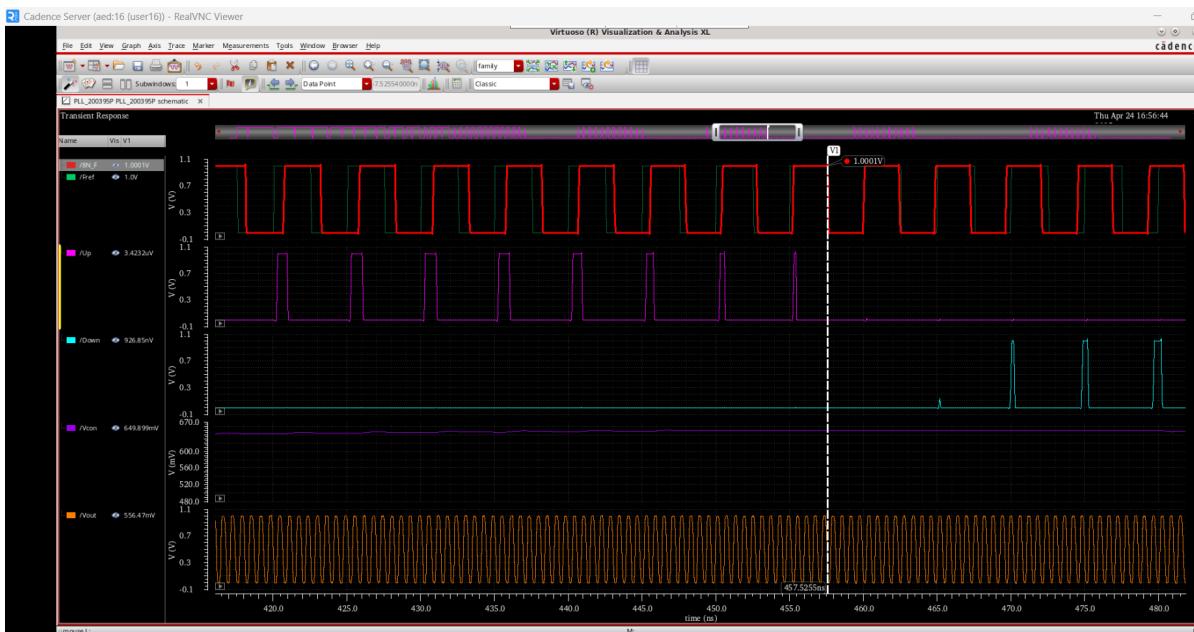


Figure 27: Transient simulation results of the PLL with a divider ratio of $N = 8$, showing the locking behavior over time with a lock time of $\approx 457.5255\text{ns}$.



Figure 28: FFT simulation results of the PLL with a divider ratio of $N = 8$, displaying the frequency spectrum with the oscillation frequency ($f_0 \approx 1.61812\text{GHz}$ MHz).

6.7 PLL's performance in a divide-by-9 configuration



Figure 29: Transient simulation results of the PLL with a divider ratio of $N = 9$, showing the locking behavior over time with a lock time of $\approx 535.0083\text{ns}$.

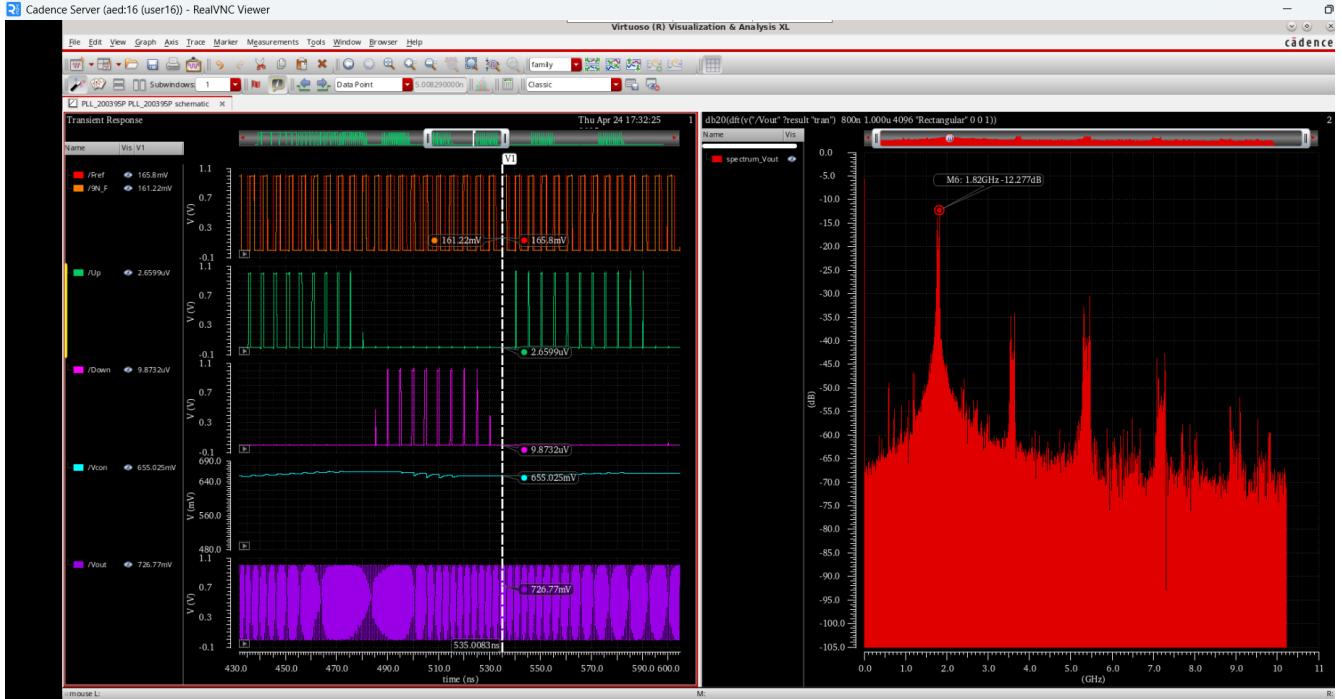


Figure 30: FFT simulation results of the PLL with a divider ratio of $N = 9$, displaying the frequency spectrum with the oscillation frequency ($f_0 \approx 1.82\text{GHz}$ MHz).

6.8 PLL's performance in a divide-by-10 configuration



Figure 31: Transient simulation results of the PLL with a divider ratio of $N = 10$, showing the locking behavior over time with a lock time of $\approx 570\text{ns}$.



Figure 32: FFT simulation results of the PLL with a divider ratio of $N = 10$, displaying the frequency spectrum with the oscillation frequency ($f_0 \approx 2.0167\text{GHz}$ MHz).

6.9 PLL's performance in a divide-by-12 configuration



Figure 33: Transient simulation results of the PLL with a divider ratio of $N = 12$, showing the locking behavior over time with a lock time of $\approx 635.0554\text{ns}$.

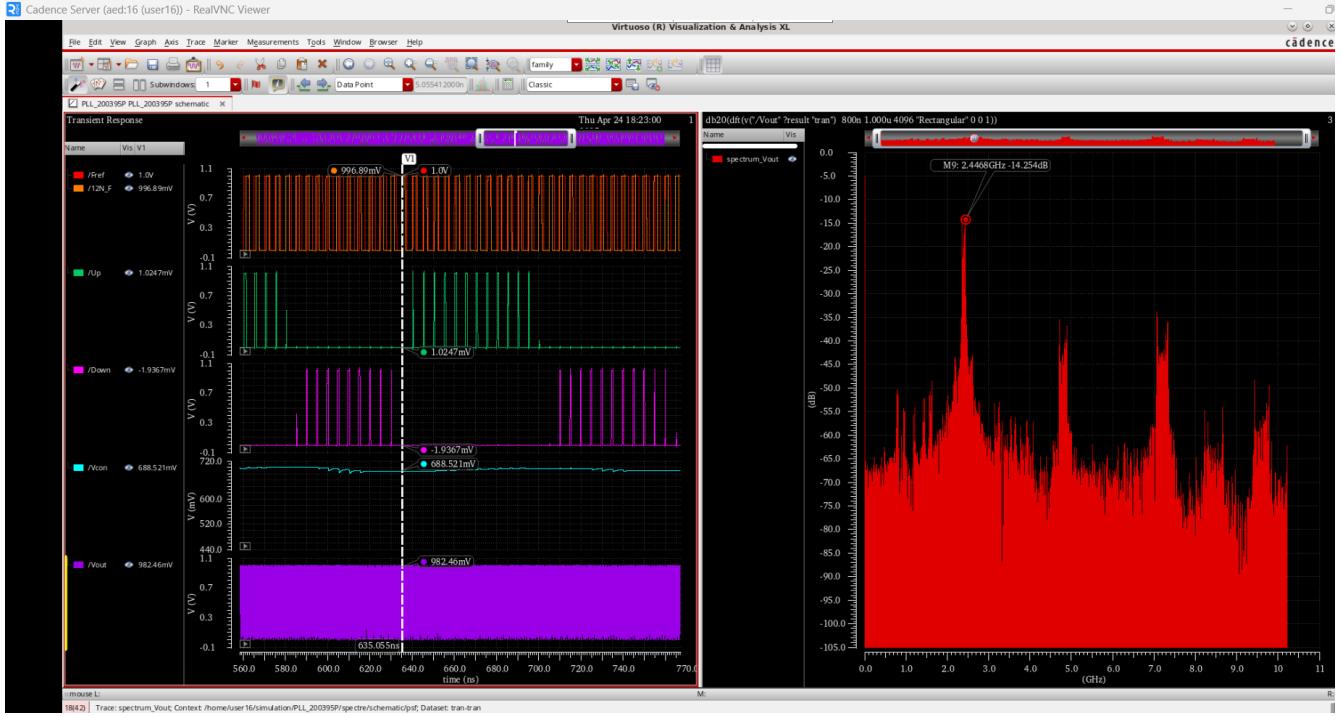


Figure 34: FFT simulation results of the PLL with a divider ratio of $N = 12$, displaying the frequency spectrum with the oscillation frequency ($f_0 \approx 2.4468\text{GHz}$ MHz).

6.10 PLL's performance in a divide-by-15 configuration



Figure 35: Transient simulation results of the PLL with a divider ratio of $N = 15$, showing the locking behavior over time with a lock time of $\approx 705\text{ns}$.

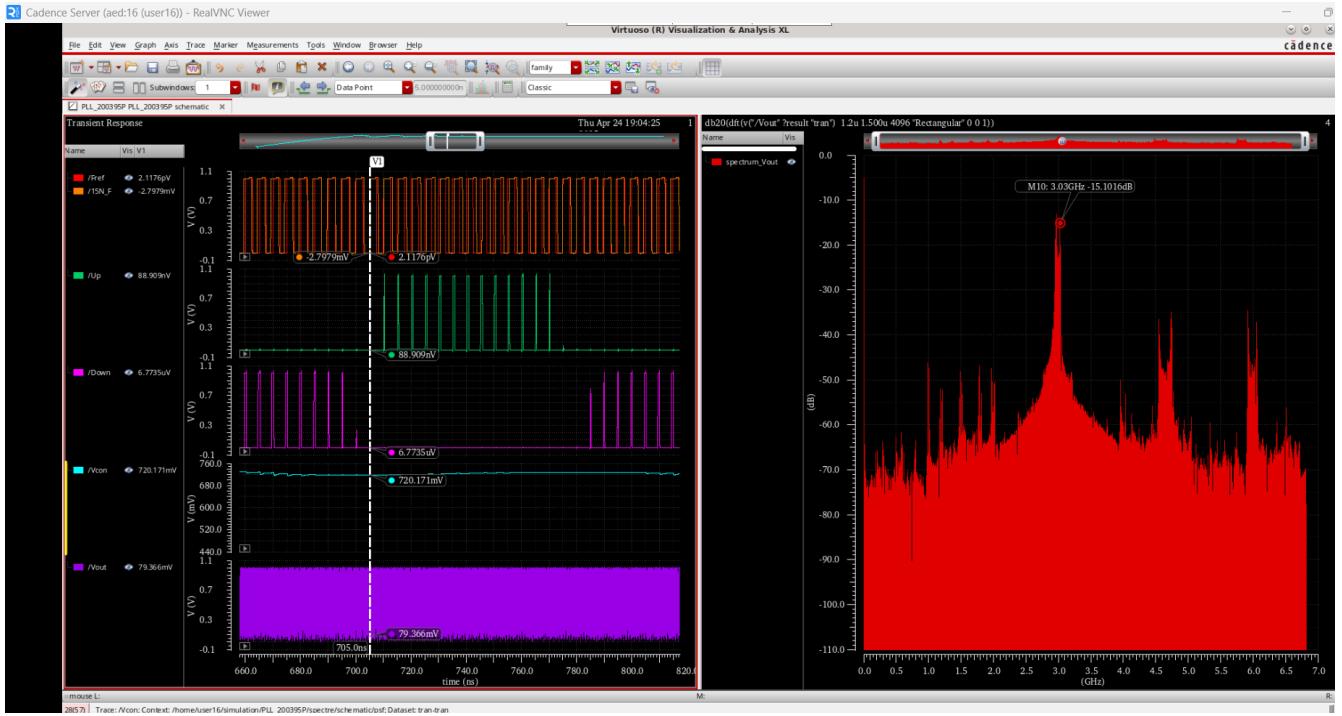


Figure 36: FFT simulation results of the PLL with a divider ratio of $N = 15$, displaying the frequency spectrum with the oscillation frequency ($f_0 \approx 3.03\text{GHz}$ MHz).

6.11 PLL's performance in a divide-by-16 configuration

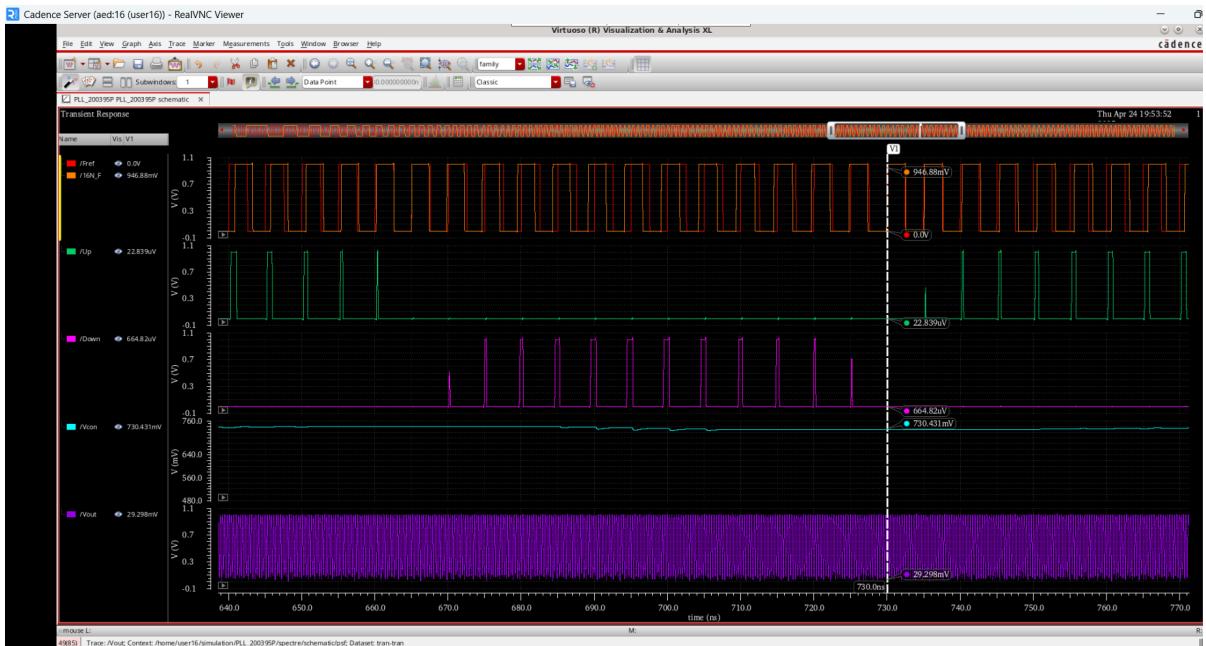


Figure 37: Transient simulation results of the PLL with a divider ratio of $N = 16$, showing the locking behavior over time with a lock time of $\approx 730\text{ns}$.



Figure 38: FFT simulation results of the PLL with a divider ratio of $N = 16$, displaying the frequency spectrum with the oscillation frequency ($f_0 \approx 3.25704\text{GHz}$ MHz).

7 Summary of Fractional Division Ratio, Output Frequency, and Locking Time

Performance data was provided for divider ratios $N = 2, 3, 4, 5, 6, 8, 9, 10, 12, 15, 16$. The output frequency f_{OUT} (3-Stages Ring VCO output frequency) and locking time for each divider ratio are summarized below:

- $N = 2$: $f_{\text{OUT}} = 0.4 \text{ GHz}$, Locking Time = $0.07 \mu\text{s}$
- $N = 3$: $f_{\text{OUT}} = 0.608108 \text{ GHz}$, Locking Time = $0.1249206 \mu\text{s}$
- $N = 4$: $f_{\text{OUT}} = 0.81559 \text{ GHz}$, Locking Time = $0.1998609 \mu\text{s}$
- $N = 5$: $f_{\text{OUT}} = 1.0549 \text{ GHz}$, Locking Time = $0.33 \mu\text{s}$
- $N = 6$: $f_{\text{OUT}} = 1.21369 \text{ GHz}$, Locking Time = $0.32 \mu\text{s}$
- $N = 8$: $f_{\text{OUT}} = 1.61812 \text{ GHz}$, Locking Time = $0.4575255 \mu\text{s}$
- $N = 9$: $f_{\text{OUT}} = 1.82 \text{ GHz}$, Locking Time = $0.5350083 \mu\text{s}$
- $N = 10$: $f_{\text{OUT}} = 2.0167 \text{ GHz}$, Locking Time = $0.57 \mu\text{s}$
- $N = 12$: $f_{\text{OUT}} = 2.4468 \text{ GHz}$, Locking Time = $0.6350554 \mu\text{s}$
- $N = 15$: $f_{\text{OUT}} = 3.03 \text{ GHz}$, Locking Time = $0.705 \mu\text{s}$
- $N = 16$: $f_{\text{OUT}} = 3.25704 \text{ GHz}$, Locking Time = $0.73 \mu\text{s}$

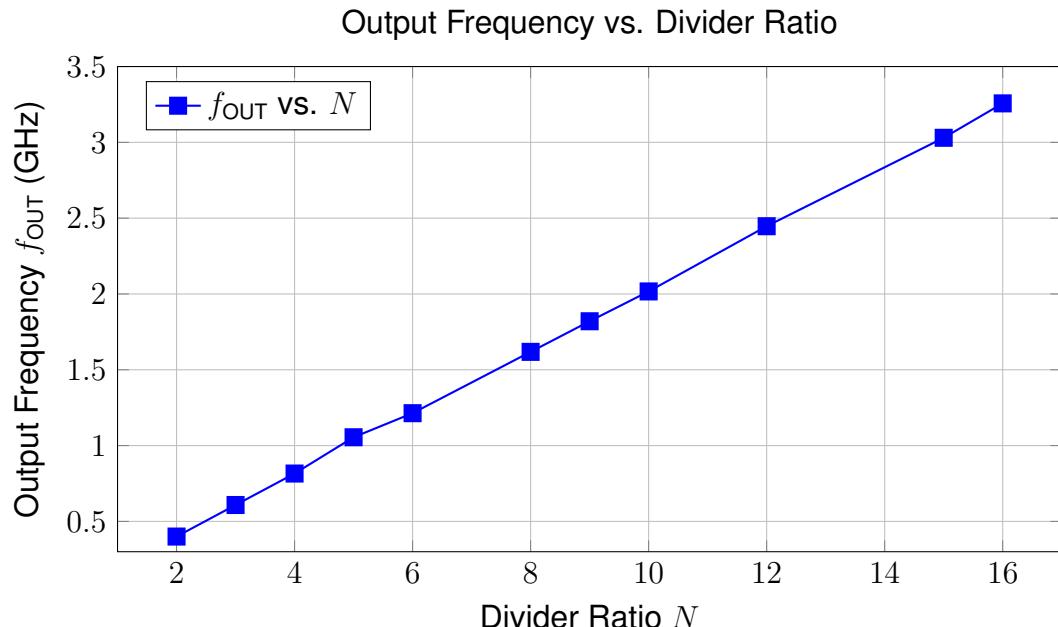


Figure 39: Plot of output frequency f_{OUT} (in GHz) versus divider ratio N for the PFD-CP Integer-N PLL, with data points for $N = 2, 3, 4, 5, 6, 8, 9, 10, 12, 15, 16$.

For $2 \leq N \leq 16$, the output frequency range, based on the tested divider ratios, is:

$$f_{\text{OUT}} \in [0.4 \text{ GHz}, 3.25704 \text{ GHz}]$$

The plot of divider ratio N vs. output frequency f_{OUT} (Figure 39) indicates that $f_{\text{OUT}} \approx N \times f_{\text{REF}}$, where f_{REF} is the reference frequency.

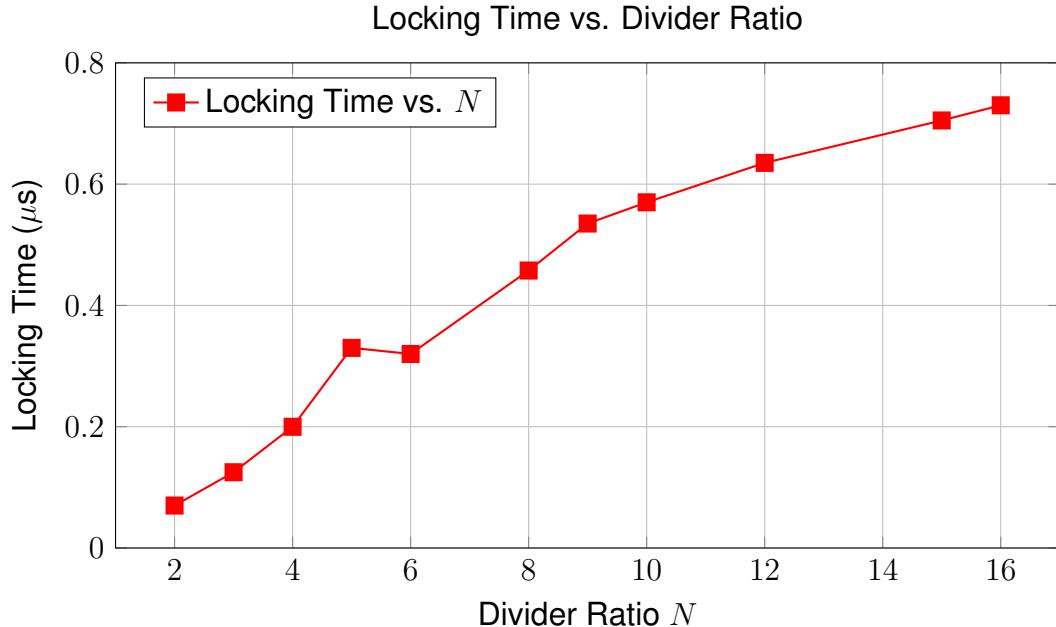


Figure 40: Plot of locking time (in μs) versus divider ratio N for the PFD-CP Integer-N PLL, with data points for $N = 2, 3, 4, 5, 6, 8, 9, 10, 12, 15, 16$.

The locking time range is:

$$\text{Locking Time} \in [0.07 \mu\text{s}, 0.73 \mu\text{s}]$$

8 Overall Power Consumption

The power consumption of the Integer-N Phase-Locked Loop (PLL) is evaluated for a 1 V supply voltage, focusing on dynamic and static contributions. The analysis is based on simulation results for divider ratios $N = 2$ and $N = 16$.

8.1 Dynamic Power Consumption

Dynamic power consumption arises from the switching activity of the PLL components, calculated as $P_{\text{dynamic}} = V \times I_{\text{avg}}$, where V is the supply voltage and I_{avg} is the average current.

8.1.1 Dynamic Power Consumption for Divide-by-2 Configuration

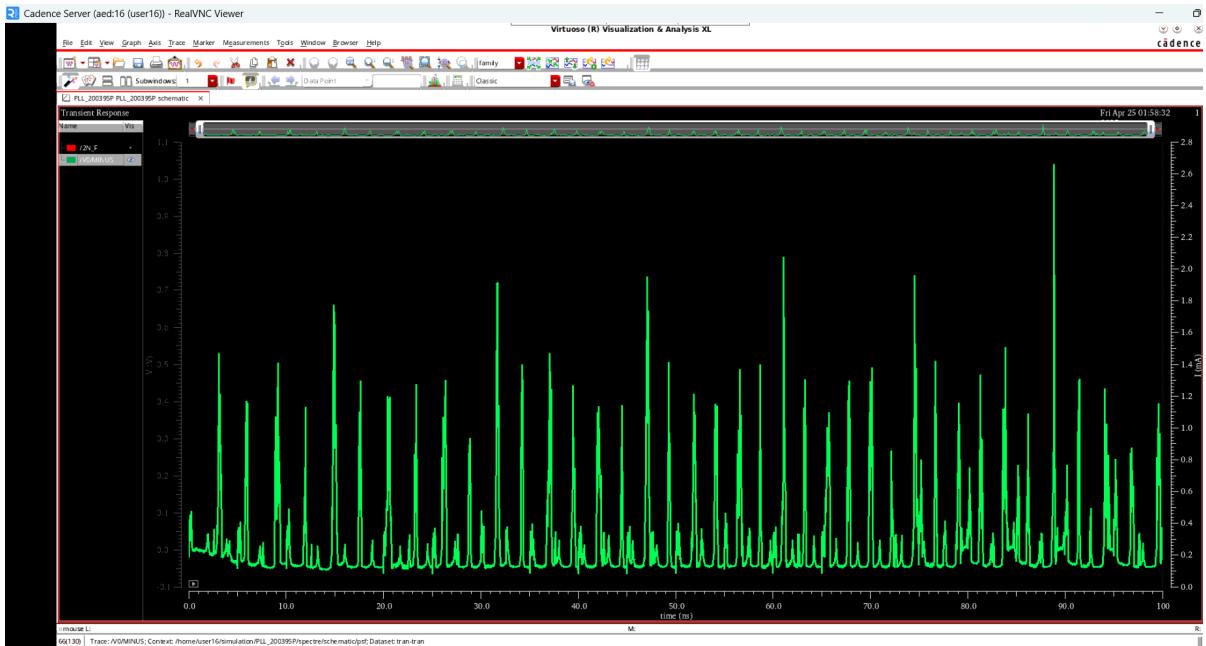


Figure 41: Total current variation of the PLL with a divider ratio of $N = 2$, showing an average current of approximately 255 μA .

For the divide-by-2 configuration, the average current is 255 μA , resulting in a dynamic power consumption of:

$$P_{\text{dynamic}} = V \times I_{\text{avg}} = 1 \text{ V} \times 255 \mu\text{A} = 255 \mu\text{W}.$$

8.1.2 Dynamic Power Consumption for Divide-by-16 Configuration

For the divide-by-16 configuration, the average current is 790 μA , resulting in a dynamic power consumption of:

$$P_{\text{dynamic}} = V \times I_{\text{avg}} = 1 \text{ V} \times 790 \mu\text{A} = 790 \mu\text{W}.$$

8.2 Static Power Consumption

In this PLL design, static power consumption is zero due to the absence of additional DC sources beyond the 1 V power supply.

8.3 Total Power Consumption

$$P_{\text{Total}} = P_{\text{dynamic}} + P_{\text{static}}$$

Since static power consumption is zero, the total power consumption equals the dynamic power consumption. For divider ratios $2 \leq N \leq 16$, the total power consumption ranges from:

$$255 \mu\text{W} \text{ to } 790 \mu\text{W},$$

9 Improvements for Fractional-N PLL Performance

1. **Phase Noise Reduction:** Use a high-Q VCO ($Q = 50\text{--}2000$) with low K_{VCO} (e.g., 2 MHz V^{-1}) to reduce the VCO noise contributions. By using a programmable loop filter, we can optimize the bandwidth (e.g., $f_{\text{REF}}/5$). These modifications help to improve phase noise by 10–20 dB [1].
2. **Faster Lock Time:** Employ a dual-mode loop filter (wide bandwidth during acquisition, narrow when locked). This is critical for cellular frequency hopping [2].
3. **Power Efficiency:** Optimize dividers and PFD in 45 nm CMOS, use power-gating, and adopt multi-loop designs (e.g., mix-and-count-down). This helps to reduce power by 20–30% [1].

References

- [1] C. Barrett, “Fractional/Integer-N PLL Basics,” Texas Instruments Technical Brief SWRA029, Aug. 1999.
- [2] N. Badiger and S. Iyer, “Design implementation of high speed and low power PLL using gpdk 45 nm technology,” *J. Inst. Eng. India Ser. B*, vol. 105, no. 3, pp. 1–10, Jan. 2024.

10 Appendices

10.1 Netlist for PFD-CP Based Integer-N Phase-Locked Loop Design

```
1 // Generated for: spectre
2 // Generated on: Apr 24 21:11:37 2025
3 // Design library name: PLL_200395P
4 // Design cell name: PLL_200395P
5 // Design view name: schematic
6 simulator lang=spectre
7 global 0
8 parameters R=1k VCO_N=1 VCO_WP=2u VCO_WN=1u VCO_LN=45n VCO_LP=45n C1=5p \
9     C2=1p
10 include "/home/aed/cadence/dicd_source/cadence_pdk/gpdk045_v_6_0/gpdk045/../../models/
11     spectre/gpdk045.scs" section=mc
12
13 // Library name: CHP_200395P
14 // Cell name: CHP_Updated_200395P
15 // View name: schematic
16 subckt CHP_Updated_200395P DN DNB ICP UP UPB VCON VDD VSS
17     PM8 (net57 net32 VDD VDD) g45p1svt w=(20u) l=120n nf=10 as=1.84p \
18         ad=1.6p ps=25.84u pd=21.6u nrd=4m nrs=4.6m sa=140n sb=140n sd=160n \
19         sca=47.43123 scb=0.04792 scc=0.00496 m=(1)
20     PM7 (net32 net32 VDD VDD) g45p1svt w=(20u) l=120n nf=10 as=1.84p \
21         ad=1.6p ps=25.84u pd=21.6u nrd=4m nrs=4.6m sa=140n sb=140n sd=160n \
22         sca=47.43123 scb=0.04792 scc=0.00496 m=(1)
23     PM6 (VCON ICP net59 VDD) g45p1svt w=(11u) l=200n nf=10 as=1.012p \
24         ad=880f ps=15.04u pd=12.6u nrd=7.27273m nrs=8.36364m sa=140n \
25         sb=140n sd=160n sca=53.73563 scb=0.04741 scc=0.00523 m=(1)
26     PM5 (net59 net28 VDD VDD) g45p1svt w=(11u) l=200n nf=10 as=1.012p \
27         ad=880f ps=15.04u pd=12.6u nrd=7.27273m nrs=8.36364m sa=140n \
28         sb=140n sd=160n sca=53.73563 scb=0.04741 scc=0.00523 m=(1)
29     PM4 (net28 ICP net62 VDD) g45p1svt w=(11u) l=200n nf=10 as=1.012p \
30         ad=880f ps=15.04u pd=12.6u nrd=7.27273m nrs=8.36364m sa=140n \
31         sb=140n sd=160n sca=53.73563 scb=0.04741 scc=0.00523 m=(1)
32     PM3 (ICP ICP VDD VDD) g45p1svt w=(4u) l=500n nf=1 as=560f ad=560f \
33         ps=8.28u pd=8.28u nrd=35m nrs=35m sa=140n sb=140n sd=160n \
34         sca=22.49589 scb=0.02034 scc=0.00174 m=(1)
35     PM2 (net62 net28 VDD VDD) g45p1svt w=(11u) l=200n nf=10 as=1.012p \
36         ad=880f ps=15.04u pd=12.6u nrd=7.27273m nrs=8.36364m sa=140n \
37         sb=140n sd=160n sca=53.73563 scb=0.04741 scc=0.00523 m=(1)
38     PM1 (net28 net22 VDD VDD) g45p1svt w=(500n) l=200n nf=1 as=70f ad=70f \
39         ps=1.28u pd=1.28u nrd=280m nrs=280m sa=140n sb=140n sd=160n \
40         sca=84.52381 scb=0.06559 scc=0.00884 m=(1)
41     PM0 (net22 net22 VDD VDD) g45p1svt w=(500n) l=200n nf=1 as=70f ad=70f \
42         ps=1.28u pd=1.28u nrd=280m nrs=280m sa=140n sb=140n sd=160n \
43         sca=84.52381 scb=0.06559 scc=0.00884 m=(1)
44     NM11 (ICP ICP VSS VSS) g45n1svt w=(2u) l=200n nf=1 as=280f ad=280f \
```

```

45      ps=4.28u pd=4.28u nrd=70m nrs=70m sa=140n sb=140n sd=160n \
46      sca=41.18123 scb=0.04022 scc=0.00387 m=(1)
47  NM10 (ICP ICP VSS VSS) g45n1svt w=(2u) l=200n nf=1 as=280f ad=280f \
48      ps=4.28u pd=4.28u nrd=70m nrs=70m sa=140n sb=140n sd=160n \
49      sca=41.18123 scb=0.04022 scc=0.00387 m=(1)
50  NM9 (net60 net57 VSS VSS) g45n1svt w=(10u) l=200n nf=10 as=920f \
51      ad=800f ps=13.84u pd=11.6u nrd=8m nrs=9.2m sa=140n sb=140n sd=160n \
52      sca=56.44654 scb=0.04900 scc=0.00553 m=(1)
53  NM8 (VCON ICP net60 VSS) g45n1svt w=(10u) l=200n nf=10 as=920f ad=800f \
54      ps=13.84u pd=11.6u nrd=8m nrs=9.2m sa=140n sb=140n sd=160n \
55      sca=56.44654 scb=0.04900 scc=0.00553 m=(1)
56  NM7 (net61 net57 VSS VSS) g45n1svt w=(10u) l=200n nf=10 as=920f \
57      ad=800f ps=13.84u pd=11.6u nrd=8m nrs=9.2m sa=140n sb=140n sd=160n \
58      sca=56.44654 scb=0.04900 scc=0.00553 m=(1)
59  NM6 (net57 ICP net61 VSS) g45n1svt w=(10u) l=200n nf=10 as=920f \
60      ad=800f ps=13.84u pd=11.6u nrd=8m nrs=9.2m sa=140n sb=140n sd=160n \
61      sca=56.44654 scb=0.04900 scc=0.00553 m=(1)
62  NM5 (net33 ICP VSS VSS) g45n1svt w=(2u) l=120n nf=1 as=280f ad=280f \
63      ps=4.28u pd=4.28u nrd=70m nrs=70m sa=140n sb=140n sd=160n \
64      sca=47.43123 scb=0.04792 scc=0.00496 m=(1)
65  NM4 (net57 DNB net33 VSS) g45n1svt w=(20u) l=120n nf=10 as=1.84p \
66      ad=1.6p ps=25.84u pd=21.6u nrd=4m nrs=4.6m sa=140n sb=140n sd=160n \
67      sca=47.43123 scb=0.04792 scc=0.00496 m=(1)
68  NM3 (net32 DN net33 VSS) g45n1svt w=(20u) l=120n nf=10 as=1.84p \
69      ad=1.6p ps=25.84u pd=21.6u nrd=4m nrs=4.6m sa=140n sb=140n sd=160n \
70      sca=47.43123 scb=0.04792 scc=0.00496 m=(1)
71  NM2 (net24 ICP VSS VSS) g45n1svt w=(2u) l=200n nf=1 as=280f ad=280f \
72      ps=4.28u pd=4.28u nrd=70m nrs=70m sa=140n sb=140n sd=160n \
73      sca=41.18123 scb=0.04022 scc=0.00387 m=(1)
74  NM1 (net28 UP net24 VSS) g45n1svt w=(20u) l=120n nf=10 as=1.84p \
75      ad=1.6p ps=25.84u pd=21.6u nrd=4m nrs=4.6m sa=140n sb=140n sd=160n \
76      sca=47.43123 scb=0.04792 scc=0.00496 m=(1)
77  NM0 (net22 UPB net24 VSS) g45n1svt w=(20u) l=120n nf=10 as=1.84p \
78      ad=1.6p ps=25.84u pd=21.6u nrd=4m nrs=4.6m sa=140n sb=140n sd=160n \
79      sca=47.43123 scb=0.04792 scc=0.00496 m=(1)
80  R0 (VCON net054) resistor r=R
81  C1 (VCON VSS) capacitor c=C2
82  C0 (net054 VSS) capacitor c=C1
83 ends CHP_Updated_200395P
84 // End of subcircuit definition.
85
86 // Library name: PFD_200395P
87 // Cell name: NAND_200395P
88 // View name: schematic
89 subckt NAND_200395P A B VDD VOUT
90      PM1 (VOUT B VDD VDD) g45p1svt w=(2u) l=45n nf=1 as=280f ad=280f \
91      ps=4.28u pd=4.28u nrd=70m nrs=70m sa=140n sb=140n sd=160n \
92      sca=56.99756 scb=0.05691 scc=0.00695 m=(1)
93      PM0 (VOUT A VDD VDD) g45p1svt w=(2u) l=45n nf=1 as=280f ad=280f \
94      ps=4.28u pd=4.28u nrd=70m nrs=70m sa=140n sb=140n sd=160n \

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95      sca=56.99756 scb=0.05691 scc=0.00695 m=(1)
96      NM1 (net21 A 0 0) g45n1svt w=(1u) l=45n nf=1 as=140f ad=140f ps=2.28u \
97          pd=2.28u nrd=140m nrs=140m sa=140n sb=140n sd=160n sca=72.26287 \
98          scb=0.06569 scc=0.00861 m=(1)
99      NM0 (VOUT B net21 0) g45n1svt w=(1u) l=45n nf=1 as=140f ad=140f \
100         ps=2.28u pd=2.28u nrd=140m nrs=140m sa=140n sb=140n sd=160n \
101         sca=72.26287 scb=0.06569 scc=0.00861 m=(1)
102  ends NAND_200395P
103 // End of subcircuit definition.
104
105 // Library name: PFD_200395P
106 // Cell name: NAND3_20095P
107 // View name: schematic
108 subckt NAND3_20095P A B C VDD VOUT
109     NM2 (net11 C 0 net8) g45n1svt w=(1u) l=45n nf=1 as=140f ad=140f \
110         ps=2.28u pd=2.28u nrd=140m nrs=140m sa=140n sb=140n sd=160n \
111         sca=72.26287 scb=0.06569 scc=0.00861 m=(1)
112     NM1 (net12 B net11 net8) g45n1svt w=(1u) l=45n nf=1 as=140f ad=140f \
113         ps=2.28u pd=2.28u nrd=140m nrs=140m sa=140n sb=140n sd=160n \
114         sca=72.26287 scb=0.06569 scc=0.00861 m=(1)
115     NM0 (VOUT A net12 net8) g45n1svt w=(1u) l=45n nf=1 as=140f ad=140f \
116         ps=2.28u pd=2.28u nrd=140m nrs=140m sa=140n sb=140n sd=160n \
117         sca=72.26287 scb=0.06569 scc=0.00861 m=(1)
118     PM2 (VOUT C VDD VDD) g45p1svt w=(2u) l=45n nf=1 as=280f ad=280f \
119         ps=4.28u pd=4.28u nrd=70m nrs=70m sa=140n sb=140n sd=160n \
120         sca=56.99756 scb=0.05691 scc=0.00695 m=(1)
121     PM1 (VOUT B VDD VDD) g45p1svt w=(2u) l=45n nf=1 as=280f ad=280f \
122         ps=4.28u pd=4.28u nrd=70m nrs=70m sa=140n sb=140n sd=160n \
123         sca=56.99756 scb=0.05691 scc=0.00695 m=(1)
124     PM0 (VOUT A VDD VDD) g45p1svt w=(2u) l=45n nf=1 as=280f ad=280f \
125         ps=4.28u pd=4.28u nrd=70m nrs=70m sa=140n sb=140n sd=160n \
126         sca=56.99756 scb=0.05691 scc=0.00695 m=(1)
127  ends NAND3_20095P
128 // End of subcircuit definition.
129
130 // Library name: PFD_200395P
131 // Cell name: Inverter_200395P
132 // View name: schematic
133 subckt Inverter_200395P INPUT OUTPUT VDD VSS
134     PM0 (OUTPUT INPUT VDD VDD) g45p1svt w=(2u) l=45n nf=1 as=280f ad=280f \
135         ps=4.28u pd=4.28u nrd=70m nrs=70m sa=140n sb=140n sd=160n \
136         sca=56.99756 scb=0.05691 scc=0.00695 m=(1)
137     NM0 (OUTPUT INPUT VSS VSS) g45n1svt w=(1u) l=45n nf=1 as=140f ad=140f \
138         ps=2.28u pd=2.28u nrd=140m nrs=140m sa=140n sb=140n sd=160n \
139         sca=72.26287 scb=0.06569 scc=0.00861 m=(1)
140  ends Inverter_200395P
141 // End of subcircuit definition.
142
143 // Library name: PFD_200395P
144 // Cell name: PFD_New_200395P

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145 // View name: schematic
146 subckt PFD_New_200395P DN DNB Ffeed Fref UP UPB VDD VSS
147     I10 (net42 net41 VDD net29) NAND_200395P
148     I9 (net27 net27 VDD net41) NAND_200395P
149     I8 (net28 net28 VDD net42) NAND_200395P
150     I7 (net38 net25 VDD net27) NAND_200395P
151     I6 (net22 net23 VDD net28) NAND_200395P
152     I5 (net46 DNB VDD net25) NAND_200395P
153     I4 (net37 net25 VDD net38) NAND_200395P
154     I3 (net29 net38 VDD net37) NAND_200395P
155     I2 (net23 net29 VDD net39) NAND_200395P
156     I1 (net22 net39 VDD net23) NAND_200395P
157     I0 (UPB net48 VDD net22) NAND_200395P
158     I12 (net29 net38 net25 VDD DNB) NAND3_20095P
159     I11 (net22 net23 net29 VDD UPB) NAND3_20095P
160     I17 (DNB DN VDD VSS) Inverter_200395P
161     I16 (UPB UP VDD VSS) Inverter_200395P
162     I14 (Ffeed net46 VDD VSS) Inverter_200395P
163     I13 (Fref net48 VDD VSS) Inverter_200395P
164 ends PFD_New_200395P
165 // End of subcircuit definition.

166
167 // Library name: VCO_200395P
168 // Cell name: RngVCO_200395P
169 // View name: schematic
170 subckt RngVCO_200395P VCON VCO_OUT VDD VSS
171     NM0 (net7 VCON VSS VSS) g45n1svt w=((VCO_WN) * (VCO_N)) l=VCO_LN \
172         nf=VCO_N as=((VCO_WN) < 119.5n) ? (((50n > (((60n) - 0) + 60n) ? 50n : (((60n)
173             - 0) + 60n)) * 120n) + ((VCO_WN) * 50n)) + (floor(((VCO_N) - 1) / 2.0) *
174             (((((60n) - 0) + 60n) * 120n) + ((VCO_WN) * 100n))) + (((VCO_N) / 2) -
175             floor((VCO_N) / 2) == 0) ? (((50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0)
176                 + 60n)) * 120n) + ((VCO_WN) * 50n)) : 0)) / 1 : (((100n > (((60n) - 0) + 80
177                 n) ? 100n : (((60n) - 0) + 80n)) * (VCO_WN)) + (floor(((VCO_N) - 1) / 2.0) *
178                 ((60n > (((60n) - 0) + 50n) ? 60n : (((60n) - 0) + 50n)) * (VCO_WN))) +
179                 (((VCO_N) / 2) - floor((VCO_N) / 2) == 0) ? ((100n > (((60n) - 0) + 80n) ?
180                     100n : (((60n) - 0) + 80n)) * (VCO_WN)) : 0)) / 1 \
181             ad=((VCO_WN) < 119.5n) ? ((floor((VCO_N) / 2.0) * (((60n) - 0) + 60n) * 120n
182                 ) + ((VCO_WN) * 100n)) + (((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ?
183                 (((50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) * 120n) + ((VCO_WN) * 50n)) : 0)) / 1 : (((floor((VCO_N) / 2.0) * ((60n > (((60n) - 0) + 50n) ? 60n : (((60n) - 0) + 50n)) * (VCO_WN))) + (((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ? ((100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n)) * (VCO_WN)) : 0)) / 1 \
184             ps=((VCO_WN) < 119.5n) ? (((2 * (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n))) + 340n) + (floor(((VCO_N) - 1) / 2.0) * ((2 * (((60n) - 0) + 60n)) + 440n)) + (((VCO_N) / 2) - floor((VCO_N) / 2) == 0) ? ((2 * (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n))) + 340n) : 0)) / 1 : (((2 * (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))) + (2 * (VCO_WN))) + (floor(((VCO_N) - 1) / 2.0) * ((2 * (60n > (((60n) - 0) + 50n) ? 60n : (((60n) - 0) + 50n))) + (2 * (VCO_WN)))) + (((VCO_N) / 2) - floor((VCO_N) / 2))
```

```

) / 2) == 0) ? ((2 * (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80
n))) + (2 * (VCO_WN))) : 0)) / 1 \
175 pd=((VCO_WN) < 119.5n) ? ((floor((VCO_N) / 2.0) * ((2 * (((60n) - 0) + 60n)) +
440n)) + (((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ? ((2 * (50n > (((60n)
- 0) + 60n) ? 50n : (((60n) - 0) + 60n))) + 340n) : 0)) / 1 : ((floor(((
VCO_N) / 2.0) * ((2 * (60n > (((60n) - 0) + 50n) ? 60n : (((60n) - 0) + 50n
)))) + (2 * (VCO_WN)))) + (((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ? ((2 *
(100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))) + (2 * (VCO_WN)
)) : 0)) / 1 \
176 nrd=((VCO_WN) < 119.5n) ? ((floor((VCO_N) / 2.0) * (((((60n) - 0) + 60n) * 120
n) + ((VCO_WN) * 100n))) + (((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ?
(((50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) * 120n) + (((
VCO_WN) * 50n)) : 0)) / 1 : ((floor((VCO_N) / 2.0) * ((60n > (((60n) - 0) +
50n) ? 60n : (((60n) - 0) + 50n)) * (VCO_WN))) + (((VCO_N) / 2) - floor(((
VCO_N) / 2) != 0) ? ((100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80
n)) * (VCO_WN)) : 0)) / 1 / ((VCO_WN) * (VCO_N) * (VCO_WN) * (VCO_N)) \
177 nrs=((VCO_WN) < 119.5n) ? (((((50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) +
60n)) * 120n) + ((VCO_WN) * 50n)) + (floor(((VCO_N) - 1) / 2.0) * (((((60n
) - 0) + 60n) * 120n) + ((VCO_WN) * 100n))) + (((VCO_N) / 2) - floor(((
VCO_N) / 2) == 0) ? (((50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n
)) * 120n) + ((VCO_WN) * 50n)) : 0)) / 1 : (((100n > (((60n) - 0) + 80n) ?
100n : (((60n) - 0) + 80n)) * (VCO_WN)) + (floor(((VCO_N) - 1) / 2.0) *
((60n > (((60n) - 0) + 50n) ? 60n : (((60n) - 0) + 50n)) * (VCO_WN))) +
(((VCO_N) / 2) - floor((VCO_N) / 2) == 0) ? ((100n > (((60n) - 0) + 80n) ?
100n : (((60n) - 0) + 80n)) * (VCO_WN)) : 0)) / 1 / ((VCO_WN) * (VCO_N) *
(VCO_WN) * (VCO_N)) \
178 sa=((VCO_WN) < 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n
)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n)) \
179 sb=((VCO_WN) < 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n
)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n)) \
180 sd=((VCO_WN) < 119.5n) ? (((60n) - 0) + 60n) + (2*5e-08) : (60n > (((60n) - 0)
+ 50n) ? 60n : (((60n) - 0) + 50n)) \
181 sca=(( (VCO_WN) * ( (((1u) * (1u) / (((VCO_WN) < 119.5n) ? (50n > (((60n) - 0)
+ 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n)
? 100n : (((60n) - 0) + 80n))+60n)) - ((1u) * (1u) / (((VCO_WN) < 119.5n)
? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n >
((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)+VCO_LN))) + ((1u) *
(1u) / (((VCO_WN) < 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) -
0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) +
80n))+60n)) - ((1u) * (1u) / (((VCO_WN) < 119.5n) ? (50n > (((60n) - 0) +
60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ?
100n : (((60n) - 0) + 80n))+60n)+VCO_LN))) + ( VCO_LN * ( (((1u) * (1u) /
(60n)) - ((1u) * (1u) / ((60n)+(VCO_WN)))) + ((1u) * (1u) / (60n)) - ((1u)
* (1u) / ((60n)+(VCO_WN)))))) / ((VCO_WN) * VCO_LN) \
182 scb=(((VCO_WN) * (((VCO_WN) < 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n :
(((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n)
- 0) + 80n))+60n)/10 + (1u)/100)*exp(-10 * (((VCO_WN) < 119.5n) ? (50n >
((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n)
- 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n) / (1u)) - (((VCO_WN) <
119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 :

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(100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)+VCO_LN)/10
+ (1u)/100)*exp(-10 * (((VCO_WN) < 119.5n) ? (50n > (((60n) - 0) + 60n) ?
50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n :
(((60n) - 0) + 80n))+60n)+VCO_LN) / (1u)) + (((VCO_WN) < 119.5n) ? (50n >
(((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n)
- 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)/10 + (1u)/100)*exp(-10 * (((VCO_WN)
< 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n))
+ 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n) /
(1u)) - (((VCO_WN) < 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n)
- 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0)
+ 80n))+60n)+VCO_LN)/10 + (1u)/100)*exp(-10 * (((VCO_WN) < 119.5n) ? (50n
> (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n)
- 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)+VCO_LN) / (1u)))) + (
VCO_LN * (((60n)/10 + (1u)/100)*exp(-10 * (60n) / (1u)) - (((60n)+(VCO_WN))
/10 + (1u)/100)*exp(-10 * ((60n)+(VCO_WN)) / (1u)) + ((60n)/10 + (1u)/100)*
exp(-10 * (60n) / (1u)) - (((60n)+(VCO_WN))/10 + (1u)/100)*exp(-10 * ((60n)
+(VCO_WN)) / (1u)))) / ((VCO_WN) * VCO_LN) \
scc=(((VCO_WN) * (((VCO_WN) < 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n :
(((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n)
- 0) + 80n))+60n)/20 + (1u)/400)*exp(-20 * (((VCO_WN) < 119.5n) ? (50n >
(((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n)
- 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n) / (1u)) - (((VCO_WN) <
119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 :
(100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)+VCO_LN) /20
+ (1u)/400)*exp(-20 * (((VCO_WN) < 119.5n) ? (50n > (((60n) - 0) + 60n) ?
50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n :
(((60n) - 0) + 80n))+60n)+VCO_LN) / (1u)) + (((VCO_WN) < 119.5n) ? (50n >
(((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n)
- 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)/20 + (1u)/400)*exp(-20 * (((VCO_WN)
< 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) +
5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n) /
(1u)) - (((VCO_WN) < 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n)
- 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0)
+ 80n))+60n)+VCO_LN) /20 + (1u)/400)*exp(-20 * (((VCO_WN) < 119.5n) ? (50n
> (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n)
- 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)+VCO_LN) / (1u)))) + (
VCO_LN * (((60n)/20 + (1u)/400)*exp(-20 * (60n) / (1u)) - (((60n)+(VCO_WN))
/20 + (1u)/400)*exp(-20 * ((60n)+(VCO_WN)) / (1u)) + ((60n)/20 + (1u)/400)*
exp(-20 * (60n) / (1u)) - (((60n)+(VCO_WN))/20 + (1u)/400)*exp(-20 * ((60n)
+(VCO_WN)) / (1u)))) / ((VCO_WN) * VCO_LN) \
m=(1)
NM1 (net23 VCON VSS VSS) g45n1svt w=((VCO_WN) * (VCO_N)) l=VCO_LN \
184
185 nf=VCO_N as=((VCO_WN) < 119.5n) ? (((50n > (((60n) - 0) + 60n) ? 50n : (((60n)
- 0) + 60n)) * 120n) + ((VCO_WN) * 50n)) + (floor(((VCO_N) - 1) / 2.0) *
186 (((60n) - 0) + 60n) * 120n) + ((VCO_WN) * 100n)) + (((VCO_N) / 2) -
floor((VCO_N) / 2) == 0) ? (((50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0)
+ 60n)) * 120n) + ((VCO_WN) * 50n)) : 0)) / 1 : (((100n > (((60n) - 0) + 80
n) ? 100n : (((60n) - 0) + 80n)) * (VCO_WN)) + (floor(((VCO_N) - 1) / 2.0) *
((60n > (((60n) - 0) + 50n) ? 60n : (((60n) - 0) + 50n)) * (VCO_WN))) +
(((VCO_N) / 2) - floor((VCO_N) / 2) == 0) ? ((100n > (((60n) - 0) + 80n) ?

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100n : (((60n - 0) + 80n)) * (VCO_WN)) : 0)) / 1 \
187 ad=((VCO_WN) < 119.5n) ? ((floor((VCO_N) / 2.0) * (((((60n - 0) + 60n) * 120n
) + ((VCO_WN) * 100n))) + (((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ?
((50n > (((60n - 0) + 60n) ? 50n : (((60n - 0) + 60n) * 120n) + ((VCO_WN) * 50n)) : 0)) / 1 : ((floor((VCO_N) / 2.0) * ((60n > (((60n - 0) + 50n) ? 60n : (((60n - 0) + 50n) * (VCO_WN))) + (((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ? ((100n > (((60n - 0) + 80n) ? 100n : (((60n - 0) + 80n)) * (VCO_WN)) : 0)) / 1 \
188 ps=((VCO_WN) < 119.5n) ? (((2 * (50n > (((60n - 0) + 60n) ? 50n : (((60n - 0) + 60n))) + 340n) + (floor(((VCO_N) - 1) / 2.0) * ((2 * (((60n - 0) + 60n)) + 440n)) + (((VCO_N) / 2) - floor((VCO_N) / 2) == 0) ? ((2 * (50n > (((60n - 0) + 60n) ? 50n : (((60n - 0) + 60n)) + 340n)) : 0)) / 1 : (((2 * (100n > (((60n - 0) + 80n) ? 100n : (((60n - 0) + 80n))) + (2 * (VCO_WN))) + (floor(((VCO_N) - 1) / 2.0) * ((2 * (60n > (((60n - 0) + 50n) ? 60n : (((60n - 0) + 50n)) + (2 * (VCO_WN)))) + (((VCO_N) / 2) - floor((VCO_N) / 2) == 0) ? ((2 * (100n > (((60n - 0) + 80n) ? 100n : (((60n - 0) + 80n))) + (2 * (VCO_WN))) : 0)) / 1 \
189 pd=((VCO_WN) < 119.5n) ? ((floor((VCO_N) / 2.0) * ((2 * (((60n - 0) + 60n) + 440n)) + (((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ? ((2 * (50n > (((60n - 0) + 60n) ? 50n : (((60n - 0) + 60n)) + 340n)) : 0)) / 1 : ((floor((VCO_N) / 2.0) * ((2 * (60n > (((60n - 0) + 50n) ? 60n : (((60n - 0) + 50n)) + (2 * (VCO_WN)))) + (((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ? ((2 * (100n > (((60n - 0) + 80n) ? 100n : (((60n - 0) + 80n))) + (2 * (VCO_WN))) : 0)) / 1 \
190 nrd=((VCO_WN) < 119.5n) ? ((floor((VCO_N) / 2.0) * (((((60n - 0) + 60n) * 120n) + ((VCO_WN) * 100n))) + (((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ? ((50n > (((60n - 0) + 60n) ? 50n : (((60n - 0) + 60n)) * 120n) + ((VCO_WN) * 50n)) : 0)) / 1 : ((floor((VCO_N) / 2.0) * ((60n > (((60n - 0) + 50n) ? 60n : (((60n - 0) + 50n)) * (VCO_WN))) + (((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ? ((100n > (((60n - 0) + 80n) ? 100n : (((60n - 0) + 80n)) * (VCO_WN)) : 0)) / 1 / ((VCO_WN) * (VCO_N) * (VCO_WN) * (VCO_N)) \
191 nrs=((VCO_WN) < 119.5n) ? (((50n > (((60n - 0) + 60n) ? 50n : (((60n - 0) + 60n)) * 120n) + ((VCO_WN) * 50n)) + (floor(((VCO_N) - 1) / 2.0) * (((((60n - 0) + 60n) * 120n) + ((VCO_WN) * 100n))) + (((VCO_N) / 2) - floor((VCO_N) / 2) == 0) ? (((50n > (((60n - 0) + 60n) ? 50n : (((60n - 0) + 60n)) * 120n) + ((VCO_WN) * 50n)) : 0)) / 1 : (((100n > (((60n - 0) + 80n) ? 100n : (((60n - 0) + 80n)) * (VCO_WN)) + (floor(((VCO_N) - 1) / 2.0) * ((60n > (((60n - 0) + 50n) ? 60n : (((60n - 0) + 50n)) * (VCO_WN))) + (((VCO_N) / 2) - floor((VCO_N) / 2) == 0) ? ((100n > (((60n - 0) + 80n) ? 100n : (((60n - 0) + 80n)) * (VCO_WN)) : 0)) / 1 / ((VCO_WN) * (VCO_N) * (VCO_WN) * (VCO_N)) \
192 sa=((VCO_WN) < 119.5n) ? (50n > (((60n - 0) + 60n) ? 50n : (((60n - 0) + 60n)) + 5e-08 : (100n > (((60n - 0) + 80n) ? 100n : (((60n - 0) + 80n))) \
193 sb=((VCO_WN) < 119.5n) ? (50n > (((60n - 0) + 60n) ? 50n : (((60n - 0) + 60n)) + 5e-08 : (100n > (((60n - 0) + 80n) ? 100n : (((60n - 0) + 80n))) \
194 sd=((VCO_WN) < 119.5n) ? (((60n - 0) + 60n) + (2*5e-08) : (60n > (((60n - 0) + 50n) ? 60n : (((60n - 0) + 50n))) \
195 sca=(( (VCO_WN) * ( ((1u) * (1u) / (((VCO_WN) < 119.5n) ? (50n > (((60n - 0) + 60n) ? 50n : (((60n - 0) + 60n)) + 5e-08 : (100n > (((60n - 0) + 80n) ? 100n : (((60n - 0) + 80n))+60n)) - ((1u) * (1u) / (((VCO_WN) < 119.5n)

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198 ) - 0) + 80n) ? 100n : (((60n) - 0) + 80n)) + 60n) + VCO_LN) / (1u))) + (
VCO_LN * (((60n)/20 + (1u)/400)*exp(-20 * (60n) / (1u)) - (((60n)+(VCO_WN))
/20 + (1u)/400)*exp(-20 * ((60n)+(VCO_WN)) / (1u)) + ((60n)/20 + (1u)/400)*
exp(-20 * (60n) / (1u)) - (((60n)+(VCO_WN))/20 + (1u)/400)*exp(-20 * ((60n)
+(VCO_WN)) / (1u)))) / ((VCO_WN) * VCO_LN) \
m=(1)
200 NM2 (net22 VCON VSS VSS) g45n1svt w=((VCO_WN) * (VCO_N)) l=VCO_LN \
201 nf=VCO_N as=((VCO_WN) < 119.5n) ? (((50n > (((60n) - 0) + 60n) ? 50n : (((60n)
- 0) + 60n)) * 120n) + ((VCO_WN) * 50n)) + (floor(((VCO_N) - 1) / 2.0) *
(((60n) - 0) + 60n) * 120n) + ((VCO_WN) * 100n)) + (((((VCO_N) / 2) -
floor((VCO_N) / 2) == 0) ? ((50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0)
+ 60n)) * 120n) + ((VCO_WN) * 50n)) : 0)) / 1 : (((100n > (((60n) - 0) + 80
n) ? 100n : (((60n) - 0) + 80n)) * (VCO_WN)) + (floor(((VCO_N) - 1) / 2.0) *
(60n > (((60n) - 0) + 50n) ? 60n : (((60n) - 0) + 50n)) * (VCO_WN))) +
(((VCO_N) / 2) - floor((VCO_N) / 2) == 0) ? ((100n > (((60n) - 0) + 80n) ?
100n : (((60n) - 0) + 80n)) * (VCO_WN)) : 0)) / 1 \
ad=((VCO_WN) < 119.5n) ? ((floor((VCO_N) / 2.0) * (((((60n) - 0) + 60n) * 120n
) + ((VCO_WN) * 100n))) + (((((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ?
((50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) * 120n) + ((VCO_WN)
* 50n)) : 0)) / 1 : ((floor((VCO_N) / 2.0) * ((60n > (((60n) - 0) + 50n) ?
60n : (((60n) - 0) + 50n)) * (VCO_WN))) + (((((VCO_N) / 2) - floor((VCO_N)
/ 2) != 0) ? ((100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80
n)) * (VCO_WN)) : 0)) / 1 \
202 ps=((VCO_WN) < 119.5n) ? (((2 * (50n > (((60n) - 0) + 60n) ? 50n : (((60n) -
0) + 60n))) + 340n) + (floor(((VCO_N) - 1) / 2.0) * ((2 * (((60n) - 0) + 60
n)) + 440n)) + (((((VCO_N) / 2) - floor((VCO_N) / 2) == 0) ? ((2 * (50n >
((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 340n) : 0)) / 1 : (((2 *
(100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))) + (2 * (VCO_WN))
) + (floor(((VCO_N) - 1) / 2.0) * ((2 * (60n > (((60n) - 0) + 50n) ? 60n :
(((60n) - 0) + 50n))) + (2 * (VCO_WN)))) + (((((VCO_N) / 2) - floor((VCO_N)
/ 2) == 0) ? ((2 * (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80
n))) + (2 * (VCO_WN))) : 0)) / 1 \
pd=((VCO_WN) < 119.5n) ? ((floor((VCO_N) / 2.0) * ((2 * (((60n) - 0) + 60n)) +
440n)) + (((((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ? ((2 * (50n > (((60n)
- 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 340n) : 0)) / 1 : ((floor((VCO_N)
/ 2.0) * ((2 * (60n > (((60n) - 0) + 50n) ? 60n : (((60n) - 0) + 50n)))
+ (2 * (VCO_WN)))) + (((((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ? ((2 *
(100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))) + (2 * (VCO_WN))
) : 0)) / 1 \
203 nrd=((VCO_WN) < 119.5n) ? ((floor((VCO_N) / 2.0) * (((((60n) - 0) + 60n) * 120
n) + ((VCO_WN) * 100n))) + (((((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ?
((50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) * 120n) + ((VCO_WN)
* 50n)) : 0)) / 1 : ((floor((VCO_N) / 2.0) * ((60n > (((60n) - 0) + 50n) ?
60n : (((60n) - 0) + 50n)) * (VCO_WN))) + (((((VCO_N) / 2) - floor((VCO_N)
/ 2) != 0) ? ((100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80
n)) * (VCO_WN)) : 0)) / 1 / ((VCO_WN) * (VCO_N) * (VCO_WN) * (VCO_N)) \
204 nrs=((VCO_WN) < 119.5n) ? (((50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) +
60n)) * 120n) + ((VCO_WN) * 50n)) + (floor(((VCO_N) - 1) / 2.0) * (((((60n)
- 0) + 60n) * 120n) + ((VCO_WN) * 100n))) + (((((VCO_N) / 2) - floor((VCO_N)
/ 2) == 0) ? ((50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) *

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)) * 120n) + (((VCO_WN) * 50n)) : 0)) / 1 : (((100n > (((60n) - 0) + 80n) ?
100n : (((60n) - 0) + 80n)) * (VCO_WN)) + (floor(((VCO_N) - 1) / 2.0) *
((60n > (((60n) - 0) + 50n) ? 60n : (((60n) - 0) + 50n)) * (VCO_WN))) +
(((VCO_N) / 2) - floor((VCO_N) / 2) == 0) ? ((100n > (((60n) - 0) + 80n) ?
100n : (((60n) - 0) + 80n)) * (VCO_WN)) : 0)) / 1 / ((VCO_WN) * (VCO_N) *
(VCO_WN) * (VCO_N)) \
206 sa=((VCO_WN) < 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)
)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n)) \
207 sb=((VCO_WN) < 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)
)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n)) \
208 sd=((VCO_WN) < 119.5n) ? (((60n) - 0) + 60n) + (2*5e-08) : (60n > (((60n) - 0)
+ 50n) ? 60n : (((60n) - 0) + 50n)) \
209 sca=(( (VCO_WN) * ( (((1u) * (1u) / (((VCO_WN) < 119.5n) ? (50n > (((60n) - 0)
+ 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n)
? 100n : (((60n) - 0) + 80n))+60n)) - ((1u) * (1u) / (((VCO_WN) < 119.5n)
? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n >
(((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)+VCO_LN))) + ((1u) *
(1u) / (((VCO_WN) < 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) -
0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) +
80n))+60n)) - ((1u) * (1u) / (((VCO_WN) < 119.5n) ? (50n > (((60n) - 0) +
60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ?
100n : (((60n) - 0) + 80n))+60n)+VCO_LN))) + ( VCO_LN * ( (((1u) * (1u) /
(60n)) - ((1u) * (1u) / ((60n)+(VCO_WN)))) + ((1u) * (1u) / (60n)) - ((1u)
* (1u)/ ((60n)+(VCO_WN)))))) / ((VCO_WN) * VCO_LN) \
210 scb=(((VCO_WN) * (((VCO_WN) < 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n :
(((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) -
0) + 80n))+60n)/10 + (1u)/100)*exp(-10 * (((VCO_WN) < 119.5n) ? (50n >
(((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n) -
0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n) / (1u)) - (((VCO_WN) <
119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 :
(100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)+VCO_LN)/10
+ (1u)/100)*exp(-10 * (((VCO_WN) < 119.5n) ? (50n > (((60n) - 0) + 60n) ?
50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n :
(((60n) - 0) + 80n))+60n)+VCO_LN) / (1u)) + (((VCO_WN) < 119.5n) ? (50n >
(((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n) -
0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n) / (1u)) - (((VCO_WN) <
119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 :
(100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)+VCO_LN) / (1u))
+ (((VCO_WN) < 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) +
60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)
/ (1u)) - (((VCO_WN) < 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) -
0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) +
80n))+60n)+VCO_LN) / (1u) + (1u)/100)*exp(-10 * (((VCO_WN) < 119.5n) ? (50n >
(((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n) -
0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)+VCO_LN) / (1u)) + ((1u) / 100) *
exp(-10 * (60n) / (1u)) - (((60n)+(VCO_WN))/10 + (1u)/100)*exp(-10 * ((60n) +
(VCO_WN)) / (1u)))) / ((VCO_WN) * VCO_LN) \
211 scc=(((VCO_WN) * (((VCO_WN) < 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n :
(((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) -
0) + 80n))+60n)/20 + (1u)/400)*exp(-20 * (((VCO_WN) < 119.5n) ? (50n >
(((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) -
0) + 80n))+60n) / (1u)) - (((60n)+(VCO_WN))/10 + (1u)/100)*exp(-10 * ((60n) +
(VCO_WN)) / (1u)))) / ((VCO_WN) * VCO_LN) \

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(((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n)
- 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n) / (1u)) - (((((VCO_WN) <
119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 :
(100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)+VCO_LN)/20
+ (1u)/400)*exp(-20 * (((VCO_WN) < 119.5n) ? (50n > (((60n) - 0) + 60n) ?
50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n :
(((60n) - 0) + 80n))+60n)+VCO_LN) / (1u)) + (((((VCO_WN) < 119.5n) ? (50n >
(((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n)
- 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)/20 + (1u)/400)*exp(-20 * (((VCO_WN) < 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n) / (1u)) - (((((VCO_WN) < 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)+VCO_LN)/20 + (1u)/400)*exp(-20 * (((VCO_WN) < 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)+VCO_LN) / (1u))) + (((((60n)/20 + (1u)/400)*exp(-20 * (60n) / (1u)) - (((60n)+(VCO_WN))/20 + (1u)/400)*exp(-20 * ((60n)+(VCO_WN))/20 + (1u)/400)*exp(-20 * (60n) / (1u)) - (((60n)+(VCO_WN))/20 + (1u)/400)*exp(-20 * ((60n)+(VCO_WN)) / (1u)))) / ((VCO_WN) * VCO_LN) \
m=(1)
NM3 (net21 VCON VSS VSS) g45n1svt w=((VCO_WN) * (VCO_N)) l=VCO_LN \
nf=VCO_N as=((VCO_WN) < 119.5n) ? (((50n > (((60n) - 0) + 60n) ? 50n : (((60n)
- 0) + 60n)) * 120n) + ((VCO_WN) * 50n)) + (floor(((VCO_N) - 1) / 2.0) *
(((60n) - 0) + 60n)) * 120n) + ((VCO_WN) * 100n)) + (((((VCO_N) / 2) -
floor((VCO_N) / 2) == 0) ? (((50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0)
+ 60n)) * 120n) + ((VCO_WN) * 50n)) : 0)) / 1 : (((100n > (((60n) - 0) + 80
n) ? 100n : (((60n) - 0) + 80n)) * (VCO_WN)) + (floor(((VCO_N) - 1) / 2.0) *
(60n > (((60n) - 0) + 50n) ? 60n : (((60n) - 0) + 50n)) * (VCO_WN))) +
(((VCO_N) / 2) - floor((VCO_N) / 2) == 0) ? ((100n > (((60n) - 0) + 80n) ?
100n : (((60n) - 0) + 80n)) * (VCO_WN)) : 0)) / 1 \
ad=((VCO_WN) < 119.5n) ? ((floor((VCO_N) / 2.0) * (((((60n) - 0) + 60n) * 120n
) + ((VCO_WN) * 100n))) + (((((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ?
(((50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) * 120n) + ((VCO_WN) * 50n)) : 0)) / 1 : ((floor((VCO_N) / 2.0) * ((60n > (((60n) - 0) +
50n) ? 60n : (((60n) - 0) + 50n)) * (VCO_WN))) + (((((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ? ((100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80
n)) * (VCO_WN)) : 0)) / 1 \
ps=((VCO_WN) < 119.5n) ? (((2 * (50n > (((60n) - 0) + 60n) ? 50n : (((60n) -
0) + 60n))) + 340n) + (floor(((VCO_N) - 1) / 2.0) * ((2 * (((60n) - 0) + 60
n)) + 440n)) + (((((VCO_N) / 2) - floor((VCO_N) / 2) == 0) ? ((2 * (50n >
(((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n))) + 340n) : 0)) / 1 : (((2
* (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))) + (2 * (VCO_WN
))) + (floor(((VCO_N) - 1) / 2.0) * ((2 * (60n > (((60n) - 0) + 50n) ? 60n
: (((60n) - 0) + 50n))) + (2 * (VCO_WN)))) + (((((VCO_N) / 2) - floor((VCO_N) /
2) == 0) ? ((2 * (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80
n))) + (2 * (VCO_WN))) : 0)) / 1 \
pd=((VCO_WN) < 119.5n) ? ((floor((VCO_N) / 2.0) * ((2 * (((60n) - 0) + 60n)) +
440n)) + (((((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ? ((2 * (50n > (((60n)
- 0) + 60n) ? 50n : (((60n) - 0) + 60n))) + 340n) : 0)) / 1 : ((floor((VCO_N) / 2.0) * ((2 * (((60n) - 0) + 60n)) + 440n)) + (((((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ? ((2 * (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n))) + 340n) : 0)) / 1 : (((((VCO_N) / 2) - floor((VCO_N) / 2) == 0) ? ((2 * (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))) + (2 * (VCO_WN)))) + (((((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ? ((2 * (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))) + (2 * (VCO_WN)))) : 0)) / 1 \

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225
    - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)/10 + (1u)/100)*exp(-10 * (((VCO_WN) < 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n) / (1u)) - (((((VCO_WN) < 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)+VCO_LN)/10 + (1u)/100)*exp(-10 * (((VCO_WN) < 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)+VCO_LN) / (1u)))) + (VCO_LN * (((60n)/10 + (1u)/100)*exp(-10 * (60n) / (1u)) - (((60n)+(VCO_WN)) / (1u)) + ((60n)/10 + (1u)/100)*exp(-10 * (60n) / (1u)) - (((60n)+(VCO_WN)) / (1u)) + (1u)/100)*exp(-10 * ((60n)+(VCO_WN)) / (1u)))) / ((VCO_WN) * VCO_LN) \
scc=(((VCO_WN) * (((((VCO_WN) < 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n))+60n)/20 + (1u)/400)*exp(-20 * (((VCO_WN) < 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n))+60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n) / (1u)) - (((((VCO_WN) < 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n))+60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)+VCO_LN)/20 + (1u)/400)*exp(-20 * (((VCO_WN) < 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n))+60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)+VCO_LN) / (1u)) + (((((VCO_WN) < 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n))+60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)+VCO_LN)/20 + (1u)/400)*exp(-20 * (((VCO_WN) < 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n))+60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)+VCO_LN) / (1u)) - (((((VCO_WN) < 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n))+60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)+VCO_LN)/20 + (1u)/400)*exp(-20 * (((VCO_WN) < 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n))+60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)+VCO_LN) / (1u))) + (VCO_LN * (((60n)/20 + (1u)/400)*exp(-20 * (60n) / (1u)) - (((60n)+(VCO_WN)) / (1u)) + ((60n)/20 + (1u)/400)*exp(-20 * (60n) / (1u)) - (((60n)+(VCO_WN)) / (1u)) + (1u)/400)*exp(-20 * ((60n)+(VCO_WN)) / (1u)))) / ((VCO_WN) * VCO_LN) \
m=(1)
226
PM0 (net7 net7 VDD VDD) g45p1svt w=((VCO_WP) * (VCO_N)) l=VCO_LP \
227
228
nf=VCO_N as=((VCO_WP) < 119.5n) ? (((50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) * 120n) + ((VCO_WP) * 50n)) + (floor(((VCO_N) - 1) / 2.0) * (((60n) - 0) + 60n)) * 120n) + ((VCO_WP) * 100n)) + (((VCO_N) / 2) - floor((VCO_N) / 2) == 0) ? (((50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) * 120n) + ((VCO_WP) * 50n)) : 0)) / 1 : (((100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n)) * (VCO_WP)) + (floor(((VCO_N) - 1) / 2.0) * ((60n > (((60n) - 0) + 50n) ? 60n : (((60n) - 0) + 50n)) * (VCO_WP))) + (((VCO_N) / 2) - floor((VCO_N) / 2) == 0) ? ((100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n)) * (VCO_WP)) : 0)) / 1 \
ad=((VCO_WP) < 119.5n) ? ((floor((VCO_N) / 2.0) * (((60n) - 0) + 60n)) * 120n) + ((VCO_WP) * 100n)) + (((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ? (((50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) * 120n) + ((VCO_WP) * 50n)) : 0)) / 1 : ((floor((VCO_N) / 2.0) * ((60n > (((60n) - 0) + 50n) ? 60n : (((60n) - 0) + 50n)) * (VCO_WP))) + (((VCO_N) / 2) - floor((VCO_N) / 2) == 0) ? ((100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n)) * (VCO_WP)) : 0)) / 1 \

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      50n) ? 60n : (((60n - 0) + 50n)) * (VCO_WP))) + (((VCO_N) / 2) - floor((
      VCO_N) / 2) != 0) ? ((100n > (((60n - 0) + 80n) ? 100n : (((60n - 0) + 80
      n)) * (VCO_WP)) : 0)) / 1 \
230   ps=((VCO_WP) < 119.5n) ? (((2 * (50n > (((60n - 0) + 60n) ? 50n : (((60n -
      0) + 60n))) + 340n) + (floor(((VCO_N) - 1) / 2.0) * ((2 * (((60n - 0) + 60
      n)) + 440n)) + (((VCO_N) / 2) - floor((VCO_N) / 2) == 0) ? ((2 * (50n >
      (((60n - 0) + 60n) ? 50n : (((60n - 0) + 60n))) + 340n) : 0)) / 1 : (((2
      * (100n > (((60n - 0) + 80n) ? 100n : (((60n - 0) + 80n))) + (2 * (VCO_WP
      ))) + (floor(((VCO_N) - 1) / 2.0) * ((2 * (60n > (((60n - 0) + 50n) ? 60n
      : (((60n - 0) + 50n))) + (2 * (VCO_WP)))) + (((VCO_N) / 2) - floor((VCO_N
      ) / 2) == 0) ? ((2 * (100n > (((60n - 0) + 80n) ? 100n : (((60n - 0) + 80
      n))) + (2 * (VCO_WP))) : 0)) / 1 \
231   pd=((VCO_WP) < 119.5n) ? ((floor((VCO_N) / 2.0) * ((2 * (((60n - 0) + 60n)) +
      440n)) + (((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ? ((2 * (50n > (((60n -
      0) + 60n) ? 50n : (((60n - 0) + 60n))) + 340n) : 0)) / 1 : ((floor((
      VCO_N) / 2.0) * ((2 * (60n > (((60n - 0) + 50n) ? 60n : (((60n - 0) + 50n
      ))) + (2 * (VCO_WP)))) + (((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ? ((2 *
      (100n > (((60n - 0) + 80n) ? 100n : (((60n - 0) + 80n))) + (2 * (VCO_WP
      )) : 0)) / 1 \
232   nrd=((VCO_WP) < 119.5n) ? ((floor((VCO_N) / 2.0) * (((((60n - 0) + 60n) * 120
      n) + ((VCO_WP) * 100n))) + (((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ?
      (((50n > (((60n - 0) + 60n) ? 50n : (((60n - 0) + 60n)) * 120n) + ((
      VCO_WP) * 50n)) : 0)) / 1 : ((floor((VCO_N) / 2.0) * (((60n > (((60n - 0) +
      50n) ? 60n : (((60n - 0) + 50n)) * (VCO_WP))) + (((VCO_N) / 2) - floor(((
      VCO_N) / 2) != 0) ? ((100n > (((60n - 0) + 80n) ? 100n : (((60n - 0) + 80
      n)) * (VCO_WP)) : 0)) / 1 / ((VCO_WP) * (VCO_N) * (VCO_WP) * (VCO_N)) \
233   nrs=((VCO_WP) < 119.5n) ? (((((50n > (((60n - 0) + 60n) ? 50n : (((60n - 0) +
      60n)) * 120n) + ((VCO_WP) * 50n)) + (floor(((VCO_N) - 1) / 2.0) * (((((60n
      ) - 0) + 60n) * 120n) + ((VCO_WP) * 100n))) + (((VCO_N) / 2) - floor(((
      VCO_N) / 2) == 0) ? (((50n > (((60n - 0) + 60n) ? 50n : (((60n - 0) + 60n
      )) * 120n) + ((VCO_WP) * 50n)) : 0)) / 1 : (((100n > (((60n - 0) + 80n) ?
      100n : (((60n - 0) + 80n)) * (VCO_WP)) + (floor(((VCO_N) - 1) / 2.0) *
      (((60n > (((60n - 0) + 50n) ? 60n : (((60n - 0) + 50n)) * (VCO_WP))) +
      (((VCO_N) / 2) - floor((VCO_N) / 2) == 0) ? ((100n > (((60n - 0) + 80n) ?
      100n : (((60n - 0) + 80n)) * (VCO_WP)) : 0)) / 1 / ((VCO_WP) * (VCO_N) *
      (VCO_WP) * (VCO_N)) \
234   sa=((VCO_WP) < 119.5n) ? (50n > (((60n - 0) + 60n) ? 50n : (((60n - 0) + 60n
      )) + 5e-08 : (100n > (((60n - 0) + 80n) ? 100n : (((60n - 0) + 80n)) \
235   sb=((VCO_WP) < 119.5n) ? (50n > (((60n - 0) + 60n) ? 50n : (((60n - 0) + 60n
      )) + 5e-08 : (100n > (((60n - 0) + 80n) ? 100n : (((60n - 0) + 80n)) \
236   sd=((VCO_WP) < 119.5n) ? (((60n - 0) + 60n) + (2*5e-08) : (60n > (((60n - 0)
      + 50n) ? 60n : (((60n - 0) + 50n)) \
237   sca=(( (VCO_WP) * ( ((1u) * (1u) / (((VCO_WP) < 119.5n) ? (50n > (((60n - 0)
      + 60n) ? 50n : (((60n - 0) + 60n)) + 5e-08 : (100n > (((60n - 0) + 80n)
      ? 100n : (((60n - 0) + 80n))+60n)) - ((1u) * (1u) / (((VCO_WP) < 119.5n)
      ? (50n > (((60n - 0) + 60n) ? 50n : (((60n - 0) + 60n)) + 5e-08 : (100n >
      (((60n - 0) + 80n) ? 100n : (((60n - 0) + 80n))+60n)+VCO_LP))) + ((1u) *
      (1u) / (((VCO_WP) < 119.5n) ? (50n > (((60n - 0) + 60n) ? 50n : (((60n - 0)
      + 60n)) + 5e-08 : (100n > (((60n - 0) + 80n) ? 100n : (((60n - 0) + 80n))+60n)) - ((1u) * (1u)/ (((VCO_WP) < 119.5n) ? (50n > (((60n - 0) +

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238

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240      m=(1)
241  PM1 (net26 net7 VDD VDD) g45p1svt w=((VCO_WP) * (VCO_N)) l=VCO_LP \
242      nf=VCO_N as=((VCO_WP) < 119.5n) ? (((50n > (((60n) - 0) + 60n) ? 50n : (((60n)
243          - 0) + 60n)) * 120n) + ((VCO_WP) * 50n)) + (floor(((VCO_N) - 1) / 2.0) *
244          (((((60n) - 0) + 60n) * 120n) + ((VCO_WP) * 100n))) + (((VCO_N) / 2) -
245          floor((VCO_N) / 2) == 0) ? (((50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0)
246          + 60n)) * 120n) + ((VCO_WP) * 50n)) : 0)) / 1 : (((100n > (((60n) - 0) + 80
247          n) ? 100n : (((60n) - 0) + 80n)) * (VCO_WP)) + (floor(((VCO_N) - 1) / 2.0) *
248          (((60n > (((60n) - 0) + 50n) ? 60n : (((60n) - 0) + 50n)) * (VCO_WP))) +
249          (((VCO_N) / 2) - floor((VCO_N) / 2) == 0) ? ((100n > (((60n) - 0) + 80n) ?
250          100n : (((60n) - 0) + 80n)) * (VCO_WP)) : 0)) / 1 \
251      ad=((VCO_WP) < 119.5n) ? ((floor((VCO_N) / 2.0) * (((((60n) - 0) + 60n) * 120n
252          ) + ((VCO_WP) * 100n))) + (((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ?
253          (((50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) * 120n) + ((
254          VCO_WP) * 50n)) : 0)) / 1 : ((floor((VCO_N) / 2.0) * ((60n > (((60n) - 0) +
255          50n) ? 60n : (((60n) - 0) + 50n)) * (VCO_WP))) + (((VCO_N) / 2) - floor((
256          VCO_N) / 2) != 0) ? ((100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80
257          n)) * (VCO_WP)) : 0)) / 1 \
258      ps=((VCO_WP) < 119.5n) ? (((2 * (50n > (((60n) - 0) + 60n) ? 50n : (((60n) -
259          0) + 60n))) + 340n) + (floor(((VCO_N) - 1) / 2.0) * ((2 * (((60n) - 0) + 60
260          n)) + 440n)) + (((VCO_N) / 2) - floor((VCO_N) / 2) == 0) ? ((2 * (50n >
261          (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 340n) : 0)) / 1 : (((2
262          * (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))) + (2 * (VCO_WP
263          )) + (floor(((VCO_N) - 1) / 2.0) * ((2 * (60n > (((60n) - 0) + 50n) ? 60n
264          : (((60n) - 0) + 50n)) + (2 * (VCO_WP)))) + (((VCO_N) / 2) - floor((VCO_N
265          ) / 2) == 0) ? ((2 * (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80
266          n)) + (2 * (VCO_WP))) : 0)) / 1 \
267      pd=((VCO_WP) < 119.5n) ? ((floor((VCO_N) / 2.0) * ((2 * (((60n) - 0) + 60n)) +
268          440n)) + (((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ? ((2 * (50n > (((60n)
269          - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 340n) : 0)) / 1 : ((floor((
270          VCO_N) / 2.0) * ((2 * (60n > (((60n) - 0) + 50n) ? 60n : (((60n) - 0) + 50n
271          ))) + (2 * (VCO_WP)))) + (((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ? ((2 *
272          (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n)) + (2 * (VCO_WP
273          )) : 0)) / 1 \
274      nrd=((VCO_WP) < 119.5n) ? ((floor((VCO_N) / 2.0) * (((((60n) - 0) + 60n) * 120
275          n) + ((VCO_WP) * 100n))) + (((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ?
276          (((50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) * 120n) + ((
277          VCO_WP) * 50n)) : 0)) / 1 : ((floor((VCO_N) / 2.0) * ((60n > (((60n) - 0) +
278          50n) ? 60n : (((60n) - 0) + 50n)) * (VCO_WP))) + (((VCO_N) / 2) - floor((
279          VCO_N) / 2) != 0) ? ((100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80
280          n)) * (VCO_WP)) : 0)) / 1 / ((VCO_WP) * (VCO_N) * (VCO_WP) * (VCO_N)) \
281      nrs=((VCO_WP) < 119.5n) ? (((50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) +
282          60n)) * 120n) + ((VCO_WP) * 50n)) + (floor((VCO_N) - 1) / 2.0) * (((((60n
283          ) - 0) + 60n) * 120n) + ((VCO_WP) * 100n)) + (((VCO_N) / 2) - floor((
284          VCO_N) / 2) == 0) ? (((50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n
285          )) * 120n) + ((VCO_WP) * 50n)) : 0)) / 1 : (((100n > (((60n) - 0) + 80n) ?
286          100n : (((60n) - 0) + 80n)) * (VCO_WP)) + (floor((VCO_N) - 1) / 2.0) *
287          (((60n > (((60n) - 0) + 50n) ? 60n : (((60n) - 0) + 50n)) * (VCO_WP))) +
288          (((VCO_N) / 2) - floor((VCO_N) / 2) == 0) ? ((100n > (((60n) - 0) + 80n) ?
289          100n : (((60n) - 0) + 80n)) * (VCO_WP)) : 0)) / 1 / ((VCO_WP) * (VCO_N) *

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50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n :
(((60n) - 0) + 80n))+60n)+VCO_LP) / (1u)) + (((VCO_WP) < 119.5n) ? (50n >
(((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n)
- 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)/20 + (1u)/400)*exp(-20 * (((VCO_WP)
< 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n))
+ 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n) /
(1u)) - (((VCO_WP) < 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n)
- 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0)
+ 80n))+60n)+VCO_LP) / 20 + (1u)/400)*exp(-20 * (((VCO_WP) < 119.5n) ? (50n
> (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n)
- 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)+VCO_LP) / (1u)))) + (
VCO_LP * (((60n)/20 + (1u)/400)*exp(-20 * (60n) / (1u)) - (((60n)+(VCO_WP)) /
20 + (1u)/400)*exp(-20 * ((60n)+(VCO_WP)) / (1u)) + ((60n)/20 + (1u)/400)*
exp(-20 * (60n) / (1u)) - (((60n)+(VCO_WP))/20 + (1u)/400)*exp(-20 * ((60n)
+(VCO_WP)) / (1u)))))) / ((VCO_WP) * VCO_LP) \
254 m=(1)
255 PM8 (net24 net7 VDD VDD) g45p1svt w=((VCO_WP) * (VCO_N)) l=VCO_LP \
256 nf=VCO_N as=((VCO_WP) < 119.5n) ? (((50n > (((60n) - 0) + 60n) ? 50n : (((60n)
- 0) + 60n)) * 120n) + ((VCO_WP) * 50n)) + (floor(((VCO_N) - 1) / 2.0) *
(((60n) - 0) + 60n)) * 120n) + ((VCO_WP) * 100n)) + (((VCO_N) / 2) -
floor((VCO_N) / 2) == 0) ? ((50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0)
+ 60n)) * 120n) + ((VCO_WP) * 50n) : 0)) / 1 : (((100n > (((60n) - 0) + 80
n) ? 100n : (((60n) - 0) + 80n)) * (VCO_WP)) + (floor(((VCO_N) - 1) / 2.0) *
((60n > (((60n) - 0) + 50n) ? 60n : (((60n) - 0) + 50n)) * (VCO_WP))) +
(((VCO_N) / 2) - floor((VCO_N) / 2) == 0) ? ((100n > (((60n) - 0) + 80n) ?
100n : (((60n) - 0) + 80n)) * (VCO_WP)) : 0)) / 1 \
257 ad=((VCO_WP) < 119.5n) ? ((floor((VCO_N) / 2.0) * (((60n) - 0) + 60n) * 120n
) + ((VCO_WP) * 100n)) + (((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ?
(((50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) * 120n) + ((VCO_WP)
* 50n) : 0)) / 1 : ((floor((VCO_N) / 2.0) * ((60n > (((60n) - 0) +
50n) ? 60n : (((60n) - 0) + 50n)) * (VCO_WP))) + (((VCO_N) / 2) - floor((VCO_N)
/ 2) != 0) ? ((100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80
n)) * (VCO_WP)) : 0)) / 1 \
258 ps=((VCO_WP) < 119.5n) ? (((2 * (50n > (((60n) - 0) + 60n) ? 50n : (((60n)
- 0) + 60n))) + 340n) + (floor(((VCO_N) - 1) / 2.0) * ((2 * (((60n) - 0) +
60n)) + 440n)) + (((VCO_N) / 2) - floor((VCO_N) / 2) == 0) ? ((2 * (50n >
((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 340n) : 0)) / 1 : (((2
* (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))) + (2 * (VCO_WP)
)) + (floor(((VCO_N) - 1) / 2.0) * ((2 * (60n > (((60n) - 0) + 50n) ? 60n
: (((60n) - 0) + 50n))) + (2 * (VCO_WP)))) + (((VCO_N) / 2) - floor((VCO_N)
/ 2) == 0) ? ((2 * (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80
n))) + (2 * (VCO_WP))) : 0)) / 1 \
259 pd=((VCO_WP) < 119.5n) ? ((floor((VCO_N) / 2.0) * ((2 * (((60n) - 0) + 60n) +
440n)) + (((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ? ((2 * (50n > (((60n)
- 0) + 60n) ? 50n : (((60n) - 0) + 60n))) + 340n) : 0)) / 1 : ((floor((VCO_N)
/ 2.0) * ((2 * (60n > (((60n) - 0) + 50n) ? 60n : (((60n) - 0) + 50n)))
+ (2 * (VCO_WP)))) + (((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ? ((2 *
(100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))) + (2 * (VCO_WP)
) : 0)) / 1 \

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) - 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0)
+ 80n))+60n)+VCO_LP)/10 + (1u)/100)*exp(-10 * (((VCO_WP) < 119.5n) ? (50n
> (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n
) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)+VCO_LP) / (1u)))) + (
VCO_LP * (((60n)/10 + (1u)/100)*exp(-10 * (60n) / (1u)) - (((60n)+(VCO_WP))
/10 + (1u)/100)*exp(-10 * ((60n)+(VCO_WP)) / (1u)) + ((60n)/10 + (1u)/100)*
exp(-10 * (60n) / (1u)) - (((60n)+(VCO_WP))/10 + (1u)/100)*exp(-10 * ((60n)
+(VCO_WP)) / (1u)))) / ((VCO_WP) * VCO_LP) \
267 scc=(((VCO_WP) * (((((VCO_WP) < 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n :
(((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n
) - 0) + 80n))+60n)/20 + (1u)/400)*exp(-20 * (((VCO_WP) < 119.5n) ? (50n >
(((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n
) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n) / (1u)) - (((((VCO_WP) <
119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 :
(100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)+VCO_LP)/20
+ (1u)/400)*exp(-20 * (((VCO_WP) < 119.5n) ? (50n > (((60n) - 0) + 60n) ?
50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n :
(((60n) - 0) + 80n))+60n)+VCO_LP) / (1u)) + (((((VCO_WP) < 119.5n) ? (50n >
(((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n
) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)/20 + (1u)/400)*exp(-20 * (((VCO_WP)
< 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 :
(100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)/20 + (1u)/400)*exp(-20 * (((VCO_WP)
< 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 :
(100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)+VCO_LP) / (1u)) - (((((VCO_WP) <
119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 :
(100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)+VCO_LP)/20
+ (1u)/400)*exp(-20 * (((VCO_WP) < 119.5n) ? (50n > (((60n) - 0) + 60n) ?
50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n :
(((60n) - 0) + 80n))+60n)+VCO_LP) / (1u)) + (((((VCO_WP) < 119.5n) ? (50n >
(((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n
) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)/20 + (1u)/400)*exp(-20 * (((VCO_WP)
< 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 :
(100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)+VCO_LP) / (1u)) - (((((VCO_WP) <
119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 :
(100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)+VCO_LP)/20
+ (1u)/400)*exp(-20 * (((VCO_WP) < 119.5n) ? (50n > (((60n) - 0) + 60n) ?
50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n :
(((60n) - 0) + 80n))+60n)+VCO_LP) / (1u))) / ((VCO_WP) * VCO_LP) \
268 m=(1)
269 PM2 (net25 net7 VDD VDD) g45p1svt w=((VCO_WP) * (VCO_N)) l=VCO_LP \
270 nf=VCO_N as=((VCO_WP) < 119.5n) ? (((50n > (((60n) - 0) + 60n) ? 50n : (((60n
) - 0) + 60n)) * 120n) + ((VCO_WP) * 50n)) + (floor(((VCO_N) - 1) / 2.0) *
(((60n) - 0) + 60n) * 120n) + ((VCO_WP) * 100n)) + (((VCO_N) / 2) -
floor((VCO_N) / 2) == 0) ? (((50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0)
+ 60n)) * 120n) + ((VCO_WP) * 50n)) : 0)) / 1 : (((100n > (((60n) - 0) + 80
n) ? 100n : (((60n) - 0) + 80n)) * (VCO_WP)) + (floor(((VCO_N) - 1) / 2.0) *
((60n > (((60n) - 0) + 50n) ? 60n : (((60n) - 0) + 50n)) * (VCO_WP))) +
(((VCO_N) / 2) - floor((VCO_N) / 2) == 0) ? ((100n > (((60n) - 0) + 80n) ?
100n : (((60n) - 0) + 80n)) * (VCO_WP)) : 0)) / 1 \
271 ad=((VCO_WP) < 119.5n) ? ((floor((VCO_N) / 2.0) * (((60n) - 0) + 60n) * 120n
) + ((VCO_WP) * 100n)) + (((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ?
(((50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) * 120n) + ((VCO_WP) * 50n)) :
0)) / 1 : (((floor((VCO_N) / 2.0) * ((60n > (((60n) - 0) + 50n) ? 60n :
(((60n) - 0) + 50n)) * (VCO_WP))) + (((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ?
((100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n)) * (VCO_WP)) : 0)) / 1 \

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272 ps=((VCO_WP) < 119.5n) ? (((2 * (50n > (((60n) - 0) + 60n) ? 50n : (((60n) -
0) + 60n))) + 340n) + (floor(((VCO_N) - 1) / 2.0) * ((2 * (((60n) - 0) + 60
n)) + 440n)) + (((((VCO_N) / 2) - floor((VCO_N) / 2) == 0) ? ((2 * (50n >
((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n))) + 340n) : 0)) / 1 : (((2
* (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))) + (2 * (VCO_WP
))) + (floor(((VCO_N) - 1) / 2.0) * ((2 * (60n > (((60n) - 0) + 50n) ? 60n
: (((60n) - 0) + 50n))) + (2 * (VCO_WP)))) + (((((VCO_N) / 2) - floor((VCO_N
) / 2) == 0) ? ((2 * (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80
n))) + (2 * (VCO_WP))) : 0)) / 1 \
273 pd=((VCO_WP) < 119.5n) ? ((floor((VCO_N) / 2.0) * ((2 * (((60n) - 0) + 60n)) +
440n)) + (((((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ? ((2 * (50n > (((60n)
- 0) + 60n) ? 50n : (((60n) - 0) + 60n))) + 340n) : 0)) / 1 : ((floor(((
VCO_N) / 2.0) * ((2 * (60n > (((60n) - 0) + 50n) ? 60n : (((60n) - 0) + 50n
))) + (2 * (VCO_WP)))) + (((((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ? ((2 *
(100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))) + (2 * (VCO_WP
))) : 0)) / 1 \
274 nrd=((VCO_WP) < 119.5n) ? ((floor((VCO_N) / 2.0) * (((((60n) - 0) + 60n) * 120
n) + ((VCO_WP) * 100n)) + (((((VCO_N) / 2) - floor((VCO_N) / 2) != 0) ?
((50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) * 120n) + (((
VCO_WP) * 50n)) : 0)) / 1 : ((floor((VCO_N) / 2.0) * ((60n > (((60n) - 0) +
50n) ? 60n : (((60n) - 0) + 50n)) * (VCO_WP))) + (((((VCO_N) / 2) - floor(((
VCO_N) / 2) != 0) ? ((100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80
n)) * (VCO_WP)) : 0)) / 1 / ((VCO_WP) * (VCO_N) * (VCO_WP) * (VCO_N)) \
275 nrs=((VCO_WP) < 119.5n) ? (((((50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) +
60n)) * 120n) + ((VCO_WP) * 50n)) + (floor(((VCO_N) - 1) / 2.0) * (((((60n
) - 0) + 60n) * 120n) + ((VCO_WP) * 100n)) + (((((VCO_N) / 2) - floor(((
VCO_N) / 2) == 0) ? (((50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n
)) * 120n) + ((VCO_WP) * 50n)) : 0)) / 1 : (((100n > (((60n) - 0) + 80n) ?
100n : (((60n) - 0) + 80n)) * (VCO_WP)) + (floor(((VCO_N) - 1) / 2.0) *
((60n > (((60n) - 0) + 50n) ? 60n : (((60n) - 0) + 50n)) * (VCO_WP))) +
((((VCO_N) / 2) - floor((VCO_N) / 2) == 0) ? ((100n > (((60n) - 0) + 80n) ?
100n : (((60n) - 0) + 80n)) * (VCO_WP)) : 0)) / 1 / ((VCO_WP) * (VCO_N) *
(VCO_WP) * (VCO_N)) \
276 sa=((VCO_WP) < 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n
)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n)) \
277 sb=((VCO_WP) < 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n
)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n)) \
278 sd=((VCO_WP) < 119.5n) ? (((60n) - 0) + 60n) + (2*5e-08) : (60n > (((60n) - 0)
+ 50n) ? 60n : (((60n) - 0) + 50n)) \
279 sca=(( (VCO_WP) * ( ((1u) * (1u) / (((VCO_WP) < 119.5n) ? (50n > (((60n) - 0)
+ 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n)
? 100n : (((60n) - 0) + 80n))+60n)) - ((1u) * (1u) / (((((VCO_WP) < 119.5n)
? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n >
((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)+VCO_LP))) + ((1u) *
(1u) / (((VCO_WP) < 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n : (((60n) -
0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) +
80n))+60n)) - ((1u) * (1u)/ (((((VCO_WP) < 119.5n) ? (50n > (((60n) - 0) +
60n) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ?
100n : (((60n) - 0) + 80n))+60n)+VCO_LP)))) + ( VCO_LP * ( (((1u) * (1u) /
(60n)) - ((1u) * (1u) / ((60n)+(VCO_WP)))) + ((1u) * (1u) / (60n)) - ((1u)

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* (1u)/ (((60n)+(VCO_WP)))))) / ((VCO_WP) * VCO_LP) \
280 scb=(((VCO_WP) * (((((VCO_WP) < 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n :
(((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n)
- 0) + 80n))+60n)/10 + (1u)/100)*exp(-10 * (((VCO_WP) < 119.5n) ? (50n >
(((60n) - 0) + 60n)) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n)
- 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n) / (1u)) - (((((VCO_WP) <
119.5n) ? (50n > (((60n) - 0) + 60n)) ? 50n : (((60n) - 0) + 60n)) + 5e-08 :
(100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)+VCO_LP)/10
+ (1u)/100)*exp(-10 * (((VCO_WP) < 119.5n) ? (50n > (((60n) - 0) + 60n)) ?
50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n :
(((60n) - 0) + 80n))+60n)+VCO_LP) / (1u)) + (((VCO_WP) < 119.5n) ? (50n >
(((60n) - 0) + 60n)) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n)
- 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)/10 + (1u)/100)*exp(-10 * (((VCO_WP)
< 119.5n) ? (50n > (((60n) - 0) + 60n)) ? 50n : (((60n) - 0) + 60n)) +
5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n) /
(1u)) - (((((VCO_WP) < 119.5n) ? (50n > (((60n) - 0) + 60n)) ? 50n : (((60n)
- 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0)
+ 80n))+60n)+VCO_LP)/10 + (1u)/100)*exp(-10 * (((VCO_WP) < 119.5n) ? (50n >
(((60n) - 0) + 60n)) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n)
- 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)+VCO_LP) / (1u))) + (
VCO_LP * (((60n)/10 + (1u)/100)*exp(-10 * (60n) / (1u)) - (((60n)+(VCO_WP))
/10 + (1u)/100)*exp(-10 * ((60n)+(VCO_WP)) / (1u)) + ((60n)/10 + (1u)/100)*
exp(-10 * (60n) / (1u)) - (((60n)+(VCO_WP))/10 + (1u)/100)*exp(-10 * ((60n)
+(VCO_WP)) / (1u))))) / ((VCO_WP) * VCO_LP) \
281 scc=(((VCO_WP) * (((((VCO_WP) < 119.5n) ? (50n > (((60n) - 0) + 60n) ? 50n :
(((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n)
- 0) + 80n))+60n)/20 + (1u)/400)*exp(-20 * (((VCO_WP) < 119.5n) ? (50n >
(((60n) - 0) + 60n)) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n)
- 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n) / (1u)) - (((((VCO_WP) <
119.5n) ? (50n > (((60n) - 0) + 60n)) ? 50n : (((60n) - 0) + 60n)) + 5e-08 :
(100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)+VCO_LP)/20
+ (1u)/400)*exp(-20 * (((VCO_WP) < 119.5n) ? (50n > (((60n) - 0) + 60n)) ?
50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n :
(((60n) - 0) + 80n))+60n)+VCO_LP) / (1u)) + (((VCO_WP) < 119.5n) ? (50n >
(((60n) - 0) + 60n)) ? 50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n)
- 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n)/20 + (1u)/400)*exp(-20 * (((VCO_WP)
< 119.5n) ? (50n > (((60n) - 0) + 60n)) ? 50n : (((60n) - 0) + 60n)) +
5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0) + 80n))+60n) /
(1u)) - (((((VCO_WP) < 119.5n) ? (50n > (((60n) - 0) + 60n)) ? 50n : (((60n)
- 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n : (((60n) - 0)
+ 80n))+60n) / (1u)) - (((((VCO_WP) < 119.5n) ? (50n > (((60n) - 0) + 60n)) ?
50n : (((60n) - 0) + 60n)) + 5e-08 : (100n > (((60n) - 0) + 80n) ? 100n :
(((60n) - 0) + 80n))+60n)+VCO_LP)/20 + (1u)/400)*exp(-20 * (((VCO_WP) <
119.5n) ? (50n > (((60n) - 0) + 60n)) ? 50n : (((60n) - 0) + 60n)) / (1u)) +
(VCO_LP * (((60n)/20 + (1u)/400)*exp(-20 * (60n) / (1u)) - (((60n)+(VCO_WP))
/20 + (1u)/400)*exp(-20 * ((60n)+(VCO_WP)) / (1u)) + ((60n)/20 + (1u)/400)*
exp(-20 * (60n) / (1u)) - (((60n)+(VCO_WP))/20 + (1u)/400)*exp(-20 * ((60n)
+(VCO_WP)) / (1u))))) / ((VCO_WP) * VCO_LP) \
282 m=(1)
283 I20 (net17 VCO_OUT VDD VSS) Inverter_200395P
284 I19 (net14 net17 net24 net21) Inverter_200395P

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285    I18 (net11 net14 net25 net22) Inverter_200395P
286    I17 (net17 net11 net26 net23) Inverter_200395P
287 ends RngVCO_200395P
288 // End of subcircuit definition.

289
290 // Library name: PFD_200395P
291 // Cell name: DFlop_200395P
292 // View name: schematic
293 subckt DFlop_200395P CLK D Q Qbar VDD VSS
294     PM4 (net1 CLK net17 VDD) g45p1svt w=(2u) l=45n nf=1 as=280f ad=280f \
295         ps=4.28u pd=4.28u nrd=70m nrs=70m sa=140n sb=140n sd=160n \
296         sca=56.99756 scb=0.05691 scc=0.00695 m=(1)
297     PM3 (Q Qbar VDD VDD) g45p1svt w=(2u) l=45n nf=1 as=280f ad=280f \
298         ps=4.28u pd=4.28u nrd=70m nrs=70m sa=140n sb=140n sd=160n \
299         sca=56.99756 scb=0.05691 scc=0.00695 m=(1)
300     PM2 (Qbar net13 VDD VDD) g45p1svt w=(2u) l=45n nf=1 as=280f ad=280f \
301         ps=4.28u pd=4.28u nrd=70m nrs=70m sa=140n sb=140n sd=160n \
302         sca=56.99756 scb=0.05691 scc=0.00695 m=(1)
303     PM1 (net13 CLK VDD VDD) g45p1svt w=(2u) l=45n nf=1 as=280f ad=280f \
304         ps=4.28u pd=4.28u nrd=70m nrs=70m sa=140n sb=140n sd=160n \
305         sca=56.99756 scb=0.05691 scc=0.00695 m=(1)
306     PM0 (net17 D VDD VDD) g45p1svt w=(2u) l=45n nf=1 as=280f ad=280f \
307         ps=4.28u pd=4.28u nrd=70m nrs=70m sa=140n sb=140n sd=160n \
308         sca=56.99756 scb=0.05691 scc=0.00695 m=(1)
309     NM5 (Q Qbar VSS VSS) g45n1svt w=(1u) l=45n nf=1 as=140f ad=140f \
310         ps=2.28u pd=2.28u nrd=140m nrs=140m sa=140n sb=140n sd=160n \
311         sca=72.26287 scb=0.06569 scc=0.00861 m=(1)
312     NM4 (net44 net13 VSS VSS) g45n1svt w=(1u) l=45n nf=1 as=140f ad=140f \
313         ps=2.28u pd=2.28u nrd=140m nrs=140m sa=140n sb=140n sd=160n \
314         sca=72.26287 scb=0.06569 scc=0.00861 m=(1)
315     NM3 (net29 CLK VSS net015) g45n1svt w=(1u) l=45n nf=1 as=140f ad=140f \
316         ps=2.28u pd=2.28u nrd=140m nrs=140m sa=140n sb=140n sd=160n \
317         sca=72.26287 scb=0.06569 scc=0.00861 m=(1)
318     NM2 (net1 D VSS VSS) g45n1svt w=(1u) l=45n nf=1 as=140f ad=140f \
319         ps=2.28u pd=2.28u nrd=140m nrs=140m sa=140n sb=140n sd=160n \
320         sca=72.26287 scb=0.06569 scc=0.00861 m=(1)
321     NM1 (net13 net1 net29 net015) g45n1svt w=(1u) l=45n nf=1 as=140f \
322         ad=140f ps=2.28u pd=2.28u nrd=140m nrs=140m sa=140n sb=140n \
323         sd=160n sca=72.26287 scb=0.06569 scc=0.00861 m=(1)
324     NM0 (Qbar CLK net44 VSS) g45n1svt w=(1u) l=45n nf=1 as=140f ad=140f \
325         ps=2.28u pd=2.28u nrd=140m nrs=140m sa=140n sb=140n sd=160n \
326         sca=72.26287 scb=0.06569 scc=0.00861 m=(1)
327     C1 (Qbar VSS) capacitor c=10f
328     CO (Q VSS) capacitor c=10f
329 ends DFlop_200395P
330 // End of subcircuit definition.

331
332 // Library name: FDivider_200395P
333 // Cell name: Freq_Divider_3N_200395P
334 // View name: schematic

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335 subckt Freq_Divider_3N_200395P CLK_IN CLK_OUT Q1bar VDD VSS
336   I1 (CLK_IN net13 CLK_OUT net8 VDD VSS) DFlop_200395P
337   I0 (CLK_IN net8 net11 Q1bar VDD VSS) DFlop_200395P
338   I2 (net8 net11 VDD net14) NAND_200395P
339   I3 (net14 net13 VDD VSS) Inverter_200395P
340 ends Freq_Divider_3N_200395P
341 // End of subcircuit definition.

342
343 // Library name: FDivider_200395P
344 // Cell name: Freq_Divider_5N_200395P
345 // View name: schematic
346 subckt Freq_Divider_5N_200395P CLK_IN CLK_OUT Q1 VDD VSS
347   I12 (net18 net17 VDD VSS) Inverter_200395P
348   I11 (net16 net19 VDD VSS) Inverter_200395P
349   I7 (CLK_IN net17 net9 net011 VDD VSS) DFlop_200395P
350   I6 (CLK_IN net19 Q1 net12 VDD VSS) DFlop_200395P
351   I8 (net011 CLK_OUT MC CLK_OUT VDD VSS) DFlop_200395P
352   I10 (net011 net12 VDD net18) NAND_200395P
353   I9 (net9 MC VDD net16) NAND_200395P
354 ends Freq_Divider_5N_200395P
355 // End of subcircuit definition.

356
357 // Library name: FDivider_200395P
358 // Cell name: Multiple_Freq_Divider_200395P
359 // View name: schematic
360 subckt Multiple_Freq_Divider_200395P \10N_Fout \12N_Fout \15N_Fout \
361   \16N_Fout \2N_Fout \3N_Fout \4N_Fout \5N_Fout \6N_Fout \8N_Fout \
362   \9N_Fout CLK_IN Q11 Q12 Q13 Q1bar1 Q1bar2 Q1bar3 Q1bar4 VDD VSS
363   I3 (\8N_Fout net21 \16N_Fout net21 VDD VSS) DFlop_200395P
364   I2 (\4N_Fout net18 \8N_Fout net18 VDD VSS) DFlop_200395P
365   I1 (\2N_Fout net15 \4N_Fout net15 VDD VSS) DFlop_200395P
366   I0 (CLK_IN net12 \2N_Fout net12 VDD VSS) DFlop_200395P
367   I10 (\4N_Fout \12N_Fout Q1bar4 VDD VSS) Freq_Divider_3N_200395P
368   I9 (\2N_Fout \6N_Fout Q1bar3 VDD VSS) Freq_Divider_3N_200395P
369   I6 (\3N_Fout \9N_Fout Q1bar2 VDD VSS) Freq_Divider_3N_200395P
370   I5 (CLK_IN \3N_Fout Q1bar1 VDD VSS) Freq_Divider_3N_200395P
371   I11 (\3N_Fout \15N_Fout Q13 VDD VSS) Freq_Divider_5N_200395P
372   I8 (\2N_Fout \10N_Fout Q12 VDD VSS) Freq_Divider_5N_200395P
373   I7 (CLK_IN \5N_Fout Q11 VDD VSS) Freq_Divider_5N_200395P
374 ends Multiple_Freq_Divider_200395P
375 // End of subcircuit definition.

376
377 // Library name: PLL_200395P
378 // Cell name: PLL_200395P
379 // View name: schematic
380 I18 (Down net48 net27 Up net46 Vcon VDD 0) CHP_Updated_200395P
381 I14 (Down net48 \4N_F Fref Up net46 VDD 0) PFD_New_200395P
382 I21 (Vcon Vout VDD 0) RngVCO_200395P
383 I19 (\10N_F \12N_F \15N_F \16N_F \2N_F \3N_F \4N_F \5N_F \6N_F \8N_F \9N_F \
384   Vout Q11 Q12 Q13 Q1bar1 Q1bar2 Q1bar3 Q1bar4 VDD 0) \

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385 Multiple_Freq_Divider_200395P
386 V0 (VDD 0) vsource dc=1 type=dc
387 V1 (Fref 0) vsource type=pulse val0=0 val1=1 period=5n rise=50p fall=50p \
388     width=2.5n
389 I16 (VDD net27) isource dc=80u type=dc
390 ic Vcon=0.5 Vout=1
391 simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27 \
392     tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5 \
393     digits=5 cols=80 pivrel=1e-3 sensfile="../psf/sens.output" \
394     checklimitdest=psf
395 tran tran stop=500n errpreset=moderate write="spectre.ic" \
396     writefinal="spectre.fc" annotate=status maxiters=5
397 finalTimeOP info what=oppoint where=rawfile
398 modelParameter info what=models where=rawfile
399 element info what=inst where=rawfile
400 outputParameter info what=output where=rawfile
401 designParamVals info what=parameters where=rawfile
402 primitives info what=primitives where=rawfile
403 subckts info what=subckts where=rawfile
404 saveOptions options save=allpub

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