Department of Electronic & Telecommunication Engineering
University of Moratuwa

EN4604 - DIGITAL IC DESIGN

LABORATORY EXPERIMENT 3: PLACE AND ROUTE

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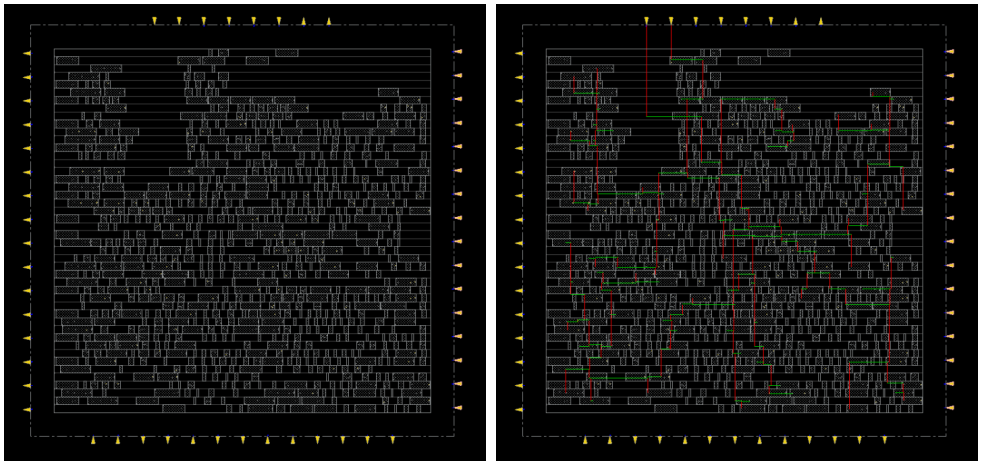
This report is submitted as the fulfillment of Lab - 03 of module EN4604

1 EXERCISE

1.1 Gate Count and Area Comparison

Restore the design you saved at part 8 of step 3 (`uart_top_prePlacement`), perform placement of standard cells without pre-place optimization and report the gate count & area. Compare and comment on the gate count & area with and without pre-place optimization.

Design without pre-place optimization.



(a) Design without any nets (b) Design with only clock nets

Figure 1 — Design without pre-place optimization.

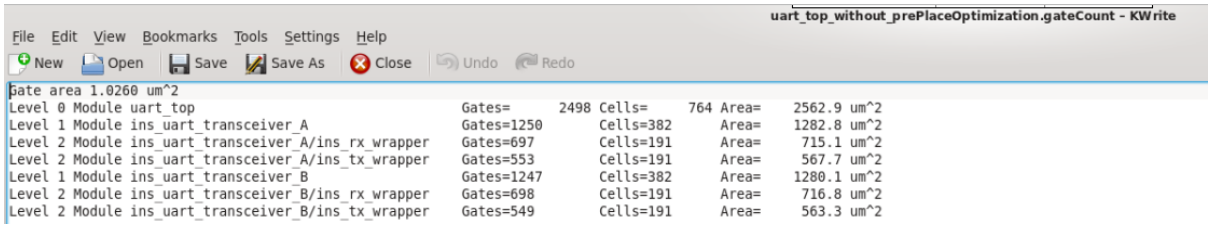
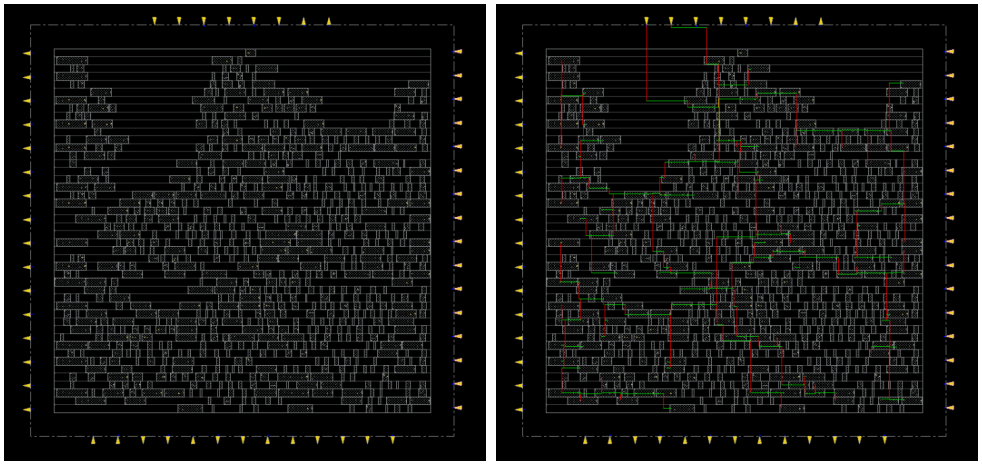


Figure 2 — Gate count & area without pre-place optimization

Design with pre-place optimization.



(a) Design without any nets (b) Design with only clock nets

Figure 3 — Design after pre-place optimization.

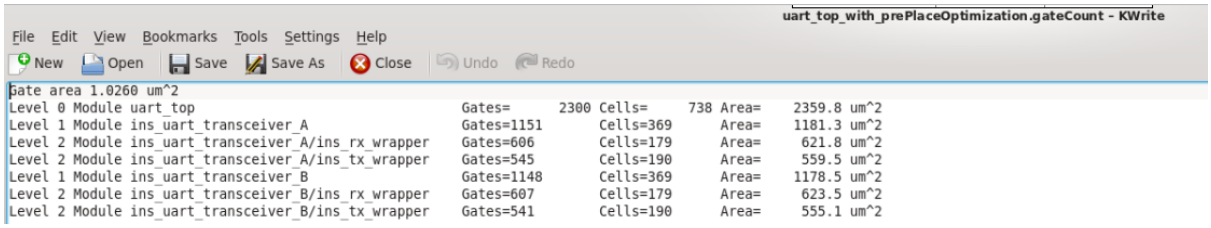


Figure 4 — Gate count & area after pre-place optimization

With pre-place optimization:

* **Gate count**: reduced from 2498 to 2300
* **Area**: reduced from 2562.9 μm^2 to 2359.8 μm^2

Pre-place optimization improves both gate count and area by optimizing the netlist before placing standard cells in the design.

1.2 Pre-CTS Timing Analysis

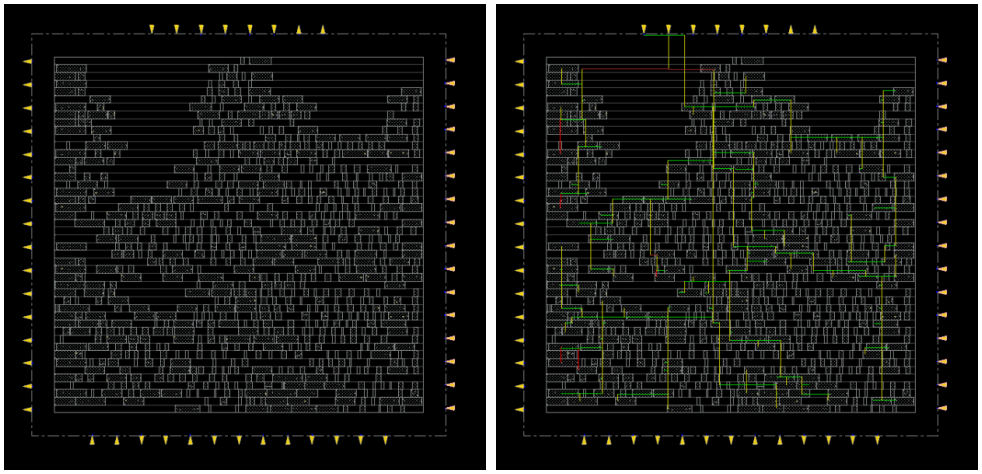
Note that we did only setup time analysis in pre-CTS timing analysis. There is little purpose in performing hold time analysis at the pre-CTS stage. What is the reason for this?

* Hold time analysis in pre-CTS is ineffective because it depends on precise clock skew information, which can only be determined after CTS. The clock tree and timing paths are incompletely determined in pre-CTS stage. Setup time analysis can effectively be run pre-CTS as it depends only on datapath delay information.

1.3 Clock Net Routing Comparison

Compare and comment on the cell count and the routing of the clock net before and after CTS. (show screenshots of the design to support your answer)

Design after CTS.



(a) Design without any nets (b) Design with only clock nets

Figure 5 — Design after CTS.

Figure 6 — Gate count & area after CTS

* Post-CTS, the gate count increased from 2300 to 2484. The cell count rise from 738 to 768, and the area expanded from 2359.8 μm^2 to 2549.3 μm^2. These increases result from adding buffers and dummy loads to balance clock skew. This enhances clock distribution and timing reliability while utilizing more area.

1.4 On-Chip Variation Analysis

What is the reason for changing the analysis mode to on-chip variation at the post-Route timing analysis stage?

* The violations can still occur after fabrication due to variation(PVT variations - Process, Voltage, Temperature) in the manufacturing process even after post-routing

timing analysis. To consider such variations, we select the on-chip variation mode for the post-routing analysis. This mode will introduce extra margins within the timing analysis and allow the consideration of the worst case. In this way, it allows on-chip variation mode to give more realistic and exact calculation of timing by considering practical variations which may affect the performance.

Figure 7 — Timing Analysis Summary After OCV

1.5 Filler Cell Placement and Metal Fill

In some designs, in addition to the placement of filler cells, a metal fill is added as well. Describe the difference between filler cell placement and metal fill.

* Filler cells are non-logical components used to ensure n-well and p-well continuity in areas without standard cells. They help maintain proper electrical characteristics. Low metal density can lead to uneven etching during the metal etching process, potentially damaging surrounding materials. Metal fill is used to address low metal density in certain areas of a chip, preventing thickness variations during fabrication.