

Department of Electronic & Telecommunication Engineering University of Moratuwa

EN4604 - DIGITAL IC DESIGN

LABORATORY EXPERIMENT 2: DFT INSERTION

Supervisors:

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Group No:- 07

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This report is submitted as the fulfillment of Lab - 02 of module EN4604

1 EXERCISE

1. Comment on the area before (output of the laboratory experiment 1) and after (uart_top_1.v) scan synthesis.

Generated by: Generated on:		4) Synthesis Solution 18.10-p003_1 2024 09:11:26 am				
	uart_top					
Technology libraries:	slow_vdo					
	fast_vdo					
Operating conditions.	physical PVT 0P9					
Operating conditions: Interconnect mode:	global	7_125C				
Area mode:		l library				
		:				
Instance		Module	Cell Count	Cell Area	Net Area	Total Area
rt top			772	2220.948	946.493	3167.441
ins uart transceiver B		uart transceiver CLOCK IN MHZ100 TX WORD LENGTH8 T	386	1110.474	423.318	1533.792
ins rx wrapper		rx_wrapper_NO_OF_WORS_IN_BUFFER1_NO_OF_DATA_BITS8_rx_buffer_WORD_SIZE8_NO_OF_WORDS1_1	197	621.072	209.103	830.175
ins_rx_buffer				292.068	61.047	353.115
ins_rx_fsm		rx_fsm_NO_OF_DATA_BITS8_PARITY_ENABLED32h54525545		200.020	77.867	258.785
ins_sampling_tick_g	enerator	sampling_tick_generator_BAUD115200_CLOCK_IN_MHZ100			62.149	210.235
ins_tx_wrapper		tx_wrapper_NO_OF_WORDS_IN_BUFFER1_NO_OF_DATA_BITS8			214.215	703.617
ins_tx_fsm		tx_fsm_NO_OF_DATA_BITS8_PARITY_ENABLED32h54525545_			103.544	313.874
ins_tx_buffer		tx_buffer_WORD_SIZE8_NO_OF_WORDS1_1	53		52.247	198.965
		sampling_tick_generator_BAUD115200_CLOCK_IN_MHZ100			46.412	178.766
.ns_uart_transceiver_A		uart_transceiver_CLOCK_IN_MHZ100_TX_WORD_LENGTH8_T rx_wrapper_NO_OF_WORS_IN_BUFFER1_NO_OF_DATA_BITS8	386		423.318 209.103	1533.792
		rx_wrapper_No_OF_WORS_IN_BUFFERI_NO_OF_DATA_BITS8_ rx_buffer_WORD_SIZE8_NO_OF_WORDS1	197 67		61.047	830.175 353.115
ins_rx_burrer		rx fsm NO OF DATA BITS8 PARITY ENABLED32h54525545	74		77.867	258.785
		sampling tick generator BAUD115200 CLOCK IN MHZ100			62.149	210.235
ins tx wrapper	cheracor	tx wrapper NO OF WORDS IN BUFFER1 NO OF DATA BITS8	189		214.215	703.617
ins tx fsm		tx_wrapper NO_OF_WORDS_IN_BUFFER1_NO_OF_DATA_BITS8 tx_fsm_NO_OF_DATA_BITS8_PARITY_ENABLED32h54525545_ tx_buffer_WORD_SIZE8_NO_OF_WORDS1	94		103.544	313.874
		tx buffer WORD SIZE8 NO OF WORDS1	53		52.247	198.965
ins tx buffer						

Figure 1 — Area Report Before Scan Synthesis (Lab 1 Experiment)

		Genus(TM) Synthesis Solution 18.10-p003_1 Sep 12 2024 02:42:45 pm							
lodule:	uart to	שני בייבי בייבי בייבי בייבי שוון ווין בייבייבי הייביבי ווין בייבייבי ווין בייבייבי בייביבי בייבייבי ווין בייבי							
echnology libraries:									
	fast vd								
	physica	l cells							
perating conditions:	PVT 0P9	/ 125C							
nterconnect mode:	global								
rea mode:	physica	l library							
Instance		Module	Cell Count	Coll Area	Not Area	Total Are			
Tilstalice		noduce		Cett Area	Net Area	TOTAL ATE			
t top			764	2570.472	987.659	3558.13			
ns wart transceiver B		uart transceiver CLOCK IN MHZ100 TX WORD LENGTH8 T	382	1285.236	443.179	1728.41			
ins rx wrapper		uart_transceiver_CLOCK_IN_MHZ100_TX_WORD_LENGTH8_T rx_wrapper_NO_OF_WORS_IN_BUFFER1_NO_OF_DATA_BITS8_ rx_buffer_WORD_SIZE8_NO_OF_WORDS1_1	191	717.516	214.481	931.99			
ins rx buffer		rx buffer WORD SIZE8 NO OF WORDS1 1	70	336.186	69.809	405.99			
ins_rx_fsm		rx_fsm_NO_OF_DATA_BITS8_PARITY_ENABLED32h54525545_	75	214.776	81.136	295.91			
		sampling_tick_generator_BAUD115200_CLOCK_IN_MHZ100	46	166.554		219.16			
ins_tx_wrapper		tx_wrapper_NO_OF_WORDS_IN_BUFFER1_NO_OF_DATA_BITS8	191			796.41			
ins_tx_fsm		tx_fsm_NO_OF_DATA_BITS8_PARITY_ENABLED32h54525545_	96		108.999	359.00			
ins_tx_buffer		tx_buffer_WORD_SIZE8_NO_OF_WORDS1_1	53	162.108		218.68			
ins_sampling_tick_g	generator	sampling_tick_generator_BAUD115200_CLOCK_IN_MHZ100	42	155.610		205.63			
ns_uart_transceiver_A		uart_transceiver_CLOCK_IN_MHZ100_TX_WORD_LENGTH8_T	382	1285.236		1728.41			
ns_uart_transceiver_A ins_rx_wrapper		rx_wrapper_NO_OF_WORS_IN_BUFFER1_NO_OF_DATA_BITS8_	191	717.516	214.481	931.99			
ins_rx_buffer		rx_buffer_WORD_SIZE8_NO_OF_WORDS1	70	336.186	69.809	405.99			
ins_rx_fsm		rx fsm NO OF DATA BITS8 PARITY ENABLED32h54525545		214.776	81.136	295.91			
		sampling tick generator BAUD115200 CLOCK IN MHZ100	46	166.554	52.608	219.16			
ins_tx_wrapper		tx_wrapper_NO_OF_WORDS_IN_BUFFER1_NO_OF_DATA_BITS8	191		228.698	796.41			
		tx_fsm_NO_OF_DATA_BITS8_PARITY_ENABLED32h54525545_	96	250.002	108.999	359.00			
		tx_buffer_WORD_SIZE8_NO_OF_WORDS1	53 42	2021200	56.580				
ins_sampting_tick_g	jenerator	sampling_tick_generator_BAUD115200_CLOCK_IN_MHZ100	42	155.610	50.023	205.63			

Figure 2 — Area Report After Scan Synthesis

Metric	Before Scan Synthesis	After Scan Synthesis
Cell Count	772	764
Cell Area	2220.948	2570.472
Net Area	946.493	987.659
Total Area	3167.441	3558.131

Table 1 — Comparison of uart_top Area Before and After Scan Synthesis

- * Cell Count: Decreased by 8 cells after scan synthesis.
- * Cell Area: Increased by 349.524 after scan synthesis.
- * Net Area: Increased by 41.166 after scan synthesis.
- * Total Area: Increased by 390.690 after scan synthesis.

Scanable Flip-Flop Area: The area of scanable flip-flops is larger compared to normal flip-flops because they contain additional multiplexers (MUX) to support scan operations

2. Comment on the number of ports before (output of the laboratory experiment 1) and after (uart_top_1.v) scan synthesis.

			o9:12:26 a	ution 18.1	0-p003_1	
	uart t		vJ.12.20 d			
		9V 125C				
	global					
		al libr	ary			
					=	
External Delays 8						
			Rise	Fall	Ext Delay	Exception
Port	Dir	Clock	Delay	Delay	0bject	Object/Type
clk a	in	clk a	0.0	no value	create clock delay domain 1 clk a R 0	N/A
_		clk_a	no_value	0.0	create_clock_delay_domain_1_clk_a_F_0	
reset_a		N/A	N/A	N/A	N/A	N/A
tx_parallel_data_in_a[7]		clk_a	6000.0			N/A
tx_parallel_data_in_a[6]	in	clk_a		6000.0	in_del_1_1	N/A
tx_parallel_data_in_a[5]	in	clk_a	6000.0	6000.0	in_del_2_1	N/A
tx_parallel_data_in_a[4]		clk_a	6000.0	6000.0	in_del_3_1	N/A
tx_parallel_data_in_a[3]		clk_a	6000.0	6000.0	in_del_4_1	N/A
tx_parallel_data_in_a[2]		clk_a	6000.0	6000.0	in_del_5_1	N/A
tx_parallel_data_in_a[1]		clk_a	6000.0	6000.0	in det 3 1 in det 3 1 in det 4 1 in det 5 1 in det 6 1 in det 7 1 in det 8 1	N/A
tx_parallel_data_in_a[0]		clk_a	6000.0	6000.0	in_del_7_1	N/A
tx_data_wr_enable_in_a		clk_a	6000.0	6000.0	in_del_8_1 in_del_9_1	N/A
rx_data_rd_enable_in_a		CCK_a	0000.0	0000.0	III_GCC_3_I	N/A
clk_b	in	clk_b		no_value	create_clock_delay_domain_1_clk_b_R_0	N/A
			no_value		create_clock_delay_domain_1_clk_b_F_0	
reset_b		N/A	N/A	N/A	N/A	N/A
tx_parallel_data_in_b[7]		clk_b	6000.0	6000.0	in_del_10_1	N/A
tx_parallel_data_in_b[6]		clk_b		6000.0	in_del_11_1	N/A
tx_parallel_data_in_b[5]	in	clk_b		6000.0	in_del_12_1	N/A
tx_parallel_data_in_b[4]		clk_b		6000.0	in_del_13_1	N/A
tx_parallel_data_in_b[3]	in	clk_b	6000.0	6000.0	in_del_14_1	N/A
tx_parallel_data_in_b[2]		clk_b			in_del_15_1	N/A
tx_parallel_data_in_b[1]		clk_b			in_del_16_1	N/A
tx_parallel_data_in_b[0]		clk_b			in_del_17_1	N/A
tx_data_wr_enable_in_b	in	clk_b	6000.0	6000.0	in_del_18_1	N/A
rx_data_rd_enable_in_b	in	clk_b	6000.0	6000.0	in_del_19_1	N/A
tx busy out a	out	clk a	6000.0	6000.0	ou del	N/A
rx full a	out	clk b	6000.0	6000.0	ou del 32 1	N/A
rx parallel data out a[7]	out	clk a	6000.0	6000.0	ou del 21 1	N/A
rx parallel data out a[6]	out	clk a	6000.0	6000.0	ou del 22 1	N/A
rx_parallel_data_out_a[5]	out	clk_a	6000.0	6000.0	ou_del_23_1	N/A
rx_parallel_data_out_a[4]			6000.0		ou_del_24_1	N/A
rx_parallel_data_out_a[3]	out	clk a	6000.0	6000.0	ou del 25 1	N/A
rx_parallel_data_out_a[2]	out	clk_a	6000.0	6000.0	ou_del_26_1	N/A
rx_parallel_data_out_a[1]	out	clk_a	6000.0	6000.0	ou_del_27_1	N/A
rx_parallel_data_out_a[0]	out	clk a		6000.0		N/A
		clk_a		6000.0		N/A
rx_stop_bit_error_a	out	clk_a		6000.0		N/A
tx_busy_out_b		clk_b			ou_del_31_1	N/A
rx full b	out	N/A	N/A	N/A	N/A	N/A
				(a)		
rx_parallel_data_out_b[7					ou_del_33_1	N/
rx_parallel_data_out_b[6		clk_b			ou_del_34_1	N/
rx_parallel_data_out_b[5		clk_b			ou_del_35_1	N/
rx_parallel_data_out_b[4] out	clk_b	6000.0	6000.0	ou_del_36_1	N/
rx parallel data out b[3] out	clk b	6000.0	6000.0	ou del 37 1	N/
rx parallel data out b[2		clk b		6000.0	ou del 38 1	N/
rx parallel data out b[1			6000.0	6000.0	ou del 39 1	N/
rx parallel data out b[0			6000.0	6000.0	ou_del_40_1	N/
rx parity error b		clk_b	6000.0	6000.0	ou_del_40_1 ou_del_41_1	N/
rx_stop_bit_error_b		clk_b	6000.0	6000.0	ou_del_42_1	N/
				(b)		

Figure 3 — Port Reports Before Scan Synthesis (Lab 1 Experiment)

Generated by:			thesis Sol			
Generated on:			02:44:12 p	m	_	
Module: Technology libraries:	uart_t	op dd1v0 1	0			
recimotogy cibraries.		ddlv0 1				
		al_cell				
Operating conditions:		9V_1250				
Interconnect mode:	global					
Area mode:	pnysic	al libr	ary		=	
External Delays 8						
			Rise	Fall	Ext Delay	Exception
Port	Dir	Clock	Delay	Delay	0bject	Object/Type
clk a	in	clk a	0.0	no value	create clock delay domain 1 clk a R 0	N/A
_			no_value		create_clock_delay_domain_1_clk_a_F_0	
reset_a	in	N/A	N/A			N/A
tx_parallel_data_in_a[7]	in	clk_a	6000.0	6000.0	in_del	N/A
tx_parallel_data_in_a[6]	in	clk_a	6000.0		in_del_1_1	N/A
<pre>tx_parallel_data_in_a[5] tx parallel data in a[4]</pre>	in in	clk_a clk_a	6000.0 6000.0		in_del_2_1 in del 3 1	N/A N/A
tx parallel data in a[3]	in	clk_a	6000.0		in del 4 1	N/A
tx parallel data in a[2]	in	clk a	6000.0		in del 5 1	N/A
tx_parallel_data_in_a[1]	in	clk_a	6000.0		in_del_6_1	N/A
tx_parallel_data_in_a[0]	in	clk_a	6000.0		in_del_7_1	N/A
tx_data_wr_enable_in_a	in	clk_a	6000.0		in_del_8_1	N/A
rx_data_rd_enable_in_a clk b	in in	clk_a	6000.0		in_del_9_1 create clock delay domain 1 clk b R 0	N/A
CCK_D	TII	clk_b	no value		create clock delay domain 1 clk b F 0	N/A
reset b	in	N/A	N/A	N/A		N/A
tx_parallel_data_in_b[7]	in	clk_b	6000.0		in_del_10_1	N/A
<pre>tx_parallel_data_in_b[6]</pre>	in	clk_b	6000.0		in_del_11_1	N/A
tx_parallel_data_in_b[5]	in	clk_b	6000.0		in_del_12_1	N/A
tx_parallel_data_in_b[4]	in	clk_b	6000.0		in_del_13_1	N/A
<pre>tx_parallel_data_in_b[3] tx parallel data in b[2]</pre>	in in	clk_b clk_b	6000.0 6000.0		in_del_14_1 in del 15 1	N/A N/A
tx parallel data in b[1]	in	clk_b	6000.0		in del 16 1	N/A
tx parallel data in b[0]		clk b	6000.0		in del 17 1	N/A
tx_data_wr_enable_in_b	in	clk_b	6000.0		in_del_18_1	N/A
rx_data_rd_enable_in_b	in	clk_b	6000.0		in_del_19_1	N/A
SE	in	N/A	N/A		N/A	N/A
tx_busy_out_a rx full a		clk_a clk_b	6000.0 6000.0		ou_del ou del 32 1	N/A N/A
rx_parallel_data_out_a[7]		clk_b	6000.0		ou del 21 1	N/A
rx parallel data out a[6]		clk a	6000.0		ou del 22 1	N/A
rx_parallel_data_out_a[5]		clk_a	6000.0		ou_del_23_1	N/A
rx_parallel_data_out_a[4]] out	clk_a	6000.0		ou_del_24_1	N/A
rx_parallel_data_out_a[3]		clk_a	6000.0		ou_del_25_1	N/A
rx_parallel_data_out_a[2]		clk_a	6000.0		ou_del_26_1 ou_del_27_1	N/A
rx_parallel_data_out_a[1] rx_parallel_data_out_a[0]		clk_a clk_a	6000.0 6000.0		ou_det_2/_1 ou_det_28_1	N/A N/A
parattot aata oat a[o	,					,
				(a)		
		-11	6000 0	` '	au dal 20 1	N / A
rx_parity_error_a		clk_a clk a	6000.0 6000.0	6000.0	ou_del_29_1	N/A
rx_stop_bit_error_a tx busy out b		clk_a	6000.0		ou_del_30_1 ou_del_31_1	N/A N/A
rx full b		N/A	N/A		N/A	N/A
rx_parallel_data_out_b[7			6000.0		ou_del_33_1	N/A
rx_parallel_data_out_b[6] out	clk_b	6000.0	6000.0	ou_del_34_1	N/A
rx_parallel_data_out_b[5	out	clk_b	6000.0		ou_del_35_1	N/A
rx_parallel_data_out_b[4]		clk_b	6000.0		ou_del_36_1	N/A
<pre>rx_parallel_data_out_b[3 rx_parallel_data_out_b[2</pre>		clk_b clk b	6000.0 6000.0	6000.0 6000.0	ou_del_37_1 ou_del_38_1	N/A N/A
rx parallel data out b[1		clk_b	6000.0	6000.0	ou del 39 1	N/A
rx parallel data out b[0]		clk b	6000.0	6000.0	ou del 40 1	N/A
rx_parity_error_b	out	clk_b	6000.0	6000.0	ou_del_41_1	N/A
rx_stop_bit_error_b	out	clk_b	6000.0	6000.0	ou_del_42_1	N/A
				(b)		
				(D)		

Figure 4 — Port Reports After Scan Synthesis

* Total Number of Ports:

– Before Scan Synthesis: 48

- After Scan Synthesis: 49

The Shift Enable (Scan Enable) (SE) port has been added to the design after the scan synthesis process as an additional port.

3. Compare how the scan input (SI) of scan cells are connected before (uart_top_1.v) and after (uart_top_2.v) scan stitching. Provide comparable code snippets to justify your answer.

```
SDFFQX2 \buffer_full_counter_reg[2] (.CK (clk), .D (n_39), .SI (buffer_full_counter[2]), .SE (1'b0), .Q (buffer_full_counter_reg[3] (.CK (clk), .D (n_40), .SI (buffer_full_counter_3]), .SE (1'b0), .Q (buffer_full_counter[3])):

Figure 5 — Before Scan Stiching
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Figure 6 — After Scan Stiching

Before scan stiching, SI (scan input) is connected to the output of the same flop while SE (scan enable/shift enable) is connected to the logic low. After scan stitching, the SI pin is connected to the data output of the preceding flop in the scan chain and the SE pin is connected to the dft_sen wire.

4.Comment on the area before (uart_top_1.v) and after (uart_top_2.v) scan stitching.

Generated by:	Genus(TM) Synthesis Solution 18.10-p003 1				
Generated by: Generated on:	Sep 12 2024 02:58:01 pm				
Module:	uart top				
Technology libraries:	slow vddlv0 1.0				
	fast vddlv0 1.0				
	physical cells				
Operating conditions:	PVT 0P9V 125C				
Interconnect mode:	global				
Area mode:	physical library				
Instance	Module	Cell Count	Cell Area	Net Area	Total Area
art top		764	2562.948	1048.744	3611.692
ins wart transceiver A	uart transceiver CLOCK IN MHZ100 TX WORD LENGTH8		1282.842	443.179	1726.021
ins rx wrapper	rx wrapper NO OF WORS IN BUFFER1 NO OF DATA BITS8		715.122	213.018	928.140
ins rx buffer	rx buffer WORD SIZE8 NO OF WORDS1	70	336.186	67.984	404.170
ins rx fsm	rx fsm NO OF DATA BITS8 PARITY ENABLED32h54525545	75	213.066	81.136	294.202
ins sampling tick g	nerator sampling tick generator BAUD115200 CLOCK IN MHZ100	9 46	165.870	52.608	218.478
ins tx wrapper	tx_wrapper_NO_OF_WORDS_IN_BUFFER1_NO_OF_DATA_BITS8	3 191	567.720	228.698	796.418
ins_tx_fsm	<pre>tx_wrapper_NO_OF_WORDS_IN_BUFFER1_NO_OF_DATA_BITS8 tx_fsm_NO_OF_DATA_BITS8_PARITY_ENABLED32h54525545</pre>	_ 96	250.002	108.999	359.001
ins_tx_buffer		53	162.108	55.117	217.225
	enerator sampling_tick_generator_BAUD115200_CLOCK_IN_MHZ100		155.610	50.023	205.633
ins_uart_transceiver_B	uart_transceiver_CLOCK_IN_MHZ100_TX_WORD_LENGTH8_1		1280.106	443.179	1723.285
ins_rx_wrapper	rx_wrapper_NO_OF_WORS_IN_BUFFER1_NO_OF_DATA_BITS8_		716.832	213.018	929.850
ins_rx_buffer	rx_buffer_WORD_SIZE8_NO_OF_WORDS1_1	70	336.186	67.984	404.170
ins_rx_fsm	rx_fsm_NO_OF_DATA_BITS8_PARITY_ENABLED32h54525545		214.776	81.136	295.912
	enerator_sampling_tick_generator_BAUD115200_CLOCK_IN_MHZ100		165.870	52.608	218.478
ins_tx_wrapper			563.274	228.698	791.972
ins_tx_fsm	tx_fsm_NO_OF_DATA_BITS8_PARITY_ENABLED32h54525545		245.556	108.999	354.555
ins_tx_buffer	tx_buffer_WORD_SIZE8_NO_OF_WORDS1_1 enerator_sampling_tick_generator_BAUD115200_CLOCK_IN_MHZ100	53	162.108	55.117	217.225
THS_Sampting_tick_g	merator sampting_tick_generator_bauditiszee_clock_in_mm21ee	42	155.610	50.023	205.633

Figure 7 — Area Report After Scan Stiching

Metric	Before Scan Stiching	After Scan Stiching
Cell Count	764	764
Cell Area	2570.472	2562.948
Net Area	987.659	1048.744
Total Area	3558.131	3611.692

Table 2 — Comparison of uart_top Area Before and After Scan Stiching

Comments

- * Cell Count: No change in cell count after scan synthesis.
- * Cell Area: Decreased by 7.524 after scan synthesis.
- * Net Area: Increased by 61.085 after scan synthesis.
- * Total Area: Increased by 53.561 after scan synthesis.

There is a slight increase in the total area because net area increases after scan stitching. The SI pin has been connected with the output of the same flop before scan stitching which could result in a shorter net length. After scan stitching, it connects with the adjacent flop in the scan chain which can be more lengthy compared to the previous case.

5. Comment on the number of ports before (uart_top_1.v) and after (uart_top_2.v) scan stitching.

Interconnect mode: Area mode: External Delays &	global physic ===== Excep	al libr ====== tions	ary		=	
External Delays &	Excep	tions			=	
External Delays &	Excep	tions				
Port						
Port						
		Clock	Rise Delay	Fall Delay	Ext Delay Object	Exception Object/Typ
		clk_a	0.0	no_value	create_clock_delay_domain_1 clk_a_R	
eset a	in	N/A	no_value N/A	N/A	create_clock_delay_domain_1_clk_a_F_	9 N/
x parallel data in a[7]		clk a	6000.0	6000.0		N/
x parallel data in a[6]		clk a	6000.0		in del 1 1	N/
x_parallel_data_in_a[5]		clk a	6000.0	6000.0	in del 2 1	N/
tx_parallel_data_in_a[4]		clk_a	6000.0	6000.0	in_del_3_1 in_del_4_1	N/
x_parallel_data_in_a[3]		clk_a	6000.0	6000.0	in_del_4_1	N/
x_parallel_data_in_a[2]		clk_a			in_del_5_1	N/
x_parallel_data_in_a[1]		clk_a			in_del_6_1	N/
:x_parallel_data_in_a[0] :x data wr enable in a		clk_a clk a	6000.0 6000.0		in_del_7_1 in_del_8_1	N/ N/
x data_wr_enable_in_a		clk_a	6000.0		in del 9 1	N/
:lk b	in	clk_b			create clock delay domain 1 clk b R	
_			no_value		create clock delay domain 1 clk b F	
eset_b	in	N/A	N/A	N/A	N/A	N/
x_parallel_data_in_b[7]		clk_b	6000.0	6000.0	in_del_10_1	N/
x_parallel_data_in_b[6]		clk_b	6000.0		in_del_11_1	N/
x_parallel_data_in_b[5]		clk_b	6000.0		in_del_12_1	N/
x_parallel_data_in_b[4]		clk_b			in_del_13_1	N/
x_parallel_data_in_b[3] x_parallel_data_in_b[2]		clk_b clk_b	6000.0 6000.0		in_del_14_1 in_del_15_1	N/ N/
x parallel data in b[1]		clk_b			in_del_16_1	N/
x parallel data in b[0]		clk b			in del 17 1	N/
x data wr enable in b		clk b	6000.0	6000.0	in del 18 1	N/
x_data_rd_enable_in_b	in	clk_b	6000.0	6000.0	in_del_18_1 in_del_19_1	N/
E .		N/A	N/A	N/A		N/
can_in_a	in	N/A	N/A	N/A		N/
scan_in_b	in	N/A	N/A	N/A		N/
x_busy_out_a x full a		clk_a clk b	6000.0 6000.0	6000.0 6000.0	ou del 32 1	N/
x parallel data out a[7]		clk a	6000.0		ou del 21 1	N/
x parallel data out a[6]		clk a	6000.0		ou del 22 1	N/
x parallel data out a[5]		clk a	6000.0		ou del 23 1	N/
x_parallel_data_out_a[4]		clk_a			ou_del_24_1	N/
x_parallel_data_out_a[3]	out	clk_a	6000.0		ou_del_25_1	N/
x_parallel_data_out_a[2]		clk_a	6000.0		ou_del_26_1	N/
rx_parallel_data_out_a[1]		clk_a	6000.0		ou_del_27_1	N/
rx_parallel_data_out_a[0] rx parity error a		clk_a clk a	6000.0 6000.0		ou_del_28_1 ou_del_29_1	N/ N/
				(a)		
rx_stop_bit_error_a		clk_a	6000.0	6000.0	ou_del_30_1	N/
tx_busy_out_b		clk_b	6000.0	6000.0		N/
rx_full_b rv_narallel_data_out_b[7]		N/A	N/A	N/A		N/
rx_parallel_data_out_b[7] rx_parallel_data_out_b[6]		clk_b	6000.0 6000.0	6000.0 6000.0		N/ N/
rx parallel data out b[5]		clk b	6000.0	6000.0		N/
rx_parallel_data_out_b[4]		clk b	6000.0	6000.0	ou del 36 1	N/
rx_parallel_data_out_b[3]		clk_b	6000.0	6000.0	ou_del_37_1	N/
rx_parallel_data_out_b[2]	out	clk_b	6000.0	6000.0	ou_del_38_1	N/
rx_parallel_data_out_b[1]		clk_b	6000.0	6000.0	ou_del_39_1	N/
rx_parallel_data_out_b[0]		clk_b	6000.0	6000.0	ou_del_40_1	N/
rx_parity_error_b	out	clk_b	6000.0	6000.0	ou_del_41_1	N/
rx_stop_bit_error_b	out	clk_b	6000.0	6000.0	ou_del_42_1	N/
scan_out_a scan_out_b	out	N/A N/A	N/A N/A	N/A N/A	N/A N/A	N/
scan_out_b	out	N/A	N/A	N/A	11/15	N/

Figure 8 — Port Reports After Scan Stitching

Comments

- * Total Number of Ports:
- Before Scan Stiching: 49

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- After Scan Synthesis: 53

sacn_in_a, scan_in_b, scan_out_a, and scan_out_b ports have been added to the design after the scan stiching process as additional ports.

6. Reiterate through the steps, but do the necessary changes in the design flow to create two scan chains per transceiver along with dedicated scan I/O ports. A single port may be used for scan enable. Use the define_scan_chain and connect_scan_chains commands to achieve this.

```
@genus:root: 23> define scan_chain -name top_chain_a0 -sdi scan_in_a0 -sdo scan_out_a0 -non_shared_output -create_ports -domain clk_a
Pin or port 'scan_in_a0' not found.
Pin or port 'scan_out_a0' not found.
scan_chain:uart top/top_chain_a0
@genus:root: 24> define scan_chain -name top_chain_a1 -sdi scan_in_a1 -sdo scan_out_a1 -non_shared_output -create_ports -domain clk_a
Pin or port 'scan_in_a1' not found.
Pin or port 'scan_out_a1' not found.
scan_chain:uart top/top_chain_a1
@genus:root: 25> define_scan_chain -name top_chain_b0 -sdi scan_in_b0 -sdo scan_out_b0 -non_shared_output -create_ports -domain clk_b
Pin or port 'scan_in_b0' not found.
Pin or port 'scan_in_b0' not found.
Pin or port 'scan_out_b0' not found.
Pin or port 'scan_out_b0' not found.

@genus:root: 26> define_scan_chain -name top_chain_b1 -sdi scan_in_b1 -sdo scan_out_b1 -non_shared_output -create_ports -domain clk_b
Pin or port 'scan_in_b1' not found.
Pin or port 'scan_in_b1' not found.
Pin or port 'scan_out_b1' not found.
```

Figure 9 — Define Four Scan Chains

Figure 10 — Summary of Four Scan Chains

```
Departing a Sear Childre (most year)

Chair 1: top Childre (most year)

Chair 1: top Childre (most year)

Local Action | Sear Childre (most year)

Local Childre (most year)

Local
```

(a) Portion of Scan Chain Report (4 Scan Chains)

```
User Chain:

User Chain:

object name: top_chain_a0

scan-in: scan_in_a0

scan-in: scan_in_a0

scan-out hookup_pin: scan_out_a0

shared out: false

shift enable object name: none

max length: no value

complete: false

test_Clock domain: clk, a

test_Clock domain: clk, a

scan-in: scan_in_a1

scan-in: scan_in_a1

scan-in nookup_pin: scan_out_a1

scan-in: scan_in_a1

scan-in hookup_pin: scan_out_a1

scan-in hookup_pin: scan_out_a1

shared out: false

shift enable object name: none

max length: no value

complete: false

test_Clock domain: clk, a

test_Clock domain: clk, a

test_Clock domain: object name: none

max length: no value

complete: false

test_Clock domain: clk, a

test_Clock domain: clk, a

test_Clock domain: clk, a

test_Clock domain: scan_in_b0

scan-in: scan_in_b0

scan-in: scan_in_b0

scan-in: scan_in_b0

scan-in: object name: none

max length: no value

complete: false

shift enable object name: none

max length: no value

complete: false

shift enable object name: none

max length: no value

complete: ralse

test_Clock domain: clk, b

test_Clock domain: clk, b

scan-out hookup_pin: scan_out_b1

scan-in: scan_in_b1

scan-in: scan_in_b1

scan-in: scan_in_b1

scan-out hookup_pin: scan_out_b1

scan-out hookup_pin: scan_out_b1

scan-in: scan_in_b1

scan-out hookup_pin: scan_out_b1

scan-in: scan_in_b1

scan-out hookup_pin: scan_out_b1

scan-out_bookup.out_scan_out_b2

scan-out_hookup.out_scan_out_b2

scan-out_hookup.out_scan_out_b3

scan-out_hookup.out_scan_out_b4

scan-out_hookup.out_scan_out_b2

scan-out_hookup.out_scan_out_b4

scan-out_hookup.out_scan_out_b4

scan-out_hookup.out_scan_out_b4

scan-out_hookup.out_scan_out_b4

scan-out_hookup.out_scan_out_b4

scan-out_hookup.out_scan_out_b4

scan-out_hookup.out_scan_out_b4

scan-out_hookup.out_scan_out_b4

scan-out_hookup.out_scan_out_b4

scan-out_ho
```

(b) Scan Set Up (4 Scan Chains)

Generated by:	Genus(TM) Synthesis So	lution 18.10-p003 1						
	Sep 30 2024 10:39:25 am							
Module:								
Operating conditions:								
	global							
Area mode:	physical library							
Instance		Module	Cell Count	Cell Area	Net Area	Total Area		
art top			764	2562.948	1050.227	3613.175		
ins uart transceiver A	uart transceiv	er CLOCK IN MHZ100 TX WORD LENGTH8 T	382	1282.842	441.354	1724.196		
ins rx wrapper	rx wrapper NO	er_CLOCK_IN_MHZ100_TX_WORD_LENGTH8_T OF_WORS_IN_BUFFER1_NO_OF_DATA_BITS8_	191	715.122	211.193	926.315		
ins rx buffer	rx buffer WORD	SIZE8_NO_OF_WORDS1	70	336.186	67.984	404.170		
ins rx fsm	rx fsm NO OF D	ATA BITS8 PARITY ENABLED32h54525545	75	213.066	81.136	294.202		
ins sampling tick ge	nerator sampling tick	generator BAUD115200 CLOCK IN MHZ100	46	165.870	50.784	216.654		
ins tx wrapper	tx wrapper NO	OF WORDS IN BUFFER1 NO OF DATA BITS8 ATA_BITS8_PARITY_ENABLED32h54525545_	191	567.720	228.698	796.418		
ins tx fsm	tx fsm NO OF D	ATA BITS8 PARITY ENABLED32h54525545	96	250.002	108.999	359.001		
ins tx buffer	tx buffer WORD	SIZE8 NO OF WORDS1	53	162.108	55.117	217.225		
ins sampling tick ge	nerator sampling tick	generator BAUD115200 CLOCK IN MHZ100	42	155.610	50.023	205.633		
ins uart transceiver B	uart transceiv	er CLOCK IN MHZ100 TX WORD LENGTH8 T	382	1280.106	441.354	1721.460		
ins rx wrapper	rx wrapper NO	OF WORS IN BUFFER1 NO OF DATA BITS8	191	716.832	211.193	928.025		
ins_rx_buffer	rx buffer WORD	er CLOCK IN MHZ100 TX WORD LENGTHS T OF WORS IN BUFFER1 NO OF DATA BITSS SIZES NO OF WORDS1 1	70	336.186	67.984	404.170		
ins rx rsm	TX TSM NO OF D	AIA BIIS8 PARIIY ENABLED32N54525545	/5	214.776	81.136	295.912		
ins_sampling_tick_ge	nerator sampling_tick_	generator_BAUD115200_CLOCK_IN_MHZ100	46	165.870	50.784	216.654		
ins tx wrapper	tx wrapper NO	OF_WORDS_IN_BUFFER1_NO_OF_DATA_BITS8	191	563.274	228.698	791.972		
ins tx fsm	tx fsm NO OF D	ATA BITS8 PARITY ENABLED32h54525545	96	245.556	108.999	354.555		
	tx_buffer_WORD		53	162.108	55.117	217.225		
ine compling tick go	nerator campling tick	generator BAUD115200 CLOCK IN MHZ100	42	155.610	50.023	205.633		

Figure 12 — Area Report (4 Scan Chains)

Parameter	2 Scan Chains	4 Scan Chains
Number of Cells	764	764
Cell Area (sq units)	2562.948	2562.948
Net Area (sq units)	1048.744	1050.227
Total Area (sq units)	3611.692	3613.175

Table 3 — Area Comparison Between Two and Four Scan Chains

- * Total Area Increase: The total area for the four-scan-chain design is slightly larger than that of the two-scan-chain design. This minor increase is due to a small change in the net area.
- * Number of Cells: Despite adding more scan chains, the number of cells remains constant at 764. This indicates that the scan chains are rerouted across the same set of cells.
- * Cell Area: The cell area is identical for both designs, which implies that the scan chains do not impact the internal cell area directly.
- * Net Area Increase: The net area slightly increases from 1048.744 to 1050.227 square units, reflecting the addition of more interconnections for the extra scan chains.

Module: Operating conditions: Interconnect mode:	Sep 30 uart_t PVT_0P global physic	2024 cop 9V_125C	10:41:42 a	m		
					-	
External Delays &						
Port	Dir	Clock	Rise Delay		Ext Delay Object	Exception Object/Type
:lk_a	in	clk_a	0.0	no_value	create_clock_delay_domain_1_clk_a_R_0	N/A
eset a	in	N/A	N/A	N/A	create_clock_delay_domain_1_clk_a_F_0 N/A	N/A
reset a x parallel data in a[7] x parallel data in a[6] x parallel data in a[5] x parallel data in a[4] xx parallel data in a[3] xx parallel data in a[2] xx parallel data in a[2]	in	clk_a	6000.0	6000.0	in del	N/A
x_parallel_data_in_a[6]	in	clk_a	6000.0	6000.0	in_del_1_1	N/A
x_parallel_data_in_a[5]	in	clk_a	6000.0	6000.0	in_del_2_1	N/A
x_parallel_data_in_a[4]	in	clk_a	6000.0	6000.0	in_del_3_1	N/A
x_parallel_data_in_a[3]	in	clk_a	6000.0	6000.0	in_del_4_1	N/A
x_parallel_data_in_a[2]	in	clk_a	6000.0	6000.0	in_del_5_1	N/A
x_parallel_data_in_a[1]	in	clk_a	6000.0	6000.0	in_del_6_1	N/A
x parattet uata in alal						N/A
x_data_wr_enable_in_a	in	cik_a	6000.0	6000.0	in_del_8_1 in_del_9_1 create_clock_delay_domain_1_clk_b_R_0	N/A
'x data rd enable in a	in	clk_a	6000.0	6000.0	in det 9 1	N/A
:lk_b		clk_b			create_clock_delay_domain_1_clk_b_R_0 create_clock_delay_domain_1_clk_b_F_0 N/A	N/A
reset_b		N/A	no_value N/A 6000.0	N/A	N/A	N/A
x_parallel_data_in_b[7]	in	clk b	6000.0	6000.0	in del 10-1	N/A
x_parallel_data_in_b[6]		clk_b	6000.0	6000.0	in_del_11_1	N/A
x_parallel_data_in_b[5]	in	clk_b	6000.0	6000.0	in_del_12_1	N/A
x_parallel_data_in_b[4] x_parallel_data_in_b[3]	in	clk_b	6000.0	6000.0	in_del_13_1 in_del_14_1 in_del_15_1	N/A
x_parallel_data_in_b[3]				6000.0	in_del_14_1	N/A
x_parallel_data_in_b[2]	in	clk_b	6000.0	6000.0	in_del_15_1	N/A N/A
x_parallel_data_in_b[1] x_parallel_data_in_b[0]	in	clk_b	6000.0	6000.0	in_del_15_1 in_del_17_1 in_del_18_1 in_del_19_1	N/A
x data wr enable in b	in	clk_b	6000.0	6888 8	in del 18 1	N/A
x_data_wr_enable_in_b rx_data_rd_enable_in_b	in	clk b	6000.0	6000.0	in del 19 1	N/A
SE	in	N/A	N/A	N/A	N/A	N/A
can_in_a0	in	N/A			N/A	N/A
can in al	in	N/A	N/A	N/A	N/A N/A N/A ou_del ou_del_32_1 ou_del_21_1	N/A
can in b0	in	N/A	N/A	N/A	N/A	N/A
can in b1	in	N/A	N/A	N/A	N/A	N/A
x_busy_out_a	out	clk_a	6000.0	6000.0	ou_del	N/A
x full a	out	clk_b	6000.0	6000.0	ou_del_32_1	N/A
x_parallel_data_out_a[7]	out	clk_a	6000.0	6000.0	ou_del_21_1	N/A
x_parallel_data_out_a[6]	out	clk a	6000.0	6000.0	ou del 22 1	N/A
x_parallel_data_out_a[5]	out	clk_a	6000.0	6000.0	ou_del_23_1	N/A
x_parallel_data_out_a[5] x_parallel_data_out_a[4] x_parallel_data_out_a[3]	out	clk_a	6000.0	6000.0	ou_del_23_1 ou_del_24_1 ou_del_25_1	N/A
x_parallel_data_out_a[3] x parallel data out a[2]	out	clk_a	6000.0	6000.0	ou del 26 1	N/A N/A
x_parallel_data_out_a[1]			6000.0	6000.0	ou_del_27_1	N/A
				(a))	
rx_parallel_data_out_a[θ]	out	clk_a	6000.0	6000.0	ou_del_28_1	N/A
rx_parattet_data_out_a[e] rx_parity_error_a rx_stop_bit_error_a	out	clk_a			ou_del_29_1	N/A
rx_stop_bit_error_a	out	clk_a	6000.0	6000.0	ou_del_30_1	N/A
tx_busy_out_b rx full b	out	clk_b	6000.0 N/A	6000.0	ou_del_31_1	N/A
rx_τuιι_b rx parallel data out b[7]	out	N/A	N/A 6000 0	N/A 6000 0	N/A ou del 33 1	N/A N/A
rx_parallel_data_out_b[7] rx_parallel_data_out_b[6]					ou_det_33_1 ou_det_34_1	N/A N/A
rx parallel data out his	out	clk b	6000.0	6000.0	ou_del_35_1	N/A
rx_parallel_data_out_b[5] rx_parallel_data_out_b[4]	out	clk b	6000.0	6000.0	ou del 36 1	N/A
rx parallel data out b[3]	out	clk b	6000.0	6000.0	ou del 37 1	N/A
rx parallel data out b[2]	out	clk b	6000.0	6000.0	ou del 38 1	N/A
rx_parallel_data_out_b[1] rx_parallel_data_out_b[0]	out	clk b	6000.0	6000.0		N/A
rx_parallel_data_out_b[0]	out	clk_b	6000.0	6000.0	ou_del_39_1 ou_del_40_1	N/A
rx_parity_error_b	out	clk_b	6000.0	6000.0	ou del 41 1	N/A
rx_parallel_data_out_b[0] rx_parity_error_b rx_stop_bit_error_b scan_out_a0	out	clk_b	6000.0	6000.0	ou_del_42_1	N/A
scan_out_a0	out	N/A N/A	N/A N/A	N/A		N/A
scan_out_a1 scan_out_b0	out	N/A N/A	N/A N/A			N/A N/A
scan_out_b0 scan_out_b1		N/A	N/A	N/A N/A	N/A	N/A N/A
	Jul	11/11	11/ /	N/A	.,	N/A

Figure 13 — Port Report (4 Scan Chains)

1.1 Port Comparison Between Two and Four Scan Chains

Parameter	2 Scan Chains	4 Scan Chains
Total Number of Ports	53	57

Table 4 — Port Comparison Between Two and Four Scan Chains

- * Port Increase: The design with four scan chains introduces four additional ports compared to the design with two scan chains. This includes two scan inputs and two scan outputs.
- 7. In a pad-limited design, using an absolute minimum number of ports is crucial. Assuming the design has 32 scan chains, which results in 65 scan I/O ports (32 SDI + 32 SDO + 1 scan_en), suggest a method to reduce the total number of scan I/O ports to less than 10. You may add additional logic/registers into the design. Provide an explanation of the method.

To optimize a pad-limited design with 32 scan chains, the number of scan I/O ports can be reduced using multiplexing and demultiplexing techniques:

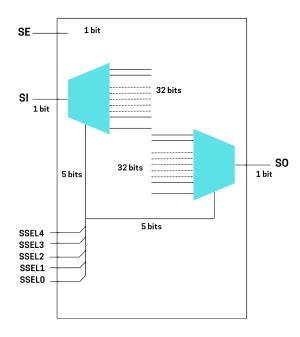


Figure 14 — Scan I/O ports using multiplexing and demultiplexing techniques

- * Scan-in port: A single scan-in port is multiplexed to serve all 32 scan chains, controlled by 5 select bits.
- * Scan-out port: A single scan-out port is demultiplexed to handle the output from the 32 scan chains, using 5 select bits for control.
- * Scan chain selection: 5 select bits (SSEL[4:0]) are used to select which scan chain is active at any given time. Only one scan chain is tested at a time.
- * Total ports required: The design requires a total of 8 ports, broken down as follows:
- 1 scan-in port (SI)

- 1 scan-out port (SO)
- 1 scan enable port (SE)
- 5 scan select bits (SSEL[4:0])

This optimization reduces the scan I/O port count from 65 to 8, meeting the design requirement of having fewer than 10 ports, making it ideal for pad-limited designs.

Calculations

$$1 + \frac{2 \times 32}{2^n} + n < 10 \tag{1}$$

$$1 + 2^{6-n} + n < 10 (2)$$

for n = 1:

$$1 + 2^5 + 1 < 10 \tag{3}$$

$$34 < 10 \tag{4}$$

$$contradiction$$
 (5)

for n = 2:

$$1 + 2^4 + 2 < 10 \tag{6}$$

$$19 < 10 \tag{7}$$

$$contradiction$$
 (8)

for n = 3:

$$1 + 2^3 + 3 < 10 \tag{9}$$

$$11 < 10 \tag{10}$$

$$contradiction$$
 (11)

for n = 4:

$$1 + 2^2 + 4 < 10 \tag{12}$$

$$9 < 10 \tag{13}$$

$$possible$$
 (14)

for n = 5:

$$1 + 2^1 + 5 < 10 (15)$$

$$8 < 10 \tag{16}$$

$$posssible$$
 (17)