Department of Electronic & Telecommunication Engineering
University of Moratuwa

EN4604 - DIGITAL IC DESIGN

LABORATORY EXPERIMENT 2: DFT INSERTION

Supervisors:
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Group No :- 07

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This report is submitted as the fulfillment of Lab - 02 of module EN4604

1 EXERCISE

1. Comment on the area before (output of the laboratory experiment 1) and after (`uart_top_1.v`) scan synthesis.

```
=============================================================
  Generated by:           Genus(TM) Synthesis Solution 18.10-p003_1
  Generated on:           Sep 12 2024  09:11:26 am
  Module:                 uart_top
  Technology libraries:   slow_vdd1v0 1.0
                          fast_vdd1v0 1.0
                          physical_cells
  Operating conditions:   PVT_0P9V_125C
  Interconnect mode:      global
  Area mode:              physical library
=============================================================

            Instance                                  Module                        Cell Count  Cell Area  Net Area   Total Area
-------------------------------------------------------------------------------------------------------------------------------
uart_top                                                                                 772   2220.948   946.493     3167.441
  ins_uart_transceiver_B          uart_transceiver_CLOCK_IN_MHZ100_TX_WORD_LENGTH8_T     386   1110.474   423.318     1533.792
    ins_rx_wrapper                rx_wrapper_NO_OF_WORS_IN_BUFFER1_NO_OF_DATA_BITS8_     197    621.072   209.103      830.175
      ins_rx_buffer               rx_buffer_WORD_SIZE8_NO_OF_WORDS1_1                     67    292.068    61.047      353.115
      ins_rx_fsm                  rx_fsm_NO_OF_DATA_BITS8_PARITY_ENABLED32h54525545_      74    180.918    77.867      258.785
      ins_sampling_tick_generator sampling_tick_generator_BAUD115200_CLOCK_IN_MHZ100      56    148.086    62.149      210.235
    ins_tx_wrapper                tx_wrapper_NO_OF_WORDS_IN_BUFFER1_NO_OF_DATA_BITS8     189    489.402   214.215      703.617
      ins_tx_fsm                  tx_fsm_NO_OF_DATA_BITS8_PARITY_ENABLED32h54525545_      94    210.330   103.544      313.874
      ins_tx_buffer               tx_buffer_WORD_SIZE8_NO_OF_WORDS1_1                     53    146.718    52.247      198.965
      ins_sampling_tick_generator sampling_tick_generator_BAUD115200_CLOCK_IN_MHZ100      42    132.354    46.412      178.766
  ins_uart_transceiver_A          uart_transceiver_CLOCK_IN_MHZ100_TX_WORD_LENGTH8_T     386   1110.474   423.318     1533.792
    ins_rx_wrapper                rx_wrapper_NO_OF_WORS_IN_BUFFER1_NO_OF_DATA_BITS8_     197    621.072   209.103      830.175
      ins_rx_buffer               rx_buffer_WORD_SIZE8_NO_OF_WORDS1                       67    292.068    61.047      353.115
      ins_rx_fsm                  rx_fsm_NO_OF_DATA_BITS8_PARITY_ENABLED32h54525545_      74    180.918    77.867      258.785
      ins_sampling_tick_generator sampling_tick_generator_BAUD115200_CLOCK_IN_MHZ100      56    148.086    62.149      210.235
    ins_tx_wrapper                tx_wrapper_NO_OF_WORDS_IN_BUFFER1_NO_OF_DATA_BITS8     189    489.402   214.215      703.617
      ins_tx_fsm                  tx_fsm_NO_OF_DATA_BITS8_PARITY_ENABLED32h54525545_      94    210.330   103.544      313.874
      ins_tx_buffer               tx_buffer_WORD_SIZE8_NO_OF_WORDS1                       53    146.718    52.247      198.965
      ins_sampling_tick_generator sampling_tick_generator_BAUD115200_CLOCK_IN_MHZ100      42    132.354    46.412      178.766
```

Figure 1 — Area Report Before Scan Synthesis (Lab 1 Experiment)

```
=============================================================
  Generated by:           Genus(TM) Synthesis Solution 18.10-p003_1
  Generated on:           Sep 12 2024  02:42:45 pm
  Module:                 uart_top
  Technology libraries:   slow_vdd1v0 1.0
                          fast_vdd1v0 1.0
                          physical_cells
  Operating conditions:   PVT_0P9V_125C
  Interconnect mode:      global
  Area mode:              physical library
=============================================================

            Instance                                  Module                        Cell Count  Cell Area  Net Area   Total Area
-------------------------------------------------------------------------------------------------------------------------------
uart_top                                                                                 764   2570.472   987.659     3558.131
  ins_uart_transceiver_B          uart_transceiver_CLOCK_IN_MHZ100_TX_WORD_LENGTH8_T     382   1285.236   443.179     1728.415
    ins_rx_wrapper                rx_wrapper_NO_OF_WORS_IN_BUFFER1_NO_OF_DATA_BITS8_     191    717.516   214.481      931.997
      ins_rx_buffer               rx_buffer_WORD_SIZE8_NO_OF_WORDS1_1                     70    336.186    69.809      405.995
      ins_rx_fsm                  rx_fsm_NO_OF_DATA_BITS8_PARITY_ENABLED32h54525545_      75    214.776    81.136      295.912
      ins_sampling_tick_generator sampling_tick_generator_BAUD115200_CLOCK_IN_MHZ100      46    166.554    52.608      219.162
    ins_tx_wrapper                tx_wrapper_NO_OF_WORDS_IN_BUFFER1_NO_OF_DATA_BITS8     191    567.720   228.698      796.418
      ins_tx_fsm                  tx_fsm_NO_OF_DATA_BITS8_PARITY_ENABLED32h54525545_      96    250.002   108.999      359.001
      ins_tx_buffer               tx_buffer_WORD_SIZE8_NO_OF_WORDS1_1                     53    162.108    56.580      218.688
      ins_sampling_tick_generator sampling_tick_generator_BAUD115200_CLOCK_IN_MHZ100      42    155.610    50.023      205.633
  ins_uart_transceiver_A          uart_transceiver_CLOCK_IN_MHZ100_TX_WORD_LENGTH8_T     382   1285.236   443.179     1728.415
    ins_rx_wrapper                rx_wrapper_NO_OF_WORS_IN_BUFFER1_NO_OF_DATA_BITS8_     191    717.516   214.481      931.997
      ins_rx_buffer               rx_buffer_WORD_SIZE8_NO_OF_WORDS1                       70    336.186    69.809      405.995
      ins_rx_fsm                  rx_fsm_NO_OF_DATA_BITS8_PARITY_ENABLED32h54525545_      75    214.776    81.136      295.912
      ins_sampling_tick_generator sampling_tick_generator_BAUD115200_CLOCK_IN_MHZ100      46    166.554    52.608      219.162
    ins_tx_wrapper                tx_wrapper_NO_OF_WORDS_IN_BUFFER1_NO_OF_DATA_BITS8     191    567.720   228.698      796.418
      ins_tx_fsm                  tx_fsm_NO_OF_DATA_BITS8_PARITY_ENABLED32h54525545_      96    250.002   108.999      359.001
      ins_tx_buffer               tx_buffer_WORD_SIZE8_NO_OF_WORDS1                       53    162.108    56.580      218.688
      ins_sampling_tick_generator sampling_tick_generator_BAUD115200_CLOCK_IN_MHZ100      42    155.610    50.023      205.633
```

Figure 2 — Area Report After Scan Synthesis

Metric	Before Scan Synthesis	After Scan Synthesis
Cell Count	772	764
Cell Area	2220.948	2570.472
Net Area	946.493	987.659
Total Area	3167.441	3558.131

Table 1 — Comparison of `uart_top` Area Before and After Scan Synthesis

Comments

* **Cell Count**: Decreased by 8 cells after scan synthesis.
* **Cell Area**: Increased by 349.524 after scan synthesis.
* **Net Area**: Increased by 41.166 after scan synthesis.
* **Total Area**: Increased by 390.690 after scan synthesis.

Scanable Flip-Flop Area: The area of scanable flip-flops is larger compared to normal flip-flops because they contain additional multiplexers (MUX) to support scan operations

2. Comment on the number of ports before (output of the laboratory experiment 1) and after (`uart_top_1.v`) scan synthesis.

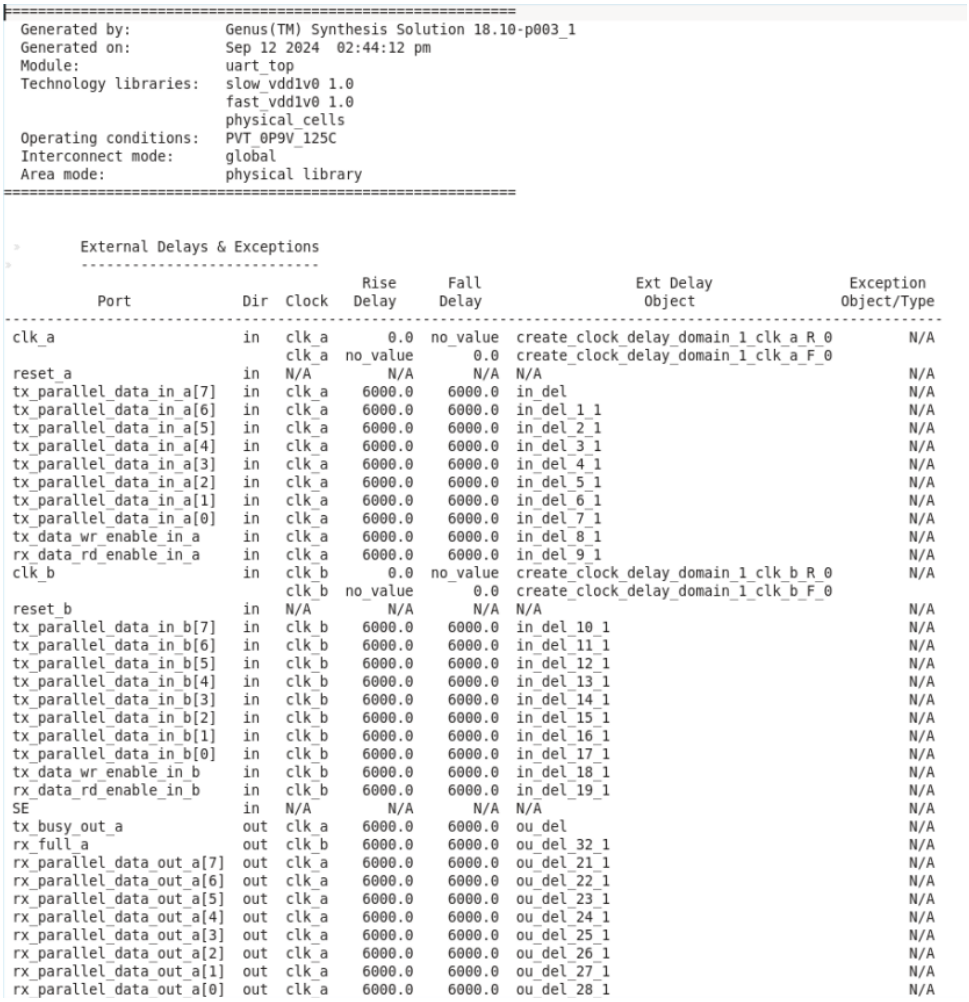
```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 18.10-p003_1
  Generated on:           Sep 12 2024  09:12:26 am
  Module:                 uart_top
  Operating conditions:   PVT_0P9V_125C
  Interconnect mode:      global
  Area mode:              physical library
============================================================


      External Delays & Exceptions
      ----------------------------
                                    Rise      Fall                 Ext Delay               Exception
        Port             Dir  Clock  Delay     Delay                 Object                Object/Type
-------------------------------------------------------------------------------------------------------
clk_a                    in   clk_a       0.0  no_value  create_clock_delay_domain_1_clk_a_R_0         N/A
                              clk_a  no_value       0.0  create_clock_delay_domain_1_clk_a_F_0
reset_a                  in   N/A         N/A       N/A  N/A                                           N/A
tx_parallel_data_in_a[7] in   clk_a    6000.0    6000.0  in_del                                        N/A
tx_parallel_data_in_a[6] in   clk_a    6000.0    6000.0  in_del_1_1                                    N/A
tx_parallel_data_in_a[5] in   clk_a    6000.0    6000.0  in_del_2_1                                    N/A
tx_parallel_data_in_a[4] in   clk_a    6000.0    6000.0  in_del_3_1                                    N/A
tx_parallel_data_in_a[3] in   clk_a    6000.0    6000.0  in_del_4_1                                    N/A
tx_parallel_data_in_a[2] in   clk_a    6000.0    6000.0  in_del_5_1                                    N/A
tx_parallel_data_in_a[1] in   clk_a    6000.0    6000.0  in_del_6_1                                    N/A
tx_parallel_data_in_a[0] in   clk_a    6000.0    6000.0  in_del_7_1                                    N/A
tx_data_wr_enable_in_a   in   clk_a    6000.0    6000.0  in_del_8_1                                    N/A
rx_data_rd_enable_in_a   in   clk_a    6000.0    6000.0  in_del_9_1                                    N/A
clk_b                    in   clk_b       0.0  no_value  create_clock_delay_domain_1_clk_b_R_0         N/A
                              clk_b  no_value       0.0  create_clock_delay_domain_1_clk_b_F_0
reset_b                  in   N/A         N/A       N/A  N/A                                           N/A
tx_parallel_data_in_b[7] in   clk_b    6000.0    6000.0  in_del_10_1                                   N/A
tx_parallel_data_in_b[6] in   clk_b    6000.0    6000.0  in_del_11_1                                   N/A
tx_parallel_data_in_b[5] in   clk_b    6000.0    6000.0  in_del_12_1                                   N/A
tx_parallel_data_in_b[4] in   clk_b    6000.0    6000.0  in_del_13_1                                   N/A
tx_parallel_data_in_b[3] in   clk_b    6000.0    6000.0  in_del_14_1                                   N/A
tx_parallel_data_in_b[2] in   clk_b    6000.0    6000.0  in_del_15_1                                   N/A
tx_parallel_data_in_b[1] in   clk_b    6000.0    6000.0  in_del_16_1                                   N/A
tx_parallel_data_in_b[0] in   clk_b    6000.0    6000.0  in_del_17_1                                   N/A
tx_data_wr_enable_in_b   in   clk_b    6000.0    6000.0  in_del_18_1                                   N/A
rx_data_rd_enable_in_b   in   clk_b    6000.0    6000.0  in_del_19_1                                   N/A
tx_busy_out_a            out  clk_a    6000.0    6000.0  ou_del                                        N/A
rx_full_a                out  clk_b    6000.0    6000.0  ou_del_32_1                                   N/A
rx_parallel_data_out_a[7] out  clk_a    6000.0    6000.0  ou_del_21_1                                   N/A
rx_parallel_data_out_a[6] out  clk_a    6000.0    6000.0  ou_del_22_1                                   N/A
rx_parallel_data_out_a[5] out  clk_a    6000.0    6000.0  ou_del_23_1                                   N/A
rx_parallel_data_out_a[4] out  clk_a    6000.0    6000.0  ou_del_24_1                                   N/A
rx_parallel_data_out_a[3] out  clk_a    6000.0    6000.0  ou_del_25_1                                   N/A
rx_parallel_data_out_a[2] out  clk_a    6000.0    6000.0  ou_del_26_1                                   N/A
rx_parallel_data_out_a[1] out  clk_a    6000.0    6000.0  ou_del_27_1                                   N/A
rx_parallel_data_out_a[0] out  clk_a    6000.0    6000.0  ou_del_28_1                                   N/A
rx_parity_error_a        out  clk_a    6000.0    6000.0  ou_del_29_1                                   N/A
rx_stop_bit_error_a      out  clk_a    6000.0    6000.0  ou_del_30_1                                   N/A
tx_busy_out_b            out  clk_b    6000.0    6000.0  ou_del_31_1                                   N/A
rx_full_b                out  N/A         N/A       N/A  N/A                                           N/A
```

(a)

```
rx_parallel_data_out_b[7] out  clk_b    6000.0    6000.0  ou_del_33_1                                   N/A
rx_parallel_data_out_b[6] out  clk_b    6000.0    6000.0  ou_del_34_1                                   N/A
rx_parallel_data_out_b[5] out  clk_b    6000.0    6000.0  ou_del_35_1                                   N/A
rx_parallel_data_out_b[4] out  clk_b    6000.0    6000.0  ou_del_36_1                                   N/A
rx_parallel_data_out_b[3] out  clk_b    6000.0    6000.0  ou_del_37_1                                   N/A
rx_parallel_data_out_b[2] out  clk_b    6000.0    6000.0  ou_del_38_1                                   N/A
rx_parallel_data_out_b[1] out  clk_b    6000.0    6000.0  ou_del_39_1                                   N/A
rx_parallel_data_out_b[0] out  clk_b    6000.0    6000.0  ou_del_40_1                                   N/A
rx_parity_error_b        out  clk_b    6000.0    6000.0  ou_del_41_1                                   N/A
rx_stop_bit_error_b      out  clk_b    6000.0    6000.0  ou_del_42_1                                   N/A
```

(b)

Figure 3 — Port Reports Before Scan Synthesis (Lab 1 Experiment)



```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 18.10-p003_1
  Generated on:           Sep 12 2024  02:44:12 pm
  Module:                 uart_top
  Technology libraries:   slow_vdd1v0 1.0
                          fast_vdd1v0 1.0
                          physical_cells
  Operating conditions:   PVT_0P9V_125C
  Interconnect mode:      global
  Area mode:              physical library
============================================================


      External Delays & Exceptions
      ----------------------------
                                        Rise      Fall                 Ext Delay               Exception
        Port              Dir  Clock    Delay     Delay                 Object                Object/Type
-------------------------------------------------------------------------------------------------------
clk_a                     in   clk_a       0.0  no_value  create_clock_delay_domain_1_clk_a_R_0         N/A
                               clk_a  no_value       0.0  create_clock_delay_domain_1_clk_a_F_0
reset_a                   in   N/A         N/A       N/A  N/A                                           N/A
tx_parallel_data_in_a[7]  in   clk_a    6000.0    6000.0  in_del                                        N/A
tx_parallel_data_in_a[6]  in   clk_a    6000.0    6000.0  in_del_1_1                                    N/A
tx_parallel_data_in_a[5]  in   clk_a    6000.0    6000.0  in_del_2_1                                    N/A
tx_parallel_data_in_a[4]  in   clk_a    6000.0    6000.0  in_del_3_1                                    N/A
tx_parallel_data_in_a[3]  in   clk_a    6000.0    6000.0  in_del_4_1                                    N/A
tx_parallel_data_in_a[2]  in   clk_a    6000.0    6000.0  in_del_5_1                                    N/A
tx_parallel_data_in_a[1]  in   clk_a    6000.0    6000.0  in_del_6_1                                    N/A
tx_parallel_data_in_a[0]  in   clk_a    6000.0    6000.0  in_del_7_1                                    N/A
tx_data_wr_enable_in_a    in   clk_a    6000.0    6000.0  in_del_8_1                                    N/A
rx_data_rd_enable_in_a    in   clk_a    6000.0    6000.0  in_del_9_1                                    N/A
clk_b                     in   clk_b       0.0  no_value  create_clock_delay_domain_1_clk_b_R_0         N/A
                               clk_b  no_value       0.0  create_clock_delay_domain_1_clk_b_F_0
reset_b                   in   N/A         N/A       N/A  N/A                                           N/A
tx_parallel_data_in_b[7]  in   clk_b    6000.0    6000.0  in_del_10_1                                   N/A
tx_parallel_data_in_b[6]  in   clk_b    6000.0    6000.0  in_del_11_1                                   N/A
tx_parallel_data_in_b[5]  in   clk_b    6000.0    6000.0  in_del_12_1                                   N/A
tx_parallel_data_in_b[4]  in   clk_b    6000.0    6000.0  in_del_13_1                                   N/A
tx_parallel_data_in_b[3]  in   clk_b    6000.0    6000.0  in_del_14_1                                   N/A
tx_parallel_data_in_b[2]  in   clk_b    6000.0    6000.0  in_del_15_1                                   N/A
tx_parallel_data_in_b[1]  in   clk_b    6000.0    6000.0  in_del_16_1                                   N/A
tx_parallel_data_in_b[0]  in   clk_b    6000.0    6000.0  in_del_17_1                                   N/A
tx_data_wr_enable_in_b    in   clk_b    6000.0    6000.0  in_del_18_1                                   N/A
rx_data_rd_enable_in_b    in   clk_b    6000.0    6000.0  in_del_19_1                                   N/A
SE                        in   N/A         N/A       N/A  N/A                                           N/A
tx_busy_out_a             out  clk_a    6000.0    6000.0  ou_del                                        N/A
rx_full_a                 out  clk_b    6000.0    6000.0  ou_del_32_1                                   N/A
rx_parallel_data_out_a[7] out  clk_a    6000.0    6000.0  ou_del_21_1                                   N/A
rx_parallel_data_out_a[6] out  clk_a    6000.0    6000.0  ou_del_22_1                                   N/A
rx_parallel_data_out_a[5] out  clk_a    6000.0    6000.0  ou_del_23_1                                   N/A
rx_parallel_data_out_a[4] out  clk_a    6000.0    6000.0  ou_del_24_1                                   N/A
rx_parallel_data_out_a[3] out  clk_a    6000.0    6000.0  ou_del_25_1                                   N/A
rx_parallel_data_out_a[2] out  clk_a    6000.0    6000.0  ou_del_26_1                                   N/A
rx_parallel_data_out_a[1] out  clk_a    6000.0    6000.0  ou_del_27_1                                   N/A
rx_parallel_data_out_a[0] out  clk_a    6000.0    6000.0  ou_del_28_1                                   N/A
```

(a)

```
rx_parity_error_a         out  clk_a    6000.0    6000.0  ou_del_29_1                                   N/A
rx_stop_bit_error_a       out  clk_a    6000.0    6000.0  ou_del_30_1                                   N/A
tx_busy_out_b             out  clk_b    6000.0    6000.0  ou_del_31_1                                   N/A
rx_full_b                 out  N/A         N/A       N/A  N/A                                           N/A
rx_parallel_data_out_b[7] out  clk_b    6000.0    6000.0  ou_del_33_1                                   N/A
rx_parallel_data_out_b[6] out  clk_b    6000.0    6000.0  ou_del_34_1                                   N/A
rx_parallel_data_out_b[5] out  clk_b    6000.0    6000.0  ou_del_35_1                                   N/A
rx_parallel_data_out_b[4] out  clk_b    6000.0    6000.0  ou_del_36_1                                   N/A
rx_parallel_data_out_b[3] out  clk_b    6000.0    6000.0  ou_del_37_1                                   N/A
rx_parallel_data_out_b[2] out  clk_b    6000.0    6000.0  ou_del_38_1                                   N/A
rx_parallel_data_out_b[1] out  clk_b    6000.0    6000.0  ou_del_39_1                                   N/A
rx_parallel_data_out_b[0] out  clk_b    6000.0    6000.0  ou_del_40_1                                   N/A
rx_parity_error_b         out  clk_b    6000.0    6000.0  ou_del_41_1                                   N/A
rx_stop_bit_error_b       out  clk_b    6000.0    6000.0  ou_del_42_1                                   N/A
```

(b)

Figure 4 — Port Reports After Scan Synthesis

Comments

* **Total Number of Ports:**

– Before Scan Synthesis: 48

– After Scan Synthesis: 49

The Shift Enable (Scan Enable) (SE) port has been added to the design after the scan synthesis process as an additional port.

3. Compare how the scan input (SI) of scan cells are connected before (`uart_top_1.v`) and after (`uart_top_2.v`) scan stitching. Provide comparable code snippets to justify your answer.

```
SDFFQX2 \buffer_full_counter_reg[2] (.CK (clk), .D (n_39), .SI
     (buffer_full_counter[2]), .SE (1'b0), .Q
     (buffer_full_counter[2]));
SDFFQX1 \buffer_full_counter_reg[3] (.CK (clk), .D (n_40), .SI
     (buffer_full_counter[3]), .SE (1'b0), .Q
     (buffer_full_counter[3]));
```

Figure 5 — Before Scan Stiching

```
SDFFQX2 \buffer_full_counter_reg[2] (.CK (clk), .D (n_39), .SI
     (buffer_full_counter[1]), .SE (dft_sen), .Q
     (buffer_full_counter[2]));
SDFFQX1 \buffer_full_counter_reg[3] (.CK (clk), .D (n_40), .SI
     (buffer_full_counter[2]), .SE (dft_sen), .Q
     (buffer_full_counter[3]));
```

Figure 6 — After Scan Stiching

Before scan stiching, SI (scan input) is connected to the output of the same flop while SE (scan enable/shift enable) is connected to the logic low. After scan stitching, the SI pin is connected to the data output of the preceding flop in the scan chain and the SE pin is connected to the dft_sen wire.

4.Comment on the area before (`uart_top_1.v`) and after (`uart_top_2.v`) scan stitching.

```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 18.10-p003_1
  Generated on:           Sep 12 2024  02:58:01 pm
  Module:                 uart_top
  Technology libraries:   slow_vdd1v0 1.0
                          fast_vdd1v0 1.0
                          physical_cells
  Operating conditions:   PVT_0P9V_125C
  Interconnect mode:      global
  Area mode:              physical library
============================================================

          Instance                                  Module                      Cell Count  Cell Area  Net Area   Total Area
-------------------------------------------------------------------------------------------------------------------------
uart_top                                                                            764   2562.948  1048.744     3611.692
  ins_uart_transceiver_A         uart_transceiver_CLOCK_IN_MHZ100_TX_WORD_LENGTH8_T  382   1282.842   443.179     1726.021
    ins_rx_wrapper               rx_wrapper_NO_OF_WORS_IN_BUFFER1_NO_OF_DATA_BITS8_  191    715.122   213.018      928.140
      ins_rx_buffer              rx_buffer_WORD_SIZE8_NO_OF_WORDS1                    70    336.186    67.984      404.170
      ins_rx_fsm                 rx_fsm_NO_OF_DATA_BITS8_PARITY_ENABLED32h54525545_   75    213.066    81.136      294.202
      ins_sampling_tick_generator sampling_tick_generator_BAUD115200_CLOCK_IN_MHZ100  46    165.870    52.608      218.478
    ins_tx_wrapper               tx_wrapper_NO_OF_WORDS_IN_BUFFER1_NO_OF_DATA_BITS8  191    567.720   228.698      796.418
      ins_tx_fsm                 tx_fsm_NO_OF_DATA_BITS8_PARITY_ENABLED32h54525545_   96    250.002   108.999      359.001
      ins_tx_buffer              tx_buffer_WORD_SIZE8_NO_OF_WORDS1                    53    162.108    55.117      217.225
      ins_sampling_tick_generator sampling_tick_generator_BAUD115200_CLOCK_IN_MHZ100  42    155.610    50.023      205.633
  ins_uart_transceiver_B         uart_transceiver_CLOCK_IN_MHZ100_TX_WORD_LENGTH8_T  382   1280.106   443.179     1723.285
    ins_rx_wrapper               rx_wrapper_NO_OF_WORS_IN_BUFFER1_NO_OF_DATA_BITS8_  191    716.832   213.018      929.850
      ins_rx_buffer              rx_buffer_WORD_SIZE8_NO_OF_WORDS1_1                  70    336.186    67.984      404.170
      ins_rx_fsm                 rx_fsm_NO_OF_DATA_BITS8_PARITY_ENABLED32h54525545_   75    214.776    81.136      295.912
      ins_sampling_tick_generator sampling_tick_generator_BAUD115200_CLOCK_IN_MHZ100  46    165.870    52.608      218.478
    ins_tx_wrapper               tx_wrapper_NO_OF_WORDS_IN_BUFFER1_NO_OF_DATA_BITS8  191    563.274   228.698      791.972
      ins_tx_fsm                 tx_fsm_NO_OF_DATA_BITS8_PARITY_ENABLED32h54525545_   96    245.556   108.999      354.555
      ins_tx_buffer              tx_buffer_WORD_SIZE8_NO_OF_WORDS1_1                  53    162.108    55.117      217.225
      ins_sampling_tick_generator sampling_tick_generator_BAUD115200_CLOCK_IN_MHZ100  42    155.610    50.023      205.633
```

Figure 7 — Area Report After Scan Stiching

Metric	Before Scan Stiching	After Scan Stiching
Cell Count	764	764
Cell Area	2570.472	2562.948
Net Area	987.659	1048.744
Total Area	3558.131	3611.692

Table 2 — Comparison of `uart_top` Area Before and After Scan Stiching

Comments

* **Cell Count**: No change in cell count after scan synthesis.
* **Cell Area**: Decreased by 7.524 after scan synthesis.
* **Net Area**: Increased by 61.085 after scan synthesis.
* **Total Area**: Increased by 53.561 after scan synthesis.

There is a slight increase in the total area because net area increases after scan stitching. The SI pin has been connected with the output of the same flop before scan stitching which could result in a shorter net length. After scan stitching, it connects with the adjacent flop in the scan chain which can be more lengthy compared to the previous case.

5. Comment on the number of ports before (`uart_top_1.v`) and after (`uart_top_2.v`) scan stitching.

```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 18.10-p003_1
  Generated on:           Sep 12 2024  02:59:16 pm
  Module:                 uart_top
  Operating conditions:   PVT_0P9V_125C
  Interconnect mode:      global
  Area mode:              physical library
============================================================


       External Delays & Exceptions
       ----------------------------
                                          Rise      Fall                Ext Delay               Exception
         Port             Dir  Clock     Delay     Delay                 Object                Object/Type
-------------------------------------------------------------------------------------------------------
clk_a                     in   clk_a       0.0  no_value  create_clock_delay_domain_1_clk_a_R_0         N/A
                               clk_a  no_value       0.0  create_clock_delay_domain_1_clk_a_F_0
reset_a                   in   N/A         N/A       N/A  N/A                                           N/A
tx_parallel_data_in_a[7]  in   clk_a    6000.0    6000.0  in_del                                        N/A
tx_parallel_data_in_a[6]  in   clk_a    6000.0    6000.0  in_del_1_1                                    N/A
tx_parallel_data_in_a[5]  in   clk_a    6000.0    6000.0  in_del_2_1                                    N/A
tx_parallel_data_in_a[4]  in   clk_a    6000.0    6000.0  in_del_3_1                                    N/A
tx_parallel_data_in_a[3]  in   clk_a    6000.0    6000.0  in_del_4_1                                    N/A
tx_parallel_data_in_a[2]  in   clk_a    6000.0    6000.0  in_del_5_1                                    N/A
tx_parallel_data_in_a[1]  in   clk_a    6000.0    6000.0  in_del_6_1                                    N/A
tx_parallel_data_in_a[0]  in   clk_a    6000.0    6000.0  in_del_7_1                                    N/A
tx_data_wr_enable_in_a    in   clk_a    6000.0    6000.0  in_del_8_1                                    N/A
rx_data_rd_enable_in_a    in   clk_a    6000.0    6000.0  in_del_9_1                                    N/A
clk_b                     in   clk_b       0.0  no_value  create_clock_delay_domain_1_clk_b_R_0         N/A
                               clk_b  no_value       0.0  create_clock_delay_domain_1_clk_b_F_0
reset_b                   in   N/A         N/A       N/A  N/A                                           N/A
tx_parallel_data_in_b[7]  in   clk_b    6000.0    6000.0  in_del_10_1                                   N/A
tx_parallel_data_in_b[6]  in   clk_b    6000.0    6000.0  in_del_11_1                                   N/A
tx_parallel_data_in_b[5]  in   clk_b    6000.0    6000.0  in_del_12_1                                   N/A
tx_parallel_data_in_b[4]  in   clk_b    6000.0    6000.0  in_del_13_1                                   N/A
tx_parallel_data_in_b[3]  in   clk_b    6000.0    6000.0  in_del_14_1                                   N/A
tx_parallel_data_in_b[2]  in   clk_b    6000.0    6000.0  in_del_15_1                                   N/A
tx_parallel_data_in_b[1]  in   clk_b    6000.0    6000.0  in_del_16_1                                   N/A
tx_parallel_data_in_b[0]  in   clk_b    6000.0    6000.0  in_del_17_1                                   N/A
tx_data_wr_enable_in_b    in   clk_b    6000.0    6000.0  in_del_18_1                                   N/A
rx_data_rd_enable_in_b    in   clk_b    6000.0    6000.0  in_del_19_1                                   N/A
SE                        in   N/A         N/A       N/A  N/A                                           N/A
scan_in_a                 in   N/A         N/A       N/A  N/A                                           N/A
scan_in_b                 in   N/A         N/A       N/A  N/A                                           N/A
tx_busy_out_a             out  clk_a    6000.0    6000.0  ou_del                                        N/A
rx_full_a                 out  clk_b    6000.0    6000.0  ou_del_32_1                                   N/A
rx_parallel_data_out_a[7] out  clk_a    6000.0    6000.0  ou_del_21_1                                   N/A
rx_parallel_data_out_a[6] out  clk_a    6000.0    6000.0  ou_del_22_1                                   N/A
rx_parallel_data_out_a[5] out  clk_a    6000.0    6000.0  ou_del_23_1                                   N/A
rx_parallel_data_out_a[4] out  clk_a    6000.0    6000.0  ou_del_24_1                                   N/A
rx_parallel_data_out_a[3] out  clk_a    6000.0    6000.0  ou_del_25_1                                   N/A
rx_parallel_data_out_a[2] out  clk_a    6000.0    6000.0  ou_del_26_1                                   N/A
rx_parallel_data_out_a[1] out  clk_a    6000.0    6000.0  ou_del_27_1                                   N/A
rx_parallel_data_out_a[0] out  clk_a    6000.0    6000.0  ou_del_28_1                                   N/A
rx_parity_error_a         out  clk_a    6000.0    6000.0  ou_del_29_1                                   N/A
```

(a)

```
rx_stop_bit_error_a       out  clk_a    6000.0    6000.0  ou_del_30_1                                   N/A
tx_busy_out_b             out  clk_b    6000.0    6000.0  ou_del_31_1                                   N/A
rx_full_b                 out  N/A         N/A       N/A  N/A                                           N/A
rx_parallel_data_out_b[7] out  clk_b    6000.0    6000.0  ou_del_33_1                                   N/A
rx_parallel_data_out_b[6] out  clk_b    6000.0    6000.0  ou_del_34_1                                   N/A
rx_parallel_data_out_b[5] out  clk_b    6000.0    6000.0  ou_del_35_1                                   N/A
rx_parallel_data_out_b[4] out  clk_b    6000.0    6000.0  ou_del_36_1                                   N/A
rx_parallel_data_out_b[3] out  clk_b    6000.0    6000.0  ou_del_37_1                                   N/A
rx_parallel_data_out_b[2] out  clk_b    6000.0    6000.0  ou_del_38_1                                   N/A
rx_parallel_data_out_b[1] out  clk_b    6000.0    6000.0  ou_del_39_1                                   N/A
rx_parallel_data_out_b[0] out  clk_b    6000.0    6000.0  ou_del_40_1                                   N/A
rx_parity_error_b         out  clk_b    6000.0    6000.0  ou_del_41_1                                   N/A
rx_stop_bit_error_b       out  clk_b    6000.0    6000.0  ou_del_42_1                                   N/A
scan_out_a                out  N/A         N/A       N/A  N/A                                           N/A
scan_out_b                out  N/A         N/A       N/A  N/A                                           N/A
```

(b)

Figure 8 — Port Reports After Scan Stitching

Comments

* **Total Number of Ports:**

– Before Scan Stiching: 49

– After Scan Synthesis: 53

sacn_in_a, scan_in_b, scan_out_a, and scan_out_b ports have been added to the design after the scan stiching process as additional ports.

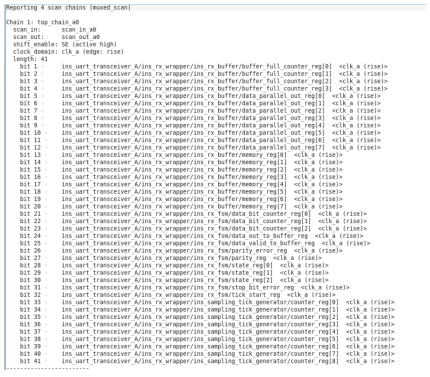
6. Reiterate through the steps, but do the necessary changes in the design flow to create two scan chains per transceiver along with dedicated scan I/O ports. A single port may be used for scan enable. Use the `define_scan_chain` and `connect_scan_chains` commands to achieve this.

```
@genus:root: 23> define_scan_chain -name top_chain_a0 -sdi scan_in_a0 -sdo scan_out_a0 -non_shared_output -create_ports -domain clk_a
Pin or port 'scan_in_a0' not found.
Pin or port 'scan_out_a0' not found.
scan_chain:uart_top/top_chain_a0
@genus:root: 24> define_scan_chain -name top_chain_a1 -sdi scan_in_a1 -sdo scan_out_a1 -non_shared_output -create_ports -domain clk_a
Pin or port 'scan_in_a1' not found.
Pin or port 'scan_out_a1' not found.
scan_chain:uart_top/top_chain_a1
@genus:root: 25> define_scan_chain -name top_chain_b0 -sdi scan_in_b0 -sdo scan_out_b0 -non_shared_output -create_ports -domain clk_b
Pin or port 'scan_in_b0' not found.
Pin or port 'scan_out_b0' not found.
scan_chain:uart_top/top_chain_b0
@genus:root: 26> define_scan_chain -name top_chain_b1 -sdi scan_in_b1 -sdo scan_out_b1 -non_shared_output -create_ports -domain clk_b
Pin or port 'scan_in_b1' not found.
Pin or port 'scan_out_b1' not found.
scan_chain:uart_top/top_chain_b1
```

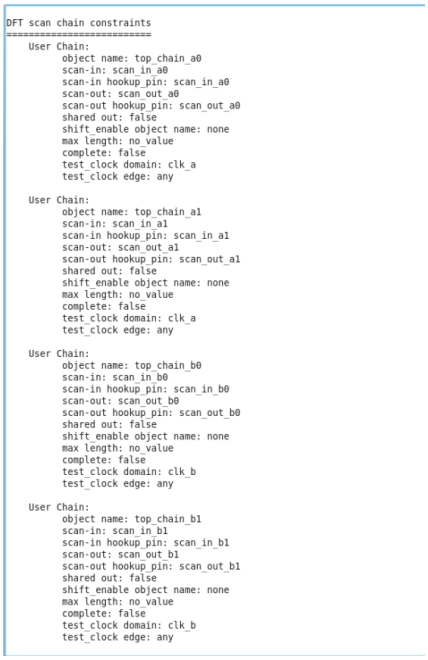
Figure 9 — Define Four Scan Chains

```
@genus:root: 27> connect_scan_chains -preview -auto_create_chains
  Starting DFT Scan Configuration for module 'uart_top' in 'normal' mode, with physical flow OFF
  Configuring 4 chains for 164 scan f/f
  Configured 2 chains for Domain: 'clk_a', edge: 'rising'
         top_chain_a0 (scan_in_a0 -> scan_out_a0) has 41 registers; Domain:clk_a, edge: rising
         top_chain_a1 (scan_in_a1 -> scan_out_a1) has 41 registers; Domain:clk_a, edge: rising
  Configured 2 chains for Domain: 'clk_b', edge: 'rising'
         top_chain_b0 (scan_in_b0 -> scan_out_b0) has 41 registers; Domain:clk_b, edge: rising
         top_chain_b1 (scan_in_b1 -> scan_out_b1) has 41 registers; Domain:clk_b, edge: rising
Processing 4 scan chains in 'muxed_scan' style.
Default shift enable signal is 'SE': 'port:uart_top/SE' active high.
4
```

Figure 10 — Summary of Four Scan Chains

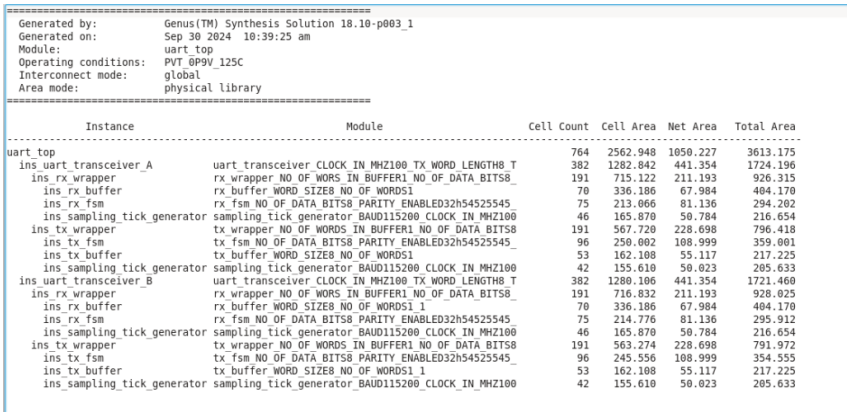


(a) Portion of Scan Chain Report (4 Scan Chains)



(b) Scan Set Up (4 Scan Chains)

Figure 11



```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 18.10-p003_1
  Generated on:           Sep 30 2024  10:39:25 am
  Module:                 uart_top
  Operating conditions:   PVT_0P9V_125C
  Interconnect mode:      global
  Area mode:              physical library
============================================================

            Instance                                  Module                        Cell Count  Cell Area  Net Area   Total Area
-------------------------------------------------------------------------------------------------------------------------------
uart_top                                                                                764   2562.948  1050.227     3613.175
  ins_uart_transceiver_A          uart_transceiver_CLOCK_IN_MHZ100_TX_WORD_LENGTH8_T    382   1282.842   441.354     1724.196
    ins_rx_wrapper                rx_wrapper_NO_OF_WORS_IN_BUFFER1_NO_OF_DATA_BITS8_    191    715.122   211.193      926.315
      ins_rx_buffer               rx_buffer_WORD_SIZE8_NO_OF_WORDS1                      70    336.186    67.984      404.170
      ins_rx_fsm                  rx_fsm_NO_OF_DATA_BITS8_PARITY_ENABLED32h54525545_     75    213.066    81.136      294.202
      ins_sampling_tick_generator sampling_tick_generator_BAUD115200_CLOCK_IN_MHZ100     46    165.870    50.784      216.654
    ins_tx_wrapper                tx_wrapper_NO_OF_WORDS_IN_BUFFER1_NO_OF_DATA_BITS8    191    567.720   228.698      796.418
      ins_tx_fsm                  tx_fsm_NO_OF_DATA_BITS8_PARITY_ENABLED32h54525545_     96    250.002   108.999      359.001
      ins_tx_buffer               tx_buffer_WORD_SIZE8_NO_OF_WORDS1                      53    162.108    55.117      217.225
      ins_sampling_tick_generator sampling_tick_generator_BAUD115200_CLOCK_IN_MHZ100     42    155.610    50.023      205.633
  ins_uart_transceiver_B          uart_transceiver_CLOCK_IN_MHZ100_TX_WORD_LENGTH8_T    382   1280.106   441.354     1721.460
    ins_rx_wrapper                rx_wrapper_NO_OF_WORS_IN_BUFFER1_NO_OF_DATA_BITS8_    191    716.832   211.193      928.025
      ins_rx_buffer               rx_buffer_WORD_SIZE8_NO_OF_WORDS1_1                    70    336.186    67.984      404.170
      ins_rx_fsm                  rx_fsm_NO_OF_DATA_BITS8_PARITY_ENABLED32h54525545_     75    214.776    81.136      295.912
      ins_sampling_tick_generator sampling_tick_generator_BAUD115200_CLOCK_IN_MHZ100     46    165.870    50.784      216.654
    ins_tx_wrapper                tx_wrapper_NO_OF_WORDS_IN_BUFFER1_NO_OF_DATA_BITS8    191    563.274   228.698      791.972
      ins_tx_fsm                  tx_fsm_NO_OF_DATA_BITS8_PARITY_ENABLED32h54525545_     96    245.556   108.999      354.555
      ins_tx_buffer               tx_buffer_WORD_SIZE8_NO_OF_WORDS1_1                    53    162.108    55.117      217.225
      ins_sampling_tick_generator sampling_tick_generator_BAUD115200_CLOCK_IN_MHZ100     42    155.610    50.023      205.633
```

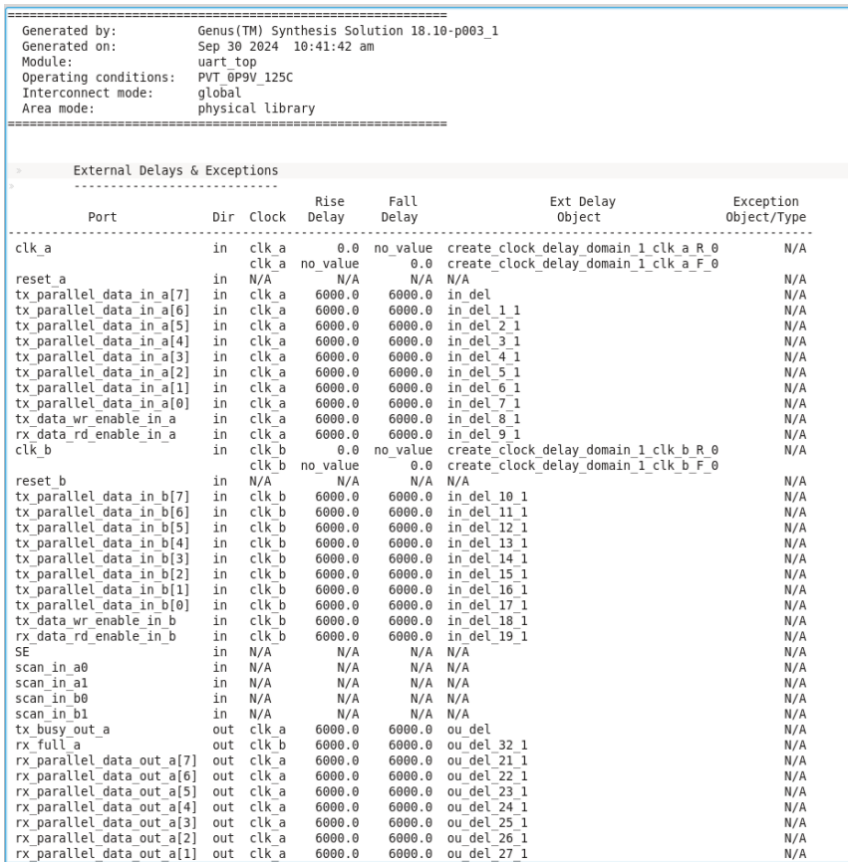
Figure 12 — Area Report (4 Scan Chains)

Parameter	**2 Scan Chains**	**4 Scan Chains**
Number of Cells	764	764
Cell Area (sq units)	2562.948	2562.948
Net Area (sq units)	1048.744	1050.227
Total Area (sq units)	3611.692	3613.175

Table 3 — Area Comparison Between Two and Four Scan Chains

Comments

* **Total Area Increase:** The total area for the four-scan-chain design is slightly larger than that of the two-scan-chain design. This minor increase is due to a small change in the net area.
* **Number of Cells:** Despite adding more scan chains, the number of cells remains constant at 764. This indicates that the scan chains are rerouted across the same set of cells.
* **Cell Area:** The cell area is identical for both designs, which implies that the scan chains do not impact the internal cell area directly.
* **Net Area Increase:** The net area slightly increases from 1048.744 to 1050.227 square units, reflecting the addition of more interconnections for the extra scan chains.



```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 18.10-p003_1
  Generated on:           Sep 30 2024  10:41:42 am
  Module:                 uart_top
  Operating conditions:   PVT_0P9V_125C
  Interconnect mode:      global
  Area mode:              physical library
============================================================


       External Delays & Exceptions
       ----------------------------
                                        Rise      Fall                 Ext Delay               Exception
          Port             Dir  Clock   Delay     Delay                 Object                Object/Type
-------------------------------------------------------------------------------------------------------
clk_a                      in   clk_a       0.0  no_value  create_clock_delay_domain_1_clk_a_R_0         N/A
                                clk_a  no_value        0.0  create_clock_delay_domain_1_clk_a_F_0
reset_a                    in   N/A         N/A       N/A  N/A                                           N/A
tx_parallel_data_in_a[7]   in   clk_a    6000.0    6000.0  in_del                                        N/A
tx_parallel_data_in_a[6]   in   clk_a    6000.0    6000.0  in_del_1_1                                    N/A
tx_parallel_data_in_a[5]   in   clk_a    6000.0    6000.0  in_del_2_1                                    N/A
tx_parallel_data_in_a[4]   in   clk_a    6000.0    6000.0  in_del_3_1                                    N/A
tx_parallel_data_in_a[3]   in   clk_a    6000.0    6000.0  in_del_4_1                                    N/A
tx_parallel_data_in_a[2]   in   clk_a    6000.0    6000.0  in_del_5_1                                    N/A
tx_parallel_data_in_a[1]   in   clk_a    6000.0    6000.0  in_del_6_1                                    N/A
tx_parallel_data_in_a[0]   in   clk_a    6000.0    6000.0  in_del_7_1                                    N/A
tx_data_wr_enable_in_a     in   clk_a    6000.0    6000.0  in_del_8_1                                    N/A
rx_data_rd_enable_in_a     in   clk_a    6000.0    6000.0  in_del_9_1                                    N/A
clk_b                      in   clk_b       0.0  no_value  create_clock_delay_domain_1_clk_b_R_0         N/A
                                clk_b  no_value        0.0  create_clock_delay_domain_1_clk_b_F_0
reset_b                    in   N/A         N/A       N/A  N/A                                           N/A
tx_parallel_data_in_b[7]   in   clk_b    6000.0    6000.0  in_del_10_1                                   N/A
tx_parallel_data_in_b[6]   in   clk_b    6000.0    6000.0  in_del_11_1                                   N/A
tx_parallel_data_in_b[5]   in   clk_b    6000.0    6000.0  in_del_12_1                                   N/A
tx_parallel_data_in_b[4]   in   clk_b    6000.0    6000.0  in_del_13_1                                   N/A
tx_parallel_data_in_b[3]   in   clk_b    6000.0    6000.0  in_del_14_1                                   N/A
tx_parallel_data_in_b[2]   in   clk_b    6000.0    6000.0  in_del_15_1                                   N/A
tx_parallel_data_in_b[1]   in   clk_b    6000.0    6000.0  in_del_16_1                                   N/A
tx_parallel_data_in_b[0]   in   clk_b    6000.0    6000.0  in_del_17_1                                   N/A
tx_data_wr_enable_in_b     in   clk_b    6000.0    6000.0  in_del_18_1                                   N/A
rx_data_rd_enable_in_b     in   clk_b    6000.0    6000.0  in_del_19_1                                   N/A
SE                         in   N/A         N/A       N/A  N/A                                           N/A
scan_in_a0                 in   N/A         N/A       N/A  N/A                                           N/A
scan_in_a1                 in   N/A         N/A       N/A  N/A                                           N/A
scan_in_b0                 in   N/A         N/A       N/A  N/A                                           N/A
scan_in_b1                 in   N/A         N/A       N/A  N/A                                           N/A
tx_busy_out_a              out  clk_a    6000.0    6000.0  ou_del                                        N/A
rx_full_a                  out  clk_b    6000.0    6000.0  ou_del_32_1                                   N/A
rx_parallel_data_out_a[7]  out  clk_a    6000.0    6000.0  ou_del_21_1                                   N/A
rx_parallel_data_out_a[6]  out  clk_a    6000.0    6000.0  ou_del_22_1                                   N/A
rx_parallel_data_out_a[5]  out  clk_a    6000.0    6000.0  ou_del_23_1                                   N/A
rx_parallel_data_out_a[4]  out  clk_a    6000.0    6000.0  ou_del_24_1                                   N/A
rx_parallel_data_out_a[3]  out  clk_a    6000.0    6000.0  ou_del_25_1                                   N/A
rx_parallel_data_out_a[2]  out  clk_a    6000.0    6000.0  ou_del_26_1                                   N/A
rx_parallel_data_out_a[1]  out  clk_a    6000.0    6000.0  ou_del_27_1                                   N/A
```

(a)

```
rx_parallel_data_out_a[0]  out  clk_a    6000.0    6000.0  ou_del_28_1                                   N/A
rx_parity_error_a          out  clk_a    6000.0    6000.0  ou_del_29_1                                   N/A
rx_stop_bit_error_a        out  clk_a    6000.0    6000.0  ou_del_30_1                                   N/A
tx_busy_out_b              out  clk_b    6000.0    6000.0  ou_del_31_1                                   N/A
rx_full_b                  out  N/A         N/A       N/A  N/A                                           N/A
rx_parallel_data_out_b[7]  out  clk_b    6000.0    6000.0  ou_del_33_1                                   N/A
rx_parallel_data_out_b[6]  out  clk_b    6000.0    6000.0  ou_del_34_1                                   N/A
rx_parallel_data_out_b[5]  out  clk_b    6000.0    6000.0  ou_del_35_1                                   N/A
rx_parallel_data_out_b[4]  out  clk_b    6000.0    6000.0  ou_del_36_1                                   N/A
rx_parallel_data_out_b[3]  out  clk_b    6000.0    6000.0  ou_del_37_1                                   N/A
rx_parallel_data_out_b[2]  out  clk_b    6000.0    6000.0  ou_del_38_1                                   N/A
rx_parallel_data_out_b[1]  out  clk_b    6000.0    6000.0  ou_del_39_1                                   N/A
rx_parallel_data_out_b[0]  out  clk_b    6000.0    6000.0  ou_del_40_1                                   N/A
rx_parity_error_b          out  clk_b    6000.0    6000.0  ou_del_41_1                                   N/A
rx_stop_bit_error_b        out  clk_b    6000.0    6000.0  ou_del_42_1                                   N/A
scan_out_a0                out  N/A         N/A       N/A  N/A                                           N/A
scan_out_a1                out  N/A         N/A       N/A  N/A                                           N/A
scan_out_b0                out  N/A         N/A       N/A  N/A                                           N/A
scan_out_b1                out  N/A         N/A       N/A  N/A                                           N/A
```

(b)

Figure 13 — Port Report (4 Scan Chains)

1.1 Port Comparison Between Two and Four Scan Chains

Parameter	**2 Scan Chains**	**4 Scan Chains**
Total Number of Ports	53	57

Table 4 — Port Comparison Between Two and Four Scan Chains

Comments

* **Port Increase:** The design with four scan chains introduces four additional ports compared to the design with two scan chains. This includes two scan inputs and two scan outputs.

7. In a pad-limited design, using an absolute minimum number of ports is crucial. Assuming the design has 32 scan chains, which results in 65 scan I/O ports (32 SDI + 32 SDO + 1 scan_en), suggest a method to reduce the total number of scan I/O ports to less than 10. You may add additional logic/registers into the design. Provide an explanation of the method.

To optimize a pad-limited design with 32 scan chains, the number of scan I/O ports can be reduced using multiplexing and demultiplexing techniques:

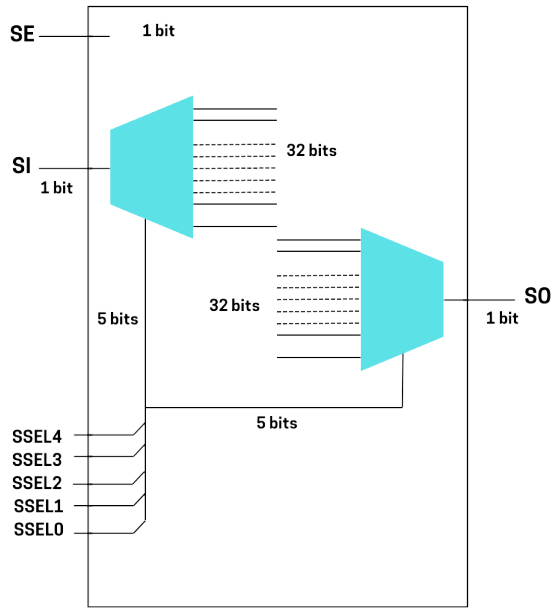


Figure 14 — Scan I/O ports using multiplexing and demultiplexing techniques

* **Scan-in port:** A single scan-in port is multiplexed to serve all 32 scan chains, controlled by 5 select bits.
* **Scan-out port:** A single scan-out port is demultiplexed to handle the output from the 32 scan chains, using 5 select bits for control.
* **Scan chain selection:** 5 select bits (`SSEL[4:0]`) are used to select which scan chain is active at any given time. Only one scan chain is tested at a time.
* **Total ports required:** The design requires a total of 8 ports, broken down as follows:

– 1 scan-in port (`SI`)

- 1 scan-out port (`SO`)
- 1 scan enable port (`SE`)
- 5 scan select bits (`SSEL[4:0]`)

This optimization reduces the scan I/O port count from 65 to 8, meeting the design requirement of having fewer than 10 ports, making it ideal for pad-limited designs.

Calculations

$$1 + \frac{2 \times 32}{2^n} + n < 10 \tag{1}$$

$$1 + 2^{6-n} + n < 10 \tag{2}$$

for n = 1:

$$1 + 2^5 + 1 < 10 \tag{3}$$

$$34 < 10 \tag{4}$$

$$contradiction \tag{5}$$

for n = 2:

$$1 + 2^4 + 2 < 10 \tag{6}$$

$$19 < 10 \tag{7}$$

$$contradiction \tag{8}$$

for n = 3:

$$1 + 2^3 + 3 < 10 \tag{9}$$

$$11 < 10 \tag{10}$$

$$contradiction \tag{11}$$

for n = 4:

$$1 + 2^2 + 4 < 10 \tag{12}$$

$$9 < 10 \tag{13}$$

$$possible \tag{14}$$

for n = 5:

$$1 + 2^1 + 5 < 10 \tag{15}$$

$$8 < 10 \tag{16}$$

$$posssible \tag{17}$$