Kuldeep Singh

ELECTRONICS

for

CSIR-UGC-NET & GATE

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Only I am responsible for whatever I choose, whether it is the starting or the way or the ending.

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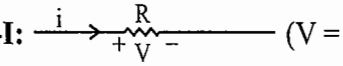
Chapter 1

Network Theory

Basic Circuit Analysis and KVL/KCL

Resistance: It is the property of a resistor to oppose current.

Case-I:  (V = iR) Conventional current flow from high to low potential.

Case-II:  (V = –iR) Electron current flow from low to high potential

In both case I and case II: $V = iR$

Where resistance of Resistor: $\boxed{R = \frac{\rho l}{A}}$

where l = length of conductor, A = Area of conductor, ρ = resistivity of conductor.

So $\boxed{\rho = \frac{RA}{l}}$ and conductivity = $\frac{1}{\text{Resistivity}}$ $\boxed{\sigma = \frac{1}{\rho}}$

Current:

- The phenomenon of transferring charge from one point in a circuit to another is described by the term electric current.
- An electric current may be defined as the time rate of net motion of electric charge across a cross-sectional boundary $\boxed{i = \frac{dq}{dt}}$ q = Coulombs, t = sec, i = Amp

Voltage:

- To move the electrons from one point to other point in particular direction external force is required. In analytical circuit external force is provided by emf and it is given by

  $\boxed{V = \frac{dW}{dq}}$ dimensionally, $\boxed{\text{Volt} = \frac{\text{Joule}}{\text{Coulomb}}}$

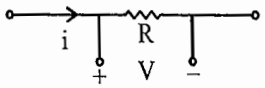
  where a differential amount of charge dq is given a differential increase in energy dW.
  Voltage = "Energy per unit charge" = "Work per unit charge"

- A voltage can exist between a pair of electrical terminal whether a current is flowing or not. An automobile battery, for example, has a voltage of 12V across its terminals even if no current flowing across it.

Ohm's Law:

- At constant temperature, the potential difference V across the terminals of a resistor R as show below, is directly proportional to the current i flowing through it. That is

$\boxed{V \propto i}$ $\boxed{V = iR}$

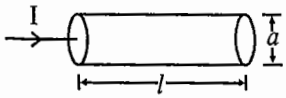


Ohm's law can also be expressed in terms of conductance G as

$\boxed{i = GV}$ $\boxed{G = \frac{1}{R}}$ G = Conductance [mho or Siemens]

Field Interpretation of Ohm's Law:

⇒ "At constant temperature current density is directly proportional to electric field intensity."



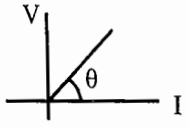
$J \propto E$

⇒ $\boxed{J = \sigma E}$ J ..... Current density (A/m^2), σ ..... Conductivity $[(\Omega - m)^{-1}]$

E ..... Electric field intensity (V/m)

Linearly test of Resistor:

When resistive element obeys ohm's law then the element is called as linear resistor otherwise it is a non-linear resistor.

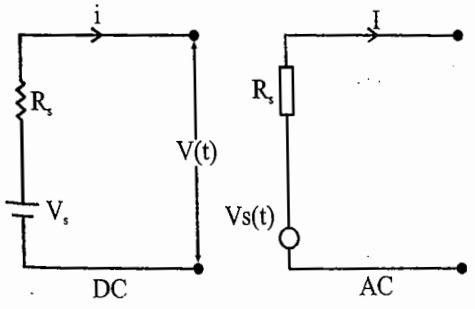


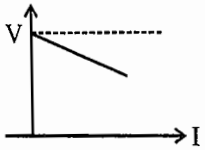
$\tan\theta = R$

Power Dissipation in a Resistor:

$$\boxed{P = Vi = (iR)i = i^2R = \frac{V^2}{R} = V^2G = \frac{I^2}{G}} \text{ volt}$$

Practical Voltage Sources: It delivers energy at specified (V) which depends on current delivers by sources.

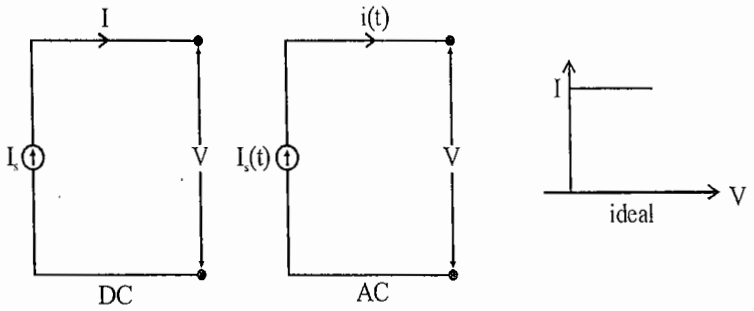




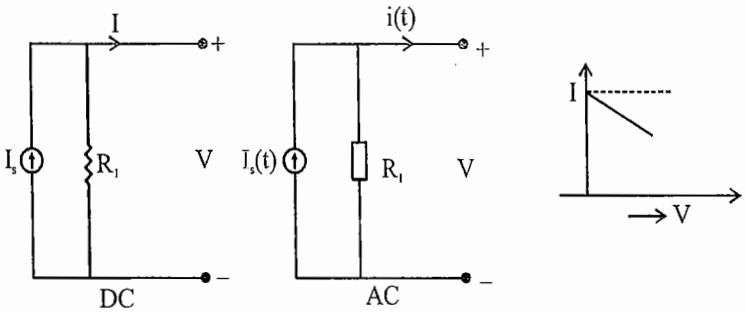
$\boxed{V(t) = Vs - IRs}$

Current Sources: Ideal current source delivers energy at a specified (I), which is independent on voltage across the source. Internal resistance of ideal current source = ∞.

w below,

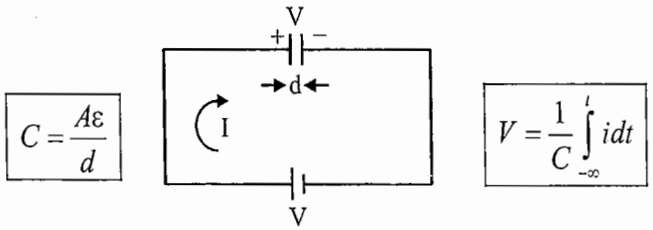


Practical Current Sources: Practical current sources delivers energy at specified current I, which is dependent on voltage across the source. In real time system current source does not exist.



Capacitance: It is the property of capacitor to hold charge q to confined electric field.

is a non-



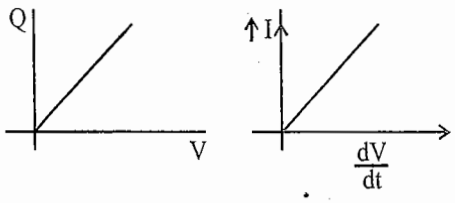
$$C = \frac{A\varepsilon}{d} \qquad V = \frac{1}{C}\int_{-\infty}^{t} i\,dt$$

d = distance between plates, A = Area of cross section of each conducting plates

Note: When the capacitance of capacitor is independent of current is called as linear capacitor.

elivers by

$$C = \frac{Q}{V}\Big|_{\text{Constant}}$$



$$i = c\frac{dV}{dt}$$

So under steady state i.e. at $t \to \infty$ $\boxed{i = 0}$ (full-charged)

Capacitor acts as open circuit:

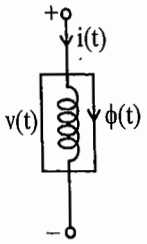
Inductance:

- If the current 'i' flowing in an element of figure below changes with time, the magnetic flux 'ϕ' produced by the current also changed which causes a voltage to be induced in the circuit, equal to the rate of flux linkage that is

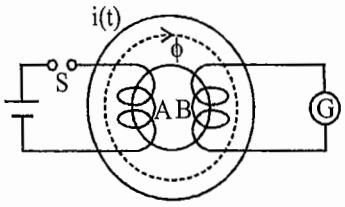
on voltage

$$V = \frac{d\phi}{dt} \quad \text{i.e.} \quad V = L\frac{di}{dt} \qquad \Rightarrow \phi \propto i \qquad \Rightarrow \phi = Li$$

where, L is constant of proportionality and is called self inductance.



(a)
Inductive circuit



(b)
Mutually coupled circuit

Therefore, there is an induced emf in coil B, which is equal to

$$\boxed{e = N\left(\frac{d\phi}{dt}\right)} \quad \text{or} \quad \boxed{e = L\left(\frac{di}{dt}\right)}$$

- As (di/dt) is directly proportional to $(d\phi/dt)$. Comparison of these two equation gives

$$\boxed{N\phi = Li}$$

From above it may noted that an inductor is a device, while inductance is the quantity L.

$$\boxed{L = \frac{N\phi}{i}}$$

- As $V = L\frac{di}{dt}$, so in steady state i.e. $t \to \infty$ $\boxed{V = 0}$ (fully-charged)

Inductor behaves like shots circuit.

Active Element: When an element is capable of delivering energy for infinite period of time is called as active element.

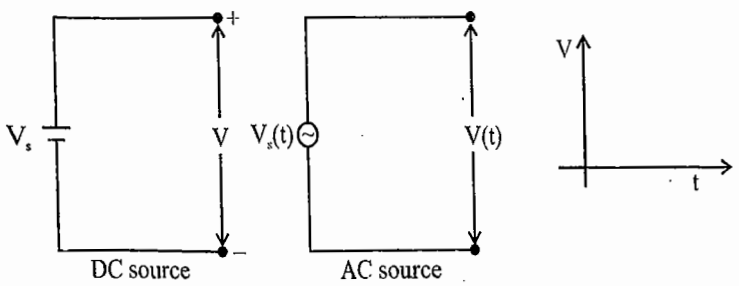
Example: Voltage, source, current source.

Passive Element: When an element is not able to deliver energy for infinite time period is called as passive element.

Example: Resistor, inductor and capacitor

Active Elements:

Voltage Source: Ideal voltage source delievers absorb energy at a specified 'V'. Internal resistance of ideal voltage source is zero.

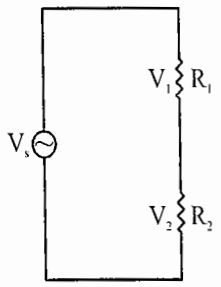


DC source AC source

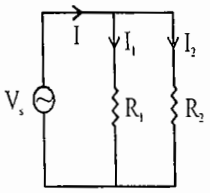
Voltage Divider Rule: Only applicable for parallel circuit.

$$R_{eq} = R_1 + R_2$$

$$V_1 = V_s\left(\frac{R_1}{R_1+R_2}\right), \quad V_2 = V_s\left(\frac{R_2}{R_1+R_2}\right)$$

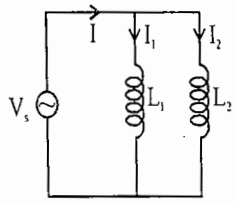


Current Division Rule: Only applicable for parallel circuit.



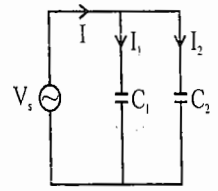
$$\frac{1}{R_{eq}} = \frac{1}{R_1} + \frac{1}{R_2} \qquad \boxed{I_1 = \left(\frac{R_2}{R_1+R_2}\right)I, \; I_2 = \left(\frac{R_1}{R_1+R_2}\right)I}$$

- Same for Inductor:



$$\frac{1}{L_{eq}} = \frac{1}{L_1} + \frac{1}{L_2} \qquad \boxed{I_1 = \left(\frac{L_2}{L_1+L_2}\right)I; \; I_2 = \left(\frac{L_1}{L_1+L_2}\right)I}$$

- **For capacitor:**



$$C_{eq} = C_1 + C_2 \qquad \boxed{I_1 = \frac{C_1}{C_1+C_2}I, \; I_2 = \frac{C_2}{C_1+C_2}I}$$

s called as

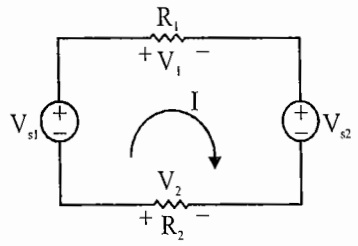
as passive

sistance of

Kirchoff's Voltage Law (KVL):

It states that algebraic sum of all voltages in a closed loop is equal to zero. It is based on conservation of energy.

$\boxed{\sum_{i=1}^{n} V_i = 0}$ Mathematically

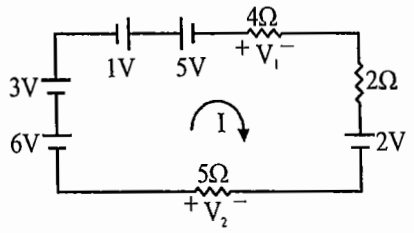


Applying KVL:

$$V_{s1} + V_2 - V_1 - V_{s2} = 0 \qquad \boxed{V_{s1} + V_2 = V_1 + V_{s2}}$$

SOLVED PROBLEMS

1. Calculate values of V_1 and V_2 across 4Ω and 5Ω resistor by KVL.



Soln. Applying KVL

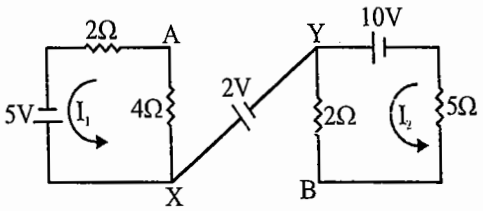
$6 + 3 + 1 - 5 - 4I - 2I - 2 - 5I = 0$

$3 = 11I,\ I = \frac{3}{11}$ Amp

$V_1 = 4I = 4 \times \frac{3}{11}$ $\boxed{V = \frac{12}{11}}$ volt

$V_2 = -5I = -5 \times \frac{3}{11} = -\frac{15}{11}$ volt

2. Calculate V_{AB} in the given circuit



Soln. KVL at loop 1: (Left loop)

$-4I_1 - 2I_1 + 5 = 0,\ I_1 = 5/6$ Amp

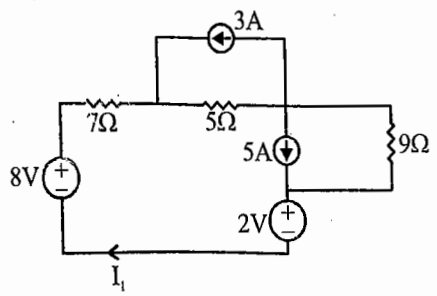
KVL at loop 2: (Right loop)

$10 - 2I_2 - 5I_2 = 0$

$I_2 = \frac{10}{7}$ Amp, $V_{AB} = V_{AX} + V_{XY} + V_{YB}$

$= -\frac{5}{6} \times 4 + 2 + 2 \times \frac{10}{7} = -\frac{20}{6} + 2 + \frac{20}{7} = \frac{32}{21}$ $\boxed{V_{AB} = 1.53\text{Volt}}$

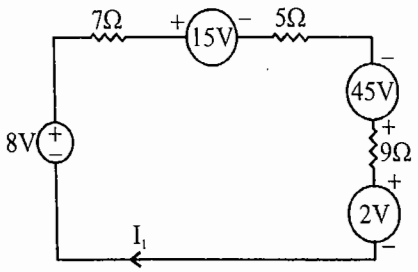
3. The value of I_1 in the circuit is



Soln. The circuit can be redrawn in the form of voltage source as [Current → voltage source]

4.

Soln.



Applying KVL

$8 - 7I - 15 - 5I + 45 - 9I - 2V = 0$

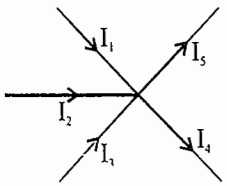
$53 - 17 - 21\ I = 0,\ I = \frac{36}{21}$ $\boxed{I = 1.71}$

Kirchoff Current Law (KCL)

(i) KCL states that algebraic sum of all current meeting at a point is equal to zero.

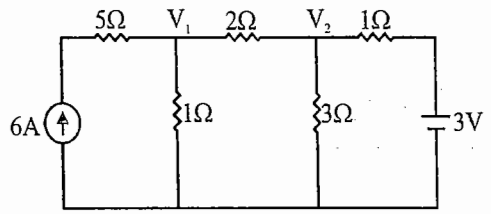
$\boxed{\sum_{i=1}^{n} I_i = 0}$, Mathematically

(ii) KCL worked on principle of law of conservation of charge.



$I_1 + I_2 + I_3 - I_4 - I_5 = 0$ $\boxed{I_1+I_2+I_3=I_4+I_5}$

4. Calculate the values of V_1 and V_2 by KCL:



Soln. Applying KCL at node 1: $6 = \frac{V_1}{1} + \frac{V_1 - V_2}{2}$ ... (1)

KCL at node (2) : $\frac{3 - V_2}{1} = \frac{V_2}{3} + \frac{V_2 - V_1}{2}$ ... (2)

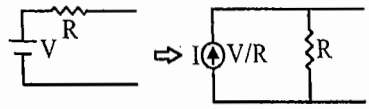
By solving equation (1) and (2);

We get $V_1 = 5V$ and $V_2 = 3V$

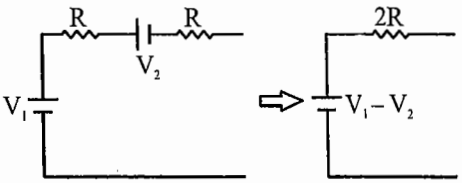
Limitations of KVL and KCL:

- KCL and KVL will fail for the high frequency circuit. **(Imp.)**
- KVL and KCL will fail in distributed elements since in distributed element it is not possible to separate effect of R, L, C.

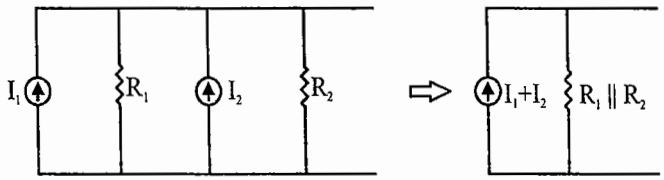
Source Transformation:



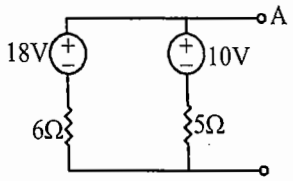
- **Series Combination of Batteries:**



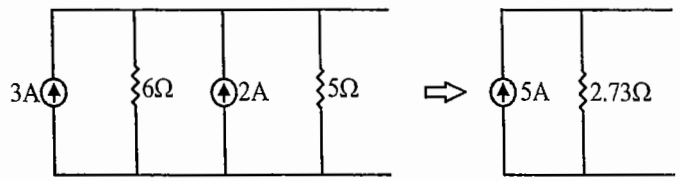
- **Parallel combination of current sources:**



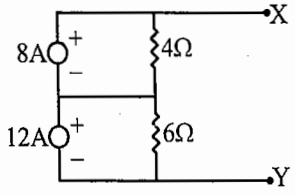
5. Obtain single current source for network shown



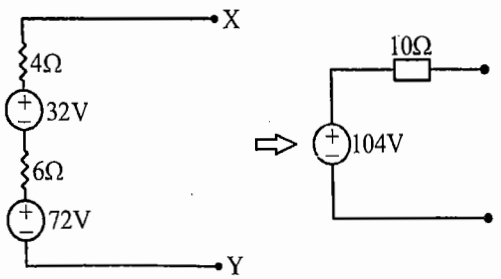
Soln.



6. Convert given circuit into a single voltage source



Soln.



Linear and non-linear Elements:

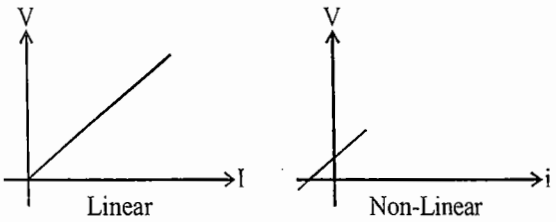
A linear network shows linear characteristics of voltage versus current. For a non-linear element the current passing through it does not change linearly with the linear change in applied voltage at a particular frequency. Semiconductor devices are usually examples of non-linear element.

In V.I. relation if output is zero for zero input and relation is linear then it is called linear network or element obeys ohm's law.

$V = ki \rightarrow$ linear $\qquad V = ki^2 \rightarrow$ Non-linear

$V = 2i + 3 \rightarrow$ Non-linear $\qquad V = i^n \rightarrow$ Non-linear

Conclusion: Only $\boxed{y = mx}$ is linear.



Simple resistors inductors and print at end capacitors are linear elements and their resistance inductance and capacitances do not change with a change in applied voltage on the circuit current .

Active and Passive Elements:

If a circuit element has the capability of enhancing the energy level of a signal passing through it then it is called an active element. Vacuum tubes and semiconductor devices are active elements on the other hand resistors, inductors, capacitors, thermistors etc. are passive elements as they do not have any intrinsic mean of signal boosting.

In V-I relation if any portion has V-I value as negative then it is active network.

Bilateral and Unilateral Element:

If the magnitude of the current passing through an element is affected due to change in polarity of polarity of the applied voltage then element is called unilateral element. On the other hand if current magnitude remains the same even if the applied voltage's polarity is changed then it is called a bilateral elements.

If by changing variable relation between both dependent variable and independent variable remains same then it is called bilateral network otherwise unilateral network.

Mesh Analysis:

Mesh is a property of a planner circuit and is undefined for a non-planner circuit.

We define a mesh as "A loop that does not contain any other loops within it."

Planer $\Rightarrow$ 2D representation circuit

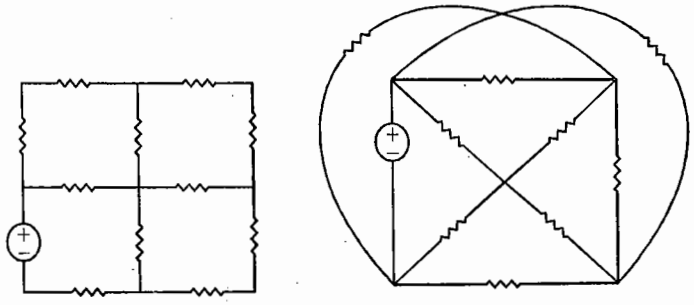


Fig. (a) [Planner] Fig. (b) [Non-Planner]

No branch passes over or under any other branch (Planer)

Network Theorem:

Superposition Theorem:

- The statement of superposition theorem follows as below:

"In any linear bilateral network having more than one source, response in any one of the branches is equal to algebraic sum of the response caused by individual source while rest of the sources are replaced by their internal impedances.

Note:

⇒ The principle of superposition is useful for linearly test of the system.

⇒ This is not valid for power relationship.

⇒ Sources can be made inoperative by

(a) Shot circuiting the voltage sources

(b) Open circuiting the current sources

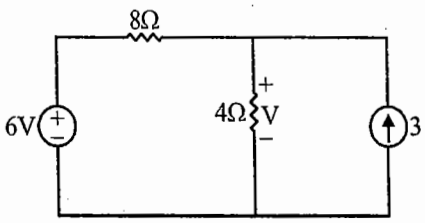
⇒ A linear network comprises independent sources, linear dependent source and linear passive elements like resistor, inductor, capacitor and transformer. Moreover, the components may either be time varying or time invariant.

Other Definition: "The superposition principle states that the voltage across (or current through) on element in a linear circuit is the algebraic sum of the voltage across or current through that element due to each independent source acting alone.

$$V_{eq} = V_1 \pm V_2 \pm V_3 ..... \pm V_n$$

7. Calculate value of V for the given circuit by using superposition theorem.

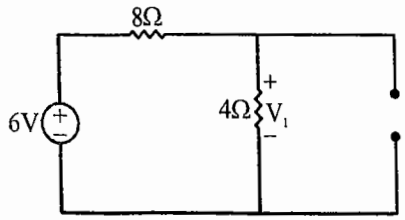
$$I_{eq} = I_1 \pm I_2 \pm I_3 ..... \pm I_n$$



Soln. At one time only effect of one source is considered. Voltage source is short circuited and current source is open circuited.

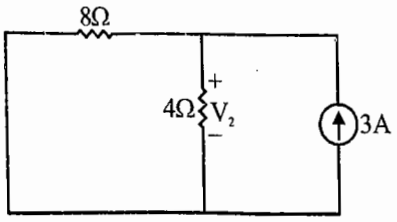
Since there are two sources, So, $V = V_1 + V_2$

Let V_1 is the voltage across 4 ohm due to 6V voltage source alone (in this case current source is open circuited).



$$V_1 = \frac{6}{8+4} \times 4, \quad V_1 = \frac{6}{12} \times 4 = 2V$$

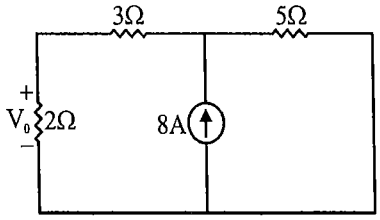
Let V_2 is the voltage due to 3A current source alone (in this case voltage source is short circuited).



$$3 = \frac{V_2}{4} + \frac{V_2}{8}, \quad 3 = \frac{V_2}{8}\{2+1\} \quad \boxed{V_2 = 8 \text{ volts}}$$

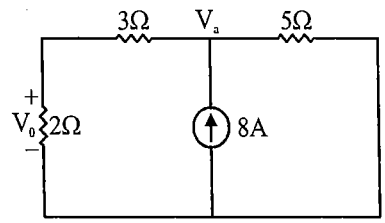
So total voltage V is $V = V_1 + V_2 = 2 + 8 = 10$ volt

8. Calculate the value of V_0 ?



Soln. Since there are two sources so total voltage due to both sources will be $\boxed{V_0 = V_1 + V_2}$

Let V_1 is the voltage only due to 8A current source, (In this case 20V source is short circuited)



$$-8 + \frac{V_a}{5} + \frac{V_a}{5} = 0$$

$$\frac{2V_a}{5} = 8$$

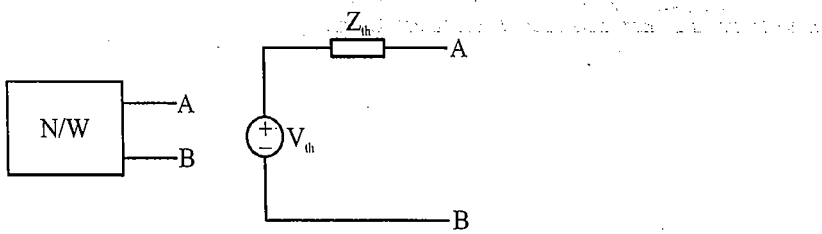
$$V_a = 20V$$

$$I_{2\Omega} = \frac{V_a}{5} = 4 \text{ amp}$$

$$V_1 = 4 \times 2 = 8 \text{ volt.}$$

Thevenin's Theorem:

Any two terminal linear bilateral network can be replaced by a voltage source in series with impedance.



Calculation of Thevenin's equivalent for independent source:

For Calculation of R_{th}: All independent current sources are open circuited and all independent voltage sources are short circuited.

For Calculation of V_{th}: Voltage across open circuit terminal.

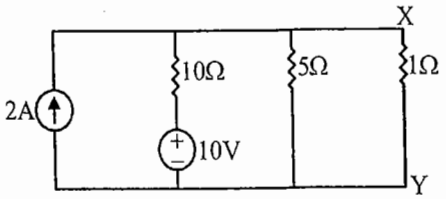
Calculation of Thevenin's equivalent for dependent source:

For calculation of V_{th}: Voltage is calculated across open circuited terminal by assuming current zero in that terminal.

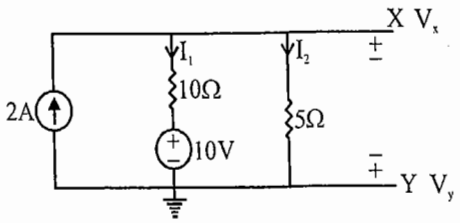
For calculation of R_{th}: First I_{SC} (Short Circuit Current across load) is calculated by assuming short-circuited terminal and then R_{th} is calculated

by $\boxed{R_{Th} = V_{Th} / I_{Sc}}$

10. For the given circuit calculate the power loss in the 1 ohm resistor by use of thevenin's theorem.



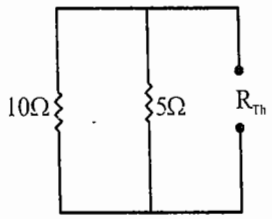
Soln. For calculation of V_{th} branch X–Y terminal is assumed as open circuited and let voltage is V_{th}-



$$2 = I_1 + I_2,\quad 2 = \frac{V_x - 10}{10} + \frac{V_x}{5},\quad 2 = V_x\left\{\frac{1}{10} + \frac{1}{5}\right\} - 1,\quad V_x\left\{\frac{3}{10}\right\} = 3$$

$$V_x = 10\ Volts,\quad V_x - V_y = 5 \times 2 = 10 \qquad \boxed{V_{Th} = 10\ Volt}$$

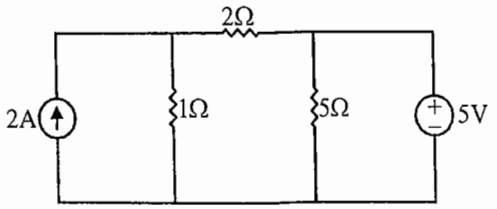
For Calculation of R_{Th}: (If dependent source is present) 2A current source is open circuited and 10V source is short circuited and let resistance is R_{Th} :



$$R_{Th} = \frac{10 \times 5}{10 + 5},\quad R_{Th} = \frac{10}{3} = 3.3\Omega,$$

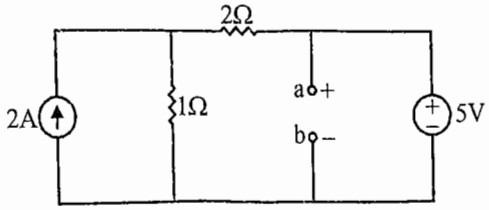
$$I_{Th} = \frac{V_{Th}}{R_{Th} + R_L} = \frac{10}{3.33 + I} = 2.31A$$

11. Find the current through the 5Ω resistor in the circuit by use of Thevenin's theorem.

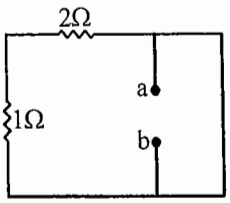


Soln. For calculation of V_{Th} = 5 ohm resistor is open circuited and so current in 5 ohm will be zero.

$$\boxed{V_{Th} = V_{ab} = 5V}$$



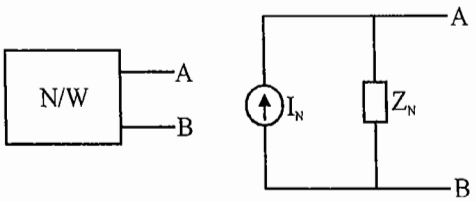
For Calculating R_{Th}: 2A current source is open circuited and 5V source is short circuited.



$$R_{Th} = \frac{0\times 3}{3+0} = 0, \quad I_L = \frac{V_{Th}}{R_{Th}+R_L} = \frac{5}{5+10} = 1A$$

Norton's Theorem: Any two terminal linear bilateral network containing active and passive element can be replaced by an equivalent current source in parallel to an equivalent impedance current source.

Relationship between Thevenin and norton (Source transformation)



$$\boxed{Z_N = Z_{Th}}$$

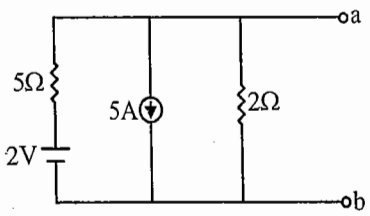
Note:

(a) Thevenin's equivalent circuit (b) Norton's equivalent circuit

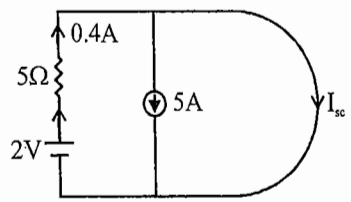
- Both of the above circuits are convertible to each other with the relations given as below:

$$\boxed{R_{Th} = R_N, V_{Th} = I_N R_N = I_N R_{Th}}$$

12. Find the Norton's equivalent circuit across a-b for the network shown in figure:



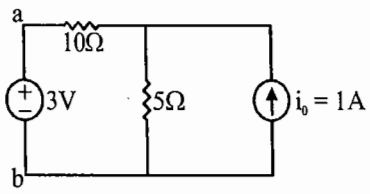
Soln.



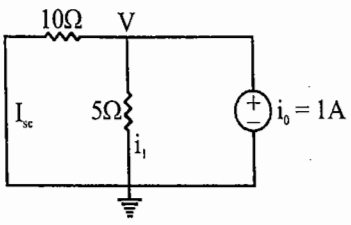
$$-2 + 5(5 + I_{sc}) = 0, \; I_{sc} = \frac{2}{5} - 5 = 0.4 - 5 \quad \boxed{I_{sc} = -4.6A}$$

$$R_{Th} = \frac{2\times 5}{2+5} = \frac{10}{7}\Omega \quad \boxed{R_{Th} = 1.43}$$

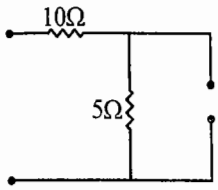
13. Find Norton's equivalent to the right of a-b terminal (across 3V source)



Soln. The equivalent circuit after shorting *ab* terminal.



(a)



(b)
[To calculate R_{Th}]

$$i_0 = i_1 + I_{sc},\ I = i_1 + \frac{V}{10}$$

$$I = \frac{V}{5} + \frac{V}{10},\ I = \frac{3V}{10},\ V = \frac{10}{3} \text{ and } I_{sc} = \frac{1}{3} = 0.33A \quad \boxed{R_{Th} = 10 + 5 = 15\Omega}$$

Reciprocity Theorem:

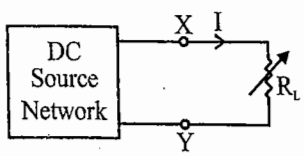
- A linear network is said to be reciprocal or bilateral if it remains invariant due to the interchange of position of cause and effect in the network.
- For verification of the reciprocity theorem following conditions must be satisfied.
  - ⇒ Circuit should consist of linear, time-invariant bilateral element.
  - ⇒ Circuit should consist of only a single independent sources.
  - ⇒ When circuit consist dependent source, reciprocity theorem can not be verified.

Maximum Power Transfer Theorem: Maximum power transferred from source to load is only possible when

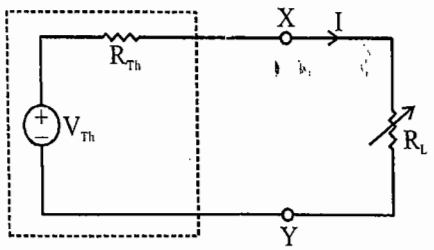
(i) Source impedance = Load impedance

(ii) Thevenin impedance = Load impedance

For DC Circuits:



(Load connected to the do source network)



(Equivalent source network and load)

$$I = \frac{V_{Th}}{R_{Th} + R_L}$$

while the power delivered to the resistance load is

$$P_L = I^2 R_L = \left(\frac{V_0}{R_{Th} + R_L}\right)^2 \times R_L \qquad \text{.... (i)}$$

Differentiating equation (i) with respect to R_L and equating to zero. We get $\boxed{R_L = R_{Th}}$

Hence, it has been provided that power transfer from a *dc* source network to a resistance network is maximum when the internal resistance of the *dc* source network is equal to the load resistance.

Again value of that maximum power is,

$$P_{\max} = \frac{V_{Th}^2 R_{Th}}{(R_{Th} + R_{Th})^2} = \frac{V_{Th}^2}{4R_{Th}} \quad \text{or} \quad \boxed{P_{\max} = \frac{V_{Th}^2}{4R_L}} \text{ Watt} \qquad [\because R_{Th} = R_2]$$

The total power supplied is thus: $P = 2\dfrac{V_{Th}^2}{4R_{Th}}$ $\boxed{P = \dfrac{V_{Th}^2}{2R_{Th}}}$

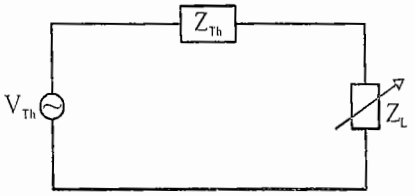
During maximum power transfer the efficiency η becomes,

$$\boxed{\eta = \frac{P_{\max}}{P} \times 100\%} \quad \Rightarrow \quad \eta = \frac{\dfrac{V_{Th}^2}{4R_{Th}}}{\dfrac{V_{Th}^2}{2R_{Th}}} \times 100\% \quad \boxed{\eta = 50\%}$$

f position So that efficiency in this case is 50% i.e. half of the total power is transferred to the load R_L.

[Maximum Power Transfer Theorem for *ac* circuits]

- Consider the Thevenin's equivalent circuit for an *ac* network as shown below:



ly possible

Here, $\boxed{Z_{Th} = R_{Th} + jX_{Th},\ Z_L = R_L - jX_L}$

- Now let us consider different cases for maximum power transfer.

Case-1: Both R_L and X_L are variable

- When both R_L and X_L are variable then maximum power from source to load will be transferred if load impedances is complex conjugate of internal impedance of the network.

i.e. $\boxed{Z_L = Z_{Th}^*}$

- In this case maximum power (active) will be calculated as $\boxed{P_{\max} = \dfrac{V_{Th}^2}{4R_L}}$

- Also during maximum power transfer efficiency will be 50%.

Case-2: R_L is variable but X_L is constant.

- In this case maximum power will be transferred when, $\boxed{R_L = |Z_{Th} + jX_L|}$

  or $R_L = \sqrt{R_{Th}^2 + (X_{Th} + X_L)^2}$

- Efficiency can be calculated as $\boxed{\eta = \left(\frac{R_L}{R_{Th} + R_L} \times 100\right)\%}$

Case-3: Load impedance is purely resistive.

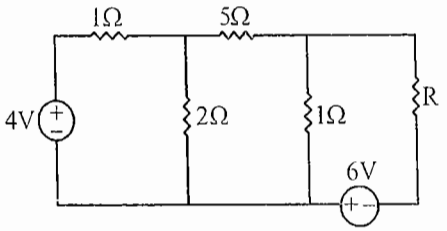
- In this case maximum power will be transferred when, $\boxed{R_L = |Z_{Th}|}$

Case-4: R_L and X_L are variable but the impedance angle is constant i.e.

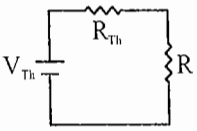
$Z_L = R_L + jX_L$ and $Q = \tan^{-1}\left(\frac{X_L}{R}\right) = \text{Constant}$

In this case maximum power will be transferred when, $\boxed{Z_L = Z_{Th}}$

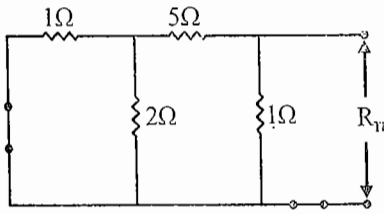
14. Calculate value of R in circuit such that maximum power transfer takes place and also calculate amount of this power.



Soln. Above circuit can be solved by Thevenin's theorem:

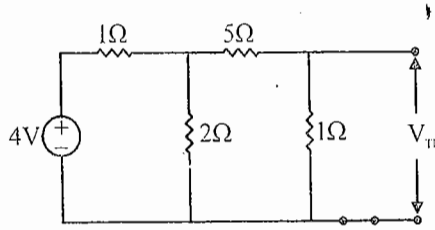


To find R_{Th}



$R_{Th} = [(2 \| 1) + 5] \| 1$ $\boxed{R_{Th} = 0.85}$

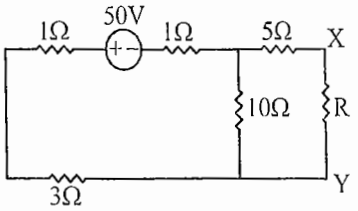
To find V_{Th} open load R



$\boxed{V_{Th} = 6.4V}$

Maximum Power $= \frac{V_{Th}^2}{4R_{Th}} = \frac{(6.4)^2}{4 \times 0.85} = 12\text{W}$

15. Assuming maximum power transfer from source to load R calculate the value of R and maximum value of power transferred.

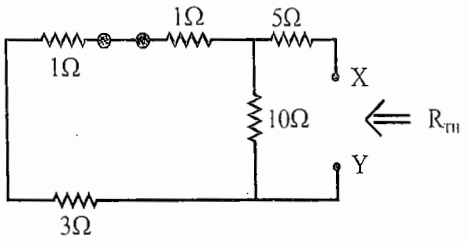


Soln. V_{Th} across XY $= -\frac{100}{3}$ V, R_{Th} across XY $= \frac{25}{3}\ \Omega$

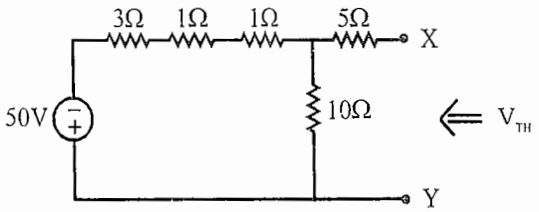
$$P_{max} = \frac{V_{Th}^2}{4R_{Th}} = \frac{(100/3)^2}{4\times\frac{25}{3}} = \frac{100}{3} \text{ Watt}$$

R_{TH} calculation:

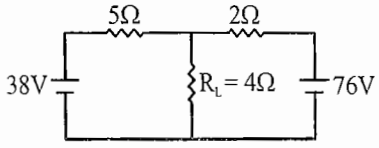
amount of



V_{TH} Calculation:



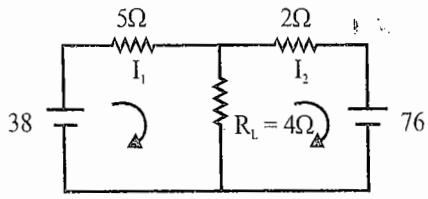
16. For the circuit shown, the potential difference (in Volts) across R_L is **[GATE 2007]**



(a) 48 (b) 52

(c) 56 (d) 65

Soln.



From node 1 we can write

$$38 = I_1(5+4) - I_2 4$$

$$\Rightarrow \quad 38 = 9I_1 - 4I_2 \qquad \ldots(i)$$

From node 2 we write

$$-76 = I_2(4+2) - I_1 4$$

$\Rightarrow \quad 76 = 4I_1 - 6I_2 \qquad \ldots (ii)$

From (i) and (ii), we get,

$I_1 = -2A$ and $I_2 = -14A$

Therefore, the voltage across the R_L is $(I_1 - I_2)R_L = 12 \times 4 = 48$ volt

Correct option is (a)

17. An a.c. voltage of 220 V_{rms} is applied to the primary of a 10:1 step-down transformer. The secondary of the transformer is centre tapped and connected to a full wave rectifier with a load resistance. The d.c. voltage appearing across the load is **[GATE 2008]**

(a) $\frac{22}{\pi}$ (b) $\frac{31}{\pi}$ (c) $\frac{62}{\pi}$ (d) $\frac{44}{\pi}$

Soln. We know that, $\frac{(v_{rms})in}{(v_{rms})out} = \frac{N_1}{N_2}$

$\Rightarrow \quad (v_{rms})_{out} = \frac{N_2}{N_1} \times v_{rms} = \frac{1}{10} \times 220 = 22$ volt

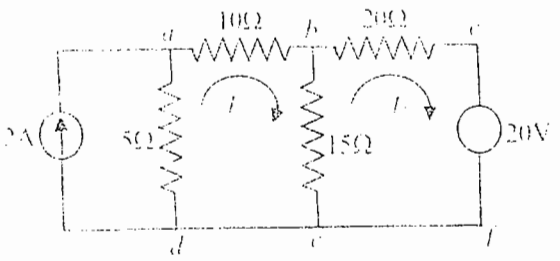
Therefore, the d.c. voltage appearing across the load is

$$v_{d.c.} = I_{d.c.}R_L = \frac{2I_0R_L}{\pi} = \frac{2V_0}{(R_1 + R_L)} \times \frac{R_L}{\pi} \qquad (\text{since, } R_f \simeq 0)$$

$$= \frac{2V_0}{\pi} = \frac{44}{\pi}$$

Correct option is (d)

18. Let I_1 and I_2 respresent mesh currents in the loop abcda and befch respectively. The correct expression describing Kirchoff's voltage loop law in one of the following loops is **[GATE 2008]**



(a) $30I_1 - 15I_2 = 10$ (b) $-15I_1 + 20I_2 = -20$

(c) $30I_1 - 15I_2 = -10$ (d) $-15I_1 + 20I_2 = 20$

Soln. From loop abcda we can, write

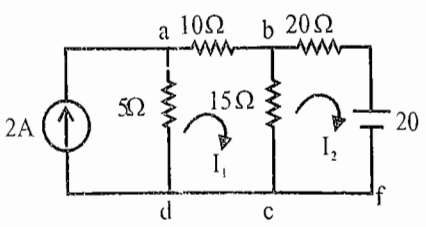
$I_1(5+10+15) - I_2 15 - 10 = 0$

$\Rightarrow \quad 30I_1 - 15I_2 = 10$

From loop befc we can write,

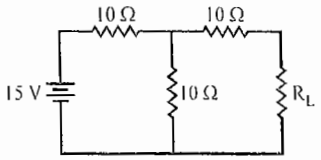
$I_2(15+20) - 20 - 15I_1 = 0$

$\Rightarrow \quad 15I_1 - 35I_2 = -20$



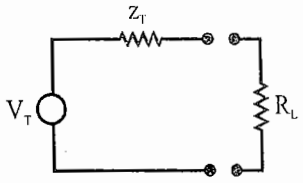
Correct option is (a)

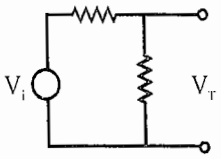
19. Assuming an ideal voltage source, Thevenin's resistance and Thevenin's voltage respectively for the below circuit are **[GATE 2009]**

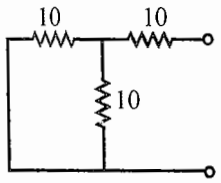


(a) 15 Ω and 7.5 V (b) 20 Ω and 5 V (c) 10 Ω and 10 V (d) 30 Ω and 15 V

Soln. According Thevenin's theorem, the equivalent circuit is given by







$$\therefore \quad V_T = \frac{15}{20} \times 10 = 7.5 \text{ volt} \qquad z_T = 10 \| 10 + 10 = \frac{10}{2} + 10 = 15\ \Omega$$

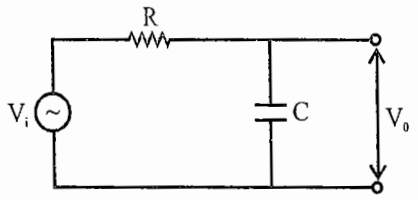
Correct option is (a)

20. A low pass filter is formed by a resistance R and a capacitance C. At the cut-off angular frequency $\omega_c = \frac{1}{RC}$, the voltage gain and the phase of the output voltage relative to the input voltage respectively, are **[GATE 2014]**

(a) 0.71 and 45° (b) 0.71 and –45° (c) 0.5 and –90° (d) 0.5 and 90°

Soln. Low pass filter is formed by R and C

From figure we can write



$$V_0 = \frac{V_i}{R + j\frac{1}{WC}} \times \frac{1}{jWC} \Rightarrow V_0 = \frac{V_i}{1 + jWCR}$$

$$\Rightarrow \quad A = \frac{V_0}{V_i} = \frac{1}{1 + jwcR}$$

$$\text{At } w = wc,\ A = \frac{1}{1 + jw_C RC} = \frac{1}{1 + j} = \frac{1 - j}{2}$$

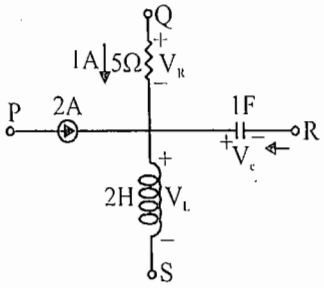
$$\therefore \quad |A| = \sqrt{\frac{1}{2}} = 0.71$$

And phase difference, $\phi = \tan^{-1}\left(\frac{-1}{1}\right) = -45°$

Correct option is (b)

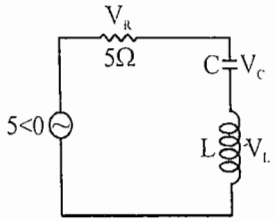
PRACTICE SET

1. A segment of a circuit is shown in figure $V_R = 5V$, $V_C = 4 \sin 2t$. The voltage V_L is given by



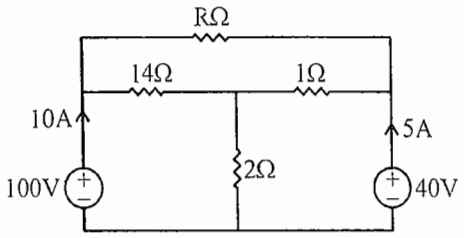
(a) $3 - 8 \cos 2t$ (b) $32 \sin 2t$ (c) $16 \sin 2t$ (d) $16 \cos 2t$

2. In the circuit of figure, the magnitudes of V_L and V_C are twice that of V_R. Given that $f = 50$ Hz, the inductance of coil is



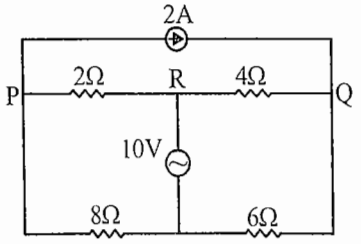
(a) 2.14 mH (b) 5.30 H (c) 31.8 mH (d) 1.32 H

3. In the figure value of R is



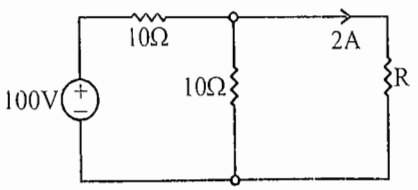
(a) 10Ω (b) 18Ω (c) 24Ω (d) 12Ω

4. In figure, the potential difference between points P and Q is



(a) 12V (b) 10V (c) –6V (d) 8V

5. In figure, the value of resistance R in Ω is

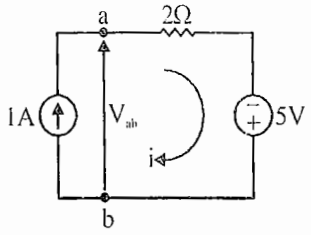


(a) 10 (b) 20 (c) 30 (d) 40

6. The RMS value of the voltage $u(t) = 3 + 4\cos(3t)$

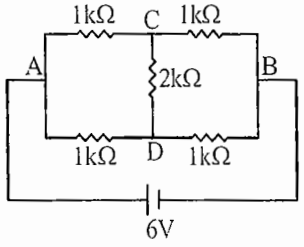
(a) $\sqrt{17}$ V (b) 5V (c) 7V (d) $(3+2\sqrt{2})$V

7. Assuming ideal element in the circuit shown below, the voltage V_{ab} will be



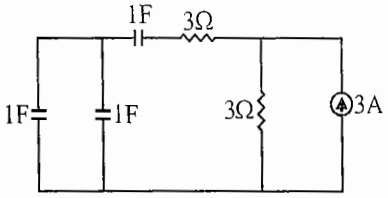
(a) –3V (b) 0V (c) 3V (d) 5V

8. The current through the 2kΩ resistance in the circuit shown is



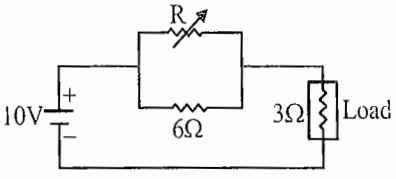
(a) 0mA (b) 1mA (c) 2ma (d) 6mA

9. The time constant for the given circuit will be



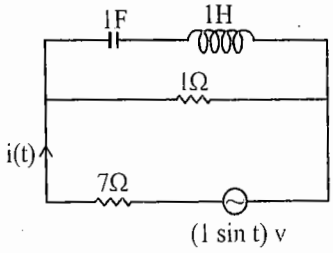
(a) 1/gs (b) 1/4s (c) 4s (d) gs

10. In the circuit given below, the value of R required for the transfer of maximum power to the load having a resistance of 3Ω is



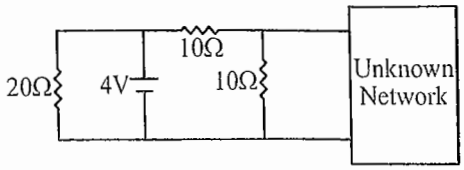
(a) 0 (b) 3Ω (c) 6Ω (d) ∞

11. The r.m.s. value of the current $i(t)$ in the circuit shown below is



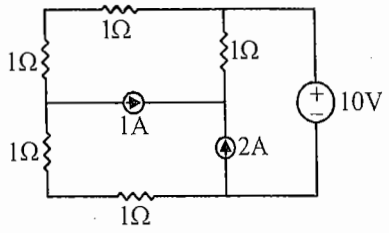
(a) $\frac{1}{2}$ A (b) $\frac{1}{\sqrt{2}}$ A (c) 1A (d) $\sqrt{2}$ A

12. In the given figure, the Thevenin's equivalent pair (voltage, impedance), as seen at the terminals P–Q, is given by



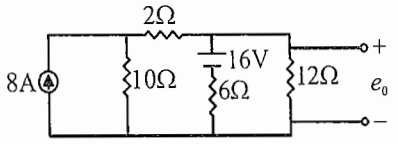
(a) (2V, 5Ω) (b) (3V, 5Ω) (c) (4V, 5Ω) (d) (2V, 7.5Ω)

13. In the circuit shown, the power supplied by the voltage source is



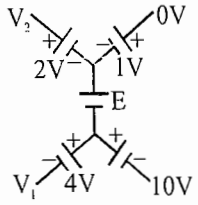
(a) 0W (b) 5W (c) 10W (d) 100W

14. The voltage e_0 in the figure is:



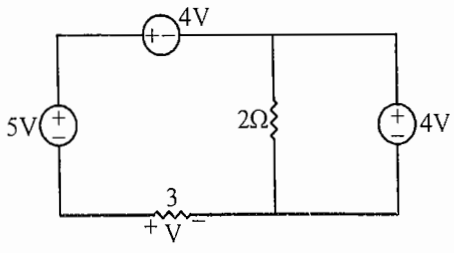
(a) 48V (b) 24V (c) 36V (d) 28V

15. In the circuit of figure, the value of the voltage source E is



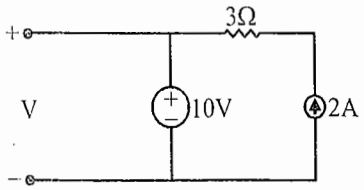
(a) –16V (b) 4V (c) –6V (d) 16V

16. The voltage V in figure is equal to:



(a) 3V (b) –3V (c) 5V (d) None of these

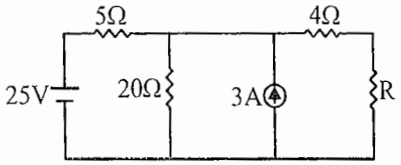
17. The voltage in figure is



(a) 10V (b) 15V (c) 5V (d) None of these

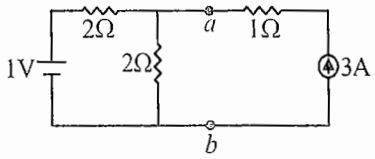
P–Q, is

18. What is the value of R required for maximum power transfer in network shown above?



(a) 2Ω (b) 4Ω (c) 8Ω (d) 16Ω

19. The voltage across the terminal *a* and *b* in figure is:



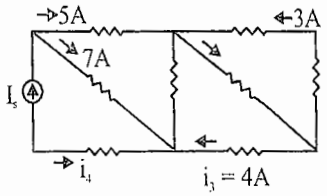
(a) 0.5V (b) 3.0V (c) 3.5V (d) 4.0V

20. The nodal method of circuit analysis is based on

(a) KVL and ohm's law (b) KCL and Ohm's law

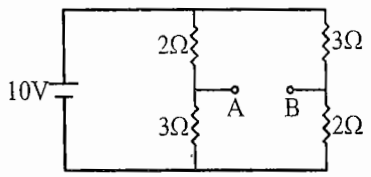
(c) KCL and KVL (d) KCL, KVL and Ohm's law

21. The current i_4 in the current of figure is equal to:



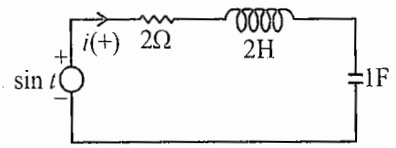
(a) 12A (b) –12A (c) 4A (d) None of these

22. Thevenin equivalent voltage V_{AB} and resistance R_{Th} across the terminals AB in the above circuit are



(a) 6V, 5Ω (b) 4V, 5Ω (c) 2V, 2.4Ω (d) 2V, 2.5Ω

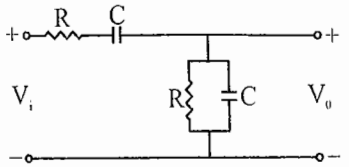
23. The differential equation for the current $i(t)$ in the circuit of the figure is



(a) $2\frac{d^2i}{dt^2}+2\frac{di}{dt}+i(t)=\sin t$ (b) $\frac{d^2i}{dt^2}+2\frac{di}{dt}+2i(t)=\cos t$

(c) $2\frac{d^2i}{dt^2}+2\frac{di}{dt}+i(t)=\cos t$ (d) $\frac{d^2i}{dt^2}+2\frac{di}{dt}+2i(t)=\sin t$

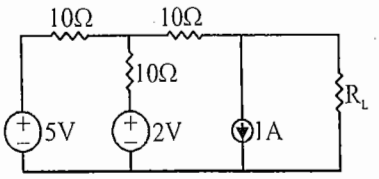
24. The RC circuit shown in the figure is



(a) a low-pass filter (b) a high-pass filter

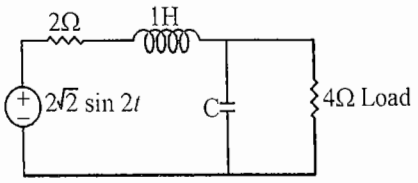
(c) a band-pass filter (d) a band-regeat filter

25. In the circuit shown below, the value of R_L such that the power transferred to R_L is maximum.



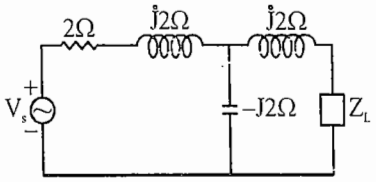
(a) 5Ω (b) 10Ω (c) 15Ω (d) 20Ω

26. Find the value of C to deliver the maximum power to load.



(a) 0.125F (b) 0.5F (c) 2F (d) 4

27. Find Z_L such that maximum power is transferred to it.

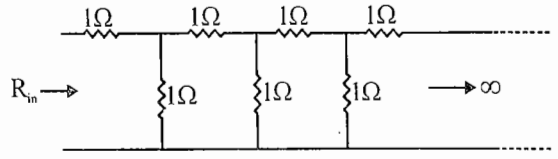


(a) $(2+j2)\Omega$ (b) $(2-j2)\Omega$ (c) $(-j2\Omega)$ (d) 2Ω

28. The voltage across a capacitor is triangular in waveform. The waveform of current is

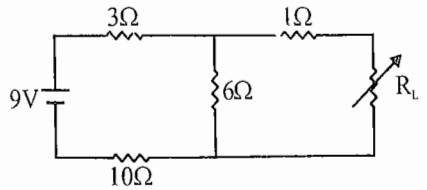
(a) triangular (b) trapezoidal (c) Sinusoidal (d) Rectangular

29. The value of R_{in} of the network



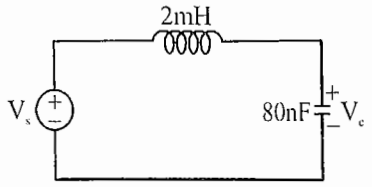
(a) 1.62Ω (b) 2Ω (c) $\frac{1}{3}\Omega$ (d) $\frac{1}{2}\Omega$

30. The maximum power that can be distributed in the load in the circuit shown is



(a) 0.396 W (b) 6W (c) 6.75W (d) 13.5W

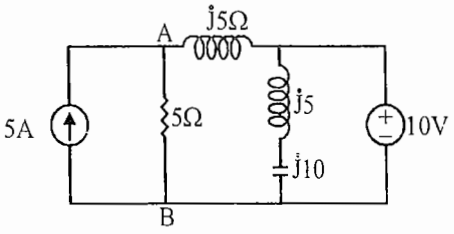
31. If $V_c(f) = 4 \cos (10^5 t)V$ in the circuit, find Vs.



(a) $-6.4 \cos 10^5 t$ V (b) $2.4 \cos 10^5 t$ V

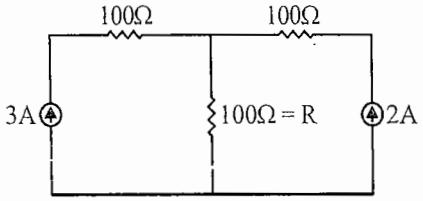
(c) $6.4 \cos 10^5 t$ V (d) $-2.4 \cos 10^5 t$ V

32. Determine the current through the branch AB of network shown below.



(a) $3.5 + j\,1.5$ (b) $3.5 - j\,1.5$ (c) $1.5 + j\,3.5$ (d) $1.5 - j\,3.5$

33. What is the ratio of currents in the circuit due to 3A and 2A source? Current is taken through R.



(a) $\frac{3}{2}$ (b) $\frac{2}{3}$ (c) $\frac{9}{4}$ (d) $\frac{4}{9}$

ANSWER KEY

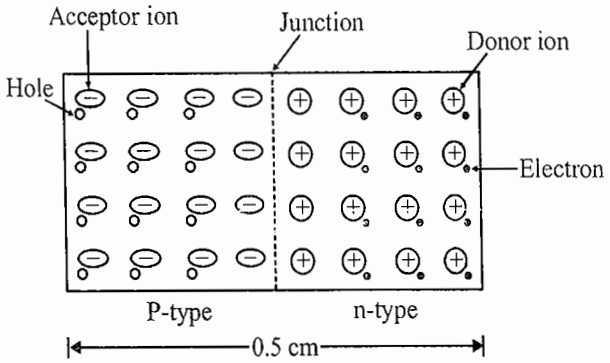
1. (b)	**2.** (c)	**3.** (d)	**4.** (c)	**5.** (b)
6. (a)	**7.** (a)	**8.** (a)	**9.** (c)	**10.** (a)
11. (b)	**12.** (a)	**13.** (a)	**14.** (d)	**15.** (a)
16. (a)	**17.** (a)	**18.** (c)	**19.** (c)	**20.** (b)
21. (b)	**22.** (b)	**23.** (c)	**24.** (c)	**25.** (c)
26. (a)	**27.** (d)	**28.** (d)	**29.** (a)	**30.** (a)
31. (d)	**32.** (a)	**33.** (a)		

Chapter 2

Semiconductors Diodes

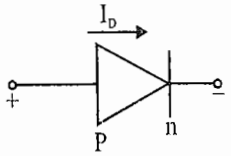
Diode:

- Diode is the simplest and most fundamental non-linear and passive circuit element. Just like a resistor. The diode has two terminals, but unlike the register, which has a linear (straight-line) relationship between the current flowing through it and the voltage appearing across it, the diode has a non-linear i-v characteristic.
- Consider a crystal of a semiconductor p-n junction is formed if donor impurities are introduced into one side and acceptors into the figure given below.



- Donor ion is represented by a plus sign because after 'donating' an electron, it becomes a positive ion. Acceptor ion is indicated by a minus sign because after this atom "accepts" an electron, it converts into a negative ion.

Diode Symbol: Arrow mark indicates direction of forward current.



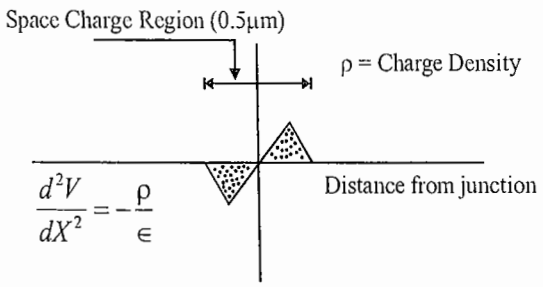
Junction Diode Characteristic:

- Some electron and holes from *n*-type and *p*-type cross into each others region and they get neutralized near junction.
- The unneutralized ions in the neighbourhood of the junction are referred to as uncovered charges.
- Since this region of the junction is depleted of mobile charges, it is called the depletion region, the space-charge region or transition region.
- The thickness of this region is of the order of wavelength of visible light (0.5 μm).
- Within this very narrow space charge layer, there are no mobile carriers.

For Step Graded p-n Junction:

1. **Shape of charge density** ρ.

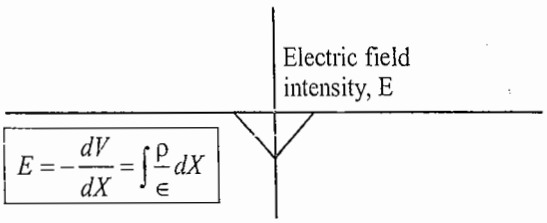
Poission's equation : $\frac{d^2V}{dX^2} = -\frac{\rho}{\epsilon}$



2. Corresponding field intensity curve is proportional to the integral of charge density curve.

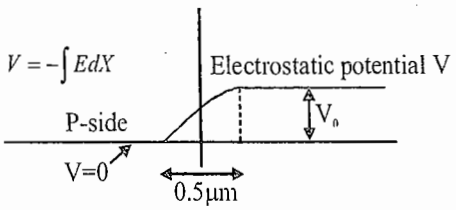
Since, $\frac{d^2V}{dX^2} = -\frac{\rho}{\epsilon} \Rightarrow \frac{d}{dX}\left(\frac{dV}{dX}\right) = -\frac{\rho}{\epsilon} \Rightarrow E = \int_{X_0}^{X} \frac{\rho}{\epsilon} dX$, $E = -\frac{dV}{dX}$;

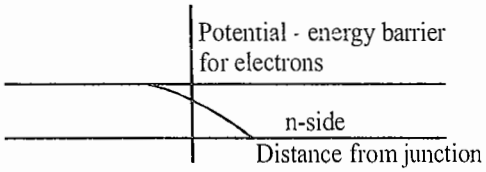
$E = 0$ at $X = X_0$



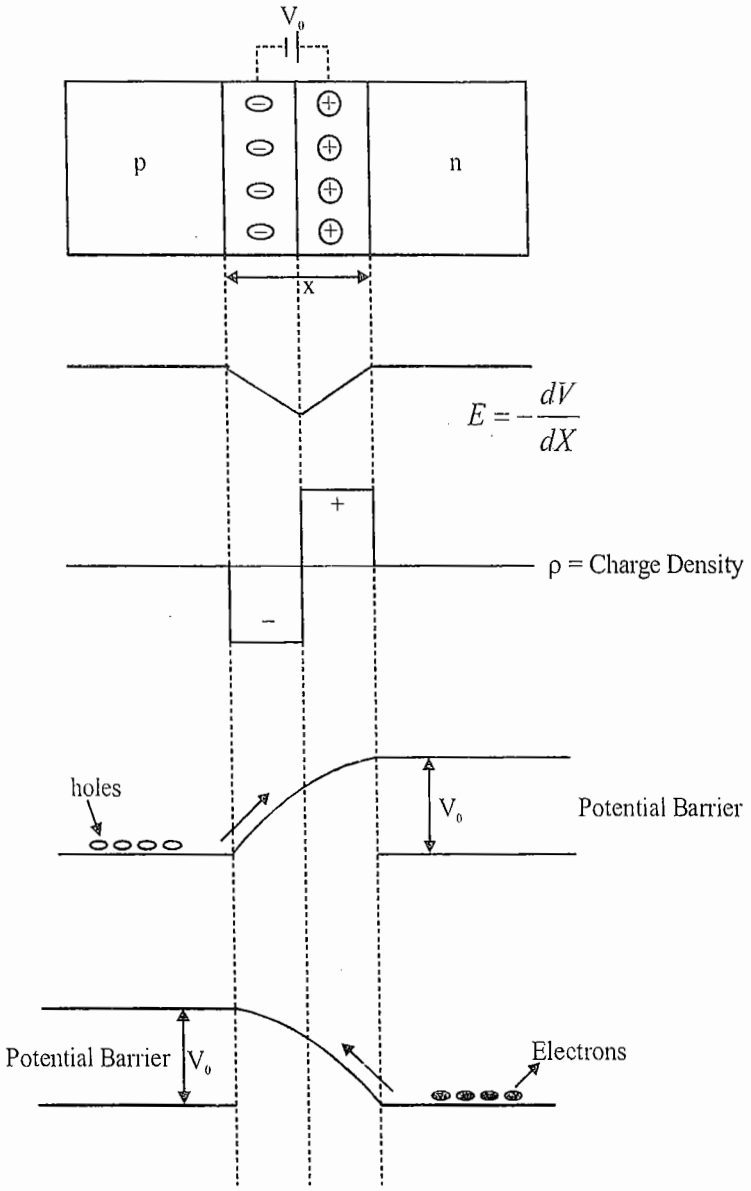
Note: Electric field intensity will be maximum at the junction.

3. **Potential:** Variation of potential in the depletion region is shown as below figure.



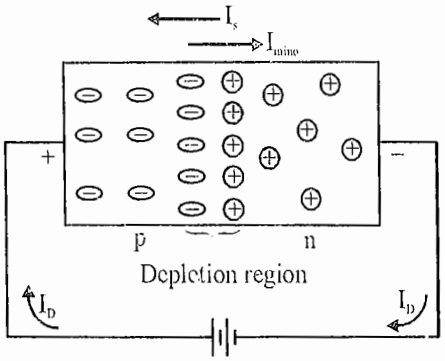


- Combination of all these diagram in depletion region shown as

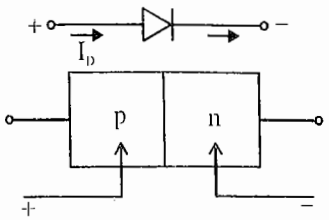


Forward Bias Region:

- A forward biased or "on" condition is established when positive terminal of battery is connected to the p-type material and negative terminal to the n-type material as shown in figure. (p-terminal at relative high potential)



(a) Internal distribution of charge under forward bias condition.



(b) Forward biased polarity.

- The application of forward bias potential will "Pressure" electrons in the n-type material and holes in the p-type material to recombine with the ions near the boundary and reduce the width of the depletion region as shown in figure (a).
- The resulting minority carrier flow has not changed in magnitude (since the conduction level is controlled primarily by the limited number of impurities in the material), but the reduction in width of depletion region has resulted in a heavy majority flow across the junction.
- An electron of the n-type material now "sees" a reduced barrier at the junction due to the reduced depletion region and a strong attraction for the positive potential applied to the p-type material.
- As the applied bias increases in magnitude, the depletion region will continue to decreases in width until a flood of electron can pass through the junction, resulting in an exponential rise in current as shown in the forward bias region of the characteristic of figure (b).

Reverse Bias Condition

- If an external potential is applied across the p-n junction such that the positive terminal is connected to the n-type material and negative terminal is connected to the p-type material as shown in figure (a).
- The number of uncovered ions will increase due to the large number of free electrons / hole drawn to the respective potential of the applied voltage. The net effect, therefore is a widening of the depletion region.
- As a result majority carrier can not cross the barrier, effectively reducing the majority current flow to zero.
- The number of minority carriers however, entering the depletion region will not change, resulting in minority carrier flow across the junction.

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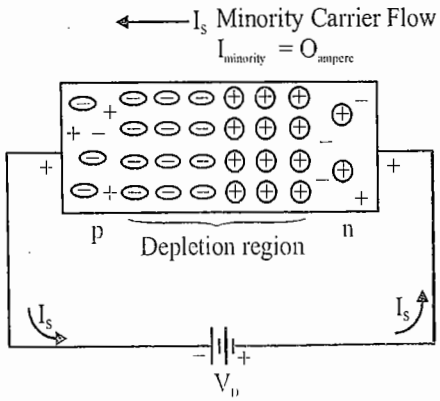
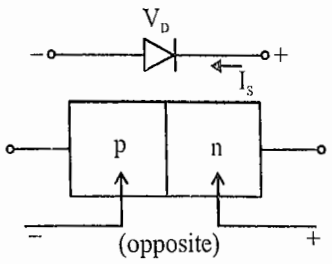


(a) Internal distribution of charge under reverse bias condition



(b) Reverse bias polarity and direction of reverse saturation current

- The current that exists under reverse bias condition is called the reverse saturation current and is represented by I_s or I_0.
- Also called as minority carrier current or leakage current or thermally generated current.
- If leakage current is small, the device will have very good thermal stability.
- It is highly sensitive to temperature. It doubles for every 10°C rise in temperature for both Si and Ge.

$$I_s(T_2) = I_s(T_1)2^{\left(\frac{T_2-T_1}{10}\right)} \text{Amp}$$

- Leakage current for $Ge\ diode = \mu A,\ Si\ Diode = nA$
- The greatest advantage of Si is smaller leakage currents.

Expression for Diode Current

The general characteristic of a semiconductor diode can be defined by Schokley's equation.

$$I = I_0\left(e^{\frac{V_D}{\eta V_T}} - 1\right)$$

I = Current flowing through the diode

I_0 = Reverse saturation current

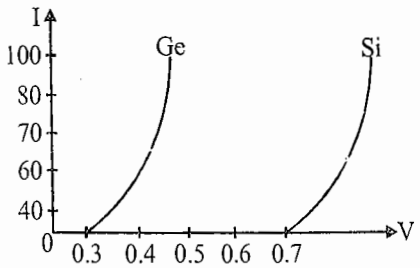
V = Voltage applied across the diode

V_T = Thermal voltage [at room temperature (i.e. T = 300°K) V_T = 25.8 mV] $= \frac{1}{11600}$

η = Ideality factor which is a function of the operating condition and physical construction.

[For Ge, η = 1 and for Si, η = 2]

Forward V-I Characteristic:



V_y = Cut-in potential

(for Ge = 0.3V and for Si = 0.7V)

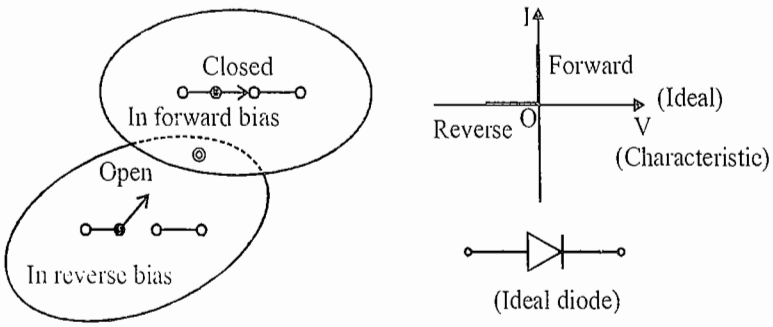
Cut in voltage (V_y) decreases with temperature for 1°C rise in temperature, it is reduced by 2.5 mV.

Logarithmic Characteristic: $\log I = \log I_0 + 0.434 \frac{V}{\eta V_T}$ at low current log I Vs. V is almost linear corresponding to $\eta = 2$. At high current diode behaves more like a resistor than a diode and current increases linearly rather than exponentially with applied voltage.

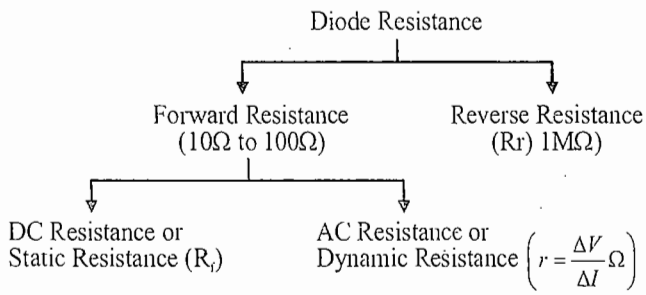
The Ideal Diode:

ent and is

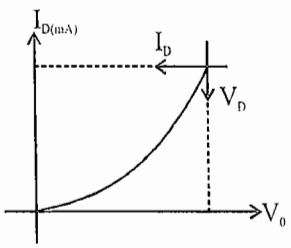
Si and Ge.



Diode Resistance:

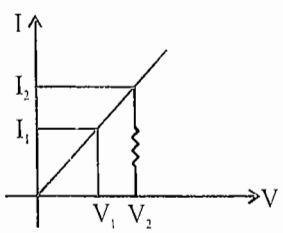


1. **Static / DC Resistance:** The static resistance of a diode is defined as the ratio V/I of the voltage to the current.



$R_D = \frac{V_D}{I_D}$; Typical $R_D = 80\,\Omega$ (very less)

2. **Dynamic / AC Resistance :** For small signal operation the dynamic, or incremental, resistance r is defined as the reciprocal of the slope of the Volt-ampere characteristic, $r = \frac{dV}{dI}$. For a semiconductor diode.



$$r_d = \frac{V_2 - V_1}{I_2 - I_1} = \frac{\Delta V}{\Delta I}, \quad r_d = \frac{\eta V_T}{I_f}\left(V_T = \frac{KT}{q}\right) \quad \boxed{r = \frac{\eta \bar{K} T}{I_f . q}}$$

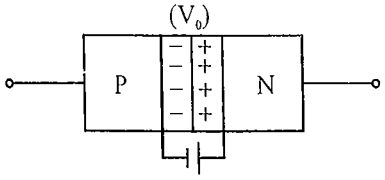
Dynamic conductance $g = \frac{1}{r}$ is $g = \frac{dI}{dV_D} = \frac{I_0 e^{\frac{V_D}{\eta V_T}}}{\eta V_T} = \frac{I + I_0}{\eta V_T}$

For a forward bias greater than a few tenths of a volts. I >> I_0, and r is given approximately by $\boxed{r = \frac{\eta V_T}{I}}$

Note: DC resistance > AC resistance

- The dynamic resistance of Ge diode with a forward current of 26mA is 7mA.
- Dynamic resistance in Si diode is more than in Ge diode.

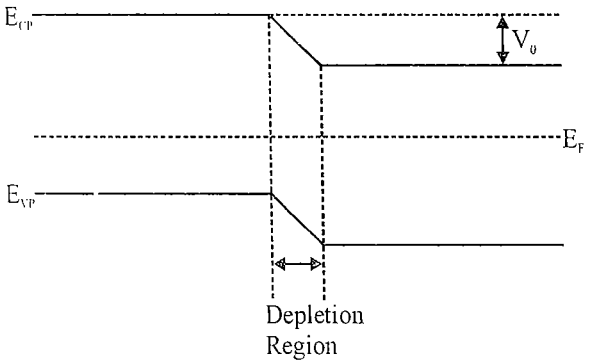
Contact Potential: (V_0)



$$V_0 = \frac{KT}{q}\ln\left(\frac{P_p}{P_n}\right), \quad V_0 = \frac{KT}{q}\ln\left(\frac{n_n}{n_p}\right)$$

If $P_p = Na^-$ and $\eta_n = N_d^+$

Then $\boxed{V_0 = \frac{KT}{q}\ln\left(\frac{N_a^- N_d^+}{h_i^2}\right)}$ $K \rightarrow$ Boltzman's constant

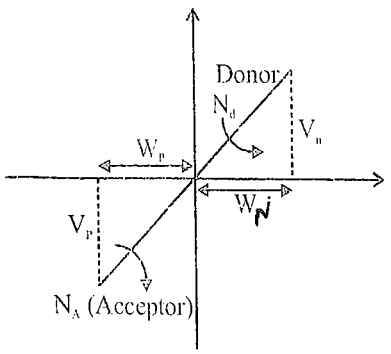


Fermi level for open circuit P-N junction.

- The contact potential V_0 cannot be read by an voltmeter connected across it because of barrier voltage balance by a metal to semiconductor contact potential at the end of diode.

Potential barrier and width of depletion layer across P-N junction:

The barrier potential V_0 is given by $\boxed{V_0 = |V_P| + |V_n|}$



W_p : Deption width on P-side

W_n : On-n-side

V_p is the potential full in P-region and V_n is the potential fall in N-region.

Width of depletion layer is given by $\boxed{W = W_p + W_n}$

Since crystal as a whole is electrically neutral the number of charge carriers on both side must be equal i.e.

$$N_a W_p = N_d W_n; \quad W = W_p + \frac{N_a}{N_d} W_p; \quad \boxed{W_p = \frac{W}{\left(1 + \frac{N_a}{N_d}\right)}}; \quad \boxed{W_n = \frac{W}{\left(1 + \frac{N_d}{N_a}\right)}}$$

So, it is clear that if doping is increased on one side then depletion layer width will increase on other side. In case of P–N, junction diode if doping is increased on P-side width of depletion layer will increase on N side.

Value of Width Depletion Layer: $W_p = \sqrt{\frac{2\varepsilon V_0}{qN_a\left(1 + \frac{N_a}{N_d}\right)}}$ and $W_n = \sqrt{\frac{2\varepsilon V_0}{qN_d\left(1 + \frac{N_a}{N_d}\right)}}$

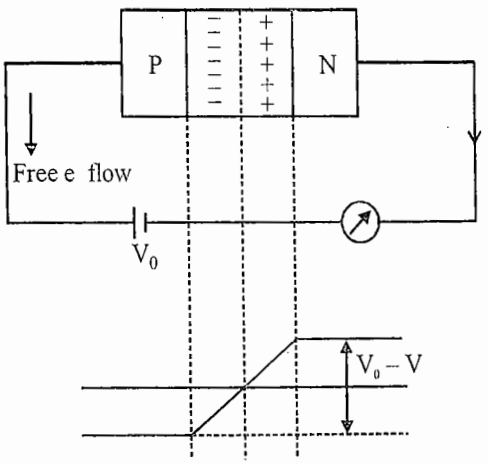
So, total width of depletion layer is given by $W = W_p - W_N$

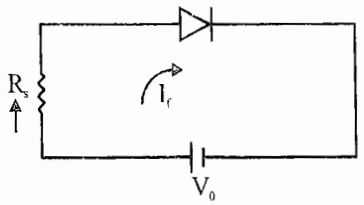
$$\boxed{W = \frac{2\varepsilon V_0}{q}\left(\frac{N_a + N_d}{N_a N_d}\right)}$$

$\varepsilon = \varepsilon_r \varepsilon_0; \quad \varepsilon_0 = 8.854 \times 10^{-12} F/m, \ \varepsilon_r = 11.7$ for Si, $\varepsilon_r = 16$ for Ge

$\varepsilon_{r_{Si}} = 11.7 \leftrightarrow 12$

Forward Biased P-N Junction Diode:



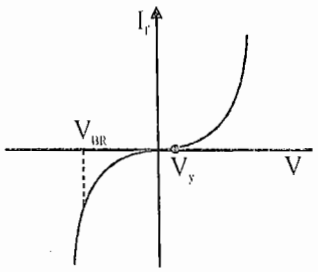


$I_f \rightarrow$ Forward current, $R_s \rightarrow$ Series resistance

When a PN junction is forward biased the width of depletion layer reduces and barrier height reduces. When a diode is properly forward the effect of barrier voltage becomes zero.

$\boxed{I_f = I_0[e^{\frac{V_d}{\eta V_T}} - 1]}$ $\eta = 2 \Rightarrow$ Si, $\eta = 1 \Rightarrow$ Ge

V-I Characteristic:



V_γ = 0.3V for Ge = 0.7V for Si

1.

Note: $V_\gamma \rightarrow$ Cut in voltage or offset Voltage or threshold voltage

$V_\gamma \rightarrow$ Defined as "minimum forward voltage required above which the forward current flow's through device.

In case of reverse biase current is due to flow of minority carriers. If voltage is further increased in reverse direction then reverse current does not increase. At the breakdown of junction, value of current increases abruptly.

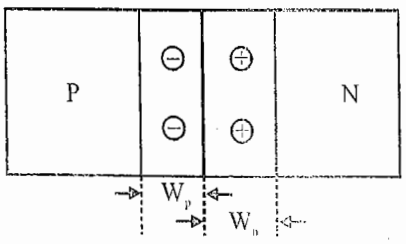
Effect of Temperature on Forward Current: $\boxed{I_f = I_0 e^{\frac{V_d}{\eta V_T}}}$

Forward current is only due to majority carrier concentration is almost independent of temperature.

Note: Cut in voltage V_γ decreases with temperature. For 1°C increase in temperature V_γ decreases by 2.3 milli volts.

Different Junction in Diode

1. **Step graded junction or Abrupt Junction:**
   - It has abrupt p-n junction. It refer's to p^+ or PN^+ diode.
   - Comparatively faster than normal diode.
   - Depletion layer will always penetrate more into lightly doped region consider P^+N diode.

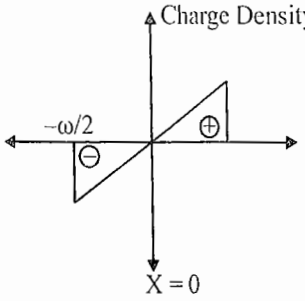


$\omega_N >> \omega_p$; $N_A > N_D$; $\boxed{\omega = \omega_N + \omega_P}$

2.

$\omega = \sqrt{\frac{2\epsilon}{q}\left[\frac{1}{N_a} + \frac{1}{N_d}\right].V_0}$, $\omega = \sqrt{\frac{2\epsilon}{q}\frac{1}{N_D}V_0}\ (N_A > N_D)$, $\boxed{V_0 = \frac{q\omega^2 N_D}{2\epsilon}}$

Linear Graded Junction: It is P^+ N^+ diode with equal doping level between P and N region.



$\boxed{\omega \propto (V_j)^{1/3}}$ V_j = Junction voltage

Different type of Capacitance in P-n Junction:

1. **Space Charge or Transition Capacitance:** When a P-N junction is reversed biased then depletion region acts like an insulator or dielectric material while P and N regions on either side have low resistance and acts as the plate. So this P-N junction in reverse bias may be regarded as a parallel plate capacitor if A is area of parallel plate capacitor and W is width of depletion layer then.

Transition Capacitance $C_T = \frac{\varepsilon A}{W} = C_J$

(a) For step graded junction, $\boxed{W \propto V_J^{1/2}}$

So, $\boxed{C_T \propto V_J^{-\frac{1}{2}}}$

(b) For linear graded junction $\boxed{W \propto V_J^{1/3}}$

So, $\boxed{C_T \propto V_J^{-\frac{1}{3}}}$

$V_k \rightarrow$ Knee voltage, $V_R \rightarrow$ Reversed biased voltage

$K \rightarrow$ Depends upon S.C. material

$n = \frac{1}{2}$ for step graded junction (Alloy junction)

$n = \frac{1}{3}$ for diffused junction / Linearly graded junction

So, $\boxed{C_T \propto (V_k + V_R)^{-1/2}}$ $\rightarrow$ Step graded / Alloy

$\boxed{C_T \propto (V_k + V_R)^{-1/3}}$ $\rightarrow$ Linearly graded / Diffused

2. **Diffusion or Storage Capacitance (C_D):** Diffusion capacitance dominates in a forward biased diode. It is mainly responsible for storage of minority carriers across the junction.

Mathematical Value: $C_D = \frac{dQ}{dV} = \tau.\frac{dI}{dV} = \frac{\tau}{r_d}$ $\boxed{C_D = \tau.g}$

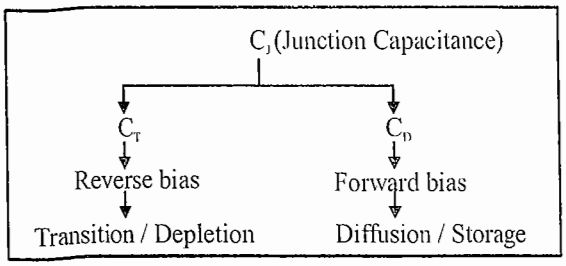
(r_d = dynamic resistance = $\frac{dV}{dI}$)

Where g_d = dynamic conductance

So, $\boxed{C_D = \frac{\tau . I_f}{\eta . V_T}}$, So $\boxed{C_D \propto I_f}$

Diffusion capacitance C_D increase linearly with the forward current.

Note:

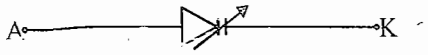


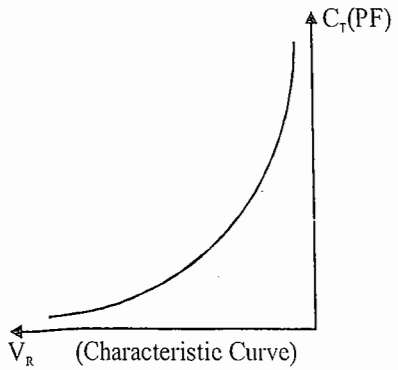
Varacter Diode:

- These are voltage variable capacitor.
- Varacters diode is a linear graded diode. Its principle of operation is transition capacitance (C_T).
- It is always operated under reversed bias condition.
- Transition capacitance (C_T) is given by $\boxed{C_T \propto V^{-n}}$

Where $\boxed{n = \frac{1}{3}}$

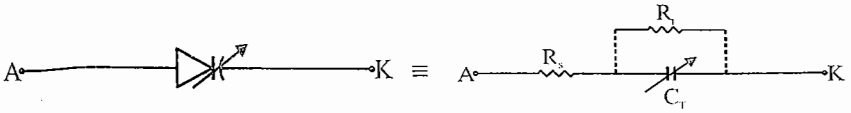
As reverse bias increases, transition capacitance decreases.





- Varacter diode is also known as "Vari-cap diode" or "volt-cap diode" or "epi-cap diode"

Equivalent Circuit:



Where, R_r = Reverse resistance $(> 1M\Omega)$, R_s = Contact resistance $(< 10\Omega)$

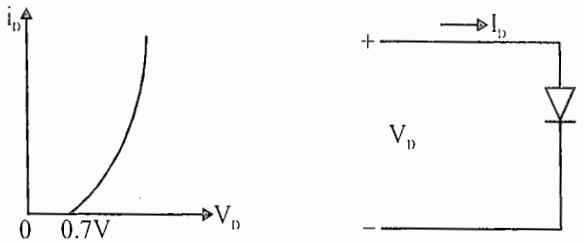
Applications: Varacter diode is a low noise microwave device. It is fabricated with Ga As.

- For direct generation of FM by using varacter diode modulator circuit.
- For fine tuning of Receivers.
- For self balancing of bridges

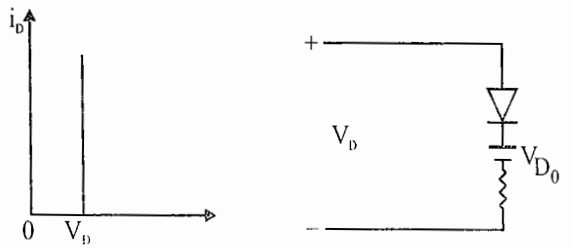
- As a para-amplifier (Parametric amplifier) and it is low noise microwave power amplifier used with satellite communication.

Various Diode models in Forward Biasing:

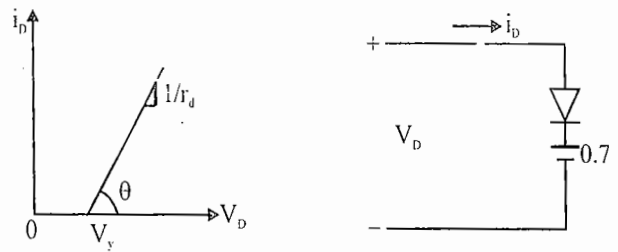
1. **Exponential Model:**



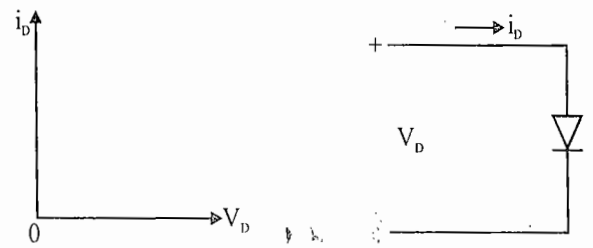
2. **Piece-wise linear Characteristic:**



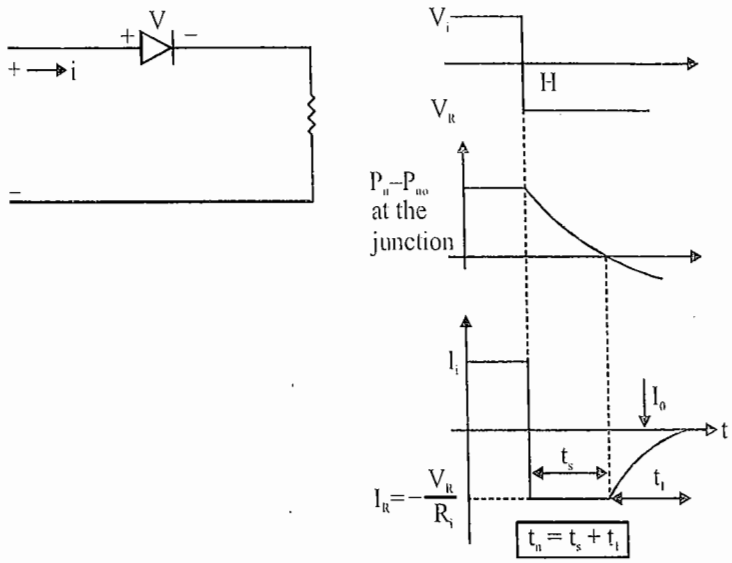
3. **Mathematical equivalent model:**



4. **Ideal-diode:**



Junction Diode Switching Time: In a given P-N junction diode when external voltage is suddenly reversed in a diode circuit which has been carrying current in forward direction the diode current will not immediately fall to its steady state reverse voltage value until injected or excess minority carrier density $P_n - P_{n0}$ has dropped normally to zero. The diode will continue to conduct easily and current will be determined by the external resistance in diode circuit, Value of t_n is generally of the order of 400n sec.



SOLVED PROBLEMS

1. Consider again the asymmetrical silicon diode we discussed in the previous two examples. Let the mean lifetime of holes be 10 nS, and let $\eta = 1$. If a forward current of 0.1 mA is flowing in the diode, determine the diffusion capacitance.

Soln. $\boxed{C_D = \frac{\tau I}{\eta V_T}}$ $V_T = 0.026V$, $C_D = \frac{10nS \times 0.1nA}{1 \times 0.026V} = 38.5pF$

2. Consider an asymmetrical silicon junction, with $N_A = 10^{14}/cm^3$ and $N_D = 10^{17}/cm^3$. If the cross-sectional area of the junction is $9.6\,\mu n^2$, determine its transition capacitance with no applied bias.

Soln. $C_T = \frac{\varepsilon A}{W}$ .... (i)

$$W = \sqrt{\frac{2\varepsilon}{qN_D} V_J}\,, \quad V_J = V_0 = \frac{KT}{q} \ln\left(\frac{N_A N_D}{hi^2}\right)$$

$$= 0.026 \ln\left(\frac{10^{19} \times 10^{17}}{(1.45 \times 10^{10})^2}\right) \quad \text{Or, } V_j = 0.94V$$

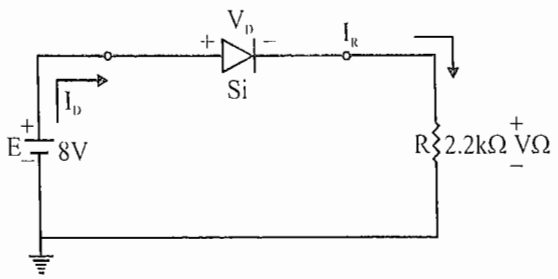
Learn

$$\text{Hence, } W = \sqrt{\frac{2 \times 11.9 \times 8.85 \times 10^{-14}}{1.6 \times 10^{-19} \times 10^{17}} 0.94} = 0.11\ \mu M$$

$$C_T = \frac{\in A\sqrt{qN_A}}{\sqrt{2 \in V_j}} = A\sqrt{\frac{qN_D \in}{2V_j}} = \frac{\in A}{W} = \frac{11.9 \times 8.85 \times 10^{-14} \times 9.6 \times 10^{-8}}{0.11 \times 10^{-4}}$$

$\boxed{C_T = 9.2F}$

3.



Soln. $V_D = 0.7V$, $V_R = E - V_D = 8 - 0.7V = 7.3V$,

$$I_D = I_R = \frac{V_R}{R} = \frac{7.3V}{2.2k\Omega} \cong 3.32mA$$

4. A P^+ n junction has a built-in potential of 0.8V, The depletion layer width at a reverse bias of 1.2V is 2 μn. For a reverse bias of 7.2V, the depletion layer width will be.

Soln. Junction potential = Built in potential + Reverse bias Voltage

$V_j = V_0 + V_R$

Now for abrupt pn junction depletion width

$W \propto V_j^{1/2}$, $W = K V_i^{1/2}$

$2\mu m = K(0.8+1.2)^{1/2}$ ... (i)

$x = K(0.8+7.2)^{1/2}$ ... (ii)

From (i) and (ii) $\frac{x}{2} = \left(\frac{8}{2}\right)^{1/2}$ $\boxed{x = 4\mu m}$

5. At 300K, for a diode current of 1mA, a certain germanium diode requires a forward bias of 0.1435V, where as a certain silicon diode requires a forward bias of 0.718V. Under the condition, stated above, the closest approximation of the ratio of reverse saturation current in germanium diode to that in silicon diode is

(a) 1 (b) 5 (c) 4×10^3 (d) 8×10^3

Soln. $\eta = 1$ for Ge, $\eta = 2$ for Si,

$$I = I_{0_{Si}}\left(e^{\frac{V_{D1}}{\eta V_T}} - 1\right) \quad \text{... (i)}$$

$$I = I_{0_{Ge}}\left(e^{\frac{V_{D2}}{\eta V_T}} - 1\right) \quad \text{... (ii)}$$

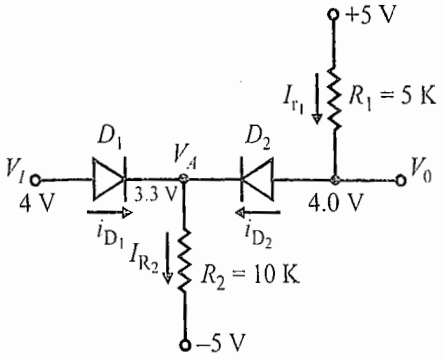
From equations (i) & (ii)

$$\Rightarrow I_{0Si}\left(e^{\frac{V_{D1}}{\eta V_T}} - 1\right) = I_{0Ge}\left(e^{\frac{V_{D2}}{\eta V_T}} - 1\right) \Rightarrow \frac{I_{0Ge}}{I_{0Si}} = \frac{e^{\frac{V_{D1}}{\eta V_T}} - 1}{e^{\frac{V_{D2}}{\eta V_T}} - 1} = \frac{e^{\frac{0.718}{2\times 26\times 10^3}} - 1}{e^{\frac{0.1435}{26\times 10^{-3}}} - 1} \Rightarrow \boxed{\frac{I_{0Ge}}{I_{0Si}} = 4\times 10^3}$$

6. Determine the output voltage V_0 and the diode currents I_{D1}, I_{D2}, shown in figure for

(i) $V_I = 0$ (ii) $V_I = 4\,V$ (iii) $V_\gamma = 0.7\,V$

Soln. (i) Let $V_I = 0$. Assume that D_1 is OFF. If V_A turns out to be positive then we are right and D_1 would be indeed OFF.



Circuit for example

If D_1 is OFF then

$$I_{R1} = I_{D2} = I_{R2} = \frac{+5 - V_\gamma - (-5\,V)}{R_1 + R_2} = \frac{5 - 0.7 + 5}{5 + 10} = 0.62\ mA$$

$\therefore\ V_0 = 5 - 0.62 \times 5 = 1.9\,V$ and $V_A = V_0 - 0.7 = 1.9 - 0.7 = 1.2\,V$

D_1 is indeed OFF for $V_I = 0$ volt and we were right.

(ii) $V_I = 4\,V$. It appears that here both D_1 and D_2 are ON. If I_{D1} and I_{D2} are positive we are right. If D_1 and D_2 are both ON then for $V_I = 4\,V$, $V_A = 4 - 0.7 = 3.3\,V$ and $V_0 = V_A + 0.7 = 3.3 + 0.7 = 4.0\,V$.

When D_1 and D_2 are ON the values of V_A and V_0 are shown in figure.

$$I_{R1} = I_{D2} = \frac{5 - V_0}{5} = \frac{5 - 4}{5} = 0.2\ mA$$

$$I_{R2} = \frac{3.3 - (-5)}{10} = 0.83\ mA$$

$$I_{D1} = I_{R2} - I_{R1} = 0.83 - 0.2 = 0.63\ mA$$

As both I_{D1} and I_{D2} are positive, hence D_1 and D_2 are both ON and $V_0 = 4\,V$.

Wave Shaping Abilities of Diodes

Clipper and Clampers

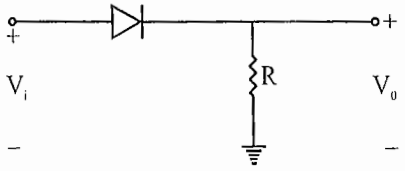
Clippers: Clipping circuits are used to select for transmission that part of an arbitrary wave form which lies above or below some reference level. Clippling circuits are also referred to as voltage / current limiters, amplitude selectors or slicers or choppers.

In Other Way: "Clippers are networks that employ diodes to "clip" away a portion of an input signal without distorting the remaining part of the applied waveform.

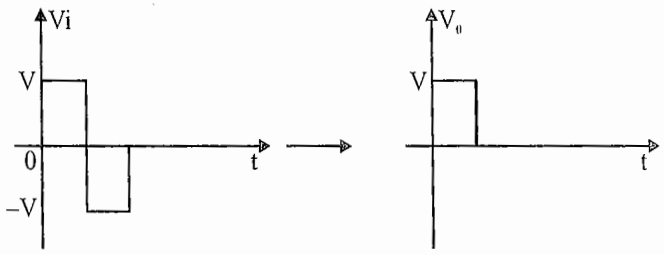
there are two general categories of clippers.

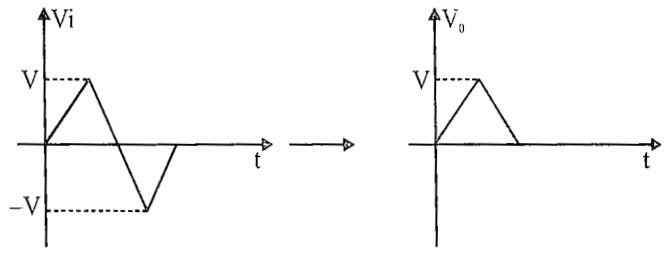
i) Series ii) Parallel

Series Clipper:

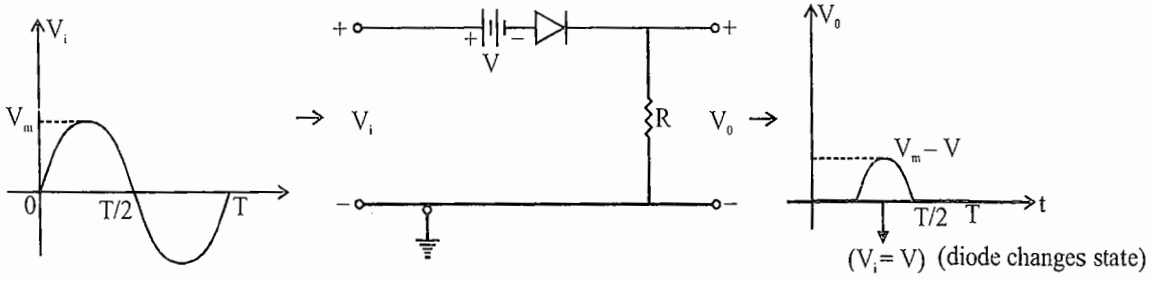


- Diode is series with local in series clipper circuit.





Series Clipper with dc Supply:



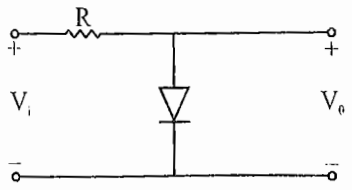
Steps to be Followed to Draw the Output Signal:

(i) Take careful note of where the output voltage is defined.

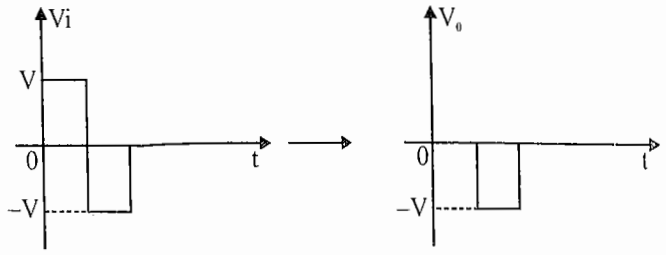
(ii) Try to develope on overall sense of the response by simply nothing the "Pressure" established by each supply and the effect it will have on the conventional current direction through the diode.

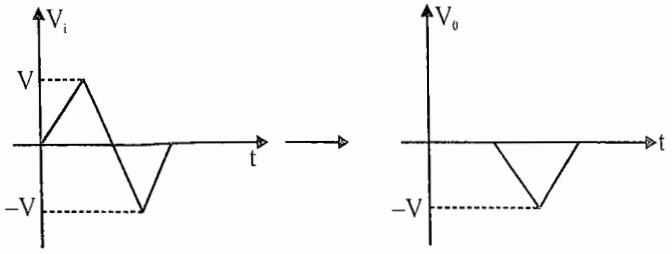
(iii) Determine the applied voltage (transition voltage) that will result in a change of state for the diode from the "off" to the "on" state.

Parallel Clipper:



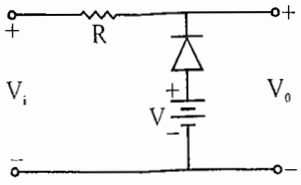
- Diode is parallel to the load in the parallel clipper circuit.
- The analysis of parallel configuration is very similar to that applied to series configurations.



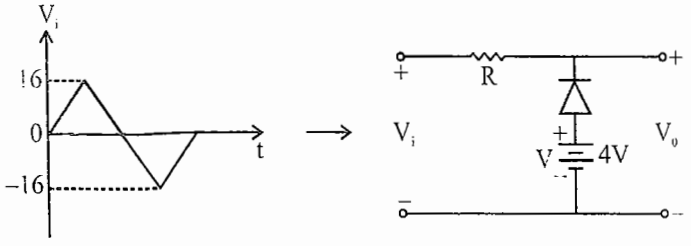


Or

7. Parallel clippler with dc supply.



8. Find the output of the given signal V_i in the parallel clippler circuit.

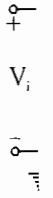


V_i	D	V_0
$V_i \le 0$	$ON\ (shot)$	$4V$
$0 \le V_i \le 4V$	$ON\ (shot)$	$4V$
$4 < V_i \le 16$	$OFF\ (open)$	$V_i\ (o/p\ follow\ i/p)$

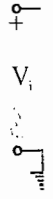
Note: To analise all the clippler, clamper, rectifier circuit always make this type of table.

Apply Input → Find the State of the diode → draw o / p

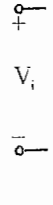
1. Sil
(a)

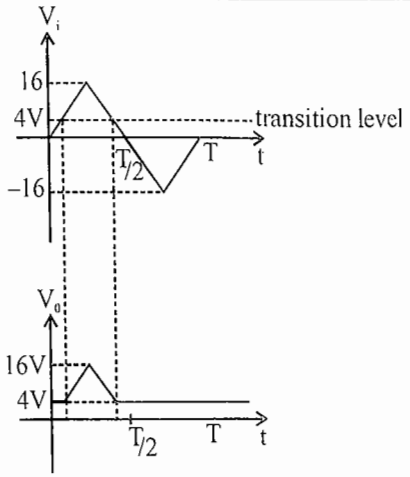


(b)

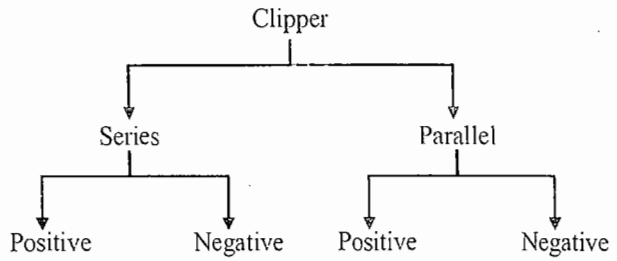


2. Bia
(a)





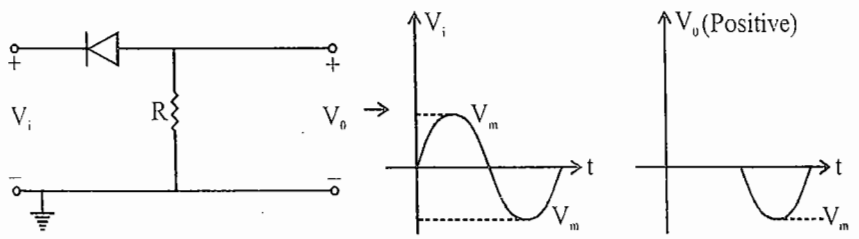
On the basis of the connection of the diode - Clipper are again divide in these manner.



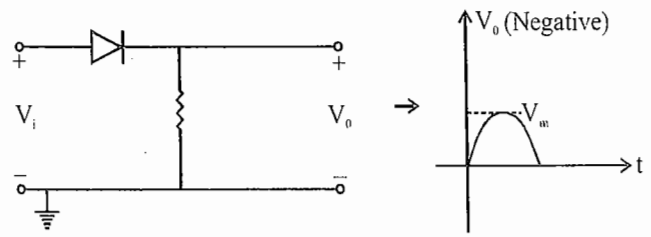
Table

1. Simple Series Clipper (Ideal Diode

(a) Positive

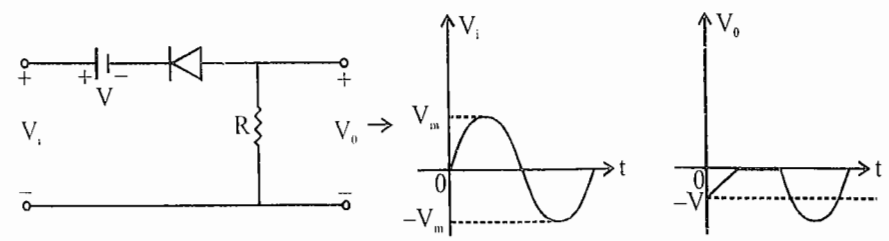


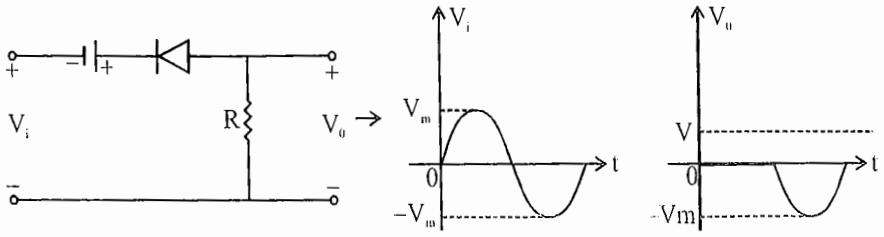
(b) Negative



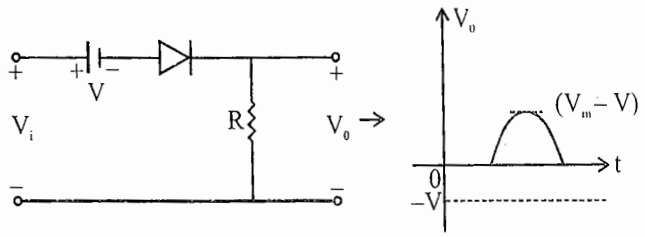
2. Biased Series Clipper (Ideal Diodes):

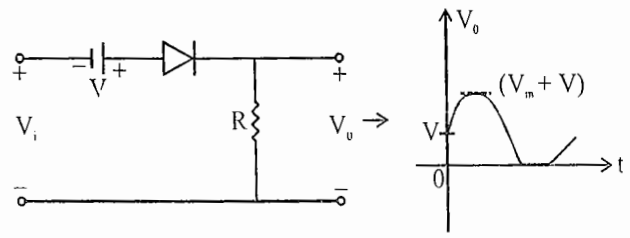
(a) Positive





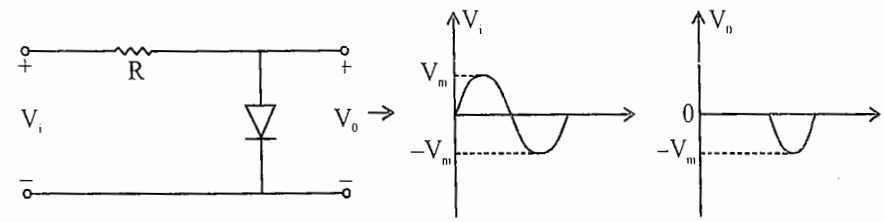
(b) Negative



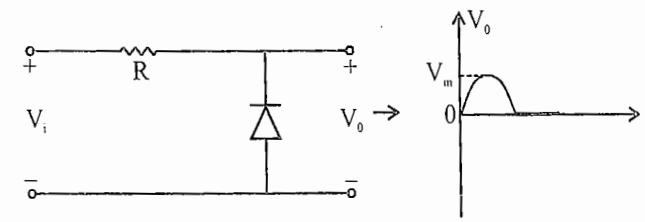


3. Simple Parallel Clipper (Ideal Diode):

(a) Positive

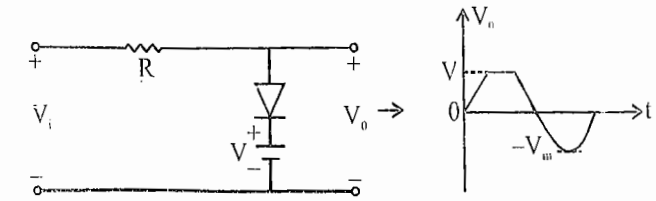


(b) Negative

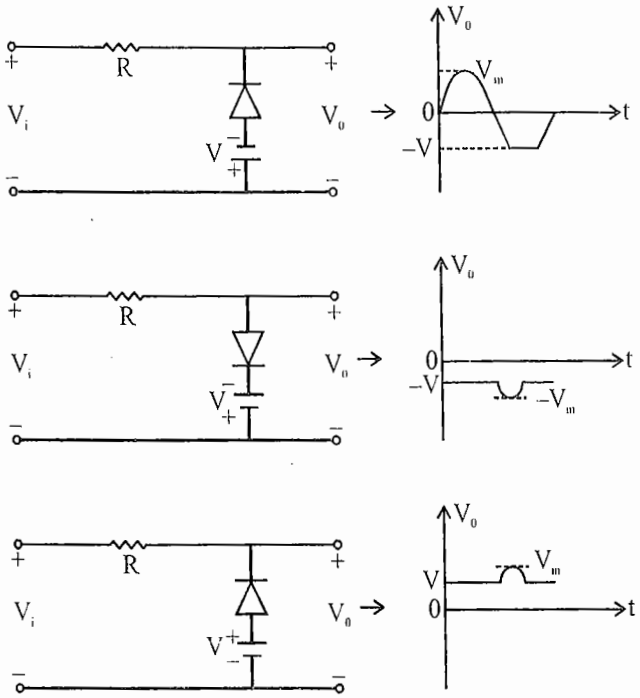


4. Biased Parallel Clippers (Ideal Diode):

(a) Positive

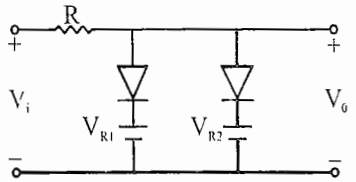


(b) Negative



Note: In all the above clipper circuit always see carefully to the connection and polarities of diode and Batteries respectively.

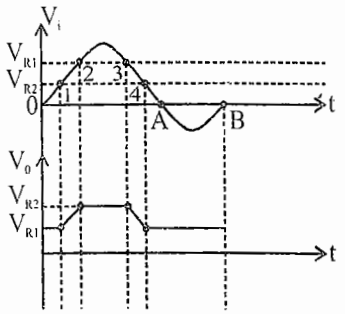
Clipping at Two Independent Levels:



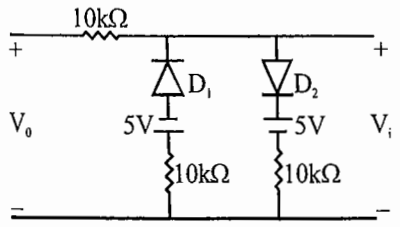
Above circuit is used to convert sinusoidal wave form into a square wave. To generate a symmetrical square wave V_R, and V_{R2} are adjusted numerically equal but of opposite sign.

Above circuit is known as slicer because the output contains a slice of input between two reference level V_{R1} and V_{R2}.

V_i	D_1	D_2	V_0
$V_i < V_{R1}$	ON	OFF	V_{R1}
$V_{R1} < V_i < V_{R2}$	OFF	OFF	V_i(o/p follow i/p)
$V_i > V_{R2}$	OFF	ON	V_{R2}



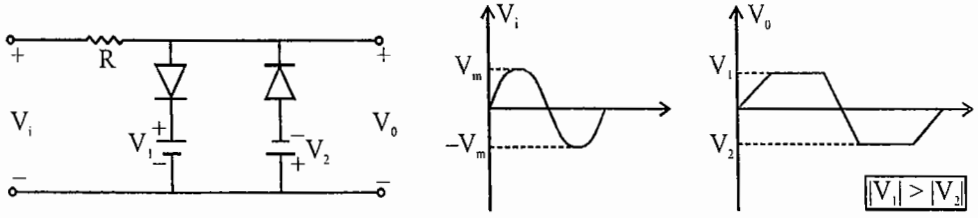
9. Assuming diodes to be ideal describe the transfer characteristic of circuit shown.



Soln. $V_0 = V_i$ for $-5 < V_i < +5$, $V_0 = \frac{V_i}{2} - 2.5$ for $V_i < -5$

$V_0 = \frac{V_i}{2} + 2.5$ for $V_i > +5$

For Level Clipping:

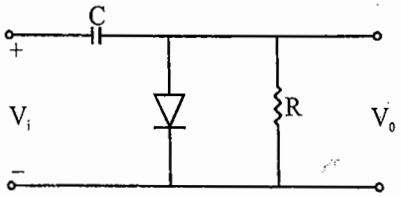


Clamper Circuit:

A clamper is a network constructed of a diode, a resistor and a capacitor that shifts a waveform to a different to level without changing the appearance of the applied signal.

Addition shift can also be obtained by introducing a do supply to the basic structure the chosen resistor and capacitor of the network must be chosen such that the time constant determined by $\tau = RC$ is sufficiently large to ensure that the voltage across the capacitor does not discharge significantly during the internal the diode is nonconducting.

Clamping network have a capacitor connected directly from input to output with a resistive element in parallel with the output.

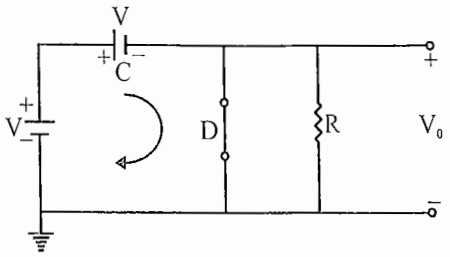


Clamping network have a capacitor connected directly from input to output with a restive element in parallel with the output signal. The diode is also in parallel with the output signal but may or may not have a series dc supply as an added element.

Analysis:

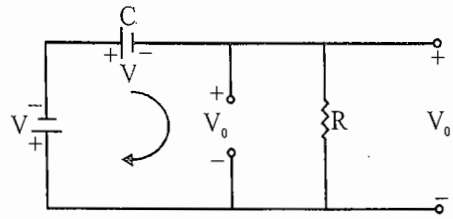
Step1: Start the analysis by examining the response of the portion of the input signal that will forward bias the diode.

Step2: During the period that the diode is "On" state, assume that the capacitor will charge up instantaneously to a voltage level determined by the surrounding network.



D (ON) → Shot

Step3: Assume that during the period when the diode is in the "off" state the capacitor holds on to its established voltage level.



D(OFF) → Open

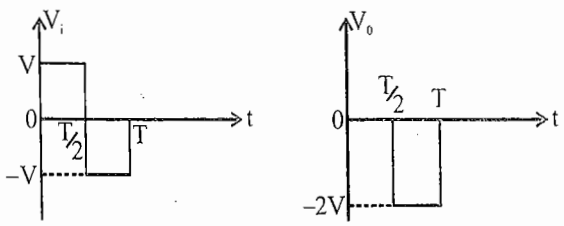
Step4: Through out the analysis, maintained a continual awareness of the location and defined polarity for V_0 to ensure that the proper levels are obtained.

Since V_0 is in the parallel with diode and resistor, it can also be drawn in the alternative position shown in step (3).

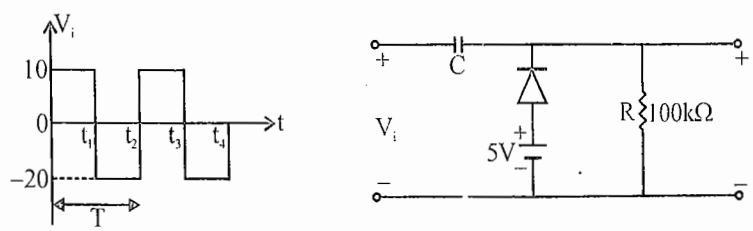
Applying KVL in input loops

$-V - V - V_0 = 0$ $\boxed{V_0 = -2V}$

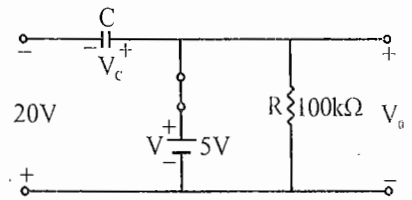
Step5: Check that the total swing of the output matches that of the input. (Very important to check the proper answer in optional questions).



10. Determine V_0 for the network given below for the indicated input?

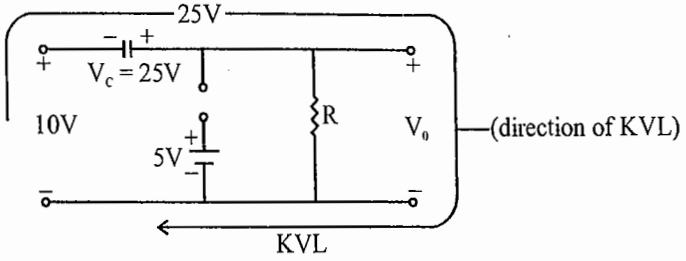


Soln. In positive half cycle



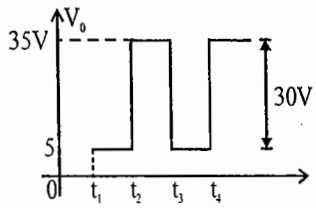
$-20V + V_C - 5V = 0$ $\boxed{V_C = 25V}$

In negative half cycle.



$+10 + 25 - V_0 = 0$ $\boxed{V_0 = 35V}$

Output signal



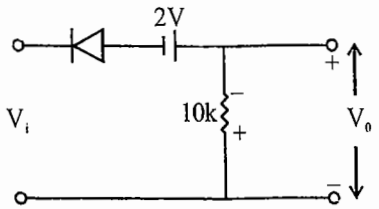
Check the total swing

Input swing = 30V ($V_{i\,max} - V_{i\,min}$), Output swing = 30v ($V_{0\,max} - V_{0\,min}$)

The wave is not start with 0 because of some finite time taken in the discharging.

11. Find the output waveform of the network.

Soln.



Step I: Condition on V_0 for the diode to be ON and OFF.

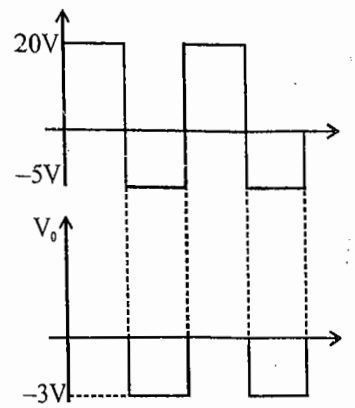
Applying KVL: $-V_i - IR - 2V = 0$, $IR = -V_i - 2V$

For D ON: $-V_i - 2V > 0 \Rightarrow V_i < -2V$

Step II: For D to be ON: $-V_i + V_0 - 2V = 0$

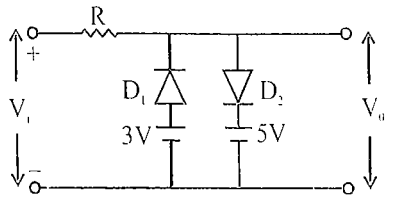
$\therefore V_0 = V_i + 2 = -5V + 2 = -3V$

D to be off: $\boxed{V_0 = 0}$



D off; $V_i > -2V$

12. Find the output waveform of the network:



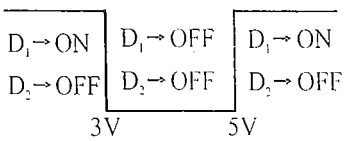
Step 1 : Let D_1 is ON, D_2 is OFF;
$-V_i - IR + 3V = 0$, $IR = -V_i + 3$

For D_1 is ON; $IR > 0 \Rightarrow -V_i + 3 > 0 \Rightarrow$ $\boxed{V_i < 3V}$

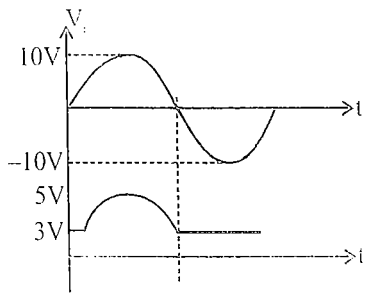
D_2 is OFF; $IR < 0 \Rightarrow$ $\boxed{V_i > 3V}$

Let D_2 is ON and D_1 is OFF; $Vi - IR - 5V = 0 \Rightarrow IR = V_i - 5$
For D_2 is ON; $IR > 0$

$\Rightarrow V_i < 5V$; D_1 is OFF $\Rightarrow IR < 0 \Rightarrow$ $\boxed{V_i < 5V}$

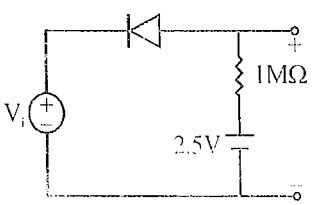


Step II:

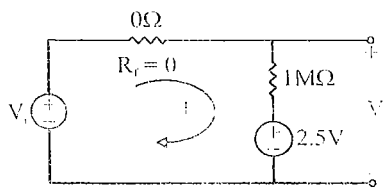


For $V_i < 3V \Rightarrow V_0 = 3V$, $3 < V_i < 5 \Rightarrow V_0 = 5V$, $V_i > 5V \Rightarrow V_0 = 3V$

13. A symmetrical 5 khz square wave whose output varies between +10V and –10V is impressed open clippling circuit shown in figure. If diode has $R_f = 0\Omega$ and $R_r = 2m\Omega$ and $V_0 = 0$. What is output waveform?



Soln.



Step-I: $-V_i - 2.5 - IR = 0$, $2.5 - V_i = IR$

D is ON; IR > 0, $V_i < 2.5V$

When D is OFF; IR < 0 $V_i > 2.5V$

Step-II: If D is ON, $V_i < 2.5V$, then output will be $\boxed{V_0 = V_i}$

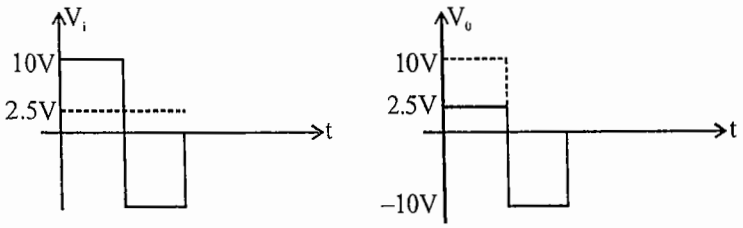
If D is off; $V_i > 2.5$ V, $V_i - 2I - 1.I - 2.5V = 0$

$$\Rightarrow 3I = V_i - 2.5V \Rightarrow \boxed{I = \frac{V_i - 2.5V}{3}}$$

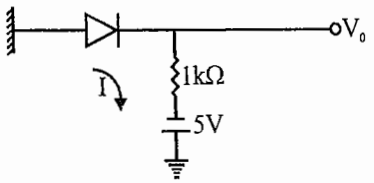
$$V_0 = 1.I + 2.5 = 1.\left(\frac{V_i - 2.5}{3}\right) + 2.5 = \frac{V_i - 2.5 + 7.5}{3}$$

$$\boxed{V_0 = \frac{V_i + 5.0}{3}}$$ (D is OFF)

Step-III: Waveform of the output



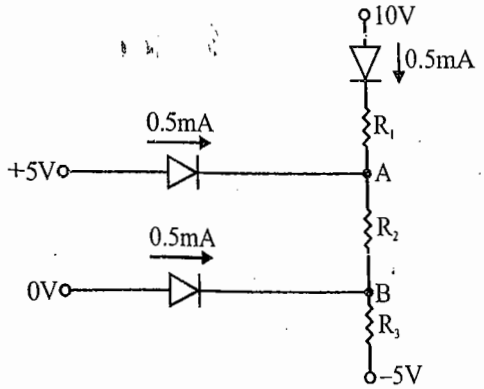
Questions Regarding Diodes



1. Calculate the value of current I in the above circuit. (Assume diode is ideal)

Soln. Apply KVL, 0 – 1K.I + 5 = 0, $\boxed{I = 5mA}$

2. The cut in voltage for each diode is 0.6V (Si) each diode current is 0.5mA. Find the value of R_1, R_2, R_3.



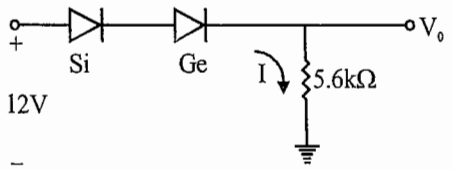
Soln. Current across R_2 = 0.5 + 0.5 = 1mA, Current across R_3 = .5 + .5 + .5 = 1.5 mA

$V_A = 5 - 0.6 = 4.4V$, $V_B = 0 - 0.6 = -0.6V$

$$R_1 = \frac{10-0.6-4.4}{0.5\,mA} = 10k\Omega, \quad R_2 = \frac{4.4-(-0.6)}{(0.5+0.5)mA} = \frac{5}{1mA} = 5k\Omega,$$

$$R_3 = \frac{-0.6-(-5V)}{(.5+.5+.5)mA} = \frac{4.4}{1.5mA}, \quad R_3 = 2.93\,k\Omega$$

3.



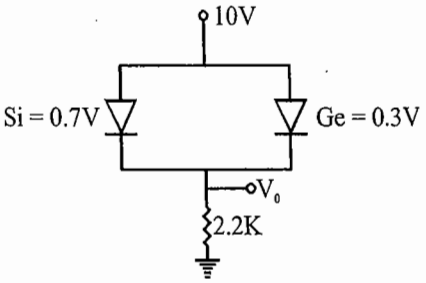
Calculate the value of current I. Cut in voltage of Si = 0.7V and Ge = 0.3V.

Soln. Applying KVL in the given circuit

$12 = 0.7 + 0.3 + I \times 5.6\ K$

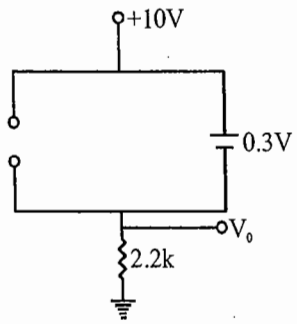
$$12 - 1 = I \times 5.6K, \quad I = \frac{11}{5.6}K \quad \boxed{I = 1.96\,mA}$$

4.



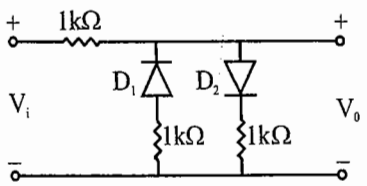
Find value of V_0 in the given circuit.

Soln. Both Si and Ge are in forward bias but Ge will attain cut off early. So Si will not conduct.



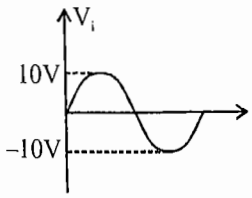
Applying KVL $10 - 0.3 = V_0$, $\boxed{V_0 = 9.7V}$

5.



$V_i = 10 \sin \omega t$

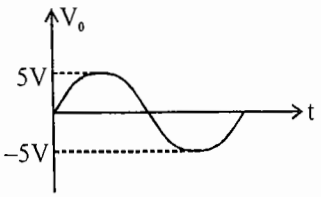
Sketch the output waveform if the input signal is indicated as:



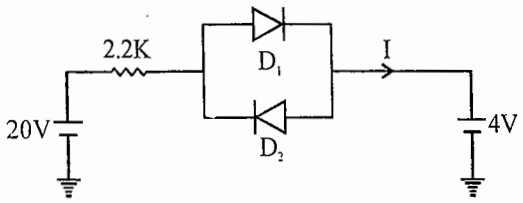
Soln. When $V_i < 0$, $D_1 \rightarrow$ ON, $D_2 \rightarrow$ OFF

$-V_i - IR - IR = 0$, $2IR = -V_i$, $IR > 0$ $\boxed{V_0 = \frac{V_i}{2}}$

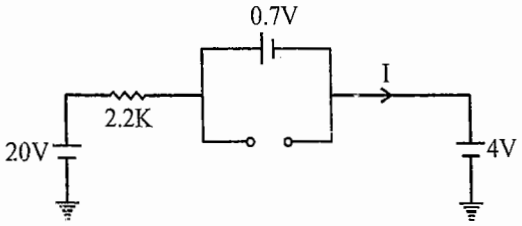
Step-II : For $V_i > 0$, $V_0 = \frac{V}{2} = 5V$, if $V_i < 0$, $V_0 = \frac{V}{2} = 5V$



6. Find the value of I in the circuit given below. (where cut in voltage of diode D_1 and $D_2 = 0.7$).



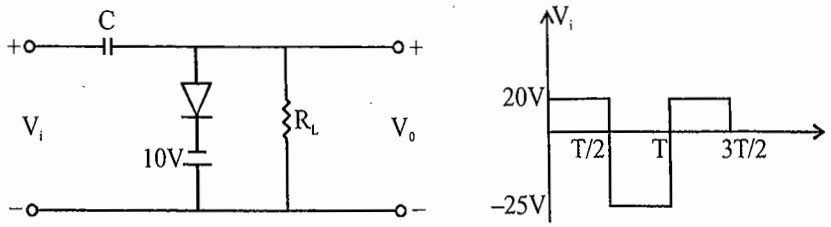
Soln. D_2 is in reverse biased so open circuited and no current flow across D_2. Only D_1 is conducting and allow to pass the current equivalent circuit is



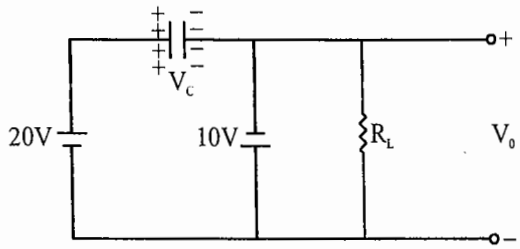
Applying KVL $20 - 2.2\,K.I - 0.7 - 4 = 0$, $I = \frac{15.3}{2.2K}$ $\boxed{I = 6.95\,mA}$

Examples on Clamper Circuit

1. Draw the waveform of the following circuit.



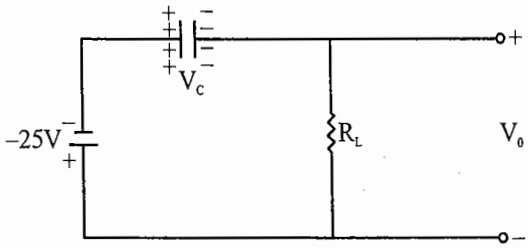
Soln. **Step-I:** (When diode is ON for $0 \rightarrow \frac{I}{2}$)



Applying KVL in left side loop

$Z_0 - V_C + 10 = 0$ $\boxed{V_C = 30V}$ $\boxed{V_0 = -10V}$

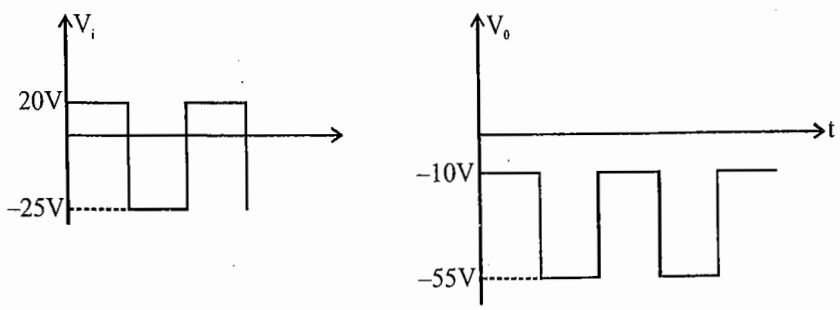
Step-II: When diode is OFF $(T/2 \rightarrow T)$



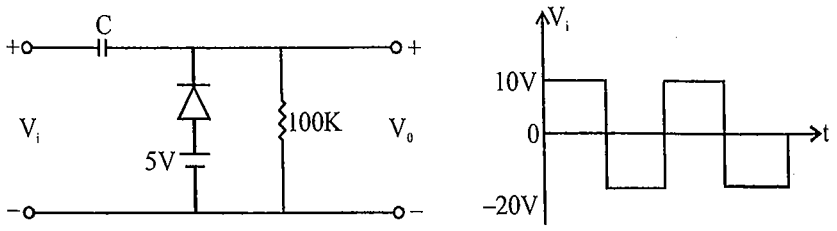
Applying KVL $-25 - V_C - V_0 = 0$, $V_0 = -25 - V_C$,

$V_0 = -25 - 30$ $\boxed{V_0 = -55V}$

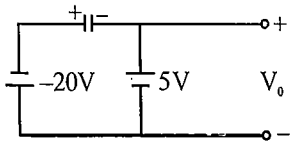
Step-III:



2. Draw the output waveform of the following circuit?

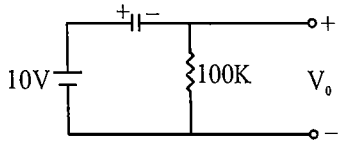


Soln. **Step-I:** When diode is on; $\left(\frac{T}{2} \to T\right)$

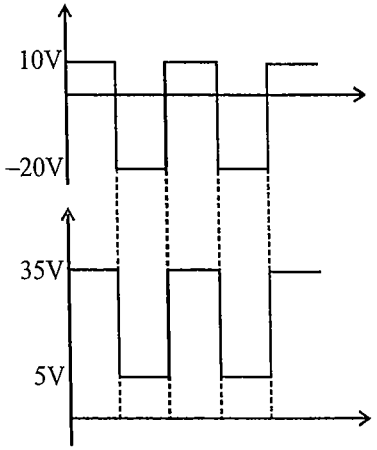


Apply KVL: $-20 - V_C - 5 = 0 \Rightarrow \boxed{V_C = -25} \Rightarrow \boxed{V_0 = 5V}$

Step-II: When diode is off; for $\left(T \to 3\frac{T}{2}\right)$



Apply KVL: $10 - V_C - V_0 = 0$; $V_0 = 10 - (-25)$ $\boxed{V_0 = 35V}$



Total swing of input = total swing of output

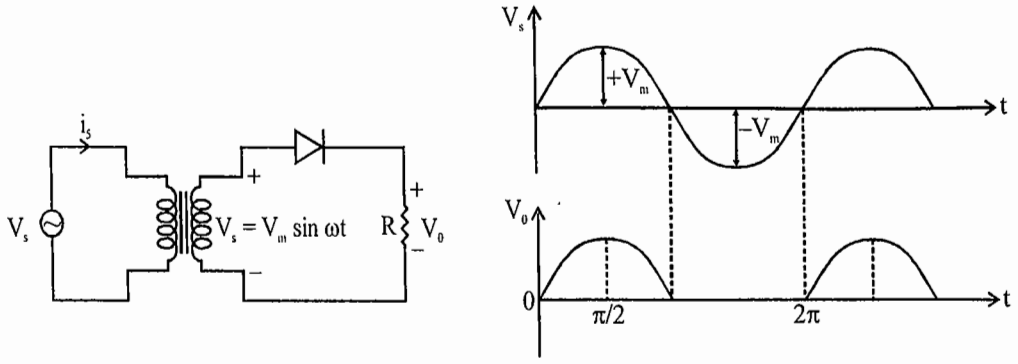
Single, Phase Diode Rectifiers:

Rectifier is a device used for converting AC signal to pulsating DC as output.

A rectifier may half wave type or full wave type.

Single Phase Half Wave Rectifier:

This is the unidirectional rectifier.



Average value of output voltage:

$$V_{avg} = \frac{1}{2\pi}\left[\int_0^{\pi} V_m \sin \omega t \; d(\omega t)\right], \quad V_{avg} = \frac{V_m}{2\pi}\left[-\cos \omega t\right]_0^{\pi}$$

$$V_{avg} = \frac{V_m}{\pi} \qquad \ldots (1)$$

RMS value of output voltage

$$V_{rms} = \left[\frac{1}{2\pi}\int_0^{\pi} V_m^2 \sin^2 \omega t . d(\omega t)\right]^{1/2} = \frac{V_m}{\sqrt{2\pi}}\left[\int_0^{\pi} \frac{1-\cos 2\omega t}{2} . d(\omega t)\right]^{1/2} = \frac{V_m}{2} \qquad \ldots (2)$$

Form factor $F = \dfrac{V_{rms}}{V_{avg}} = \dfrac{V_m/2}{V_m/\pi} = \dfrac{\pi}{2}$

$$\boxed{F = 1.57} \qquad \ldots (3)$$

Ripple factor $(r) = \sqrt{F^2 - 1} = \sqrt{(1.57)^2 - 1}$

$= 1.21$ ... (4)

Ripple frequency is the same as the input frequency in this case.

Peak Inverse Voltage (PIV):

PIV is the rating of diode. It is defined as the maximum reverse voltage, diode can withstand.

$$\boxed{PIV = V_m} \qquad \ldots (5)$$

Ripple Voltage:

$$V_r = \sqrt{V_{rms}^2 - V_{avg}^2} \qquad \ldots (6)$$

$$V_r = \sqrt{\left(\frac{V_m}{2}\right)^2 - \left(\frac{V_m}{\pi}\right)^2} \qquad \boxed{V_r = 0.3856\, V_m}$$

Rectifier Efficiency: $\eta = \dfrac{P_{dc}}{P_{ac}}$

$\because$ Output d.c. power, $P_{dc} = V_{avg} . I_{avg} = \dfrac{V_m}{\pi} \times \dfrac{I_m}{\pi}$ ... (7)

R.M.S. Output Voltage:

$$V_{rms} = \frac{V_m}{2} \qquad \ldots (8)$$

and r.m.s. output current $I_{rms} = \frac{V_{rms}}{(R + r_d)} = \frac{V_m}{2(R + r_d)}$

Where r_d is the diode, resistance for ideal diode, $\boxed{r_d = 0}$

$$I_{rms} = \frac{V_m}{2R} = \frac{I_m}{2}$$

Output Power $P_{ac} = V_{rms} . I_{rms} = \frac{V_m}{2} \times \frac{I_m}{2}$

$\therefore$ Rectification efficiency $(\eta) = \frac{P_{dc}}{P_{ac}} = \frac{V_m I_m / \pi^2}{V_m I_m / 4} = \frac{4}{\pi^2} = 0.4053$

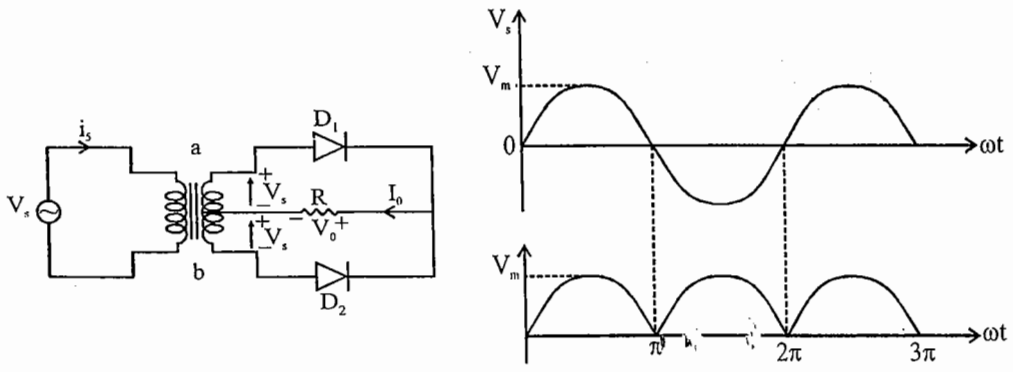
$\boxed{\eta = 40.53\%}$

R.M.S. value of source current $I_{RMS} = \frac{I_m}{2}$ ... (19)

Crest factor = $\frac{\text{Peak Value}}{\text{RMS Value}} = \frac{I_m}{I_m / 2}$ ... (20)

= 2

Single Phase Full wave Mid-point Rectifier (Centre Tap):



D.C. or average output voltage

$$V_{avg} = \frac{2V_m}{\pi} \qquad \ldots (1)$$

D.C. output current

$$I_{avg} = \frac{2V_m}{\pi R} = \frac{2}{\pi} I_m \qquad \ldots (2)$$

Where, I_m = Maximum value of load current = $\frac{V_m}{R}$

Output d.c. power, $P_{dc} = V_{avg}\ I_{avg} = \frac{4}{\pi^2} V_m\ I_m$ ... (3)

RMS output current $I_{rms} = \frac{V_m}{\sqrt{2}R} = \frac{I_m}{\sqrt{2}}$ ... (4)

Output a.c. power

$$P_{ac} = V_{rms}\ I_{rms} = \frac{V_m}{\sqrt{2}} \cdot \frac{I_m}{\sqrt{2}} = \frac{V_m \cdot I_m}{2}$$ ... (5)

Rectifier Efficiency:

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{4}{\pi^2} V_m\ I_m \times \frac{2}{V_m\ I_m} = \frac{8}{\pi^2} = 0.8106$$

$$\boxed{\eta = 81.06\%}$$ ... (6)

Form factor (f) = $\frac{V_{rms}}{V_{avg}} = \frac{V_m/\sqrt{2}}{2V_m/\pi} = \frac{\pi}{2\sqrt{2}}$

$$\boxed{F = 1.11}$$ ... (7)

Ripple Voltage

$$V_r = \sqrt{V_{rms}^2 - V_{avg}^2} = \left[\left(\frac{V_m}{\sqrt{2}}\right)^2 - \left(\frac{2V_m}{\pi}\right)^2\right]^{1/2} = 0.3077\ Vm$$ ... (8)

Voltage ripple factor (VRF) = $\frac{V_r}{V_{avg}} = 0.3077\ V_m \times \frac{\pi}{2V_m}$

= 0.483 ... (9)

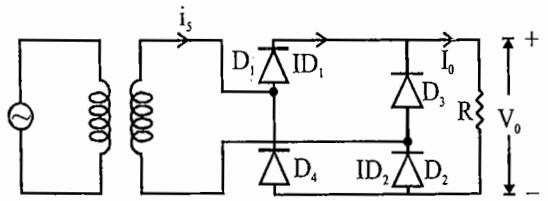
PIV for each diode = $2V_m$ ... (10)

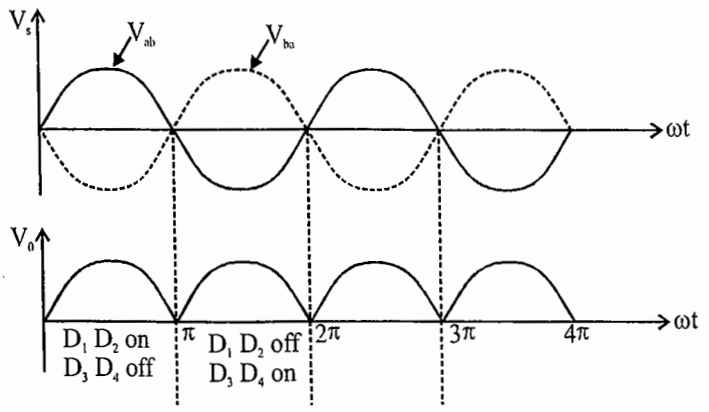
Peak value of source current, $\left(I_s = \frac{I_m}{\sqrt{2}}\right)$ ... (11)

Crest factor of input current = $\frac{I_{peak}}{I_{rms}}$ ... (12)

$$= \frac{I_m}{I_m/\sqrt{2}} = \sqrt{2}\ \boxed{C.F. = 1.414}$$

Single Phase Full Wave Bridge Rectifier:





Average output voltage: $\boxed{V_{ag} = \frac{2V_m}{\pi}}$ ... (i)

Average output current: $\boxed{I_{avg} = \frac{2I_m}{\pi}}$ ...(ii)

RMS value of output voltage $\boxed{V_{rms} = \frac{V_m}{\sqrt{2}}}$ ... (iii)

and $\boxed{I_{rms} = \frac{I_m}{\sqrt{2}}}$ ... (iv)

RMS value of source voltage $V_S = \frac{V_m}{\sqrt{2}}$

RMS value of source current $I_S = \frac{I_m}{\sqrt{2}}$

Source current waveform for both types are identical, therefore

$\boxed{CF = \sqrt{2}}$ ... (v)

A comparison of three types of 1-phase diode rectifier which are given below:

	Parameter	Half Wave (or one Pulse)	Full Wave (or two Pulse) Centre-top	Bridge
1.	DC output voltage V_{avg}	$\frac{V_m}{\pi}$	$\frac{2V_m}{\pi}$	$\frac{2V_m}{\pi}$
2.	RMS value of output voltage V_{rms}	$\frac{V_m}{2}$	$\frac{V_m}{\sqrt{2}}$	$\frac{V_m}{\sqrt{2}}$
3.	Ripple voltage V_r	0.3856 V_m	0.3077 V_m	0.3077 V_m

Dra
(i)
(ii)
Note

1. Whe V_0 is

(a)

(c)

Soln. Duri curr The Cor

2. If the (a) 1

Soln. We k

4.	Voltage ripple factor (V.R.F.)	1.211	0.482	0.482
5.	Rectification efficiency (η)	40.53%	81.06%	81.06%
6.	TUF	0.2865	0.672	0.8106
7.	PIV	V_m	$2V_m$	V_m
8.	No. of diodes	1	2	4
9.	Ripple frequency	f	2f	2f

Drawback of Centre-tapped type Rectifiers:

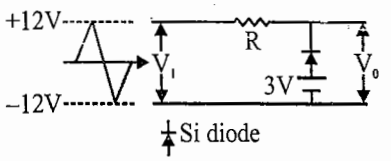
(i) This is costly and bulky because secondary winding is doubled.

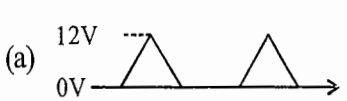
(ii) Tapping exactly centre is not all feasible.

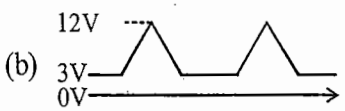
Note: Overall bridge rectifier is better than centre tapped type rectifier.

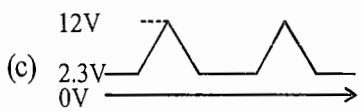
SOLVED PROBLEMS

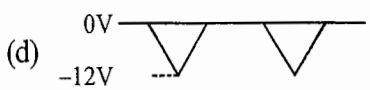
1. When an input voltage V_i, of the form shown, is applied to the circuit given below, the output voltage V_0 is of the form **[GATE 2007]**











Soln. During positive half cycle it input voltage $V_i < 3$ then the diode will be in forward biased and conducts current. So, out will be 3 volt. But when $v_i > 3$ then the diode is reverse biased and does not conduct. The input wave form is then simply transmitted to the output.

Correct option is (b)

2. If the peak outoput voltage of a full wave rectifier is 10 V, its d.c. voltage is **[GATE 2012]**

(a) 10.0V (b) 7.07V (c) 6.36 V (d) 3.18V

Soln. We know that,

$$V_{dc} = \frac{2V_0}{\pi} = \frac{2\times 10}{\pi} = 6.36 \text{ volt}$$

3. A Ge semiconductor is doped with acceptor impurity concentration of 10^{15} atoms/cm^3. For the given hole mobility of 1800 cm^2 / V – s, the resistivity of this material is: **[GATE 2012]**

(a) 0.288 Ω cm (b) 0.694 Ω cm (c) 3.472 Ω cm (d) 6.944 Ω cm

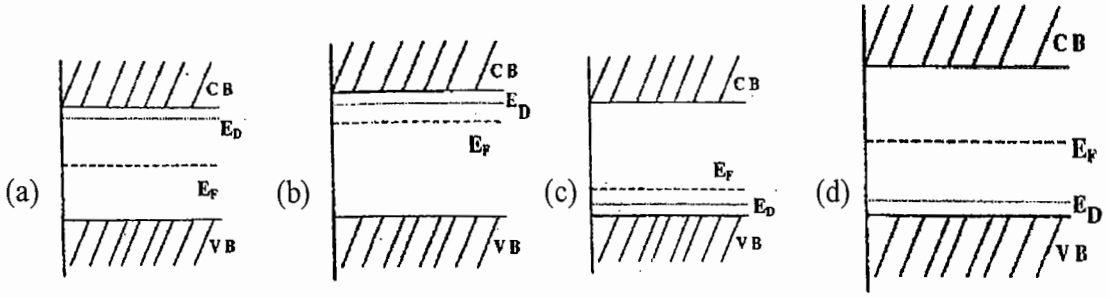
Soln. We know that,

$$\text{Conducting, } \sigma = eN_C\mu_e = 1.6\times10^{-19}\times10^{15}\times1800 = 0.288\ mho/cm$$

$$\text{Therefore, resistivity, } \rho = \frac{1}{\sigma} = 3.472\ cm\Omega$$

Correct option is (c)

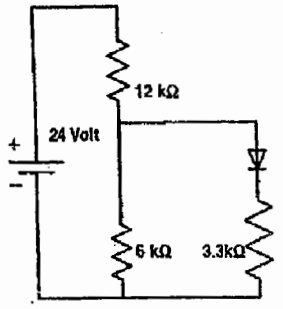
4. Identify the CORRECT energy band diagram for silicon doped with Arsenic. Here CB, VB, E_D and E_F conduction band, valence band, impurity level and Fermi level, respectively. **[GATE 2012]**



Soln. Arsenic is a pentavalent atom. So, it will produce n-type semiconductor. So, Fermi level move towards conducting band.

Correct option is (b)

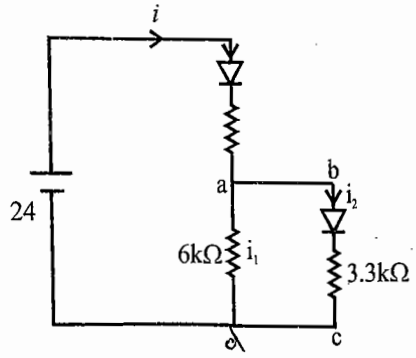
5. In the following circuit, the voltage drop across the ideal diode in forward bias condition is 0.7 V.



The current passing through the diode is **[GATE 2012]**

(a) 0.5 mA (b) 1.0 mA (c) 1.5 mA (d) 2.0 mA

Soln.



From node abcd we can write,

$$6i_1 = 0.7 + 3.3i_2$$

$$\Rightarrow \quad 6i_1 - 3.3i_2 = 0.7 \qquad \ldots (i)$$

Also, we can write,

$$24 = 12 \times (i_1 + i_2) + 6i_1$$

$$\Rightarrow \quad 4 = 2(i_1 + i_2) + i_1$$

$$\Rightarrow \quad 3i_1 + 2i_2 = 4 \qquad \ldots (ii)$$

Multiply by 2 in equation (ii) and (ii)-(i), we get

$$4i_2 + 3.3i_2 = 7.3$$

$$\Rightarrow \quad i_2 = 1\ mA$$

Correct option is (b)

PRACTICE SET

1. While analyzing circuits with a diode, the graphical method is often used because

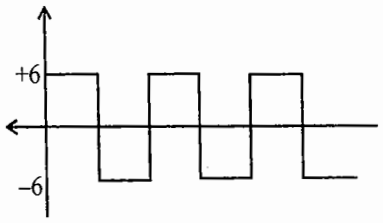
(a) graphs give more accurate answer than solutions of equations

(b) nodal or mesh analysis can not be used for the non-linear diode circuits

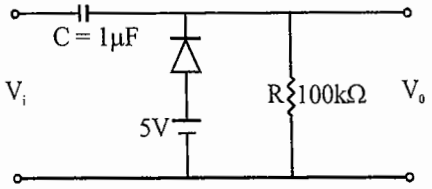
(c) solution of circuits equations leads to multiple answer, which is unphysical

(d) the non-linear diode equation makes the solution of the circuit equations very difficult.

2. V_i is given by

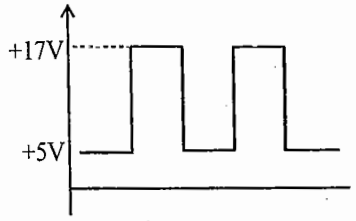


The input V_i is given to the circuit shown below:

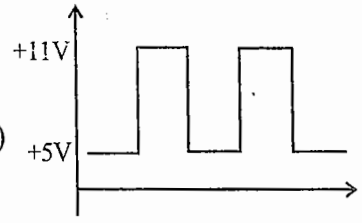


The V_0 is

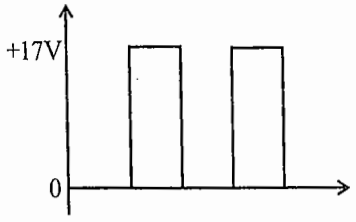
(a)



(b)

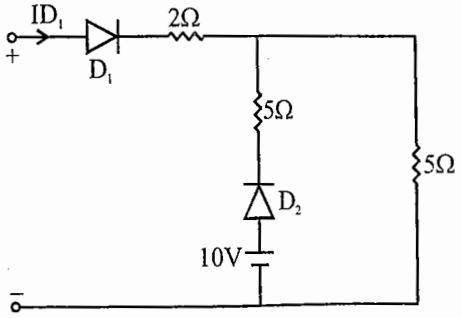


(c)



(d) NOT

3. Calculate I_D and ID_2 in the circuit shown below. Assume the diodes are ideal.



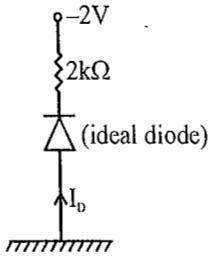
(a) $ID_1 = -0.5A$; $ID_2 = IA$

(b) $ID_1 = 0A$; $ID_2 = IA$

(c) $ID_1 = -0.5A$; $ID_2 = 2A$

(d) $ID_1 = 0A$; $ID_2 = 2A$

4. Calculate the current I_D in the circuit shown below

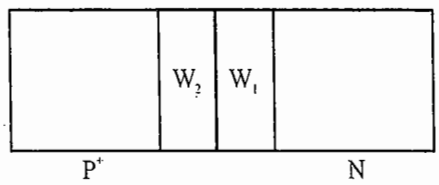


(a) 1 mA (b) –1 mA (c) 0 (d) 2 mA

5. The width of the depletion layer is proportion to

(a) $\sqrt{\text{Doping}}$ (b) $\frac{1}{\sqrt{\text{Doping}}}$ (c) Doping (d) $\frac{1}{\text{Doping}}$

6. Which of the following option is correct for P^+N diode shown below:

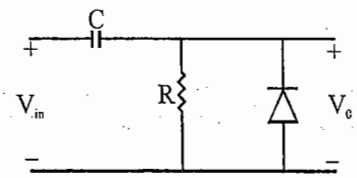


(a) $W_2 = W_1$ (b) $W_1 > W_2$ (c) $W_1 < W_2$ (d) $W_1 = W_2 = 0$

7. The transition capacitance of a diode is proportion to

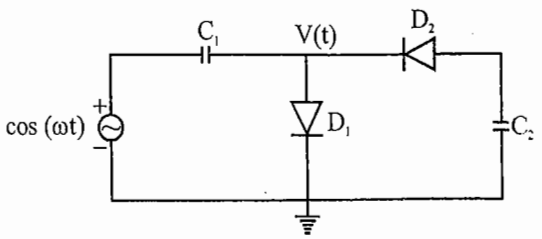
(a) $\frac{1}{\sqrt{\text{Reverse bias}}}$ (b) $\frac{1}{\text{Reverse bias}}$ (c) Reverse bias (d) $\sqrt{\text{Reverse bias}}$

8. The circuit in figure is



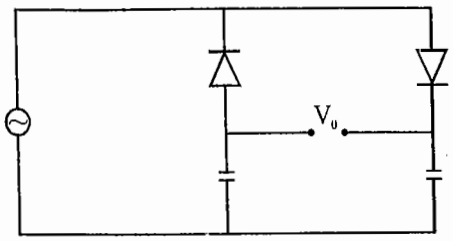
(a) Positive clamper (b) Negative clamper
(c) Positive peak clipper (d) Negative peak clipper

9. The diodes and capacitors in the circuit shown are ideal. The voltage V(t) across the diode D_1 is:



(a) $\cos(\omega t) - 1$ (b) $\sin(\omega t)$ (c) $1 - \cos(\omega t)$ (d) $1 - \sin(\omega t)$

10. The circuit shown in the figure is best described as a

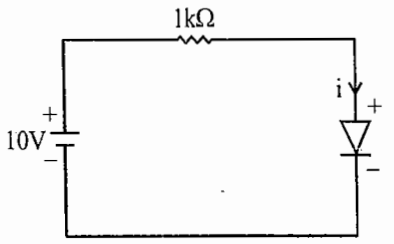


(a) bridge rectifier (b) ring modulator

(c) frequency discrimination (d) voltage doubler

11. The i-V characteristic of the diode in the circuit given below are

$$i = \begin{cases} \dfrac{V-0.7}{500} A & V \geq 0.7V \\ 0A & V < 0.7V \end{cases}$$



The current in the circuit is

(a) 10 mA (b) 9.3 mA (c) 6.67 mA (d) 6.2 mA

12. A p^+ n junction has a built in potential of 0.8V. The depletion layer width at a reverse bias of 1.2V is 2μm. For a reverse bias of 7.2 V, the depletion layer width will be

(a) 4μm (b) 4.9 μm (c) 8μm (d) 12 μm

13. In a P^+ n junction diode under reverse bias, the magnitude of electric field is maximum at

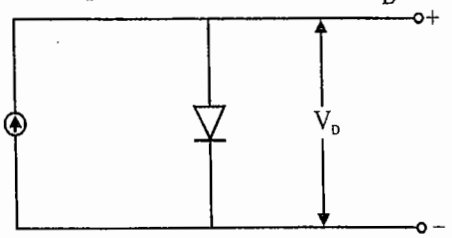
(a) the edge of the depletion region on the p-side

(b) the edge of the depletion region on the n-side

(c) the p^+n junction

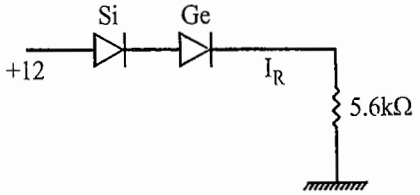
(d) the centre of the depletion region on the n side.

14. In the figure, silicon diode is carrying a constant current of 1mA, when the temperature of the diode is 20°C, V_D is final to be 700 mV. If the temperature rises to 40°C, V_D becomes approximately equal to



(a) 740 mV (b) 660mV (c) 680 mV (d) 700 mV

15. Value of I_R is {V cutin for Si = 0.7V, Gi = 0.2V}



(a) 2.56mA (b) 0 (c) 1.25 mA (d) 1.96mA

16. For an ideal diode operating in forward bias, change in diode voltage required for a 10 times inverse diode current is

(a) 83 mV (b) 59 mV (c) 60 mV (d) 62.10 mV

17. A p-n junction diode is operating in reverse bias region. The applied reverse bias at which the ideal reverse current reaches 80% of its reverse saturation value is

(a) 41.68 mV (b) 59.6 mV (c) 4.8 mV (d) 42.3 mV

18. Reverse saturation current of silicon diode of 25°C is 20nA. The reverse saturation current at 60°C will be

(a) 20×4.5 nA (b) $20 \times e^{4.5}$ nA

(c) $20 \times 2^4.2^5$ nA (d) $20 \times (4.5)^2$ nA

19. The leakage currents of a transistor are $I_{CBO} = 5\,\mu A$, $I_{CEO} = 0.4$ nA and $I_B = 30\,\mu A$. The value of I_C is

(a) 247 nA (b) 257 nA (c) 277 nA (d) 287 nA

20. Si is preferred over Ge because

(a) Silicon has higher PIV

(b) Silicon is cost effective

(c) Silicon is found in abundance in nature

(d) N.O.T.

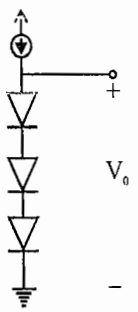
21. In a centre tapped FULL WAVE rectifier the PIV of each diode is

(a) $\geq 2Vm$ (b) $\geq Vm$ (c) $\leq 2Vm$ (d) $\geq Vm$

22. PIV of a full wave bridge type rectifier should be at least.

(a) Vm (b) 2Vm (c) $\frac{Vm}{2}$ (d) $\frac{2Vm}{\pi}$

23. The circuit shown uses three identical diode having $n = 1$, $I_S = 10^{-14}$ A. Find the value of the current I to produce $V_0 = 2$ volt.



(a) 3.81 nA (b) 3 nA (c) 2.8 nA (d) 6 nA

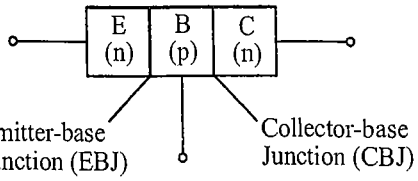
ANSWER KEY

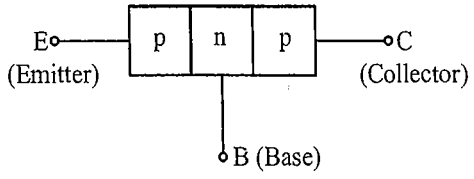
1. (d)	**2.** (a)	**3.** (b)	**4.** (a)	**5.** (c)
6. (b)	**7.** (d)	**8.** (a)	**9.** (a)	**10.** (d)
11. (d)	**12.** (a)	**13.** (c)	**14.** (b)	**15.** (d)
16. (b)	**17.** (a)	**18.** (b)	**19.** (c)	**20.** (c)
21. (a)	**22.** (a)	**23.** (a)		

Chapter 3

Bipolar Junction Transistors

- The bipolar junction transistor has three separately doped regions and contains two pn junctions.
- A single p-n junction has two modes of operation forward bias and reverse bias.
- The bipolar transistor, with two P-N junction, therefore has four possible modes of operation, depending on the bias condition of each p-n junction, which is one region for the vergatility of device.
- With three separately doped regions, the bipolar transistor is a three terminal device.
- The basic transistor principle is that the voltage between the two terminals controls the current through the third terminal.
- Current in the transistor is due to the flow of both electrons and holes, hence the name bipolar.
- The n-p-n bipolar transistor contains a thin p-region between two n-regions. In contrast the p-n-p bipolar transistor contains a thin n-region sandwiched between two p-regions.
- The three regions and their terminal connections are called the emitter, base and collector.
- The operation of the device depends, on the two p-n junction being in close proximity, so the with of the base must be very narrow, normally in the range of tenths of a micrometer (10^{-6} m).



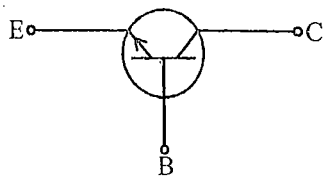


- Of the tree regions, emitter is heavily doped. The next level of doping is collector and base is less than that of collector.

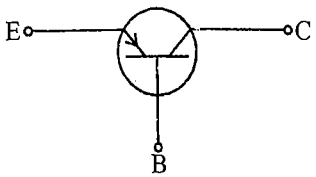
$$N_E > N_C > N_B$$

- The doping of the sandwiched layer is considerably less than that of the outer layers
- Emitter is provided with medium area.
- Base is provided with smallest area to reduce the transit time.
- Collector is provided with the largest area to withstand heat dissipation.

Symbol:



(n-p-n transistor symbol)



(p-n-p transistor symbol)

Modes of Operation:

Mode of Operations	J_1 (B-E)	J_2 (C-B)	Applications
Active region	FB	RB	As an amplifier
Saturation region	FB	FB	As an electronic switch
ON/OFF region	RB	RB	In digital circuit
Reverse active mode or inverted mode	RB	FB	As an amplifier with voltage and current gain to be low

- In a transistor

Emitter current - drift current

Base current - recombination current

Collector current - diffusion current

- The flow of charge carriers in a transistor between base and collector is due to the diffusion of minority carriers and this action is called "transistor action". Hence, transistor action takes place in the base region.
- The total current flowing into the transistor must be equal to the total current flowing out of if (applying Kirchhoff's current law to the transistor as if it were a single node). Hence, the emitter current is equal to the sum of the collector are and base currents.

$$\boxed{I_E = I_C + I_B}$$

- The collector current comprise two components the majority and the minority carriers. The minority carrier current is called the leakage current and is given the symbol I_{CO} (I_C current will with emitter terminal open).

$$\boxed{I_C = I_{C\,majority} + I_{CO<minority}}$$

I_{CO}:

- It is also known as collector reverse saturation current or thermally generated current in the transistor.
- I_{CO} for
  Ge transistor is μA range, Si transistor is nA range.
- I_{CO} is very sensitive to temperature.
- I_{CO} doubles for every 10°C rise in temperature
- For 1°C, I_{CO} approximately increases by 7%.

$$\boxed{I_{CO(T_2)} = I_{CO(T_1)}\, 2^{\left(\frac{T_2 - T_1}{10}\right)}}$$

- I_{CO} is independent of collector supply voltage.
- The collector current is less than the emitter current. There are two reasons for this. Firstly, a part of the emitter current consists of holes that do not contribute to the collector current secondly, not all the electrons injected into the base are successful in reaching the collector.

Equation for Emitter Current:

- In a transistor under active region, emitter current is the forward current of emitter diode.

$$\boxed{I_E = I_{CO}\, e^{V_{BE}/\eta V_T}} \cong I_C$$

- The emitter current exponentially increases with base to emitter voltage of transistor.
- In a transistor under active region $V_{BE} < 1V$.

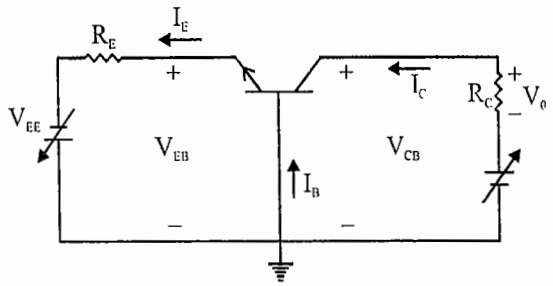
  Typical value 0.2 V, For Si transistor $\boxed{V_{BE} = 0.6V \text{ to } 0.9V}$

  Typical value 0.7V
- V_{BE} reduced by 2.5 mV for 1°C rise in temperature, i.e.

$$\boxed{\frac{\partial V_{BE}}{\partial T} = -2.5\,mV/^{\circ}C}$$

Common Base Configuration:

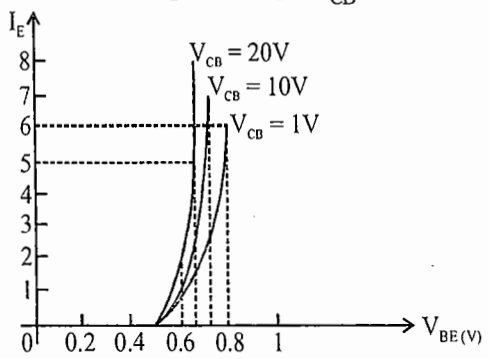
- To fully describe the behaviour of a three terminal devices such as the common base amplifier, requires two set of characteristics one for the 'driving point' or input parameters and the other for the output side.



(n-p-n transistor C-B configuration)

Input Characteristics:

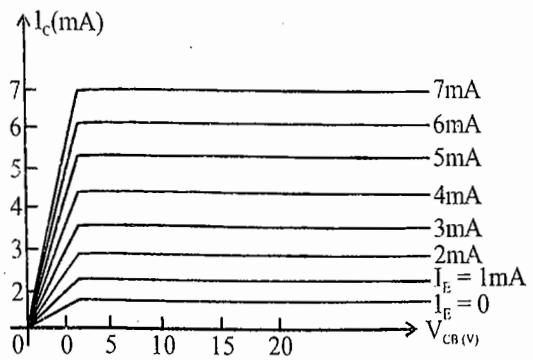
- The input set for the common-base amplifier as shown in figure relates an input current (I_E) to an input voltage (V_{BE}) for various levels of output voltage V_{CB}.



(Input or driving painting characteristic for CB silicon transistor amplifier)

Output Characteristic:

- It relates I_C to V_{CB} for various levels of input current I_B as shown.



(Output or collector characteristics for a CB transistor amplifier)

- CB transistor is basically a current controlled current source (CCCS).
- The curves clearly indicate that a first approximation to the relationship between I_E and I_c in the active region is given by

$$\boxed{I_C \cong I_E}$$

Properties of CB Configuration:

- Lowest input resistance ($R_i < 100\,\Omega$)
- Highest output resistance ($R_0 > 1M\Omega$)
- Lowest current gain ($\alpha < 1$)
- Highest voltage gain
- Medium power gain (typical value 68)
- Output and input voltages are in phase i.e. phase shift is 0°.
- In CB amplifier current gain is loss and therefore bandwidth is large and hence CB amplifier is widely used as high frequency (Cascode amplifier)

Alpha (α):

- In the dc mode the levels of I_C and I_E due to the majority carriers are related by a quantity called alpha and defined by the following equation.

$$\boxed{\alpha_{dc} = \left|\frac{I_C}{I_E}\right|} \qquad \boxed{I_C = \alpha I_E + I_{CBO}}$$

Where I_{CBO} is collector to base current when emitter terminal is open.

- For ac situations where the point of operation moves on the characteristic curve, an ac alpha is defined by.

$$\boxed{\alpha_{ac} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}=\text{Constant}}}$$

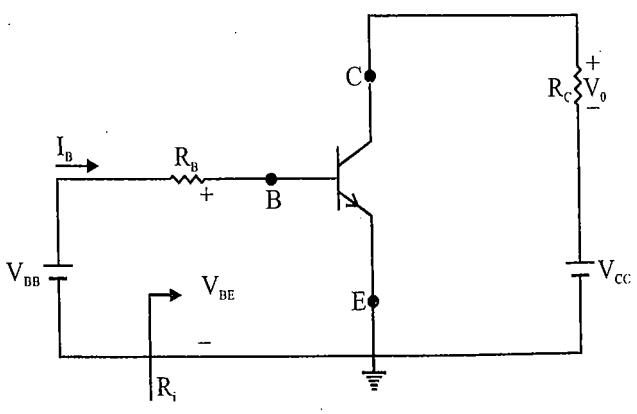
α : CB current gain

- The alpha is formally called common base amplification factor on current gain of common base transistor.

Note: The transistor's amplifying action i's basically due to its capability of transfer its signal current from a low resistance circuit to high resistance circuit, contracting the two terms transfer and resistor results in the name transistor; i.e.

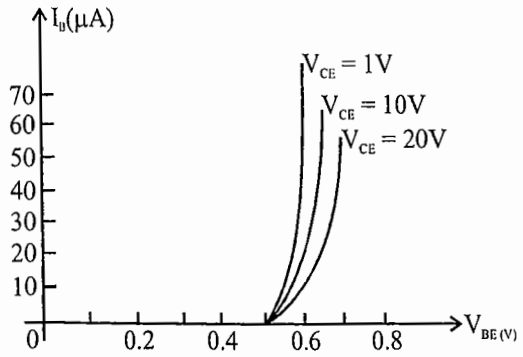
$$\boxed{\text{transfer} + \text{resistance} \rightarrow \text{transistor}}$$

Common-Emitter Configurations:



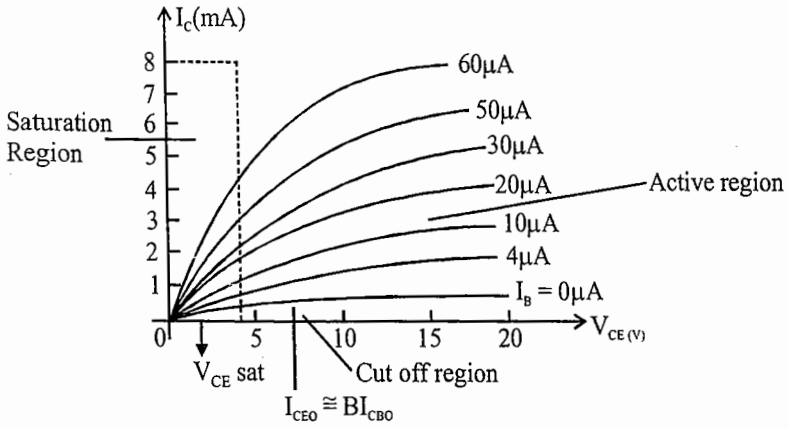
Input Characteristics:

The input characteristics are a plot of the input current (I_B) versus the input voltage (V_{BE}) for a range of values of output voltage V_{CE}.



Output Characteristics:

The output characteristics are a plot of the output current (I_C) versus output voltage (V_{CE}) for a range of values of input current (I_B).



Properties:

- Moderate input resistance (around 1kΩ)
- Moderate output resistance (50kΩ to 500 kΩ)
- Moderate current gain (typical value 49)
- Moderate voltage gain
- Highest power gain (typical value 4226)
- Output and input voltages are out of phase shift = 180°.
- It is most common and frequency used amplifier.

Beta (β):

In dc model $\boxed{\beta_{dc} = \frac{I_C}{I_B}}$ $(\beta > 1)$ For ac $\boxed{\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}=\text{constant}}}$

Range of β is 30 to 300. β in terms of α is $\boxed{\beta = \frac{\alpha}{1-\alpha}}$ $\boxed{\alpha = \frac{\beta}{1+\beta}}$

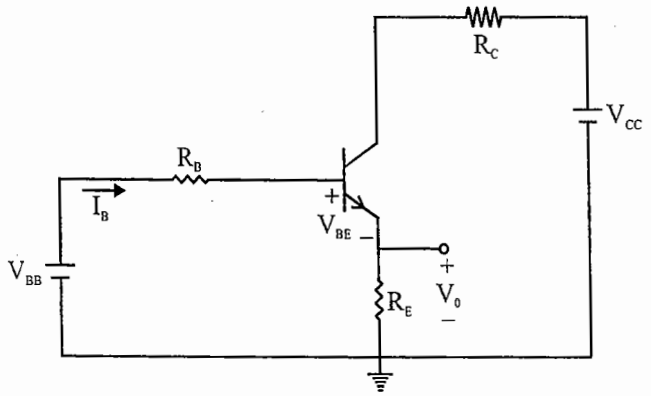
β is called the current gain of transistor in CE mode. It is the most important specification of the transistor.

β is also denoted by h_{fe} and always.

$\boxed{\beta_{dc} > \beta_{ac}}$ or $\boxed{h_{FE} > h_{fe}}$ $\boxed{I_C = \beta I_B}$

$I_E = I_C + I_B = \beta I_B + I_B$ $\boxed{I_E = (\beta+1) I_B}$

Common Collector Configuration (C-C):



(n-p-n transistor C-C configuration)

It is popularly known as "Emitter follower".

In common collector, collector resistance must be zero and output voltage is taken across the emitter resistance.

Properties:

- Highest input resistance (50kΩ to 500 kΩ)
- Lowest output resistance (<100 Ω)
- Highest current gain
- Lowest voltage gain (close to unity and ideally one)
- Output and input voltages are in phase i.e. phase shift is 0°.
- Emitter follower is basically a current controlled voltage source (CCVS).

Applications:

- As an audio frequency power amplifier
- As a buffer (impedance matching device between high resistance to low resistance)
- In designing of voltage sweep circuits.
- As an high input resistance devices.
- As a "Boot strap emitter follower".

Gamma (γ):

$$\gamma = \left|\frac{I_E}{I_B}\right| = 1+\beta \quad \boxed{\gamma = 1+\beta = \frac{1}{1-\alpha}} \quad \boxed{\alpha < \beta < \gamma}$$

Note: The output characteristics of transistor in any configuration is divided in three regions.

⇒ Saturation region, ⇒ Active region, ⇒ Cut-off region

1. **Saturation Region:**

Minimum I_B required to keep the transistor under saturation region.

$$I_{B\min} = \frac{I_C}{\beta_{dc}} \quad \text{or} \quad I_{B\min} = \frac{I_C}{h_{FE}}$$

Conditions for saturation region: $V_{CE} \le 0.2V$

$$I_C \ge I_{Cma}\alpha \;\; or \;\; I_C \ge \beta_{dc} I_B \;\; or \;\; I_C \ge h_{EF} I_B$$

Where $I_{C\max} = \frac{V_{CC}}{R_C + R_E}$, if $R_E = 0$ $\quad I_{C\max} = \frac{V_{CC}}{R_C}$

2. **Cut-off Region:** Condition for cut-off region is $V_{CE} \simeq V_{CC}$

3. **Active Region:**

Conditions for transistor under active region $0.2V < V_{CE} < V_{CC}$

$$I_C < I_{C\max} \;\; or \;\; I_C < \beta_{dc} I_B \;\; or \;\; I_C < h_{fe} I_B$$

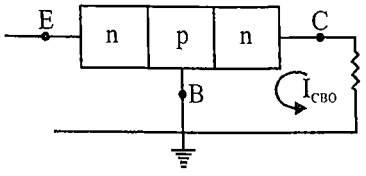
$\Rightarrow V_{CE(sat)}$ = 0.2V for Si transistor, 0V for Ge transistor

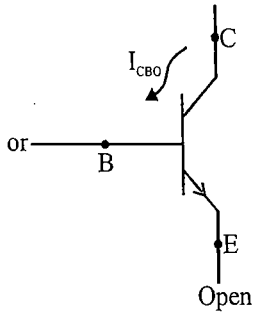
$\Rightarrow V_{BE(active)}$ = 0.2V for Ge transistor, 0.7V for Si transistor

Note: Theory says under saturation $I_C \ge I_{C\max}$ but in a practical circuit the maximum collector current is I_{Cmax} under the saturation region i.e. $I_C = I_{C\max}$

I_{CBO}:

It is the leakage current passing from collector to base with emitter open circuited, it is also called emitter cut-off current of the transistor.



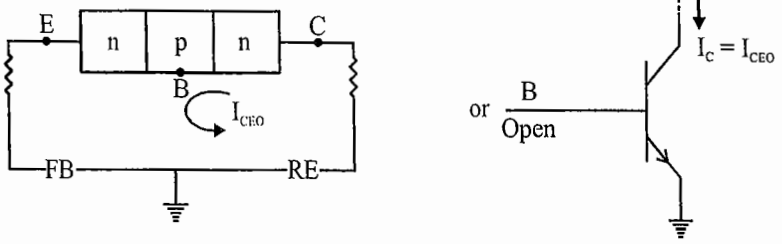


At low frequencies $I_{CBO} = I_{CO}$

At high frequencies $I_{CBO} = I_{CO}$ + Surface Current

Where surface current is due to skin effect. Skin effect appears only at high frequencies. Surface current is independent of temperature and depends upon only applied voltage. It increases with frequency.

I_{CEO}:



As $\boxed{I_C = \beta I_B + (1+\beta) I_{CO}}$

Since base is open circuited, so $I_B = 0$;

$\Rightarrow I_{CEO} = (1 + \beta)\, I_{CO}$

$\boxed{I_{CEO} = (1+\beta) I_{CO}}$ or $\boxed{I_{CEO} = \frac{I_{CBO}}{1-\alpha}}$

Note: In transistor if various leakage current are arranged in the sequence in ascending order then

$\boxed{I_{CO} < I_{CBO} < I_{CEO}}$

Power Dissipation of Transistor:

$P_T = |I_C|\, V_{CE}$ watts

In cut-off region collector current $I_C = 0$ $\boxed{P_T = 0 \text{ Watts}}$

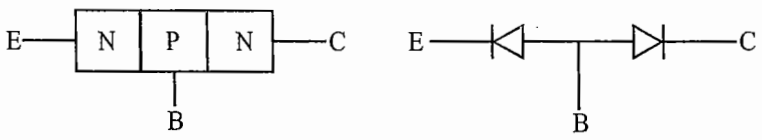
In saturation region; $I_C = I_{Cmax}$, $V_{CE} = V_{CEmin}$

So P_T is minimum

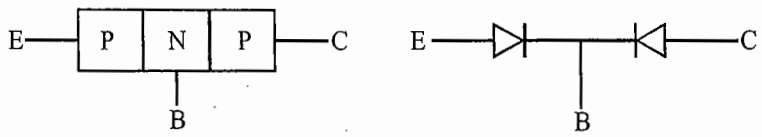
In active region; I_C = medium, V_{CE} = medium

So, maximum power consumed by the transistor when it is biased under active region.

Diode Equipment Circuit of A Transistor:



(a) NPN transistor



(a) PNP transistor

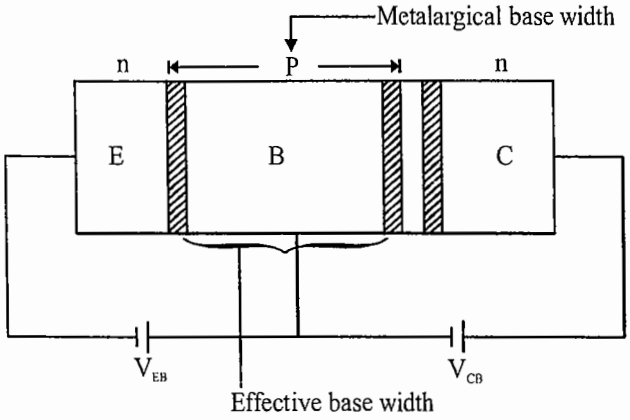
- A transistor is represented as two diodes connected back to back.
- When two diodes are connected as shown in the figure. It can not replace the BJT practically because

1. There is no crystalline continuity in between the two diodes.
2. The base width will became very large and therefore transit time will be large and hence no charge carriers will be reaching the collector.

Early Effect:

- As the voltage applied across the CB junction increases, the transition region penetrates deeper into the collector and base. Since doping in the base is ordinarily substantially smaller than that of collector, the penetration of the transition region into the base is much larger than into the collector. As a result the electrical base width of the transistor is reduced in comparison to metallurgical base width. This modulation of the effective base width by the collector voltage is known as the early effect after J.M. Early, who first interpreted it.

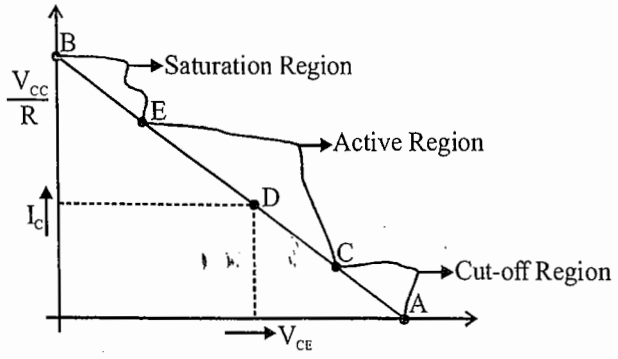
$$r_0 = \frac{V_{CE} + V_A}{I_C}$$



- The decrease in base width with increasing reverse collector voltage has three consequences.
- Their is less chance for recombination within the base region. Hence α increases with increasing $|V_{CB}|$.
- The concentration gradient of minority carriers is increased within the base, since the hole current injected across the emitter is proportional to the gradient of minority carriers at emitter junction, then I_E increases with increasing reverse collector voltage.
- For extremely large voltages, base width may be reduced to zero causing voltage breakdown in the transistor. This phenomenon is known as punch through or reach through.

Quiescent Point:

It is a point on dc load line, which represent the value of I_C and V_{CE} that exist in a transistor circuit when no input signal is applied.



It is also known as the DC operating point on working point. The best position of this point is midway between cut-off and saturation point where $V_{CE} = \frac{1}{2} V_{CC}$ life point D.

Transistor Biasing:

- The proper flow of zero signal collector current and the maintenance of proper V_{CE} during the passage of signal is known as transistor biasing.

- For faithful amplification, a transistor amplifier must satisfy three basic condition.
- Proper zero signal collector current.
- Proper V_{BE} at any instant.
- Proper V_{CE} at any instant.

Stabilization:

- The process of making operating point independent of temperature changes or variations in transistor parameter is known as stablization.

Need for Stablization:

- Temperature dependence of I_C
- Individual variations
- Thermal runway

Stability Factor

- The rate of change of collector current I_C w.r.t. the collector leakage current I_{CO} at constant B and I_B is called stability factor.

$$\boxed{S = \frac{dI_C}{dI_{CO}} \text{ at constant } I_B \text{ and } B}$$

For CE configuration $\boxed{I_C = \beta I_B + (\beta+1) I_{CO}}$

Differentiating above expressions w.r.t. I_C we get

$$1 = \beta \frac{dI_B}{dI_C} + (\beta+1)\frac{dI_{CO}}{dI_C}, \quad 1 = \beta \frac{dI_B}{dI_C} + \frac{(\beta+1)}{S} \quad \boxed{S = \frac{\beta+1}{1-\beta\frac{dI_B}{dI_C}}}$$

Procedure to derive stability factor S by any given circuit:

- Apply KVL to the input mesh of the given circuit.
- Put emitter current $I_E = I_C + I_B$ and simplify the equation.
- Find $\frac{\partial I_B}{\partial I_C}$ from the above equation and substitute in general equation of S

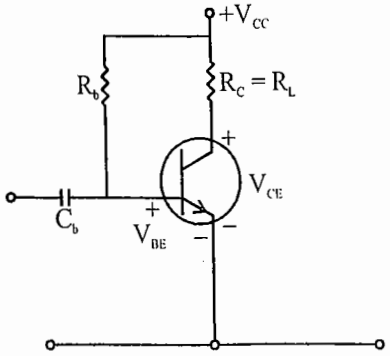
$$\boxed{S = \frac{1+\beta}{1-\beta\frac{\partial I_B}{\partial I_C}}}$$

Method of Transistor Biasing:

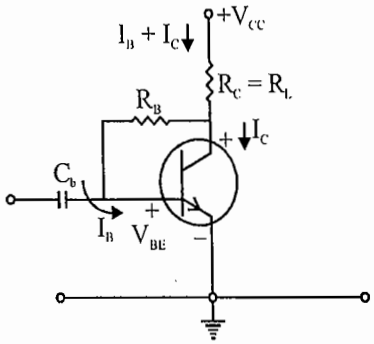
- Base resistor method (fixed bias), $S = \beta + 1$
- Biasing with feedback resistor, $S < \beta + 1$
- Voltage divided bias: $S \approx 10$

$S_{\text{fixed bias}} > S_{\text{feedback bias}} > S_{\text{self bias}}$

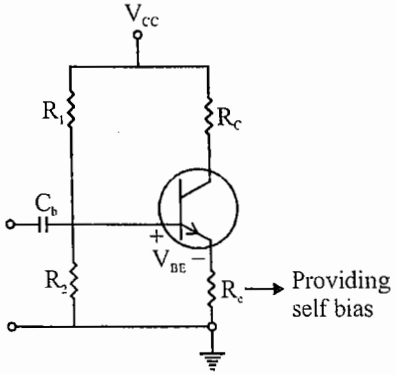
Fixed Biasing/Resistor bias:



Collector to base biasing/feedback bias:



Potential Divider or Self Biasing:



Note:

- The stability factor indicates the change in collector current I_C due to the change in collector leakage current I_{CO}.
- In order to achieve greater thermal stability. It is desirable to have as low stability factor as possible.

Steps for determining Q-Point:

- Assume BJT is in active, $V_{BE} = 0.7V$
- Apply KVL in base emitter loop.
- Determining the $I_C = I_{C(active)} = \beta I_B$
- $I_{C\,(sat)} = \dfrac{V_{CC} - V_{CE}(sat)}{R_C + R_E}$
- If $I_{C(active)} < I_{C(sat)}$

Then BJT is in active mode otherwise BJT is in saturation mode.

Comparison Table

Properties	CE	CB	CC
Voltage gain	Medium	High	less than1
Current gain	Medium	1–0.98	High
Phase shift	180°	0°	0°
Input Impedance (Zi)	Medium	Lowest	Highest
O/p Impedance (Z_0)	Medium	Highest	Lowest
Application	Because of High Power gain used as an amplifier	Used in video amplifier	Impedance matching

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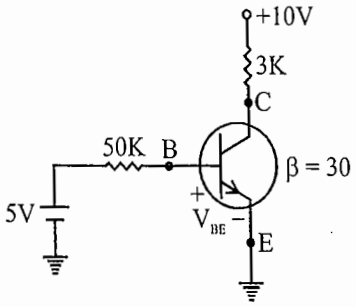
SOLVED PROBLEMS

1.



Check this transistor is in saturation or not, ($V_{BE\ sat} = 0.8V$, $V_{CE,\ sat} = 0.2V$).

Soln. Apply KVL in BE loop

$5 - 50I_B - V_{BEsat} = 0, \quad 5 - 50I_{B1} - 0.8 = 0$

$$I_{B1} = \frac{4.2}{50K} \quad \boxed{I_{B1} = 84\mu A}$$

In CE loop, $10 = I_C R_C + V_{CE\ sat}$

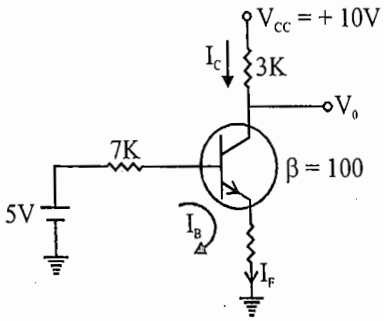
$$10 = I_C R_C + 0.2, \ I_C = \frac{10-.2}{R_C}, \ I_C = \frac{9.8}{3}\text{mA}, \ I_{B2} = \frac{I_C}{\beta} = \frac{9.8}{50\times 3}\ \text{mA}$$

For transistor is saturation or not apply $I_{B1} \geq I_{B2}$

$$\boxed{84\times 10^{-3} mA \geq \frac{9.8}{50\times 3} mA} \quad \boxed{I_{B1} \geq I_{B2}}$$

So given transistor is in the saturation region.

2.



Given, V_{BE}, active = 0.7, $V_{BE\ sat} = 0.8$, $V_{CE\ sat} = 0.2$

If the transfer is in active mode, then what is the value of I_C, V_0?

Soln. Apply KVL in BE loop

$V_{BB} = I_B R_B + V_{BE}$, active $+ (I_B + I_C) R_E$

or $5 = 7I_B + 0.7 + 0.5\ (I_B + I_C)$

$4.3 = 7.5\ I_B + 0.5\ I_C$

$4.3 = 7.5\ I_B + 0.5 \times 100 I_B$

$4.3 = 57.5\ I_B$

$$\Rightarrow I_B = \frac{4.3}{57.5} = 0.0747mA = 74\mu A \quad \Rightarrow I_C = \beta I_B = 100\times 0.747 = 7.47mA$$

Apply KVL in CE loop

$V_{CC} = I_C R_C + V_{CE} + (I_B + I_C) R_E$

V_0 means potential of collector point w.r.to ground

$$\begin{cases} V_0 = V_C + V_{CE} & \text{if } R_E = 0 \\ V_0 = V_{CC} - I_C R_C & \text{if } R_E \neq 0 \end{cases}$$

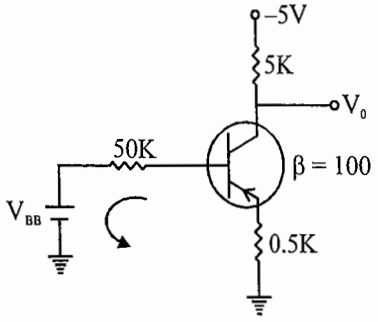
$V_{CC} = I_C R_C + V_{CE} + (I_C + I_B)R_E$ (V_i or V_0)

$\Rightarrow V_0 = V_{CC} - I_C R_C$

$= 10 - 3 \times 7.47$ mA $= 10 - 22.41 = -12.41$ volt

Negative sign indicates that transistor is not in active mode.

3.



Calculate value of V_0 if $V_{BB} = 2$ volt.

Soln. $V_{BB} = 2V$

Applying KVL in EB loop

$2 - V_{EB} - 50\ I_B - (I_B + I_C) \times 0.5 = 0$

$V_0 = -5 + 0.3 \times 5 = -5 + 1.5$ $\boxed{V_0 = -3.5V}$

$\Rightarrow 50.5\ I_B + 0.5 I_C = 1.2$ .... (1)

Apply KVL in CE loop

$5 - I_C R_C - V_{CE} - 0.5\ (I_B + I_C) = 0$

$\Rightarrow 5.5\ I_C + 0.5\ I_B = 4.8$ .... (2)

Solving equation (1) and (2), we get

$I_B = 0.015$ mA; $I_C = 0.87$ mA

We have $I_B = I_B = 0.015$mA

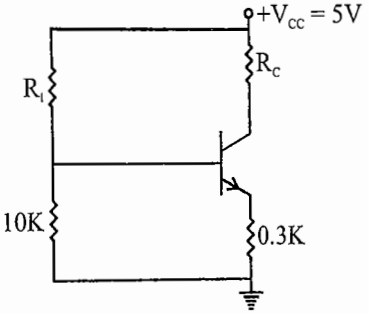
Also, $I_{B2} = \dfrac{I_C}{\beta} = \dfrac{0.87}{100} = 0.0087mA \Rightarrow \boxed{I_{B1} > I_{B2}}$

Therefore transfer is in saturation mode:

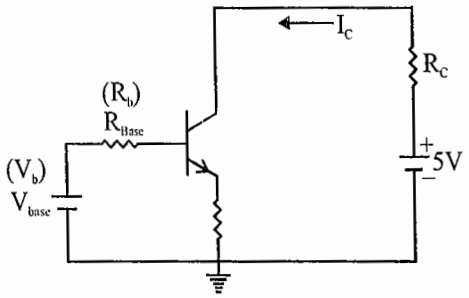
Now, $V_0 + 5 = I_C R_C$

$\Rightarrow V_0 = 0.87 \times 5 - 5 = 4.35 - 5 = -0.65$ volt

4. The BJT amplifier of figure below has $h_{fe} = 100$ $V_{BE} = 0.7V$, $I_{CO} = 0$. Calculate the values of R_1 and R_C such that its $I_C = 1$mA and $V_{CE} = 2.5$ V.



Soln. Thevenin equivalent of base ground terminal



$$V_{base} = \frac{5}{R_1+10}\times 10 = \frac{V_{CC}}{R_1+R_2}.R_2 \quad \text{and} \quad R_{base} = \frac{10R_1}{10+R_1}k\Omega = \frac{R_1R_2}{R_1+R_2}$$

Let us consider BJT is in active region by applying KVL around the base-emitter loop, then we get,

$V_b - I_B R_b - V_{BE} - (I_B + I_C)0.3 = 0.$

$$\frac{50}{R_1+10} - I_B \times \left(\frac{10R_1}{10+R_1}\right) - 0.7 = I_B(101)\times 0.3 \quad I_b = \frac{I_C}{\beta} = \frac{1}{100} \quad (\because I_C = \beta I_B)$$

$$\frac{50}{R_1+10} - \left(\frac{R_1\times 10}{10+R_1}\right)\times\frac{1}{100} - 0.7 = \frac{1}{100}(101)\times 0.3$$

$$\therefore 500 - R_1 = \left[0.7 + 1\left(\frac{101}{100}\right)0.3\right]\times 10(R_1+10)$$

$\therefore$ $500 - R_1 = 10R_1 + 100$

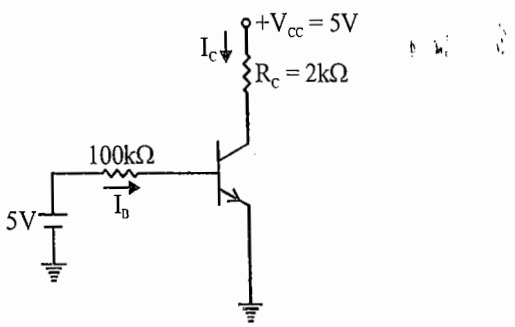
$11R_1 = 400$ $\boxed{R_1 = 36.36k\Omega}$

Applying KVL in collector emitter loop

$5 - I_C R_C - V_{CE} - (I_B + I_C)0.3 = 0$

$$R_C = \frac{5-2.5-0.303}{1} \quad \boxed{R_C = 2.194k\Omega}$$

5. Find out Q-point (V_{CC}, I_C) where, $\beta = 100$



Soln. **Step-I:** Assuming BJT is in active mode $V_{BE} = 0.7V$, for Si.

Step-II: Applying KVL in base emitter loop

$5 - I_B \times 100 \times 10^3 - V_{BE} = 0$, $I_B = 4.3 \times 10^{-5}$

Step-III: $I_{C\,(active)} = \beta I_B = 4.3 \times 10^{-5} \times 100 = 4.3mA$

Step-IV: Applying KVL in collector emitter loop for $I_{C\,(saturation)}$

$V_{CC} - 2 \times 10^3 I_C - V_{CE} = 0$

$V_{CE} = 0.2V$, this is the typically value in saturation mode for Si,

$\therefore\ 5 - 0.2 = 2 \times 10^3 I_C$

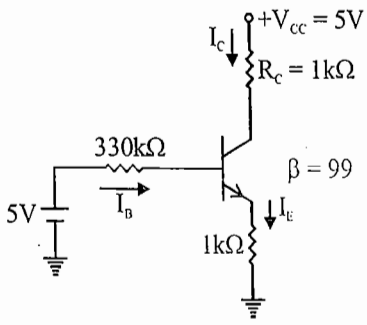
$I_{C\,(saturation)} = 2.4\ mA$

Step-V: $I_{C\,(active)} > I_{C\,(saturation)}$

BJT is in saturation region

Q-point $[I_{C(saturation)} = 2.4\ mA,\ V_{CE\,(sat)} = 0.2V]$.

6. Find out Q-point?



Soln. **Step-I:** Assume BJT is in active mode $V_{BE} = 0.7$ volt

Step-II: Apply KVL in base-emitter loop

$5 - 330 \times 10^3 I_B - 0.7 - 1 \times 10^3 I_E = 0$

$4.3 = 330 \times 10^3 I_B + 1 \times 10^3 (I_B + I_C)$

$4.3 = I_B (330 \times 10^3 + 100 \times 10^3)$ $\boxed{(I_C = \beta I_B)(I_C = 99 I_B)}$

$I_B = 10\,\mu A$

Step-III: $I_{C(active)} = \beta I_B = 99 \times 10 \times 10^{-6} = 0.99mA$

Step-IV: Apply KVL in collector emitter loop for $I_{C(saturation)}$

$5 - I_C \times 10^3 - V_{CE\,(sat)} - I_E \times 10^3 = 0$

$5 - 0.2 = I_C \times 10^3 + (I_B + I_C) \times 10^3$

$4.8 = I_C (2 \times 10^3)$

$I_{C\,(sat)} = 2.4\ mA$

Step-V : $I_{C(active)} < I_{C(saturation)}$

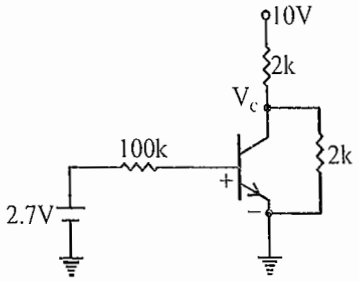
BJT is in active mode

Step-VI: $V_{CE} = V_{CC} - I_C (R_C + R_E)$

$= 5 - 0.99 \times 10^{-3} (2 \times 10^3)$

$= 5 - 1.98 = 3.02$

Q-point = $(I_{C(active)} = 0.99mA,\ V_{CE\,(active)} = 3.02)$

7. 

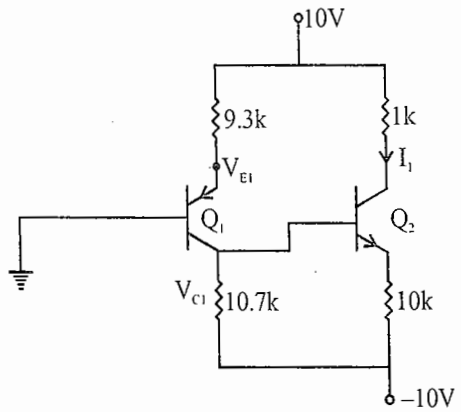
Find the collector voltage V_C if $\beta = 100$.

Soln. Assuming the transistor in active mode, KVL for the base circuit gives

$$I_B = \frac{2.7-0.7}{100} = 0.02\text{mA}, \quad I_C = \beta I_B = 2\text{mA}$$

KCL at the collector node yields $\frac{V_C - 10}{2} + \frac{V_C}{2} + I_C = 0$

Combining the last two equations, and solving for V_C yields $\boxed{V_C = 3V}$

8. 

In the circuit shown, assume that the transistor have very large β values, so that the base current can be assumed negligible (in active region). Find the current I_1.

Soln. We assume both transition to be in the active mode. Writing KVL for the base circuit of Q_1 yields.

$-10 + 9.3\ I_{E1} + 0.7 = 0 \Rightarrow I_{E1} = 1\text{mA}$

Since $I_{B1} \simeq 0$, $I_{C1} \approx I_{E1}$,

Hence $V_{C1} = (10.7)\ I_{E1} - I_0 = 10.7 - 10 = 0.7$

V_{C1} positive indicates that Q_1 is in active region,

Now, KVL for the base circuit of Q_2 yields

$-V_{C1} + V_{BE2} + (10)I_{E2} - 10 = 0$

$-0.7 + 0.7 + (10)\ I_{E2} - 10 = 0$

$I_{E2} = 1\text{mA} \simeq I_{C2} = I_1$

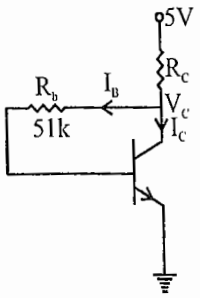
$V_{C2} = 10 - (1\text{k})\ (1\text{mA})$

$V_{C2} = 9\text{V}$

So that $V_{CB2} = 9 - 0.7 = 8.3$ V

Since V_{CB2} is positive, Q_2 is in the active region. Therefore I_1 is 1mA.

9.



Determine the value of R_C needed if $V_C = 2V$. Use $\beta = 50$ for the transistor.

Soln. Writing a KVL in the collector base loop yields

$-5 + R_C (I_B + I_C) + R_b I_B + 0.7 = 0$

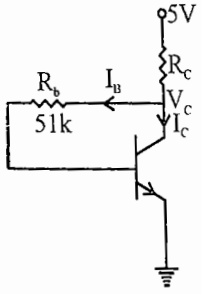
$I_C = \beta I_B$ (the transistor is in active mode because $V_{CE} = V_C = 2V$)

$$I_B = \frac{4.3}{51R_C + R_b} = \frac{4.3}{51R_C + 51} = \frac{4.3}{51(R_C + 1)}$$

Now, $V_C = 5 - R_C (I_C + I_B) = 5 - (R_C)51\ I_B$ $\boxed{V_C = 2V}$

$$V_C = 2 = 5 - R_C \frac{4.3}{(R_C + 1)} \quad \boxed{R_C = 2.3k\Omega}$$

10.



Find stability factor S'' of the given circuit: Where $\boxed{S'' = \frac{\partial I_C}{\partial \beta}}$

Soln. Apply KVL in (C–B) lop:

$-5 + R_C(I_B + I_C) + R_b I_B + 0.7 = 0$

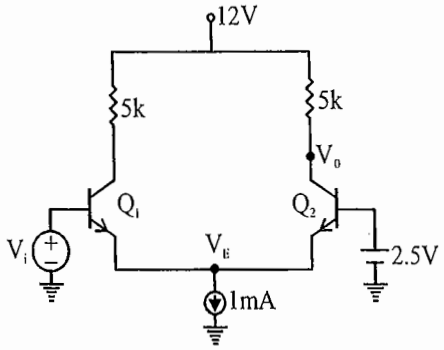
$I_B = I_C/B$ (assuming active mode)

$$R_C I_C \left(\frac{1}{\beta} + 1\right) + R_b \frac{I_C}{\beta} = 4.3$$

$$I_C = \frac{4.3\beta}{R_C(1+\beta) + R_b} = \frac{4.3\beta}{2.3(1+\beta) + 51} = \frac{4.3\beta}{53.3 + 2.3\beta}$$

$$S'' = \frac{\partial I_C}{\partial \beta} = \frac{4.3(53.3 + 2.3\beta) - 4.3\beta \times 2.3}{(53.3 + 2.3\beta)^2}$$

With $\beta = 50$, we obtained $S'' = 0.008$

11. 

(Differential amplifier)

The silicon transistor have $\beta = 100$

Find V_0 if (i) $V_i = 5V$ (ii) $V_i = 0V$

Soln. (a) The circuit is called a differential amplifier. Let us assume Q_2 to be off and Q_1 in the active mode, based on the voltage given

$I_{E1} = 1nA$, $I_{C1} = \beta I_{E1}/(1+\beta) = 0.99nA$

and $V_{CB1} = 12 - (5k)(0.99nA) - 5 = 2.05V$

Since V_{CBI} is positive, Q_1 is in active mode. Assuming $V_{BE1} = 0.7V$, $V_E = 5 - 0.7 = 4.3$ V,

which means that $V_{BE2} = 2.5 - 4.3 = -1.8V$

Since V_{BE2} is negative, our assumption of Q_2 being off is confirmed. As no current flows through Q_2

$\boxed{V_0 = 12V}$

(b) Let us assume Q_1 to be off and Q_2 in active mode

$I_{E2} = 1nA$, $I_{C2} = 0.99nA$

$V_{CB2} = 12 - (5k)(0.99nA) - 2.5 = 4.55$ V

which confirmed that Q_2 is in active mode.

$V_E = 2.5 - 0.7 = 1.8V$

$V_{BE\,1} = 0 - 1.8 = -1.8V$

Hence Q_1 is off and finally $V_0 = 12 - (5k)(0.99\ nA)$

$\boxed{V_0 = 7.05V}$

12. A power amplifier gives 150W output for an input of 1.5W. The gain, in dB, is **[GATE 2007]**

(a) 10 (b) 20 (c) 54 (d) 100

Soln. $P_{in} = 1.5w$, $P_{out} = 150\ w$

Therefore, $\text{gain} = 10\log\frac{P_{out}}{P_{in}} = 10\log\frac{150}{1.5} = 10\log 100 = 20\ dB$

13. In a typical *npn* transistor the doping concentrations in emitter, base and collector regions are C_E, C_B and C_C respectively. These satisfy the relation **[GATE 2007]**

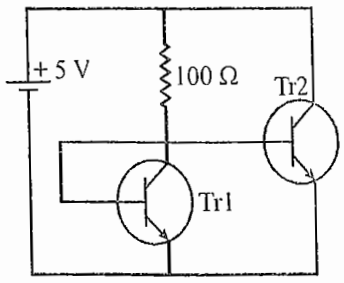
(a) $C_E > C_C > C_B$ (b) $C_E > C_B > C_C$

(c) $C_C > C_B > C_E$ (d) $C_E = C_C > C_B$

Soln. $C_E > C_C > C_B$

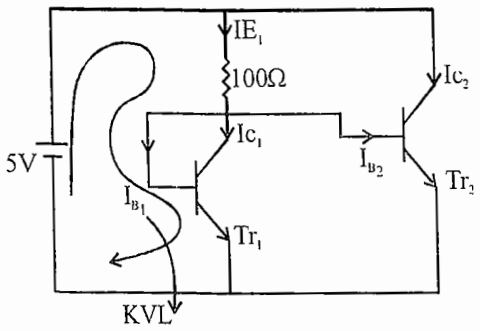
Correct option is (a)

14. In the following circuit, Tr1 and Tr2 are identical transistors having $V_{BE} = 0.7$ V. The current passing through the transistor Tr2 is **[GATE 2011]**



(a) 57 mA (b) 50 mA (c) 48 mA (d) 43 mA

Soln. Given, Tr_1 & Tr_2 are identical $V_{be} = 0.7V$



$\because$ β of BJT not given so we can neglect I_B

$\Rightarrow$ applying KVL is shown in figure

$5 = I_{E_1} \times 100 + 0.7$

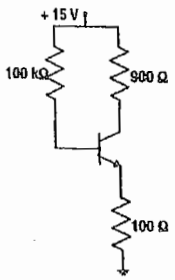
$4.3 = I_{E_1} \times 100$

$I_{E_1} = 43$ mA

$\boxed{I_{E_1} = I_{C_2}}$ identical *npn* transistor

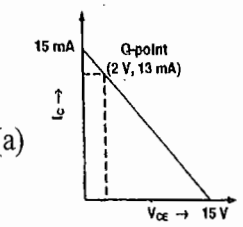
Correct option is (d)

15. Consider the following circuit in which the current gain β_{dc} of the transistor is 100.

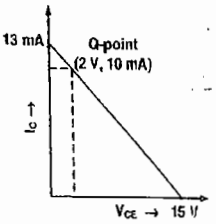


Which one of the following correctly represents the load line (collector current I_c with respect to collector-emitter voltage V_{CE}) and Q-point of this circuit? **[GATE 2012]**

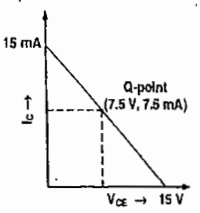
(a)



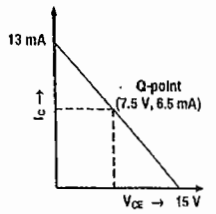
(b)



(c)



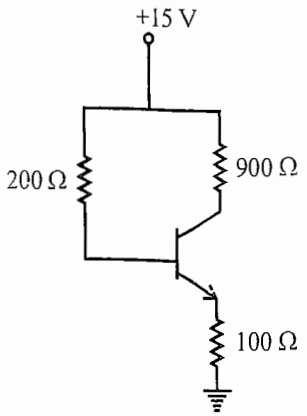
(d)



Soln. Applying KVL around the bias-emitter loop.

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E$$

$$I_C = \beta I_\beta \qquad I_E = I_\beta + I_C = (1+\beta) I_\beta$$



$$\therefore \qquad I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_E} = \frac{15 - 0.7}{100 \times 10^3 + 101 \times 100} = 0.129\ mA \simeq 0.13 mA$$

$$\therefore \qquad I_C = \beta \times I_\beta \simeq 13\ mA$$

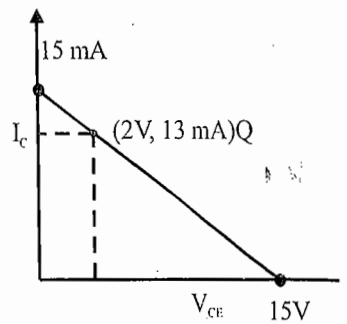
Now, applying KVL in collector circuit

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$\Rightarrow \qquad V_{CC} = V_{CE} + I_C (R_C + R_E)$$

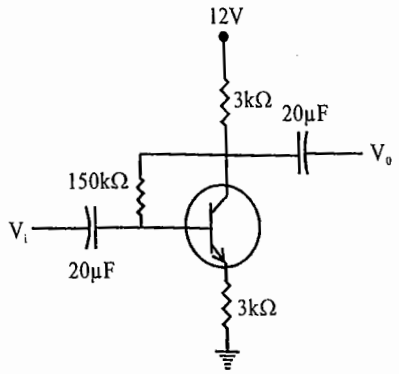
$$\Rightarrow \qquad V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$$\Rightarrow \qquad V_{CE} = 15 - I_C \times 1000 = 15 - 13 = 2 \text{ volt}$$



Correct option is (a)

16. The current gain of the transistor in the following circuit is $\beta_{dc} = 100$. The value of collector current I_C is _____ mA. **[GATE 2014]**



Soln. We can write from the figure,

$$V_{CC} = \left(I_\beta + I_C\right)R_C + V_{CE} + I_E R_E$$

$$\beta\alpha = \frac{\beta}{1+\beta} = \frac{100}{101}$$

$$\Rightarrow \quad V_{CC} = I_\beta\left(1+\beta\right)R_C + V_{CE} + \left(I_C + I_\beta\right)R_E$$

And $\quad V_{CE} = I_B R_B + V_{BE}$

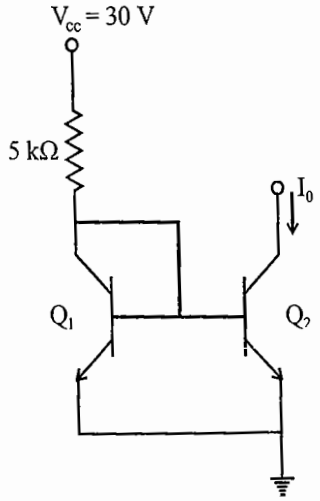
$$\therefore \quad V_{CC} = I_B\left(1+\beta\right)\left(R_C + R_E\right) + I_B R_B + V_{BE}$$

$$\Rightarrow \quad I_\beta = \frac{V_{CC} - V_{BE}}{\left(1+\beta\right)\left(R_C + R_E\right) + R_B} = \frac{12 - 0.7}{101\times(6) + 150} \simeq 0.014\ mA$$

$$\therefore \quad I_C = \beta I_\beta = 0.14\times 100 = 1.4\ mA$$

Correct answer is (1.4) mA

17. In the simple current source shown in the figure, Q_1 and Q_2 are identical transistors with current gain $\beta = 100$ and $V_{BE} = 0.7\,V$ **[GATE 2015]**



The current I_0 (in mA) is _____ (upto two decimal places)

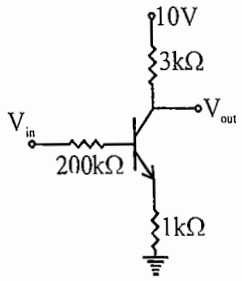
Soln. Let current I_{C_1} in transistor Q1

$$\therefore \quad I_{C_1} = \frac{30 - V_{BE}}{R_C} = \frac{30 - 0.7}{5} = 5.86\ mA$$

According mirror image problem same current will pass through the second transistor

Correct answer is (5.86) mA.

18. For the transistor shown in the figure, assume $V_{BE} = 0.7$V and $\beta_{dc} = 100$. If $V_{in} = 5$V, V_{out} (in Volts) is _____. (Give your answer upto one decimal place).



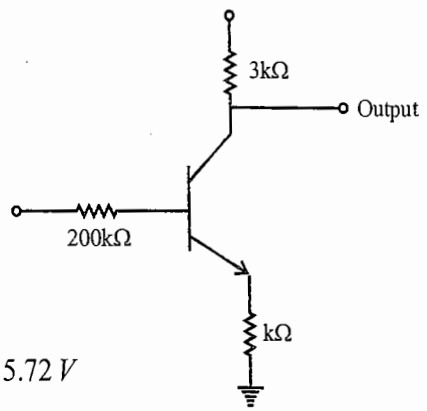
Soln. From input loop we can write

$$5 = I_B R_B + V_{BE} + I_E R_E$$

$$4.3 = \frac{I_C}{100} \times 200 \times 10^3 + \frac{I_C \times 101}{100} \times 10^3$$

$$\Rightarrow \quad I_C = \frac{4.3}{3.01} \times 10^{-3}$$

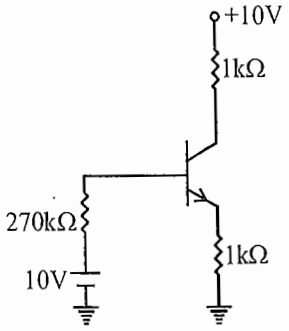
$$\therefore \quad V0 = V_{CC} - I_C R_C = 10 - \frac{4.3}{3.01} \times 3 = (10 - 4.28)V = 5.72\ V$$



Correct answer is (5.72) V

PRACTICE SET

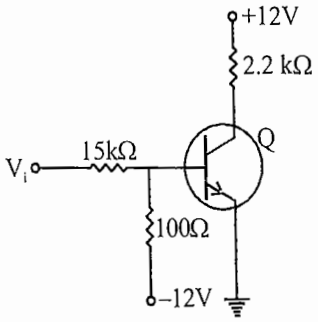
1. The common emitter forward current gain of the transistor shown is $B_F = 100$.



The transistor is operated in

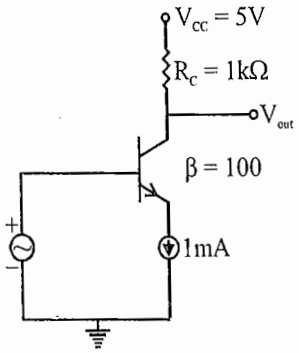
(a) Saturation region
(b) Cutoff region
(c) Reverse active region
(d) Forward active region

2. Consider the circuit shown in figure. If the β of the transistor is 30 and I_{CBO} is 20nA and the input voltage is +5V, the transistor would be operated in



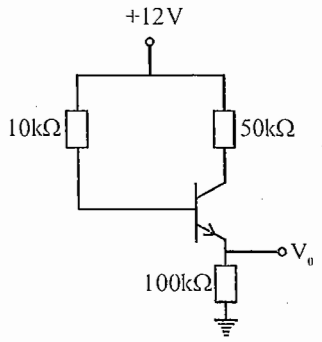
(a) Saturation region
(b) Cut off region
(c) Active region
(d) Break down region

3. The common emitter amplifier shown in the figure is biased using a 1nA ideal current source. The approximate base current value.



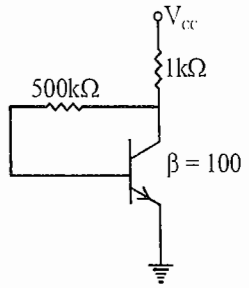
(a) 0μA
(b) 10μA
(c) 100μA
(d) 1000μA

4. Transistor circuit shown uses a silicon transistor with $V_{BE} = 0.7V$, $I_C \approx I_E$ and a dc current gain of 100. The value of V_0 is



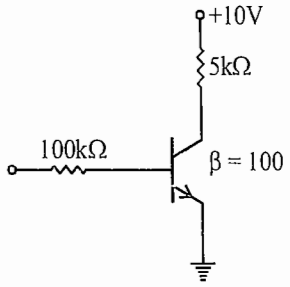
(a) 4.65V (b) 5V (c) 6.3V (d) 7.23V

5. Calculate the stablization factor for the below circuit.



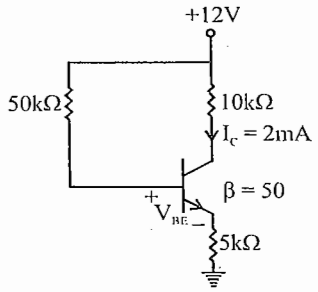
(a) 48 (b) 84 (c) 24 (d) N.O.T.

6. If the transistor shown below is operating at saturation region, then the base current will be



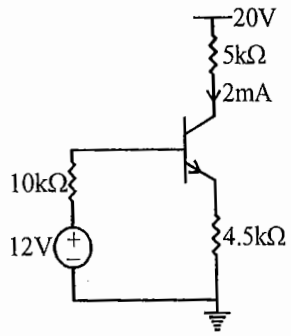
(a) $I_B = 20\mu A$ (b) $I_B > 20\mu A$ (c) $I_B = 20mA$ (d) $I_B > 20mA$

7. Calculate V_{BE} in the circuit shown below



(a) 0V (b) 1V (c) –0.8V (d) –0.2V

8. Calculate the current gain (β) in the circuit given below (Give $V_{BE} = 1V$).



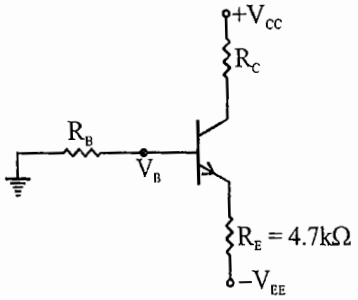
(a) 20 (b) 14.5 (c) 49 (d) 30

9. Input and output resistance respectively are low for which of the following amplifier

(a) Common base and common collector (b) Common collector and common base

(c) Common base and common emitter (d) Common emitter and common collector

10. Find base voltage V_B with respect to ground given ($I_E = 1.8mA$, $V_{EE} = -10V$, $V_{CC} = 10V$)

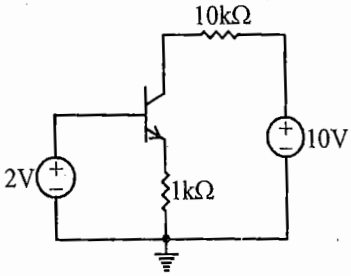


(a) 10.7V (b) 8.2V (c) 9.3V (d) N.O.T.

11. The DC current gain (β) of a BJT is 50, assuming that the emitter injection efficiency is 0.995, the base transport factor is

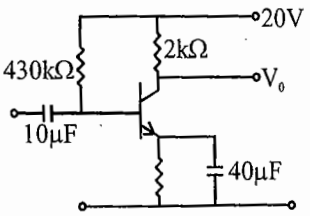
(a) 0.980 (b) 0.985 (c) 0.990 (d) 0.995

12. For the BJT circuit shown, assume that the β of the transistor is very large and $V_{BE} = 0.7$. The mode of operation of the BJT is



(a) Cut-off (b) Saturation (c) Normal active (d) Reverse active

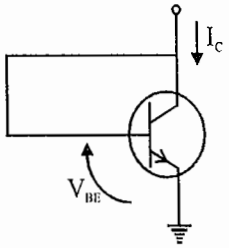
13. The circuit using a BJT with $\beta = 50$ and $V_{BE} = 0.7V$ is shown in the figure. The base current I_B and collector voltage V_C are respectively.



(a) 43 μA and 11.4 V (b) 40 μA and 16 volts

(c) 45 μA and 11V (d) 50 μA and 10V

14. For an n-p-n transistor connected as shown in figure, $V_{BE} = 0.7V$. Given that reverse saturation current of the junction at room temperature 300°K is 10^{-13} A, the emitter current is



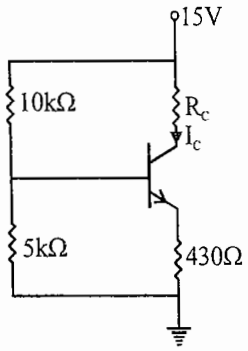
(a) 30 mA (b) 39 mA (c) 49 mA (d) 20 mA

15. Generally, the gain of a transistor amplifier falls at high frequencies due to the

(a) Internal capacitance of the device (b) Coupling capacitor at the input

(c) Skin effect (d) Coupling capacitor at the output

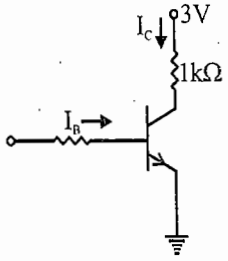
16. In the circuit of the figure, assume that the transistor is in the active region. It has a large β and its base emitter voltage is 0.7V. The value of I_C is



(a) Indeterminate since R_C is not given (b) 1 nA

(c) 5 nA (d) 10 nA

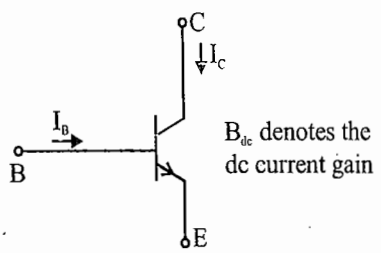
17. Assuming $V_{CE(sat)} = 0.2$ V and B = 50, the minimum base current (I_B) required to drive the transistor in the figure to saturation is



(a) 56 μA (b) 140 μA (c) 60 μA (d) 3 μA

18. If the transistor in the figure is in the saturation region then

$$I_{B_{min}} \leq \frac{I_C}{\beta}$$



(a) I_C is always equal to $\beta_{dc} I_B$ (b) I_C is always equal to $-\beta_{dc} I_B$

(c) I_C is greater than or equal to $\beta_{dc} I_B$ (d) I_C is less than or equal to $\beta_{dc} I_B$

19. The early effect in a bipolar junction transistor is caused by
(a) fast turn-on
(b) fast turn off
(c) large collector base reverse bias
(d) large emitter base forward bias

20. Thermal runway in junction transistor will take place if the quiescent point is such that
(a) $V_{CE} > \frac{1}{2} V_{CC}$
(b) $V_{CE} \leq V_{CC}$
(c) $V_{CE} \geq 2V_{CC}$
(d) $V_{CE} < \frac{1}{2} V_{CC}$

21. Early effect in BJT refers to
(a) a valance breakdown
(b) thermal runway
(c) base narrowing
(d) Zener breakdown

22. Which one of the following statements is correct? in a transistor
(a) I_{CBO} is greater than I_{CEO} and does not depend upon temperature.
(b) I_{CBO} is greater than I_{CO} and doubles for every ten degrees rise in temperature
(c) I_{CBO} is equal to I_{CO} and double for every ten degrees rise in temperature
(d) I_{CEO} is equal to I_{CO} and doubles for every ten degrees rise in temperature

23. What is the reverse recovery time for a diode when switched from forward bias V_F to reverse bias V_R?
(a) Time taken to remove the stored minority carriers
(b) Time taken by the diode voltage to attain zero value
(c) Time to remove stored minority carriers plus the time to bring the diode voltage to reverse bias V_R
(d) Time taken by the diode current to reverse

24. The operation of BJT is based upon the flow of current due to which one of the following?
(a) Donor and acceptor ions
(b) Electrons only
(c) Holes only
(d) Both electrons and holes

25. Consider the following statements: specific features of BJT are
1. Very small on-state resistance
2. Presence of second breakdown
3. Infinite input resistance
4. Good performance in parallel operation

Which of these statements are correct?
(a) 1, 2, 3 and 4 (b) 1, 2 and 3 (c) 3 and 4 (d) 1 and 2

26. The breakdown voltage of a transistor with its base open is BV_{CEO} and that with emitter open is BV_{CBO} then
(a) $BV_{CEO} = BV_{CBO}$
(b) $BV_{CEO} > BV_{CBO}$
(c) $BV_{CEO} < BV_{CBO}$
(d) BV_{CEO} is not related to BV_{CBO}

ANSWER KEY

1. (d)	2. (c)	3. (b)	4. (a)	5. (b)
6. (b)	7. (d)	8. (b)	9. (a)	10. (d)
11. (b)	12. (b)	13. (b)	14. (c)	15. (a)
16. (d)	17. (a)	18. (c)	19. (c)	20. (a)
21. (c)	22. (c)	23. (a)	24. (d)	25. (d)
26. (c)				

Chapter 4

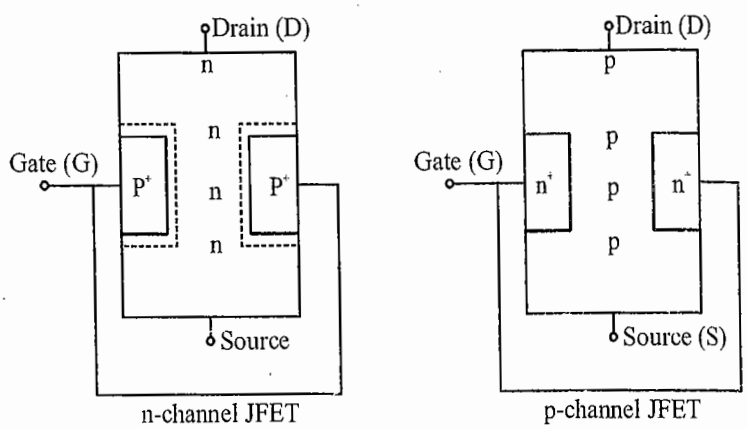
Field Effect Transistors (FET)

- It is voltage controlled device.
- It is a unipolar device.
- It is a majority carrier device.
- Leakage current almost $\simeq$ 0 since no minority carrier.
- Excellent thermal stability since no minority carrier.
- Less noise.
- FET can be designed without self bias circuit.
- It is fabricated with Si only.
- Offset voltages are zero.
- High input resistance device ($\geq M\Omega$)
- Large B.W. Device
- GAIN B.W. product almost constant
- Smaller in size than BJT.

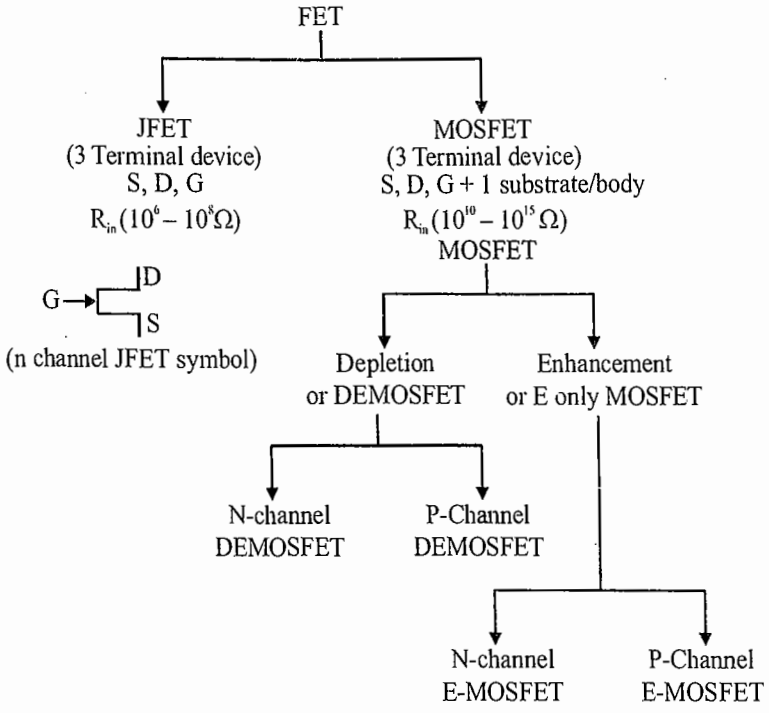
Disadvantages of FET:

(1) Smaller gain (2) Smaller gain band width product.

Construction: Three terminals are present and one channel is also present. GATE, DRAIN and SOURCE are three terminals channel may be *n*-channel or *p*-channel.

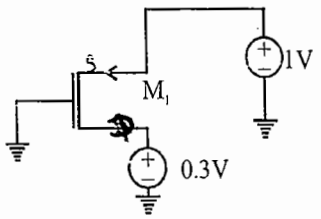


Classification of FET:



Problems of FET:

1. In the given circuit of figure if $V_{TH} = 0.4V$, the transistor M_1 is operating in



(a) Linear region
(b) Saturation region
(c) M_1 is Off
(d) Cannot be determined

Soln. For P-channel MOSFET

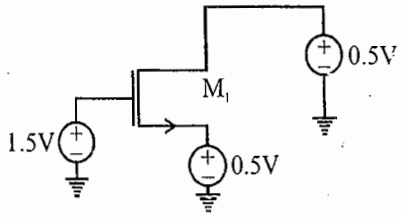
$V_{SD(sat)} = V_{SG} + V_{TH} = (1 - 0) - 0.4 = 0.6$

$V_{SD} = V_S - V_D = (1 - 0.3) = 0.7$, Here $V_{SD} > V_{SD\ (Sat)}$

So, M_1 is in saturation region.

Correct option is (b)

2. In the following circuit of figure, the region of operation of M_1 is ($V_{TH} = 0.4V$).



(a) Linear
(b) Saturation
(c) M_1 is Off
(d) Cannot be determined

Soln. In the circuit,

$V_{GS} = V_G - V_S = 1.5 - 0.5 = 1V$, $V_{DS} = V_D - V_S = 0.5 - 0.5 = 0V$

$V_{DS\,(sat)} = V_{GS} - V_{TH} = 1 - 0.4 = 0.6V$

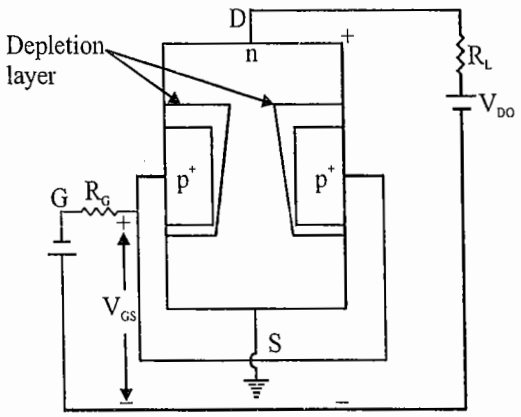
here, $V_{DS} < V_{DS(sat)}$ and $V_{GS} > V_{TH}$

So, M_1 is in linear (triode) region.

Correct option is (a).

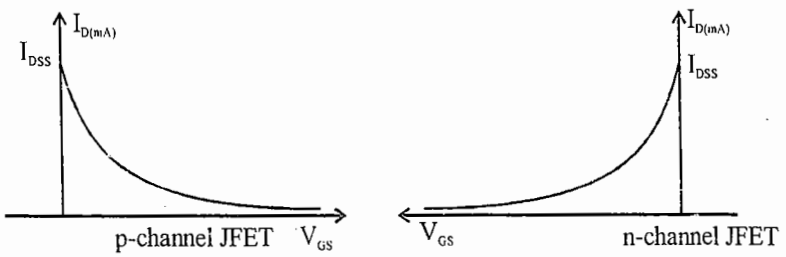
N-Channel JFET: It is unbiased JFET, channel cross sectional area is maximum and channel current density is minimum.

JFET Baising:



In a n-channel JFET depletion layer is more penetrated into the channel near drain for n-channel JFET. Gate voltage is (–) ve.

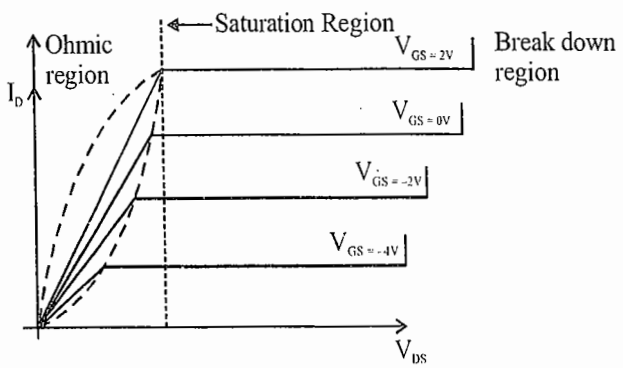
Transfer Characteristic:



Minimum gate to source voltage V_{GS} required to cut off the channel is called as V_{GS} eff.

Drain Characteristic:

Pinch off Voltage:



Drain characteristics I_D Vs. V_{DS} / V_{GS} cont.

Parameters of JFET:

1. Gate to source voltage, $I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_p}\right]^2 \Rightarrow \boxed{V_{GS} = V_p\left[1-\sqrt{\frac{I_D}{I_{DSS}}}\right]}$

2. Transconductance $\{g_m\}$, $I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_p}\right]^2$ $\boxed{g_m = \frac{\partial I_D}{\partial V_{GS}} = -\frac{2I_{DSS}}{v_p}\left[1-\frac{V_{GS}}{V_P}\right]}$

$$g_m = g_{m_0}\left[1-\frac{V_{GS}}{V_P}\right];\ g_{m_0} = \left[\frac{2I_{DSS}}{V_P}\right]$$

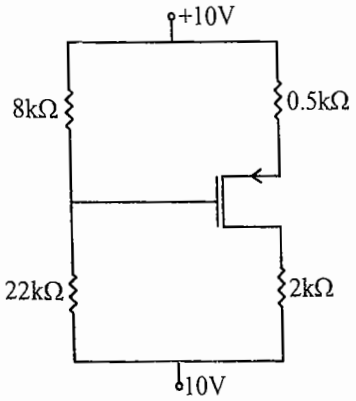
3. Amplification factor (μ), $\mu = \left.\frac{\Delta V_{DS}}{\Delta V_{GS}}\right|_{I_{D const}}$; $\boxed{\mu = g_m \times r_d}$

range of μ = 2.5 to 150

4. Drain resistance $(Rd) = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS const}}$; typical value = 500 kΩ

SOLVED PROBLEMS

1. In the circuit of shown below the transistor parameter are as follow:
$V_{TP} = -2V$, $K_P = 1mA/V^2$



(i) The value of V_{SG} is

(a) –3.77V (b) 3.77 V (c) –1.77V (d) 1.77

Soln. $R_i = 8k\Omega$, $R_L = 22k\Omega$, $R_S = 0.5k\Omega$, $R_D = 2k\Omega$.

$$V_G = \left(\frac{R_2}{R_1+R_2}\right)(20-10) = \frac{22}{(8+22)}(20-10) = 4.67V$$

Assume transistor in saturation

$$I_D = \frac{10-V_S}{R_S} = Kp(V_{SG}+V_{TP})^2,\ V_S = V_G + V_{SG}$$

$10 - (4.67 + V_{SG}) = (0.5)\ (1)\ (V_{GS})$

$\Rightarrow V_{SG} = 3.77V, -1.77V$

V_{SG} is positive voltage.

Correct option is (b)

2. The value of I_D is

(a) 3.12 mA (b) 18.2 mA (c) 7.12 mA (d) 14.2 mA

Soln. $I_D = \dfrac{10 - V_S}{R_S} = \dfrac{10 - (V_G + V_{GS})}{R_S} = \dfrac{10 - (4.67 + 3.77)}{0.5} = 3.12\text{mA}$

Correct option is (a)

3. The value of V_{SD} is

(a) 15.5V (b) 2.2V (c) 12.2V (d) 5.5V

Soln. $10 = I_D(R_S + R_D) + V_{SD} - 10$

$V_{SD} = 20 - I_D(R_S + R_D) = 20 - 2.12\ (2 + 0.5) = 12.2\ \text{V}$

Correct option is (c)

4. The following reading were obtained experimentally from a JFET:

V_{GS}	0V	0V	–0.2V
V_{DS}	7V	15V	15V
I_D	10mA	10.25mA	9.65mA

Determine (i) a.c. drain resistance (ii) transconductance and (iii) amplification factor.

Soln. (i) With V_{GS} constantly at 0V, the increase in V_{DS} from 7V to 15V increases the drain current from 10mA to 10.25 mA i.e.

Change in drain-source voltage, $\Delta V_{DS} = 15 - 7 = 8\text{V}$.

Change in drain current, $\Delta I_D = 10.25 - 10 = 0.25\text{mA}$

$\therefore$ a.c. drain resistance $r_d = \dfrac{\Delta V_{DS}}{\Delta I_D} = \dfrac{8V}{0.25\text{mA}} = 32\text{k}\Omega$

(ii) With V_{DS} constant at 15V, drain current changes from 10.25mA to 9.65mA as V_{GS} is changed from 0V to –0.2V.

$\Delta V_{GS} = 0.2 - 0 = 0.2\text{V},\ \Delta I_D = 10.25 - 9.65 = 0.6\text{mA}$

$\therefore$ Transconductance, $g_m = \dfrac{\Delta I_D}{\Delta V_{GS}} = \dfrac{0.6mA}{0.2V} = 3\text{mA/V} = 3000\ \mu\text{mho}$

(iii) Amplification factor: $\mu = g_m \times r_d = (32 \times 10^3) \times (3000 \times 10^{-6}) = 96$

JFET Biasing: For the proper operation of n-channel JFET, gate must be negative w.r.t. source. This can be achieved either by inserting a battery in the gate circuit or by a circuit known as biasing circuit. The latter method is preferred because batteries are cost by and required frequent replacement.

(i) Self bias: Fig. (A) shows the self bias method. The resistor R_S is the bias resister. The d.c. component of drain current flowing through R_S produces the desired bias voltage. The capacitor C_S by passes the a.c. component of the drain current.

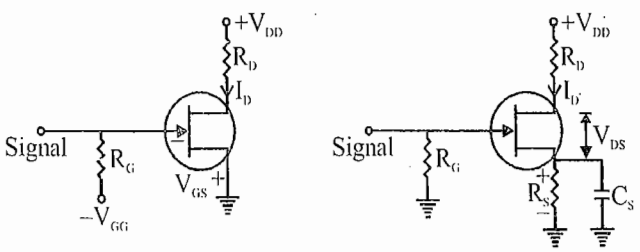


Fig. (A)

Voltage across R_S, $\boxed{V_S = I_D R_S}$

Since gate current is negligibly small, the gate terminals is at d.c. ground i.e. $V_G = 0$

$V_{GS} = V_G - V_S = 0 - I_D R_S$; $V_{GS} = -I_D R_S$

Operating Point: The operating point (i.e. zero signal I_D and V_{DS}) can be easily determined. Since the parameters of the JFET are usually known, zero signal I_D can be calculated from the following relation.

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$. Also $V_{DS} = V_{DD} - I_D(R_D + R_S)$

Thus d.c. conditions of JFET amplifier are fully specified.

(ii) Voltage Divider Method: Fig. (b) shows potential divider method of biasing a JFET. This circuit is identical to that used of a transistor. The transistor R_1 and R_2 for ma voltage divider across drain supply V_{DD}. The voltage V_2 across R_2 provides the necessary bias.

$$V_2 = \frac{V_{DD} \times R_2}{R_1 + R_2} \Rightarrow V_2 = V_{GS} + I_D R_S; \quad \boxed{V_{GS} = V_2 - I_D R_S}$$

The circuit is so designed that $I_D R_S$ is larger than V_2 so that V_{GS} is negative. This provides correct bias voltage. We can find the operating point as under:

$$I_D = \frac{V_2 - V_{GS}}{R_S}$$ and $V_{DS} = V_{DD} - I_D(R_D + R_S)$

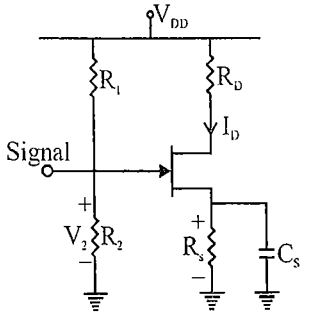
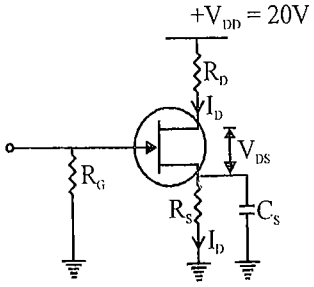


Fig. (b)

Modes of Operation:

1. Common source connection
2. Common drain connection
3. Common gate connection

Common Source Connection: The common source connection is most widely used arrangement. It is because this connection provides high input impedance, good voltage gain and a moderate output impedance. However, the circuit produces a phase reversal i.e. output signal is 180° out of phase with the input signal.



5. In a self bias n-channel JFET, the operation point is to be set at $I_D = 1.5mA$ and $V_{DS} = 10V$. The JFET parameters are $I_{DSS} = 5mA$ and $V_p = -2V$. Find the values of R_S and R_D. Given that $V_{DD} = 20V$.

Soln. Figure shown above.

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_p}\right)^2 ; 1.5 = 5\left(1+\frac{V_{GS}}{2}\right)^2$$

$$1+\frac{V_{GS}}{2} = \sqrt{1.5/5} = 0.55 \text{ or } V_{GS} = -0.9V$$

Now, $V_{GS} = V_G - V_S$

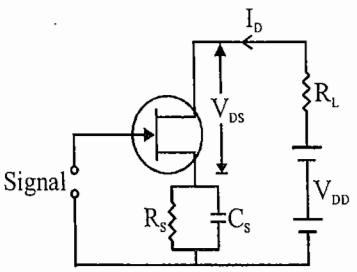
or $V_S = V_G - V_{GS} = 0 - (-0.9) = 9V \therefore R_S = \frac{V_S}{I_D} = \frac{0.9V}{1.5mA} = 0.6k\Omega$

Applying Kirchoff's voltage law to the drain circuit, we have

$V_{DD} = I_D R_D + V_{DS} + I_D R_S$; $20 = 1.5mA \times R_D + 10 + 0.9$

$$\therefore R_D = \frac{(20-10-0.9)}{1.5mA} = 6k\Omega$$

Voltage Gain of JFET Amplifier: Fig. (c) shows a typical circuit of a JFET amplifier. The JFET is a self biased by using the biasing network R_5 C_5. The d.c. component of the drain current flowing through the source biasing resistance R_5 produces the derived bias voltage, the capacitor C_S by pass the a.c. component of drain current. It may be noted that biasing circuit is similar to the cathode bias for a vacuum tube. The value of R_5 can be determined from the following relation.



$$R_S = \frac{V_{GS}}{I_D}$$

Where V_{GS} = Voltage drop across R_S and I_D = current through R_S like a vacuum tube, a JFET is a voltage driven device. Therefore, the voltage gain of a JFET amplifier can be determined in the same manner as for a vacuum tube.

$\therefore$ Voltage gain of JFET amplifier is $A_V = \frac{\mu R_{LS}}{r_d + R_L}$

Since $\mu = r_d \times g_m$ $\therefore$ $\boxed{A_V = \frac{r_d g_m R_L}{r_d + R_L}}$

If $r_d > R_L$ then the latter can be neglected as compared to the farmer.

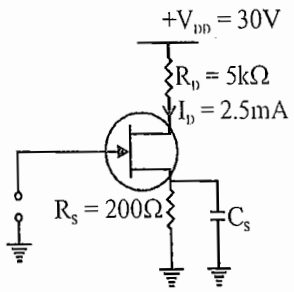
$\therefore$ Voltage gain, $A_V = \frac{r_d g_m R_L}{r_d}$ or $\boxed{A_V = g_m \times R_L}$

6. The transconductance of a JFET used in a voltage amplifier circuit is 3000 μmho and load resistance is 10kμ. Calculate the voltage amplification of the circuit assuming that $r_d >> R_L$.

Soln. $g_m = 3000$ μmho, $R_L = 10k\Omega$,

As $r_d >> R_L$ $\therefore A_V = g_m R_L = 3000 \times 10^{-6} \times 10{,}000 = 30$.

7. In the JFET circuit shown in figure. Find (i) V_{PS} and V_{GS}.

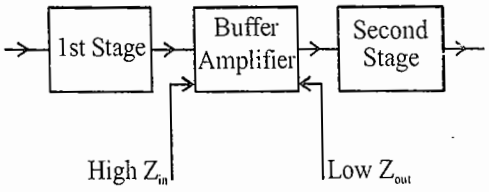


Soln. (i) $V_{DS} = V_{DD} - I_D(R_B + R_S) = 30 - 2.5mA\ (5 + 0.2) = 30 - 13 = 17V$

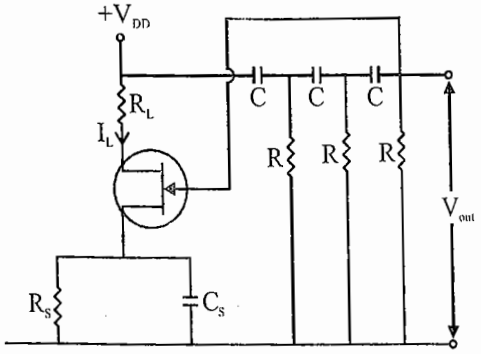
(ii) $V_{GS} = -I_D R_S = -(2.5 \times 10^{-3}) \times 200 = 0.5$ volt.

JFET Application: The high input impedance and low output impedance and low noise level make JFET for superior to the BJT. Some of the circuit applications of JFET are.

(i) As a Buffer Amplifier: A buffer amplifier is a stage of amplification that isolates the preceding stage from the following stage. Because of the high input impedance and low output impedance a JFET can act as an excellent buffer amplifier.



(ii) Phase Shift Oscillators: The high input impedance of JFET is especially valuable in phase shift oscillators to minimize the loading effect. Shows the phase shift oscillators using n-channel JFET.



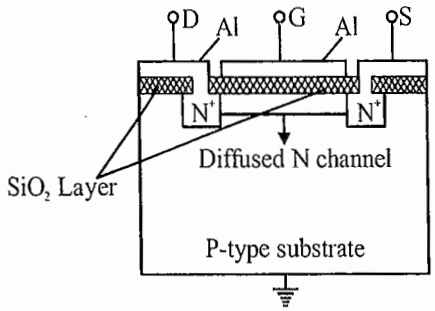
$$f = \frac{1}{2\pi RC\sqrt{6}}$$

(iii) As RF Amplifier: In communication electronics, we have to use JFET RF amplifier in a R_x instead of BJT amplifier far the following reasons.

(a) The noise level of JFET is very low.

(b) The antenna of the Receiver receives a very weak signal that has an extremely low amount of current. Since JFET is voltage controlled device. It will well respond to low current signally provides by the antenna.

MOSFET: It is an integrated circuit Si chip. It is fabricated by VLSI by using planner technology.

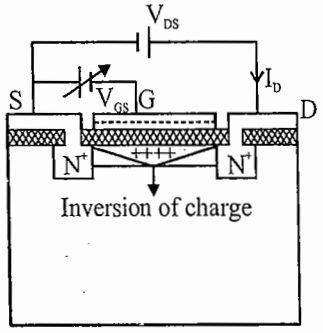


The entire area of MOSFET is less than 5% of total area of BJT.

- MOSFET are less noisy as compared to JFET.
- InMOSFET minority carrier storage time is zero.
- MOSFET are suitable for high free application.
- In depletion MOSFET. There is a pre-existing channel and the channel is diffused channel.

Operation of N-channel Depletion MOSFET:

Principle:



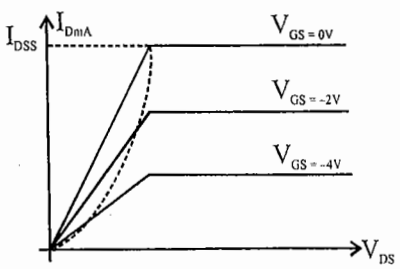
To operate N-MOS under depletion mode gate is negatively biased with reference to source.

For N-MOS V_{DD} is positive.

When $V_{GS=0}$: No charges available on aluminium plate. So, inversion charge will be zero. Maximum drain current is present is I_{DSS}.

When V_{GS} applied: The gate provided with negative voltage and therefore positive charges are created over the diffused n-channel and due to recombination less e^- will be reaching the drain I_D decreasing.

Drain Characteristics:

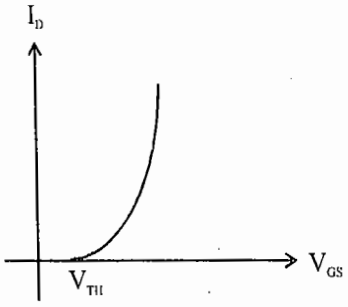


$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$I_D = k\left[V_{GS} - V_{TH}\right]$$

Transfer Characteristics:

I_D V/s. V_{GS} / V_{DS} constant



Homojunction: A homojunction is a semiconductor interface that occurs between layers of similar semiconductor material, there materials have equal band gaps but typically have different doping. In most practical case a homojunction occurs at the interface between on n-type (do nor doped) and p-type (acceptor doped) semiconductor such as Si, this is called pn junction. This does not have to be the are through, the only requirement is that the same semiconductor (same band gap) is found on both sides of the junction, in contrast to be a heterojunction.

Heterojunction: A heterojunction is the interface that occurs between two layers or regions of dissimilar crystalline semiconductors. There semiconductors materials have unequal band gaps as opposed to a homojunction. It is often advantageous to engineer the electronic energy bands in many solid state device applications including semiconductor lasers, solar cells and transistors to name a few. The combination of multiple heterojunctions together in a device is called a heterostructure although the two terms are commonly used interchangeably. The requirement that each material be a semiconductor with unequal gaps is some what loose especially on small length scales where electronic properties depends on spatial properties. A more modern definition may be to say that a heterojunction is the interface between any two solid state materials including crystalline and amorphous structure of metallic, insulating, fast ion conductor and semiconductor material.

8. The value of V_{SG} is

(a) –3.77V (b) 3.77V (c) –1.77V (d) 1.77V

Soln. $R_i = 8k\Omega$, $R_L = 22k\Omega$, $R_S = 0.5k\Omega$, $R_D = 2k\Omega$.

$$V_G = \left(\frac{R_2}{R_1+R_2}\right)(20-10) = \left(\frac{22}{8+22}\right)(20-10) = 4.67V$$

$$I_D = \frac{10-V_S}{R_S} = K_p(V_{SG}+V_{TP})^2,\ V_S = V_G + V_{SG}$$

$10 - (4.67 + V_{SG}) = (0.5)\ (1)\ (V_{GS})$

$\Rightarrow V_{SG} = 3.77V, -1.77V$, V_{SG} is positive voltage

Correct option is (b)

9. The value of I_D is

(a) 3.12 mA (b) 18.2 mA (c) 7.12 mA (d) 14.2 mA

Soln. $$I_D = \frac{10-V_s}{R_s} = \frac{10-(V_G+V_{GS})}{R_S} = \frac{10-(4.67+3.77)}{0.5} = 3.12mA$$

Correct option is (a)

10.

Soln.

10. The value of V_{SD} is

(a) 15.5V (b) 2.2V (c) 12.2V (d) 5.5V

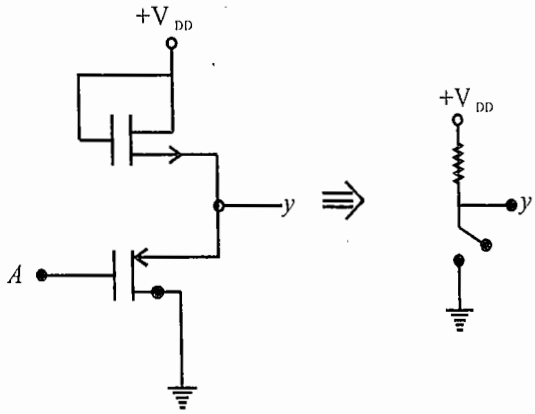
Soln. $10 = I_D (R_S + R_D) + V_{SD} - 10$

$V_{SD} = 20 - I_D(R_S + R_D) = 20 - 2.12(2 + 0.5) = 12.2V$

Correct option is (c)

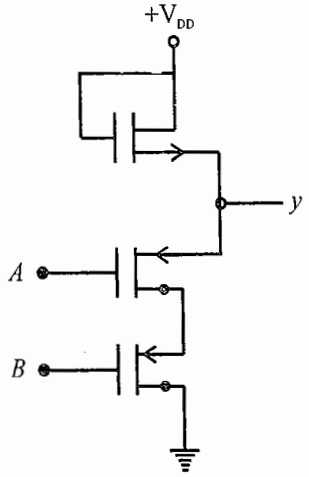
Implementation of Logic gates with help of PMOS:

PMOS NOT gate:



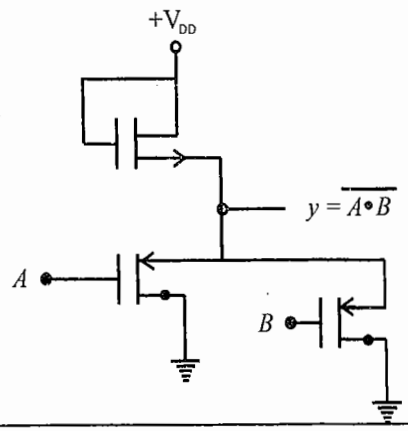
A	O/P voltage	y
0	*Gnd*	1
1	$-V_{DD}$	0

PMOS NOR gate:

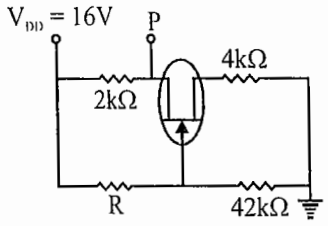


A	B	y
0	0	1
0	1	0
1	0	0
1	1	0

NMOS NOR gate:



11. In the circuit shown, the voltage at test point P is 12V and the voltage between gate and source is –2V. The value of R (in $k\Omega$) is **[GATE 2007]**



(a) 42 (b) 48

(c) 56 (d) 70

Soln. Drain current,

$$I_D = \frac{16-12}{2k\Omega} = 2mA$$

$$\therefore \quad V_G = \frac{16\times 42}{R+42}$$

$$V_s = I_D \times R_s = 2\times 4k\Omega = 8 \text{ volt}$$

$$\therefore \quad V_{GS} = V_G - V_s = \frac{16\times 42}{R+42} - 8 = -2$$

$$\Rightarrow \quad \frac{16\times 42}{R+42} = 6 \Rightarrow 16\times 7 = R+42$$

$$\Rightarrow \quad R = 70\,k\Omega$$

Correct option is (d)

12. An n-channel junction field effect transistor has $5mA$ source to drain current at shorted gate (I_{DSS}) and –5V pinch off voltage (V_P). Calculate the drain current in mA for a gate-source voltage (V_{GS}) of –2.5V. The answer should be up to two decimal places _____ **[GATE 2013]**

Soln. We have, $I_{DSS} = 5$ mA, $V_P = -5$V, $V_{GS} = -2.5$ V

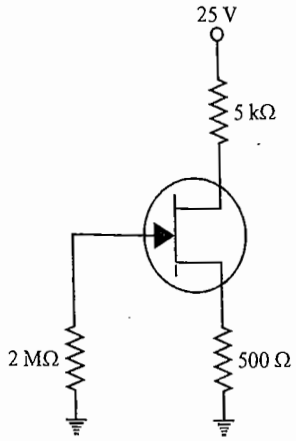
$I_D = ?$

We know that,

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 = 5\,mA\left(1-\frac{2.5}{5}\right)^2 = 1.25\,mA$$

Correct answer is (1.25) mA

13. In the given circuit, the voltage across the source resistor is 1 V. The drain voltage (in V) is _____ **[GATE 2015]**



Soln. We have, $I_D R_s = 1$, $I_D = \frac{1}{500} = 2mA$

Therefore, drain voltage $= 25 - I_D R_D = V_D = 15V$

Correct answer is (15) volt.

Chapter 5

Zener Diode & Opto Electronics

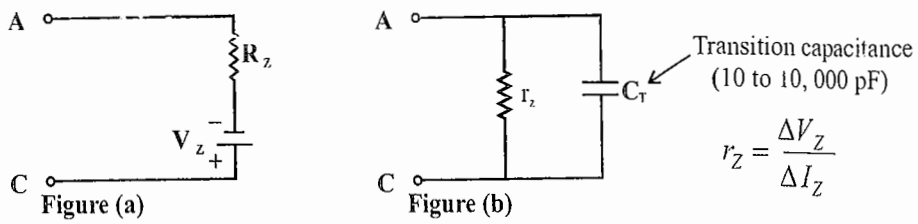
Zener Diode: Diodes which are designed with adequate power dissipation to operate in breakdown region may be employed voltage reference or constant voltage devices. Such diodes are known as avalanche, breakdown or zener diode.

Zener Diode Models:

The zener diode characteristics shown in Figure(a) may be approximated by a piece-wise linear V-I relationship (as was done for a forward-biased diode). Figure(a) gives the DC model where R_Z represents the static resistance. When the breakdown is virtually vertical Figure (a), then $R_Z = 0$.

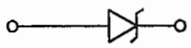
The small-signal model, is shown in Figure (b) where,

Dynamic resistance, $r_Z = \frac{\Delta V_Z}{\Delta I_Z}$

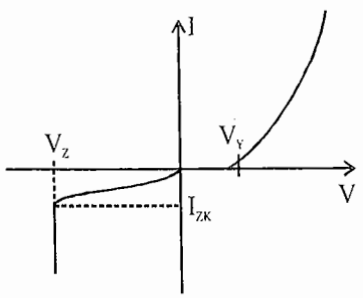


Figure(a) DC model of the zener diode, Figure (b) Small signal model of the zener diode.

Ideally, $r_Z = 0$, corresponding to the vertical characteristic. Practically, r_Z is a few ohms. However, for currents below I_{ZK}, r_Z may be a few hundred ohms. As zener diode operates in the reverse-bias, the transition capacitance, C_T must also be taken into account in the small-signal model as shown in Figure (b) and is proportional to the cross-sectional area of the diode. C_T may vary from 10, 000 pF for high-power avalanche diodes.

Symbol 

V-I characteristic :



$V_z \rightarrow$ Zener voltage or break down voltage, $V_y \rightarrow$ Cut in voltage, $I_{zk} \rightarrow$ Zener current

Zener diode is reversed biased heavily doped Si or Ge P-N junction diode which is operated in breakdown region Si is preferred to Ge due to it's high temperature and current carrying capability.

Forward bias V-I characteristic of zener diode is same as ordinary diode. When reverse biased voltage applied to zener diode, on increasing the reverse voltage, zener current is increased greatly from it's normal cut off value. This voltage is V_2 or break down voltage. There are two mechanism of zener break down.

(1) (i) Zener break down / tunneling (ii) Avalanche multiplication.

(i) Zener break down / tunneling: When reverse bias is applied a very strong electric field is set up across the depletion layer and is enough to break or rupture the covalent bonds. Due to rupture of covalent bond large number of electron hole pairs are produced which constituted the reverse saturation current. It occurs in heavily doped p-n junction diode.

(ii) Avalanche break down: It occurs in case of lightly doped p-n junction diode. Here minority carriers accelerated by field applied, they collide with semiconductor atoms in the depletion region. Due to collision with valance electrons covalent bonds are broken and electron hole pairs are generated. These new carriers so produced acquire energy from applied potential and turn produce additional carriers. This forms cumulative process called as avalanche multiplication.

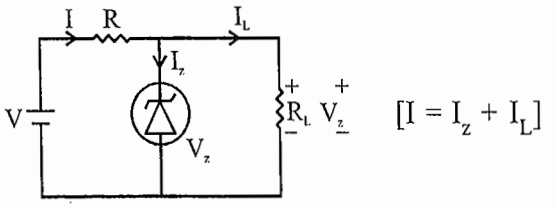
Difference Between zener and Avalanche:

Zener :

S.No.	Zener	S.No.	Avalanche
1.	Zener diode caused by field ionisation	1.	It is caused by impatt ionisation
2.	Bond raptures due to high electric field	2.	Bond raptures due to high velocity electrons
3.	Zener effect occurs when voltage approx. 6V	3.	Avalanche occur when voltage above 7V
4.	Zener effect is a negative temperature coefficient	4.	This is positive temperature coefficient.

Temperature Characteristic of Zener Diode: If reference voltage is above 6 volt (where physical mechanism involved is avalanche multiplication) temperature coefficient is positive. But below 6 volt where zener breakdown is involved and temperature coefficient is negative.

Explanation of Above Mechanism:



$[I = I_z + I_L]$

The source V and resistor R are selected in such a manner that diode is operating in breakdown region. Voltage across R_L is V_Z and diode current is I_Z. It have two type of regulation.

(i) **Line Regulation:** V_i = Vary, R_L = constant, V_0 = constant

$V_i \uparrow I \uparrow V_z \uparrow$ (slightly) $I_z \uparrow$ (highly)

$V_i = V_{max}, I_{max}, I_{z\,max}$

$\therefore$ I_L = almost constant

$V_0 = I_L R_L$ = constant

Load Regulation: R_L Vary, V_i = constant, V_0 = constant

$\because$ V_i = constant, I = constant

$R_L \uparrow V_0 \uparrow V_z \uparrow$ (slightly) $I_z \uparrow$ (highly) $I_L \downarrow$

$R_L = R_{Lmax}$, $I_z = I_{z\,max}$, $I_L = I_{L\,min}$

$\therefore$ $V_0 = I_L R_L$ = almost constant.

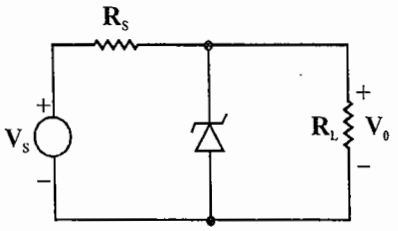
We have to take care of I_z other wise zener diode will burst.

A simple zener regulator:

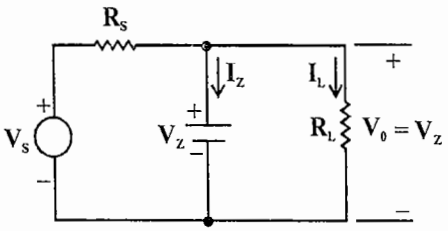
A zener diode regulator circuit shown in Figure (a) is used to maintain a constant output voltage, $V_0 = V_Z$ for varying load R_L and for unregulated source voltage $V_S > V_Z$. The equivalent circuit is shown in Figure (b). It can be seen that

$$I_S = I_L + I_Z$$

$$I_Z = I_S - I_L = \frac{V_S - V_Z}{R_S} - \frac{V_Z}{R_L} \qquad \left(\because V_0 = V_Z = I_L R_L\right)$$



Figure(a)



Figure(b)

If V_S is constant, I_Z varies with variation of load R_L. Also, for V_S constant, $I_S = (V_S - V_Z)/R_S$ is constant. As I_L increases, I_Z decreases and vice versa. A zener diode is specified by low as well as high current limitations. The high current limitation is determined by the power dissipation capability of of the zener diode. The limitation of lower limit zener current is I_{ZK}. For $I_Z < I_{ZK}$ (the knee point zener current) the regulation is poor and the output voltage deviates from V_Z. For a given diode, the limits on I_Z also restrict the minimum and maximum values of the source voltage V_S.

Generally, the value of knee current I_{ZK} is specified by the manufacturers. However, as a rule of thumb choose I_{ZK} to be 5 to 10% of the maximum rated current, in case I_{ZK} is not specified.

Rule to solve numericals for zener regulators designs:

Let V_S have values $V_{S\,min}$ to $V_{S\,max}$. (minimum to maximum DC voltage). Let zener diode with V_Z voltage have $I_{Z\,min}$ and $I_{Z\,max}$ as the limiting current (minimum to maximum zener currents). Let the load currents vary from $I_{L\,min}$ to $I_{L\,max}$. Then

(1) Ensure that $V_{S\,min}$ is greater than V_Z (the required regulated output voltage).

(2) Ensure that the range $(I_{Z\,max} - I_{Z\,min})$ is greater than $(I_{L\,max} - I_{L\,min})$

(3) Use the relations:

$$\frac{(V_{S\,max} - V_Z)}{R_S} = I_{Z\,max} + I_{L\,min}$$

$$\frac{V_{S\min} - V_Z}{R_S} = I_{Z\min} + I_{L\max}$$

Zener maximum power rating, $P_Z = I_{Z\max} \cdot V_Z$

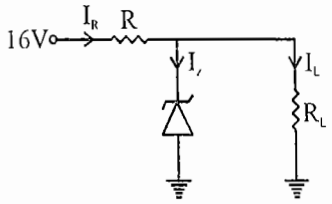
Example: For the circuit shown in figure, find out the output voltage v_0 for the cases

(a) $V_1 = V_2 = 5V$ (b) $V_1 = 5V, V_2 = 0\,V$ (c) $V_1 = V_2 = 0\,V$

For the Silicon diodes D_1 and D_2 used in the circuit assume $V_\gamma = 0.7\,V, R_f = 0,\ R_r \to \infty$ and reverse saturation current $I_S = 0$ for reverse-bias diodes.

SOLVED PROBLEMS

1. For the given circuit what is the value of R_S so that voltage across R_L is maintained at 12 volt. If load current variation I_L is from 0 – 200 mA. In this case also determine the value of P_z max.



Soln. $I_R = (I_Z)_{min} + (I_L)_{max}$, $I_R = 0 + 200 = 200mA$

$16 - V_L = I_R.R_S \Rightarrow R_S = \dfrac{16-12}{200\times10^{-3}} = 20\Omega$ $\because$ I_L varies from 0 to 200mA.

So, $(I_z)_{max.} = I_R - (I_L)_{min} = 200 - 0 = 200mA$

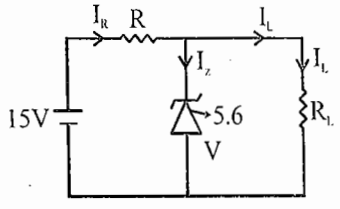
$(P_z)_{max.} = V_z.(I_z)_{max} = 12vx\ 200\ mA = 2.4$ watt

2. A zener-diode exhibits a constant voltage of 5.6 volt for currents greater than 5 times the knee current. I_{zk} is specified to be 1mA. The zener is to be used in design of a sheet regulator fed from a 15 volt supply. The load current varies over the range of (0 – 15) mA. Find a suitable value of resistor R. What is the maximum power dissipation of zener diode.

Soln. Given, $V_z = 5.6$ volt, $V_i = 15$ volt, $T_L = (0 - 15)$mA, $I_{zk} = 5mA$

(i) $I_R = (I_L)_{max} + (I_{2k})_{min} = 15 + 5 = 20mA$

$$R = \frac{V_i - V_z}{I_R} = \frac{15-5.6}{20mA} = \frac{9.4\times10^3}{20} \Rightarrow 470\Omega$$

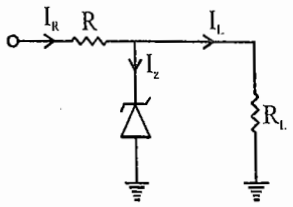


(ii) maximum power dissipation

$I_z = 20mA$, $P = V_z\, I_z = 5.6 \times 20mA = 112m$ watt

3. Design a voltage regulator that will maintain an output voltage of 20V across a $1k\Omega$ load with an input that will vary between 30V and 50v. Determine value of R_S and maximum current I_{zm}.

Soln. $I_L = \dfrac{20}{1k\Omega} = 20mA$



$(I_R)_{max} = (I_z)_{max} + 20mA$, $(I_R)_{min} = (I_{z\,min}) + 20mA = 20mA$

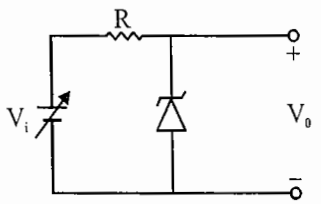
$(V_i)_{min} = (I_R)_{min.} R_S + V_z$

$30 = 20 \times R_S + 20$; $R_S = \dfrac{10}{20\times10^{-3}}$

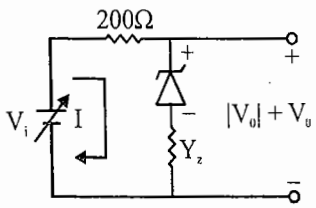
$(I_R)_{max} = \dfrac{50+20}{0.5} = 60mA = I_{zm} + I_L$, So, $I_{ZM} = 60 - 20 = 40$ mA.

4. For zener diode shown in figure the (V_z) at knee is 7 volt, the knee current is negligible and zener diode dynamic resistance is 10Ω. If the input voltage V_i range is from (10 to 16 volt) then what is the range of output voltage?

Soln.



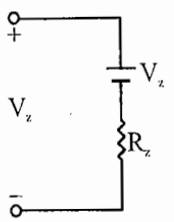
If zener dynamic resistance is considered



$(I)_{min} = \dfrac{10-7}{210} = \dfrac{3}{210}$ Amp, $(V_0)_{min} = 7 + \dfrac{10\times3}{210} = 7.14$ volt

$I_{max} = \dfrac{16-7}{210}$, $(V_0)_{max} = 7 + \dfrac{9\times10}{210}$, $(V_0)_{max} = 7.43$ volt

Use of Zener diode as a Shunt Regulator: Zener diode is used in designed of shunt regulator so named because the regulator circuit appears in parallel circuit with load.



Steps for Solving Problems:

(i) Check the states of zener diode (ON or OFF) by removing in from the network and calculating the voltage across the resulting open circuit.

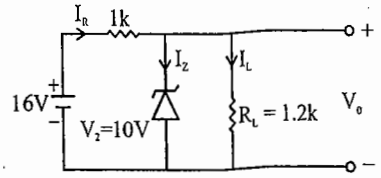
$V_0 = \frac{V_i R_L}{R + R_L}$, ON $\rightarrow$ $V_z < V_0$, OFF $\rightarrow$ $V_z > V_0$

(ii) Substitute the appropriate equivalent circuit and solved for the derived unknown.

Tunneling: In case of tunneling number of electron in valance band in p-type will be (increases) and due to that value of current will (increase). So, breakdown is achieved at smaller value of V_z.

Type I: Far fixed V_i and R_L $\rightarrow$

5.

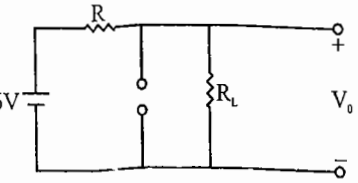


For the given circuit calculate

(a) V_0 (b) V_R (c) I_z (d) P_z

Soln. Check the status of zener diode (ON or OFF)

Step-I:



Let there is no diode in the circuit

$\therefore I = \frac{16}{1.2+1} = \frac{16}{2.2}$ mA $\therefore V_0 = \frac{16}{2.2} \times 1.2 = 8.73V$

$V_0 = \frac{V_i \times R_L}{R + R_L} = 8.73$ i.e. $V_0 < V_z$

diode will be OFF.

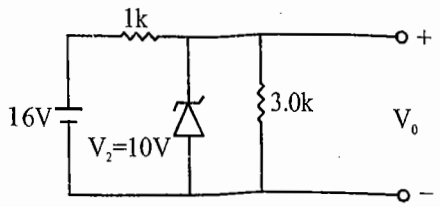
But $V_z = 10V$, i.e. $\boxed{V_z > V_0} \Rightarrow$ Zener diode can not inter into breakdown region. Thus circuit across diode will be open.

Step-II: The equivalent, circuit will be same as above drawn

$\boxed{I_Z = 0} \Rightarrow \boxed{P_z = 0}$

$V_0 = 8.73V$ and $V_R = 16 - 8.73 = 7.27$ volt.

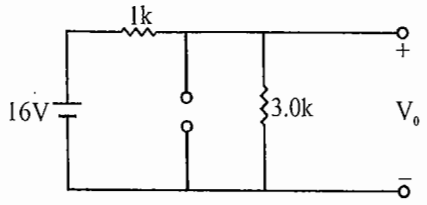
6.



Find

(a) V_0 (b) I_z (c) P_z (d) V_R

Soln. **Step-I:** Remove diode

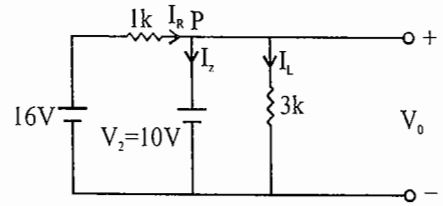


$V_0 = \frac{16 \times 3}{4} = 12\,\text{Volt}$, But $V_z = 10V < 12V$

Zener diode will go in breakdown region and output will remain 10V not 12V.

$\therefore \boxed{V_0 = 10V}$

Step-II: Draw equivalent circuit



Applying KCL at point P

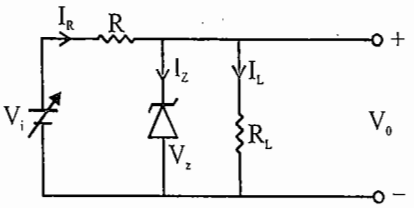
$I_R = I_z + I_L$

$\frac{16-10}{1} = I_z + \frac{10}{3} \Rightarrow 6 = I_z + \frac{10}{3} \quad \therefore \boxed{I_z = \frac{8}{3} mA}$

$P_z = V_z.I_z = \frac{8}{3} \times 10 = 26.7mW$, $V_R = 16 - 10 = 6V$

Type-II: Calculating of range of V_i[$V_{i(max)}$ and $V_{i(min)}$] assuming R_L and R are fixed.

Theory:



Given diode is on; $I_z(0 \rightarrow I_{ZM})$ because it is not fixed. Since diode is ON. So, V_0 will be fixed. Given R_L is fixed. So I_L will be fixed.

$\therefore V_i = V_R + V_Z$, here $V_Z \rightarrow$ fixed, $\therefore I_Z \rightarrow$ fixed

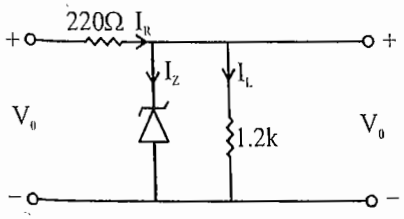
only variables are V_R and so I_R also

$\therefore (V_R)_{max} = (I_R)_{max}.R = [(I_z)_{max} + I_L].R \quad \therefore (V_i)_{max} = (V_R)_{max.} + V_z$

$I_R = I_L + I_Z$

$\Rightarrow \boxed{(V_i)_{max} = [(I_z)_{max} + I_L]R + V_Z} \quad \boxed{(V_i)_{min} = [(I_z)_{min} + I_L]R + V_Z}$

7. Calculate range of V_i for which zener diode is in ON state.



$V_z = 20V$, $I_{ZM} = 60mA$] given

Soln. ∵ Diode is ON, ∴ $V_0 = V_z = 20V$

$$\therefore I_L = \frac{20}{1.2} = \frac{50}{3} mA \quad \therefore I_R = I_Z + I_L$$

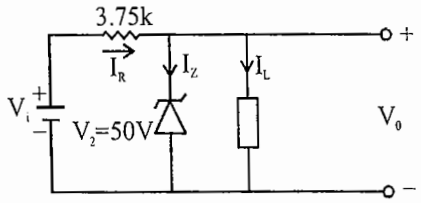
$$\text{or } (I_R)_{max} = I_{z\,max} + I_L = 60 + \frac{50}{3} = \frac{230}{3} \text{ mA}$$

$$(I_R)_{min} = I_{z\,min} + I_L = 0 + \frac{50}{3} = \frac{50}{3} \text{ mA} \therefore (V_i)_{max} = [(I_R)_{max} \times R] + V_z$$

$$= \frac{230}{3} \times 0.220 + 20 = 36.87V$$

$$(V_i)_{min} = [(I_R)_{min} \times R] + V_z = \frac{50}{3} \times 0.22 + 20 = 23.67 \text{ volts}$$

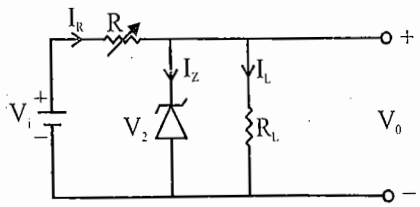
8. If diode current varies from 5mA to 40mA and load current is 25mA. What are the limits between for which V_i may vary without loss of regulation in circuit.



Given $I_{TD(range)}$ = 5mA to 40mA
I_L = 25mA (Fixed) and V_2 = 50V, Range V_i = ?
Since diode is ON; $V_D = V_Z = 50V$
or $(I_R)_{max} = (I_z)_{max} + I_L = 40 + 25 = 65$ mA
$(I_F)_{min} = (I_Z)_{min} + I_L = 5 + 25 = 30$ mA
$\therefore (V_i)_{max} = (V_R)_{max} + V_Z = (I_R)_{max}.R + V_Z = (65 \times 3.75) + 50 = 293.75V$
$\therefore (V_i)_{min} = (V_R)_{min} + V_z = (I_Z)_{min} \times R + V_Z = 30 \times 3.75 + 50 = 162.50V$
$\therefore$ Range of $V_i = 162.50V < V_i < 293.75V$.

Type-III: Calculation of range of R, assuming V_i and R_L are fixed.

Theory:



here V_i and R_L are fixed, $V_0 = V_z$ is fixed.

$I_z \rightarrow [0 \text{ to } (I_z)_{max}]$

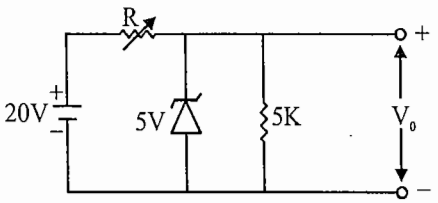
$\because V_i = I_R.R + V_z$

$(I_R)_{max} = (I_Z)_{max} + I_L$

$(I_R)_{min} = (I_Z)_{min} + I_L$

$$\boxed{R_{max} = \frac{V_R}{(I_R)_{min}}} \quad \boxed{R_{min} = \frac{V_R}{(I_R)_{max}}}$$

9. For given circuit $V_z = 5V$, $I_{ZM} = 4A$. Calculate value of R.



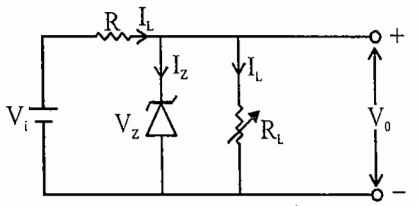
Soln. Given, $V_z = 5V$, $V_i = 20V$, $I_{zm} = 9mA$,

$$I_L = \frac{V_0}{R_L} = \frac{5}{5} = 1mA$$

$$(R_{max}) = \frac{20-5}{0+I_L} = \frac{15}{1} = 15K\Omega = \frac{V_R}{(I_R)_{min}}, \quad (R_{min}) = \frac{V_R}{(I_R)_{max}} = \frac{15}{1+9} = 1.5K\Omega$$

Range of R : $1.5K\Omega < R < 15K\Omega$

Type-IV: Range of I_L for which diode is ON



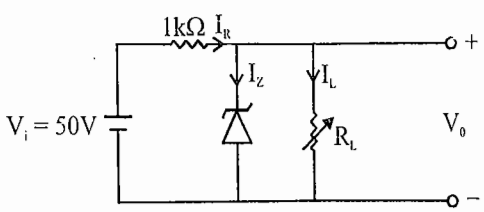
Apply KCL

$I_R = I_Z + I_L \Rightarrow I_L = I_R - I_Z$

$\therefore (I_L)_{max} = I_R - (I_Z)_{min}$, $(I_L)_{min} = I_R - (I_Z)_{max}$.

$$\boxed{(R_L)_{max} = \frac{V_0}{(I_L)_{min}} = \frac{V_Z}{(I_L)_{min}}} \quad \boxed{(R_L)_{min} = \frac{V_0}{(I_L)_{max}} = \frac{V_Z}{(I_L)_{max}}}$$

10. Find range of R_L and I_L, that will result in output voltage at 10 volt.



$V_Z = 10V$, $I_{ZM} = 32mA$, $V_0 = 10V$.

Soln. $V_R = 50 - 10 = 40$ volt

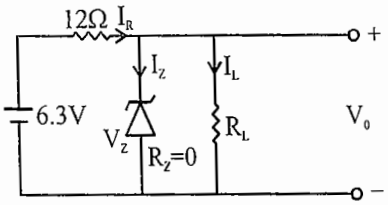
$\therefore I_R = \frac{V_R}{R} = \frac{40}{1K\Omega} = 40$ mA

$(I_L)_{max} = (I_R)_{max} - (I_Z)_{min} = 40 - 0 = 40mA$, $(I_L)_{min} = (I_R)_{max} - (I_Z)_{max} = 40 - 32 = 8mA$

$\therefore (R_L)_{max} = \frac{V_Z}{(I_L)_{min}} = \frac{10}{8} = 1.25\ K\Omega$

$\therefore (R_L)_{min} = \frac{V_Z}{(I_L)_{max}} = \frac{10}{40} = 0.25K\Omega$

11. In voltage regulator circuit, Zener diode is to be limited to range $5mA \le I_2 \le 100mA$.



(a) What is possible range of load current?

(b) What is possible range of load resistance?

Soln. $V_0 = V_Z = 4.8V$

$\therefore I_R = \frac{V_i - V_Z}{R} = \frac{6.3 - 4.8}{12} = 0.125Amp = 125mA$

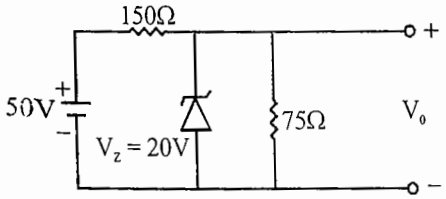
$(I_L)_{max} = I_R - (I_Z)_{min} = 125 - 5 = 120mA$, $(I_L)_{min} = I_R - (I_Z)_{max} = 125 - 100 = 25mA$

$(R_L)_{max} = \frac{4.8}{25} = 192\Omega$, $(R_L)_{min} = \frac{4.8}{120} = 40\Omega$

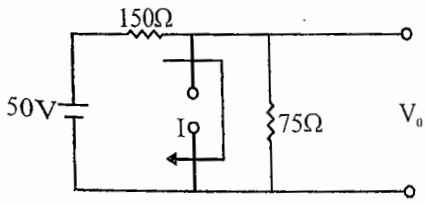
Mixed Problem:

12. For voltage regulator circuit, shown in figure below, what is power dissipation in zener diode?

Soln.



Here, $V_Z = 20V$. Also we have not given, the diode is ON or OFF. To check this, we remove diode and use KVL, we get.

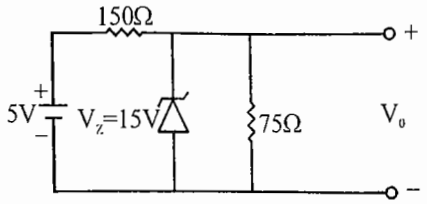


$I = \frac{50}{225} \Rightarrow V_0 = \frac{50}{225} \times 75 = \frac{50}{3}$ Volt $= 16.66$ volt

Here, $V_0 < V_Z$ (not break down)

$\therefore$ Diode will be off $\therefore \boxed{V_Z = V_0 = 0}$ $\therefore \boxed{P_Z = V_Z I_Z} = 0$

13. For power dissipation along Zener diode shown below.

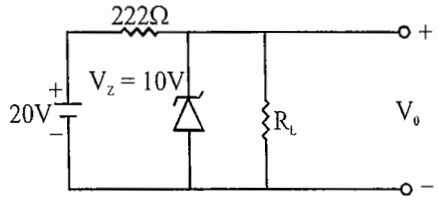


Soln. To check status, we remove the diode and get, $V_0 = \frac{50}{3}V > V_Z$

$\therefore$ V_0 will be = V_Z = 15 V

$\therefore$ $I_Z = I_R - I_L = \frac{35}{150} - \frac{15}{75} = \frac{35-30}{150} = \frac{1}{30}\,Amp$

14. In voltage regulator shown in figure power rating of zener diode is 400 mW. What is the value of R_L that will established?



Soln. **Note:** The maximum power dissipation along zener diode means maximum current flow through the diode (i.e. I_{ZM}) and minimum current flow through load [i.e. $(I_L)_{min.}$].

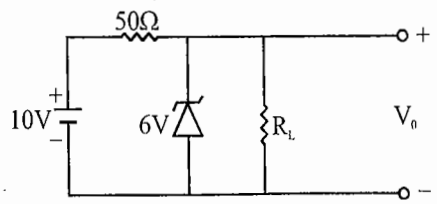
Given P_Z = 400 mW = 400×10^{-3} = $I_{ZM}.V_z$

$$I_{zM} = \frac{400\times10^{-3}}{10} = 40mA$$

$$\therefore I_R = I_{ZM} + I_L \Rightarrow \frac{V_i - V_Z}{222} = I_{ZM} + I_L \quad I_L = 45 - 40 = 5mA$$

$$R_L = \frac{10}{5} = 2K\Omega$$

15. A 6V zener diode has $R_Z = 0$ and I_{ZK} of 5mA, what is the value of R. So that voltage across it does not fall below 6V.



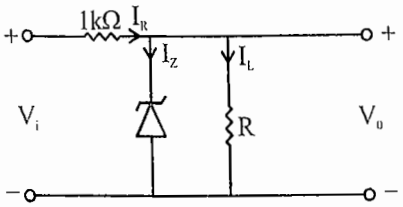
Soln. **Note:** For given any unknown voltage for zener diode, we assume it may be any value between 0 and V_Z, then we find the current across diode, that will be between 0 and I_{ZM}, but here it is given (I_{ZM} = 5mA), $\therefore$ $I_R = I_L + I_Z$

or, $\frac{10-6}{50} = 5\times10^{-3} + I_L \quad \therefore I_L = 0.08 - 0.005 = 0.075, \quad \therefore I_L = 0.08 - 0.005 = 0.075$

$$\therefore R = \frac{6\times10^3}{0.075} = 80\Omega$$

16. Zener diode in regulator circuit has zener voltage of 5.8V and zener knee current of 0.5mA. What is maximum value of load current when input voltage varies from 20-30 volt.

Soln.



Given, $V_Z = 5.8V$, $I_{ZK} = 0.5mA$ (fixed)V

$V_i = 20$ to $30V$, $\boxed{I_R = I_Z + I_L}$

or $(I_L)_{max} = (I_R)_{max} - I_Z$ and $(I_L)_{min} = (I_R)_{min} - I_Z$

$\because (I_R)_{max} = \frac{24.2}{1} = 24.2mA$ $(I_R)_{min} = \frac{14.2}{1} = 14.2mA$.

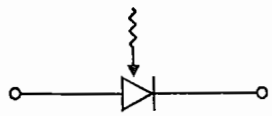
$\therefore (I_L)_{max} = 24.2 - 0.5 = 23.7$ mA, $(I_L)_{min} = 14.2 - 0.5 = 13.7$ mA

OPTO ELECTRONICS

1. **Bulk Type, Photo Conductors:** If energy of photon is greater than gap of semiconductor then covalent bonds of SC will be broken and new electron hole pairs are created which will increase conductivity of semiconductor. This effect is known as photo conductive effect.

Due to increase in conductivity resistivity will decrease i.e. resistance will decrease hence device is called photo resistor or photo conductor. Photo conductive cell is a device in form of either a slab of a semiconductor in bulk form or a thin film of semiconductor deposited on an insulating substrate with ohmic contacts at opposite end.

Symbol:



$\boxed{E_\lambda \geq E_g}$

Examples of photo conductive cells are Cds, Cds and Pbs. The most popularly used photo conductive cell in visible spectrum is Cds cell. In case of Cds in absolute darkness resistance is as high as $2M\Omega$ but in strong incident light it has resistance as small as 10Ω.

Cds photo conductive cells has merits

(1) High dissipation capability

(2) Excellent sensitivity in visible spectrum

(3) Low resistance when irradiated by light

Application of Photo Conductive Cells:

(1) To measure the intensity of light

(2) As a voltage regulator

(3) To record modulated light intensity

(4) Used in counting applications

2. **Junction Type Photo Conductors**

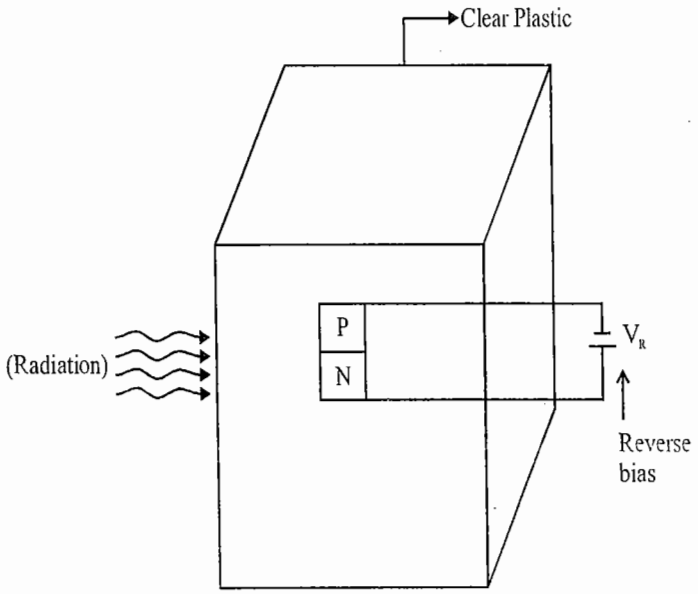
(a) P-N photo diodes

(b) Solar cells

(c) PIN photo diodes

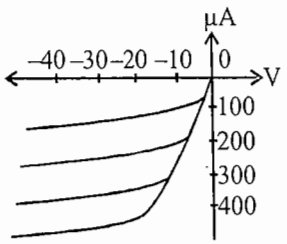
(d) Avalanche photo diodes

(a) P-N Photodiodes: A P-N photo diode is essentially a reverse biased P-N junction in which light is permitted on one surface of junction. This device consists of a P-N junction embedded in clear plastic as indicated in figure. Radiation is allowed to fall upon one surface across the junction. The remaining sides of plastics are either painted black or enclosed in a metallic care.



V-I Characteristic of Photo Diode: If reverse voltage in excess of a few tenth of a volt are applied then a reverse current independent of magnitude of reverse voltage applied. This dark current corresponds to reverse current due to thermally generated minority carriers. If light falls upon surface additional electron hole pair are created proportional to number of incident photons. So here, total current is given by $I_{total} = I_0 + I_5$, where I_5 is the short circuit current proportional to light intensity.

Typical V-I characteristics of Photo diode are shown in figure.



The curves don't pass through origin (with the exception of dark current curve).

Note: Radiation must be focussed near the junction. If radiation is focussed into a small spot away from the junction the injected minority carrier can recombine before diffusing the junction and hence a much smaller current will result.

Application of photo diode:

(1) High speed reading of computer punch card and tapes.
(2) Light detection requirement.
(3) Reading of film sound track
(4) Light operated switches
(5) Switching
(6) Optical communication

Photo Voltaic Potential: In case of photo diode if forward bias is applied then potential barrier is lowered and majority current increase when majority current equals to minority current then this total current is reduce to zero. The voltage at which zero current is obtained is called the photo voltaic potential. When

light falls on the P-N junction diode then reverse current increases and forward current also increases to make total current equal to zero. This photo voltaic potential is of the order of magnitude of 0.5 volt far Si and 0.1 volt for Ge. In open circuited condition for I = 0 then photo voltaic voltage is generated and voltage is V_{max}.

$$\boxed{V_{max} = \eta V_T \ln\left(1+\frac{I_S}{I_0}\right)} \quad \text{Since } \frac{I_S}{I_0} >> 1$$

So, V_{max} increases logarithmically with I_S there I_S changes with intensity of light.

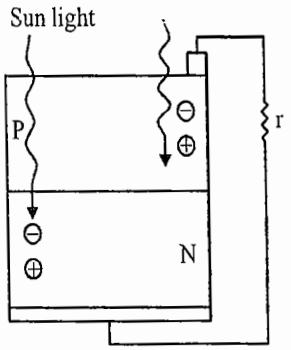
Solar Energy Converters: It is clear that a definite non-zero current is obtained for zero applied voltage. Hence a junction photo cell may be used under short circuited condition. As here I_S is proportional to light intensity. The current drain from a photo voltaic cell may be used to power electronics equipment or more commonly to charge auxiliary storage batteries. Such energy converters using sun light as primary energy are called solar batteries and are used in solar cells.

(b) Solar Cell: The solar cell is basically a P-N junction diode that converts sunlight directly to electricity with large conversion efficiency. The action of solar cell is explained as follows.

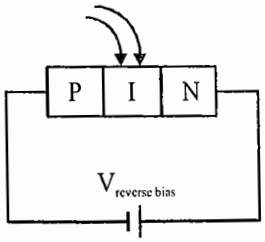
When a P-N junction diode is expired to light photons are absorbed and EHP_S are generated in both P and N side of junction. The electron move to N-side and holes move to P-side.

If a load resistance is connected across the diode a current will flow in circuit. The maximum current called short circuit current is obtained when an electric short is connected across the diode terminals. Note that flows as long as the diode is exposed to sun light and magnitude of current is proportional to light intensity.

Solar cells are constructed with Si, GaAs, Cds and with many others. It is used in satellite and space vehicle.



(c) PIN Photo Diode: An intrinsic silicon water is inserted between heavily doped P and N-type silicon materials. The intrinsic Si reduces the transit time of photo induced electron hole pairs. The reason is that carriers generated by light photons incidents on middle of this layer have less distance to travel than if generated at one side or the other side of the layer. The response time of PIN diode is ultra fast with a switching speed of nano second. So PIN photo diodes are used in ultra fast switching and logic circuits.



(d) Avalanche Photo Diode: When photo diode is operated in break down region then this diode is Avalanche photo diode. Current sensitivity is increased by 30-100 time is care of APD. There diodes are operated at high reverse bias voltage so that break down of diode takes place.

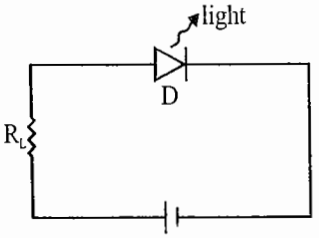
Main advantages of APD is it's high sensitivity.

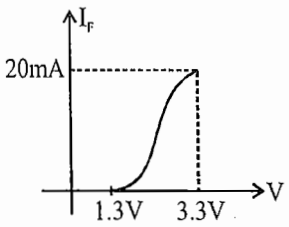
(e) Photo Transistor: The photo transistor is a junction transistor with collector base junction exposed to light. It is similar to photo diode but has a sensitivity gain of 50 to 100 times more. Generally N-P-N transistor are used to its increased gain and created sensitivity.

Light Emitting Diode (LED):

Principle : Electron luminescence.

(Limiting Resistance)





In LED light is emitted due to a large number of recombinations at the junctions popularity used material for fabrication Ga As with 20mA of current LED gives max intensity of light. It operates in forward biased condition when temperature (increases) efficiency of LED (decreases).

Advantage of LED:

(1) Low working voltage and current
(2) Less power consumption
(3) Very fast action
(4) Small size and weight
(5) Long life

Liquid Crystal Display (LCD):

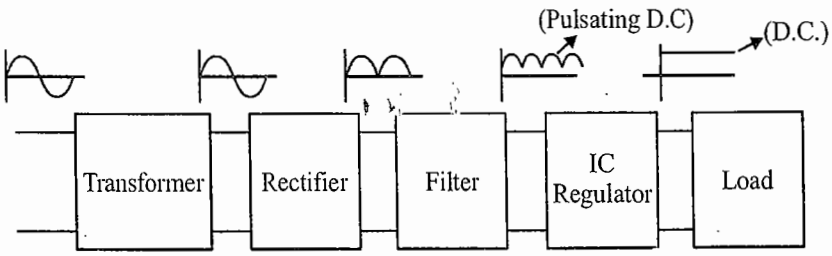
Principle: Dynamic scattering of light LCD are requires less power than LED i.e. of the order of μ watt.

LCD are having lesser operating time is compared to LED.

Note: Material used for construction is compared crystal material.

Example: Pneumatic crystal:

Block Diagram of a Power Supply:



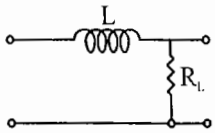
(1) Transformer: It consists of two separate coils wound around an iron case that magnetically couples the two windings. It provides appropriate sinusoidal input for the supply and also provides isolation between electronics equipment.

(2) Rectifier: Explained previously

(3) Filter: The output of rectifier filter is much more constant than without filter but still it contains time dependent component called ripple.

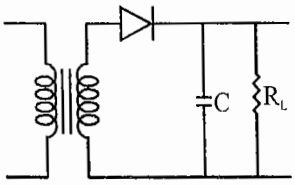
Types of Filter:

(1) Series L Filter:



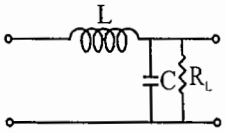
Ripple factor $\gamma = \frac{R_L}{3\sqrt{2}\,\omega L}$

(2) Shunt Capacitor Filter:



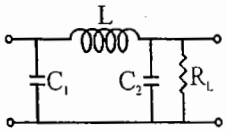
Ripple factor $\gamma = \frac{1}{4\sqrt{3}\,fc\,R_L}$

(3) LC Filter:



Ripple factor $\gamma = \frac{\sqrt{2}}{12\omega^2 L_C}$

(4) CLC Filter or π Filter:



Ripple factor $\gamma = \frac{V}{12\omega^3 C_1 C_2 R_L . L}$

Regulated Power Supply: There are three reasons why an unregulated power supply is not good for many applications.

(1) Poor regulation output is not constant as the load varies

(2) D.C. output voltage varies with ac input.

(3) D.C. output varies with temperature, particularly because S.C. devices are used.

Types of Voltage Regulator:

(1) Bleeder resister regulator

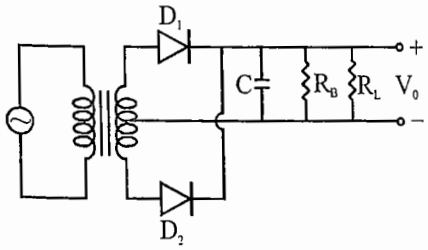
(2) Zener diode shunt regulator

(3) Transistor series regulator

(4) Transistor shunt regulator

(5) OP-Amp voltage regulator

(1) Bleeder Resister Regulator: Some times a resister called bleeder is connected across output.



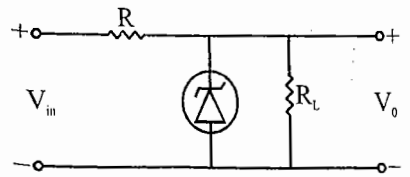
Functions per formed by bleeder resister

(i) It improves voltage regulation as it act as a preload to power supply and causes an initial voltage drop. Difference between no load and full load voltage is reduced.

(ii) It improves the filtering action by maintaining a constant current through the chock.

(iii) It provides safety to technician handling the equipment

(2) Zener Diode Shunt Regulator:



Series resistance R limits input current where a zener diode operates in break down region, then voltage across it is constant for large charge in current through it.

Limitation of Zener Diode:

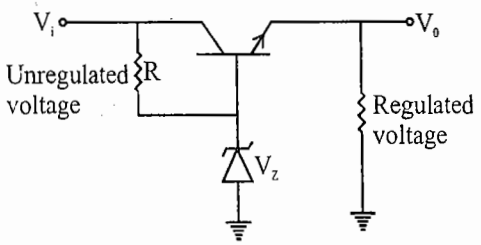
(i) It has low efficiency for heavy load currents because there is considerable power loss in R.

(ii) The output voltage changes slightly due to zener imedance.

Series Regulator Circuit: Transistor Q_1 is the series control element and zener diode provides reference voltage. The regulating operation can be described as follows:

(i) If the output voltage decreases then increase base-emitter voltage causes transistor Q_1 to conduct more thereby laising the output increases then, decrease base-emitter voltage causes transistor Q_1 to conduct less and thereby reducing the output voltage and maintain output constant.

The collector and emitter are in series with the load so circuit is known as series voltage regulator. By increase in input voltage appears across transistor, so that output voltage tries to remain constant.

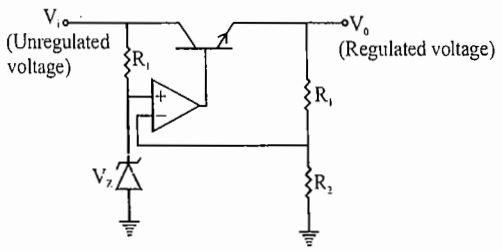


The collector and emitter are in series with the load so circuit is known as series voltage regulator. By increase in input voltage appears across transistor, so that output voltage tries to remain constant.

$$\boxed{\text{Value of output Voltage} = V_0 = V_z - V_{BE}}$$

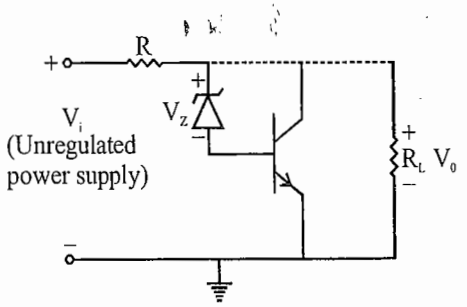
The limitation of this circuit is that output is not constant because V_{BE} and V_Z both decrease with increase in temperature.

OP-AMP Series Regulator:



$$\boxed{V_0 = \left(1 + \frac{R_2}{R_1}\right) V_z}$$

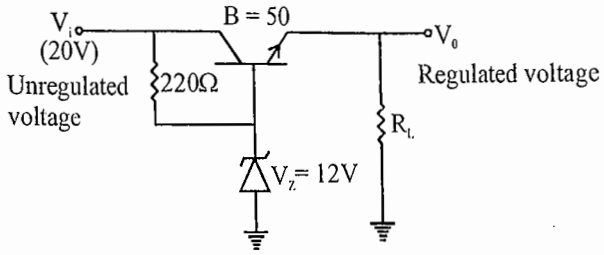
(4) Shunt Voltage Regulation: A shunt voltage regulator provides regulation by shunting current away from the load to regulate the output voltage. Figure shows the block diagram of such a voltage regulator.



The output voltage across the load $\boxed{V_L = V_Z + V_{BE}}$

SOLVED PROBLEMS

1. Calculate output voltage and zener current in regulator circuit for $R_L = 1K\Omega$.

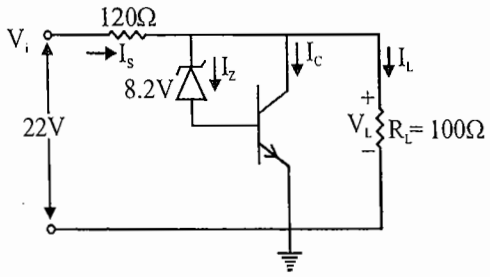


Soln. $V_0 = 12 - 0.7 = 11.3$ V, $V_{CE} = 20 - 11.3 = 8.7$ volt

$$I_R = \frac{V_i - V_z}{R} = \frac{8}{220} = 36.4 \text{ mA}, I_L = I_C = \frac{11.3}{R_L} = 11.3 \text{ mA}$$

$$I_B = \frac{I_C}{B} = 222\,\mu\text{A},\ I_Z = I_R - I_B = 36 \text{ mA}$$

2. Determine regulated voltage and circuit currents for given shunt regulator.

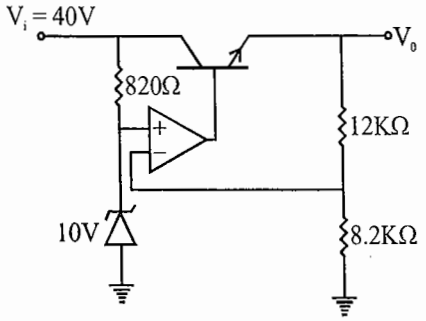


$V_L = 8.2 + 0.7 = 8.9$ Volt

$$I_L = \frac{V_L}{R_L} = \frac{8.9}{100\Omega} \Rightarrow 0.089A \Rightarrow 89mA$$

$$I_S = \frac{22 - 8.9}{120} \Rightarrow \frac{13.1}{120} \Rightarrow 109mA \quad \boxed{I_C = 20mA}$$

3. Calculate regulated output voltage for given circuit.



Soln. 24.6 Volt.

Zener

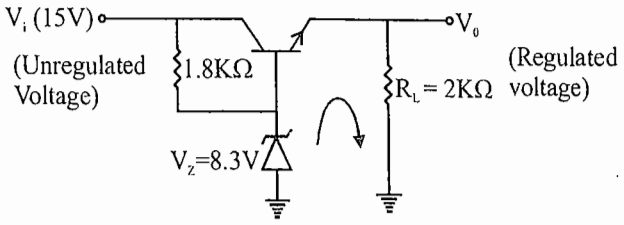
4.

Soln.

5.

Soln.

4. Calculate output voltage and zener diode current in regulator circuit.



Soln. $V_0 = 7.6V$, $I_Z = 3.66$ mA $\quad -8.3 + 0.7 + V_0 = 0;\ V_0 = 7.6$ V

IC Voltage Regulators:

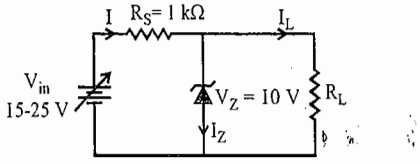
Positive Voltage Regulators in 7800 series.

		(Output Voltage)
1.	7805	+5V
2.	7806	+6V
3.	7808	+8V
4.	7810	10V
5.	7812	12V
6.	7815	15V
7.	7818	18V
8.	1724	24V

Negative Voltage Regulation in 7900 Series:

1.	7905	–5V
2.	7906	–6V
3.	7908	–8V
4.	7909	–9V
5.	7912	–12V
6.	7915	–15V
7.	7718	–18V

5. Pick the correct statement based on the below circuit. **[GATE 2009]**



(a) The maximum zener current, $I_{Z(max)}$, when $R_L = 10\ k\Omega$ is 15 mA

(b) The minimum zener current, $I_{Z(min)}$, when $R_L = 10\ k\Omega$ is 5 mA

(c) With $V_{in} = 20$ V, $I_L = I_Z$, when $R_L = 2\ k\Omega$

(d) The power dissipated across the zener when $R_L = 10\ k\Omega$ and $V_{in} = 20$ V is 100 mW

Soln. $V_{in} = 20V$, $V_z = 10V$, $R_L = 2\,k\Omega$, $I_s = I_z + I_L$

$$I_s = \frac{V_{in} - V_z}{R_s} = \frac{20-10}{1k\Omega} = \frac{10}{1\,k\Omega} = 10\,mA$$

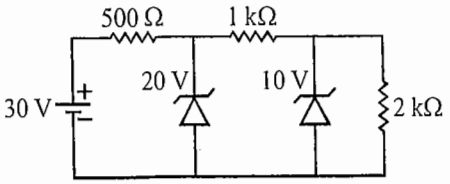
Now, $I_L = \frac{V_z}{R_L} = \frac{10}{2\,k\Omega} = 5mA$

$\therefore \quad I_z = I_s - I_L = (10-5)nA = 5\,mA$

Now, $I_z = I_s - I_L = (10-5)nA = 5mA$

Correct option is (c)

6. In the following circuit, the voltage across and the current through the 2 kW resistance are



[GATE 2011]

(a) 20 V, 10 mA (b) 20 V, 5 mA (c) 10 V, 10 mA (d) 10 V, 5 mA

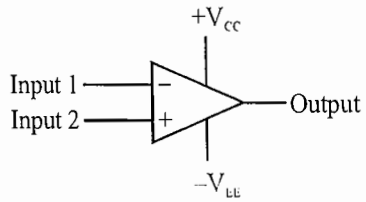
Soln. In reverse bias zener diode behave like a voltage regulator. Therefore, voltage across the resistance, 2 $k\Omega$ will be 10 volt and current $I_2 = \frac{V_z}{2\,k\Omega} = \frac{10}{2} = 5\,mA$

nics

Chapter 6

Operational Amplifier

Symbol:



(+) Non-inverting terminal, (–) Inverting terminal

Input impedance : Few mega Ω (Very high), Output impedance : Less than 100 Ω (Very low)

Differential and Common Mode Operation: One of the more important features of a differential circuit connection as provided in an op-amp is the circuit ability to greatly amplify signals that are opposite at the two inputs while only slightly amplifying signals that are common to both inputs.

An op-amp provides an output component that is due to the amplification of the difference signals applied to the plus and minus input and a component due to the signals common to both inputs.

Since amplification of the opposite input signals is much greater than that of common input signals the circuit provides a common-mode rejection as described by a numerical value called COMMON MODE REJECTION RATIO (CMRR).

Differential Input: When separate inputs are applied to the op-amp, the resulting difference signal is the difference between the two inputs. $\boxed{V_d = V_2 - V_1} = V_+ - V_-$

Common Input: When both input signals applied to an op-amp is common, signal element due to the two inputs can be defined as the average of the sum of the two signals. $\boxed{V_C = \left(\frac{V_1 + V_2}{2}\right)}$.

Output Voltage: Since any signal applied to op-amp in general have both in phase and out of phase components the resulting output can be expressed as $\boxed{V_0 = A_d V_d + A_c V_c}$.

Where V_d = difference voltage, V_C = common mode voltage,

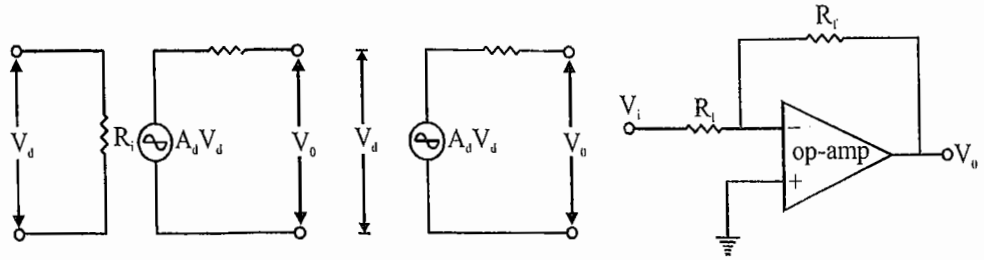
A_d = difference mode gain of the amplifier, A_c = Common mode gain of the amplifier.

CMRR {Common Mode Rejection Ratio}: $\boxed{CMRR = \frac{A_d}{A_c}}$

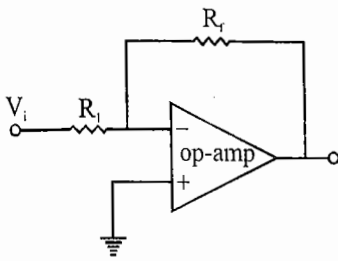
The value of CMRR can also be expressed in log term as

$$\boxed{CMRR(\text{in } d_B) = 20 \log_{10} \frac{A_d}{A_c}} (dB)$$

Equivalent Circuit: While an input to the minus (–) input results in on opposite polarity output. The ac equivalent circuit of the op-amp is shown in figure. As shown the input signal applied between input terminals sees as input impedance Ri typically very high. The output voltage is shown to be the amplifier gain times the input signal taken through output impedance R_0, which is typically very low. An ideal op-amp circuit, as shown in figure would have infinite input impedance zero output impedance and infinite voltage gain.



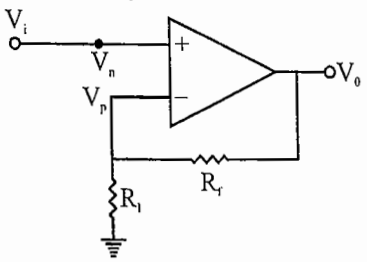
Inverting Amplifier: The most widely used constant gain amplifier circuit is the inverting amplifier.



. We can write $\boxed{V_0 = -\frac{R_f}{R_1} V_1}$

(–) sign represent 180° phase.

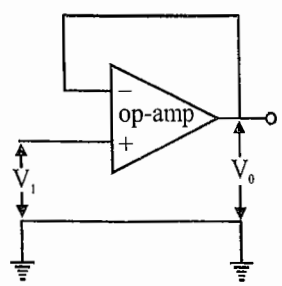
Non-inverting Amplifier: The connection of figures shows an op-amp that works as a non-inverting amplifier or constant gain multiplier. It should be noted that the inverting amplifier connection is more widely used because it has better frequency stability.



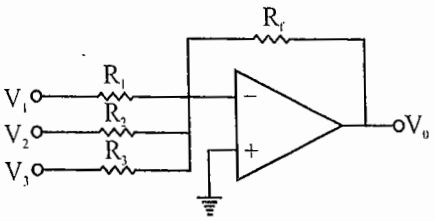
By virtual ground law: $V_n = V_p = V_i$

$$\Rightarrow V_i = \frac{R_1 V_0}{R_1 + R_f} \Rightarrow \frac{V_0}{V_i} = \frac{R_1 + R_f}{R_1} = 1 + \frac{R_f}{R_1} \Rightarrow \boxed{V_0 = \left(1 + \frac{R_f}{R_1}\right) V_i}$$

Voltage Follower or Unity Follower: The unity follower circuit as shown in figure provides a gain of unity (1) with number polarity or phase reversal. From the equivalent circuit, it is clear that $\boxed{V_0 = V_1}$ and that the output is the same polarity and magnitude as the input. The circuit operates like an emitter or source follower circuit except that the gain is exactly unity.



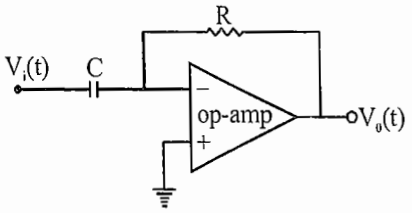
Summing Amplifier: Three input summing amplifier.



$$V_0 = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right)$$

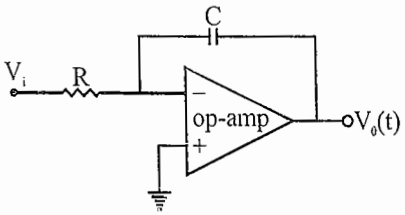
Differentiator : A differentiator circuit is shown in figure while not as useful as the circuit forms covered above the differentiator does provide a useful operation, the resulting far the circuit being

$$V_0(t) = -RC\frac{dV_1(t)}{dt}$$



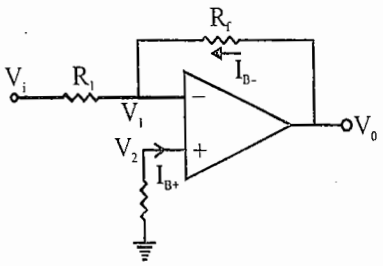
where the scale factor is –RC.

Integrator:



$$V_0(t) = -\frac{1}{RC}\int V_1(t)dt$$

Offset Currents and Voltages {d.c. characteristic of op-amp}:



(1) Input bias current : $\frac{i_B^+ + i_B^-}{2}$

(2) Input offset current: $I_{0s} = |I_B^+| - |I_B^-|$

(3) Input offset voltage : $V_{0s} = V_2 - V_1$

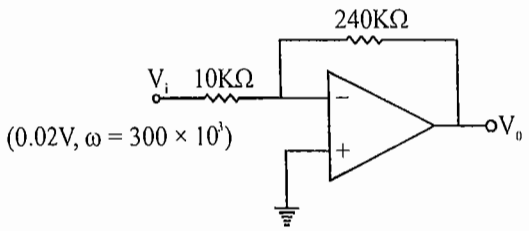
Note: Due to mismatching between V_1 and V_2 output voltage may be positive or negative so we apply offset voltage (V_{os}).

Slew Rate: Another parameter reflecting the op-amp's ability to handling varying signal is slew rate, defined as slew rate = maximum rate at which amplifier output can change in volts per micro second.

$$SR = \frac{\Delta V_0}{\Delta t} V/\mu s$$ with t in μs.

SOLVED PROBLEMS

1. Calculate the slew rate of given circuit.

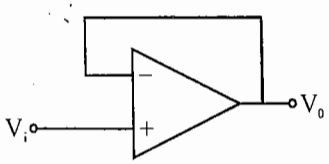


Soln. For a gain of magnitude $A_{CL} = \left|\frac{R_F}{R_1}\right| = \frac{240K\Omega}{10K\Omega} = 24$. The output voltage provides.

$K = A_{CL}$, $V_i = 24(0.2V) \Rightarrow 0.48V$

$$\omega \le \frac{SR}{K} = \frac{0.5v/\mu s}{0.48} = 1.1\times10^6 \text{ rad/sec}$$

Voltage Buffer: A voltage buffer circuit provides a means of isolation on input signal from a load by using a stage having unity gain with no phase or polarity inversion.



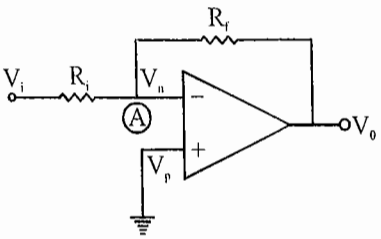
$$\boxed{V_0 = V_i}$$

Controlled Sources: Op-amp can be used to form various types of controlled sources. An input voltage can be used to control on output voltage or current or an input current can be used to control on output voltage or current. There type of connections are suitable far use in various instrument system (circuit). It has four types:

(1) Voltage Controlled Voltage Source
(2) Voltage Controlled Current Source
(3) Current Controlled Current Source
(4) Current Controlled Voltage Source

(1) Voltage Controlled Voltage Source: An ideal form of a voltage source whose output V_0 is controlled by on input voltage V_J is shown in figure. The output voltage is seen to be independent on the input voltage. This type of circuit can be built using an op-amp as shown in figure.

(i) Iuverting op-amp:

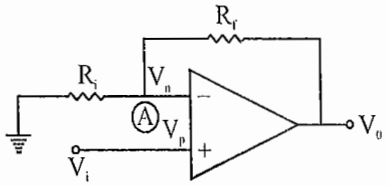


$$\boxed{K = -\frac{R_f}{R_i}}$$

By virtual ground condition $V_n = V_p = 0$

Now KCL at point A, $\frac{V_i - 0}{R_i} = \frac{0 - V_0}{R_f} \Rightarrow \boxed{\frac{V_0}{V_i} = -\left(\frac{R_f}{R_i}\right)}$

(ii) Non-inverting op-amp:



$$K = 1 + \frac{R_f}{R_i}$$

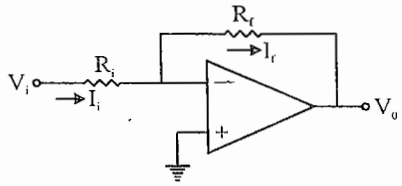
By virtual ground condition $V_p = V_n = V_i$

Now KCL at point A

$$\frac{O - V_i}{R_i} = \frac{V_i - V_o}{R_f} \Rightarrow \frac{V_0}{R_f} = \left(\frac{R_f + R_i}{R_f + R_i}\right) V_i \Rightarrow \boxed{\frac{V_0}{V_i} = 1 + \frac{R_f}{R_i}}$$

(2) Voltage Controlled Current Source: An ideal form of circuit providing an output current controlled by an input voltage is that of figure. The output current is dependent on the input voltage.

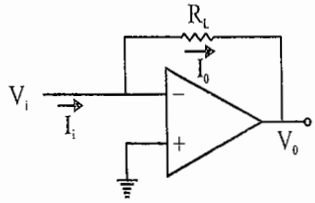
Practical Circuit:



$$I_i = \frac{V_i}{R_i}$$

(3) Current Controlled Voltage Source: An ideal form of a voltage source controlled by a input current is shown in figure. The output voltage is dependent on the input current.

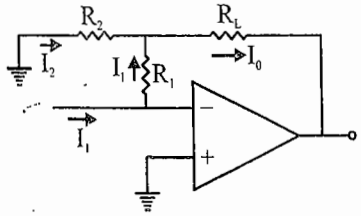
Practical Circuit:



$$V_0 = -I_i R_L$$

(4) Current Controlled Current Source: An ideal form of a circuit providing on output current dependent on an input current is shown in figure. In this type of circuit on output current is provided dependent on the input current.

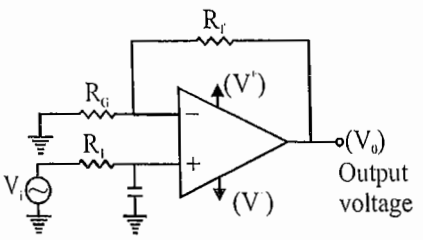
Practical Circuit:

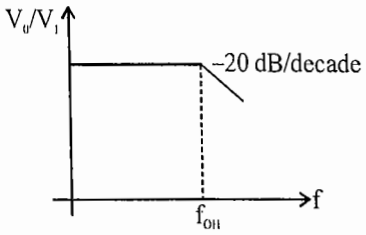


$$I_0 = I_1 + I_2 = I_1 + \frac{I_1 R_1}{R_2} = \left(1 + \frac{R_1}{R_2}\right) I_1 = K I_1$$

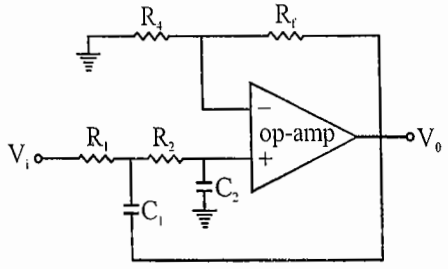
Low Pass Filter: A 1st order, low pass filter using resistor and capacitor as in figure shown has a practical slope of –20 dB per decade as shown in figure (rather them the ideal response of figure). The voltage gain below the cutoff frequency is constant at

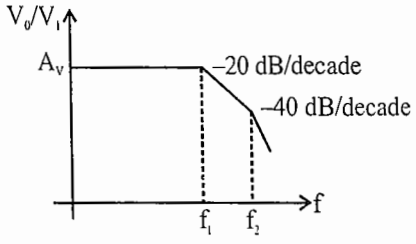
$\boxed{A_v = 1 + \frac{R_f}{R_G}}$, at a cut off frequency of $\boxed{f_{OH} = \frac{1}{2\pi R_1 C_1}}$





Second Order Filter: Connecting two sections of filter as in given figure result in a second order low pass filter with cut off at 40 dB decade closer to the ideal characteristic.

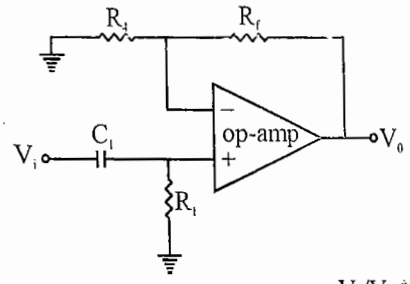


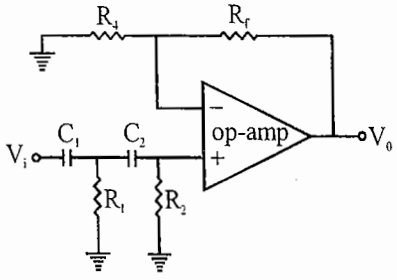


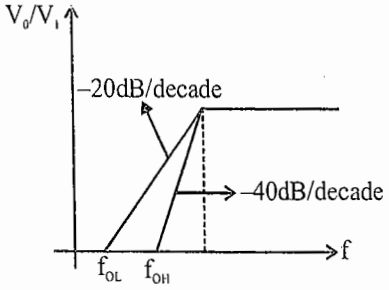
$\boxed{f_2 > f_1}$

High-Pass Active Filter: First and second order high-pass active filter can be built as shown in figure.

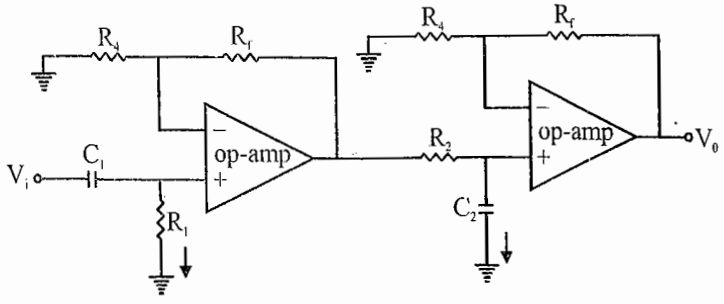
The amplifier cut off frequency is $\boxed{f_{OL} = \frac{1}{2\pi R_1 C_1}}$ with a second order filter $R_1 = R_2$ and $C_1 = C_2$ result is the same cut off frequency as in figure.

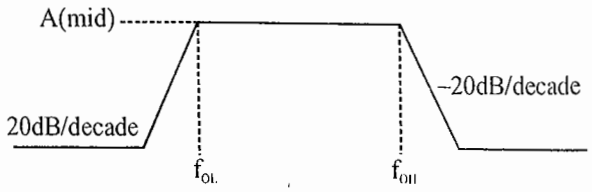




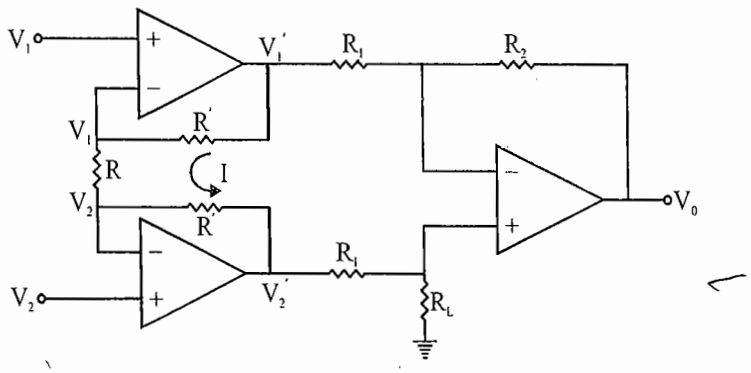


Band Pass Filter: Figure shows a band pass filter using two stages. The 1st a high pass filter and the second a low pass filter. The combined operation being the desired band pass response.





Instrument Amplifier:



Calculation of output voltage:

$$V_0 = \frac{R_2}{R_1}(V_2' - V_1') \qquad I = \frac{V_1 - V_2}{R} \qquad \text{... (1)}$$

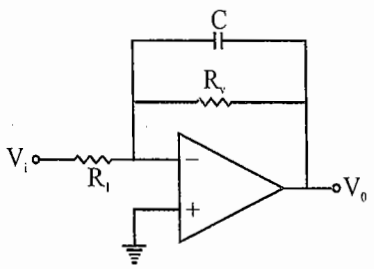
$$V_1' - V_1 = IR' \qquad \text{... (2)}$$

$$V_2 - V_2' = IR' \qquad \text{... (3)}$$

$$V_1' - V_2' = 2IR' + V_1 - V_2 \qquad I = \frac{V_1 - V_2}{R}$$

$$\Rightarrow V_1' - V_2' = \frac{(2R' + R)(V_1 - V_2)}{R} \quad \Rightarrow \boxed{V_0 = \left(1 + \frac{2R'}{R}\right)\left(\frac{R_2}{R_1}\right)(V_2 - V_1)}$$

2. An Active filter shown in figure. The DC gain and 3dB out off frequency are nearly.



$R_1 = 15.9K\Omega$, $R_2 = 159K\Omega$, C = 1nF

(a) 40dB, 3.14KHz (b) 40dB, 1KHz (c) 20dB, 628KHz (d) 20dB, 1KHz

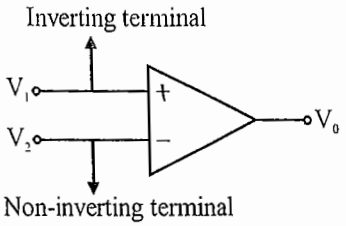
Soln: $\dfrac{V_{D(s)}}{V_{i(S)}} = \dfrac{-R_2/(1+R_2C_1S)}{R_1} = \dfrac{-R_2}{R_1(1+R_2C_1S)}$

$$A_V = -\frac{R_2}{R_1} = 10 = 20\log_{10}10 = 20dB \ \{\log_{10}10 = 1\}$$

At 3dB frequency $\left|\frac{V_{0(S)}}{V_{1(S)}}\right| = \frac{1}{\sqrt{2}}; \frac{1}{\sqrt{1+(R_2C_1\omega)^2}} = \frac{1}{\sqrt{2}}$ Since, DC gain $\boxed{\omega = 0}$

On putting the value of R_2, C_1 and comparing L.H.S. and R.H.S. ω = 1KHz

3. In the given op-amp find, the value of output voltage. Given $V_1 = 2\mu V$ d.c. and $V_2 = 4\mu V$ d.c., $A_{OL} = 2 \times 10^5$, $V_{CC} = \pm 15V$. **4.**



Soln: Let A_{OL} is open loop voltage gain. In this care $V_0 = (V_2 - V_1)A_{OL}$ **Soln.**

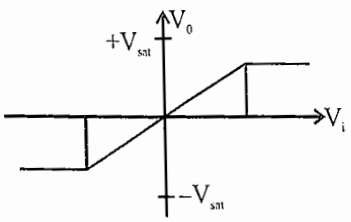
$\Rightarrow V_0 = (4.2) \times 2 \times 10^5 \times 10^{-6} \Rightarrow 4 \times 10^{-1} = 0.4V$

[V_{sat} → output will vary between + V_{sat} and $-V_{sat}$]

If $V_1 = -2\mu V$, $V_2 = \pm 4\mu V$

$V_0 = (4 + 2) \times 2 \times 10^5 \times 10^{-6} = 12 \times 10^{-1} = 1.2V$

For Ideal Op-amp (Open Loop): Input and output voltage characteristic of open loop Op-amp. **5.**

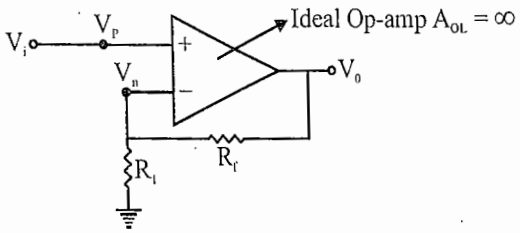


It is clear that open loop op-amp is able to amplify signals of very small amplitude. So, practically, open loop Op-amp is not used.

For Ideal Op-Amp (Open loop): **Soln.**

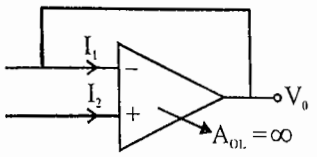
(i) $R_i = \infty$, (ii) $A_{OL} = \infty$, (iii) $R_0 = 0$, (iv) Slew rate = ∞ (v) CMRR = ∞

(vi) Band width = ∞



$$\Rightarrow V_0 = A_{OL}(V_p - V_n) \Rightarrow (V_p - V_n) = \frac{V_0}{A_{OL} \to \infty} \qquad \boxed{V_p = V_n}$$

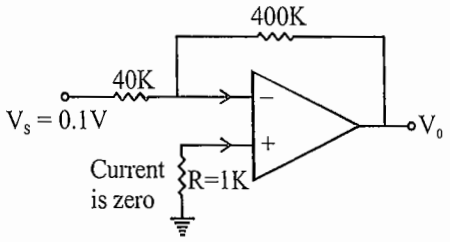
Concept of Virtual Ground:



$$V_1 - V_2 = \frac{V_0}{A_{OL} \to \infty (\text{ideal case})} = 0 \Rightarrow \boxed{V_1 = V_2}$$

In ideal case, $I_1 = I_2 = 0$

4. In the given op-amp circuit. Find the output voltage.

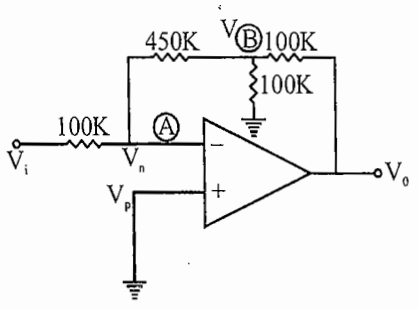


Soln. The given op-amp is inverting amplifier. By the inverting amplifier gain formula

$A = \frac{V_0}{V_i} = -\frac{R_f}{R_1}$. Given, R_f = 400K, R_1 = 40K, V_i = 0.1V

$$\Rightarrow V_0 = -\frac{400}{40} \times 0.1 = -1V$$

5. For the given op-amp circuit. Find voltage gain $\left(\frac{V_0}{V_i}\right)$.



Soln. Applying KCL at point A.

$$\frac{V_i - 0}{100} = \frac{0 - V}{450} \Rightarrow \frac{V_i}{V} = \frac{-100}{450} \Rightarrow V = -4.5V_i \qquad \text{(i)}$$

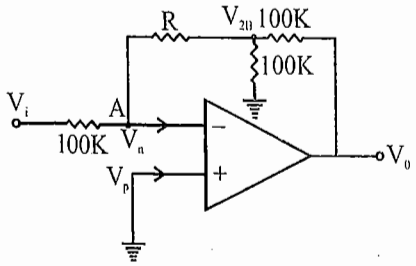
Now KCL at point B.

$$\frac{0 - V}{450} = \frac{V}{100} + \frac{V - V_0}{100} \qquad \text{(Now by equation (i) } V = -4.5\ V_i\text{)}$$

$$\Rightarrow \frac{+4.5V_i}{450} = \frac{-4.5V_i}{100} \frac{-4.5V_i - V_0}{100}$$

$$\text{On solving} \Rightarrow \frac{-V_0}{100} = \frac{4.5V_i}{450} + \frac{4.5V_i}{100} + \frac{4.5V_i}{100} \Rightarrow \frac{V_0}{V_i} = \frac{20}{9}$$

6. In the given figure of OP-amp. Find the value of resistance R. Given $\frac{V_0}{V_i} = -10$



Soln. By virtual ground condition $V_p = V_n = 0$

KCL at point A

$$\frac{V_i - 0}{100K} = \frac{0 - V_2}{R} \Rightarrow \frac{V_i}{100K} = \frac{-V_2}{R}$$

$$\Rightarrow V_2 = \frac{-R.V_i}{100K} \quad \text{... (i)}$$

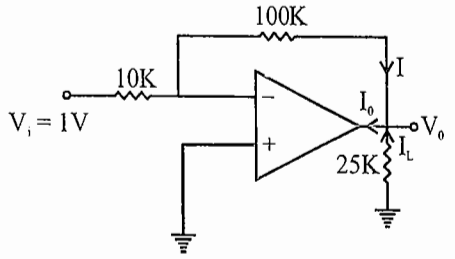
Now KCL at point B

$$\frac{0 - V_2}{R} = \frac{V_2 - V_0}{100K} + \frac{V_2}{100K} \quad \text{... (ii)}$$

$$\frac{V_0}{V_i} = -10 \text{ (Given)} \quad \text{... (A)}$$

By equation (i), (ii) and (A), R = $450K\Omega$

7. In the given circuit of op-amp. Find I_0 and I_L.



Soln. This is inverting amplifier $\frac{V_0}{V_i} = -\left(\frac{R_f}{R_i}\right) = -\left(\frac{100}{10}\right) = -10$

$V_0 = -10V$

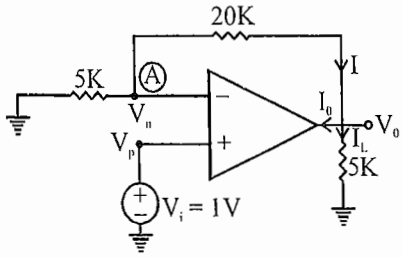
$\Rightarrow$ For current I_L $0 - (-10) = I_L \times 25K\Omega$

$\Rightarrow I_L = \frac{10}{25} = 0.4mA$ $\Rightarrow$ For current I,

$\Rightarrow$ $0 - (-10) = 100K \times I$ $\Rightarrow$ I = 0.1mA

$\Rightarrow$ $I_0 = I + I_L = 0.4 + 0.1 \Rightarrow 0.5$ mA

8. Based on Non-inverting amplifier.



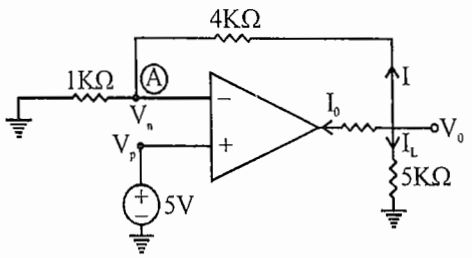
. From the above given op-amp. Find I_L and I_0?

Soln. By VGP, $V_n = V_p = 1V$. KCL at point A, $\frac{0-1}{5} = \frac{1-V_0}{20} \Rightarrow V_0 = 5V$

$I_L = 1mA = \frac{5}{5} = 1mA$, $I = \frac{1-5}{20} = -0.2mA$, $I_0 = I - I_L = -(1 + 0.2) = -(1.2)mA$

So, the current direction of I and I_0 will be reverse.

9. In the given figure of op-amp. Find the value of I_0 and I_L?



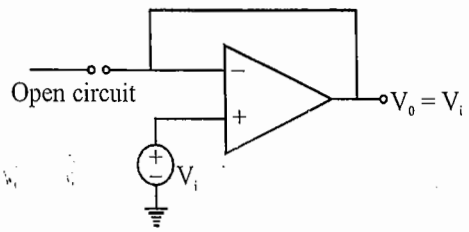
Soln. This is non-inverting amplifier. $V_p = V_n = 5V$ by VGP.

Now, KCL at point A,

$$\frac{0-5}{1K} = \frac{5-V_D}{4K} \Rightarrow V_D = 25V,\ I_L = \frac{25}{5K} = 5mA,\ I = \frac{5-25}{4K} = -\frac{20}{4} = -5mA$$

$$I_0 = I - I_L = -5 - 5 = -10mA$$

Voltage Follower: Means a unity gain non-inverting op-amp.



(a) $R_f = 0, R_1 = 0$ (b) $R_f = 0, R_1 = \infty$ (c) $R_f = 0$, any value of R_1

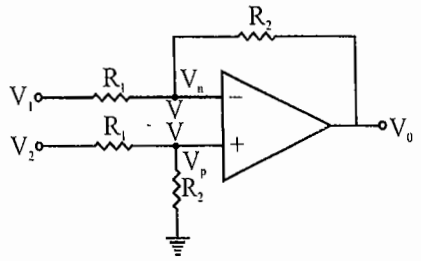
(d) $R_f = R_1$

For which value of R_f and R_1 it makes voltage follower.

Voltage Follower: $\begin{Bmatrix} R_{in} = \text{Very high} \\ R_{out} = \text{Very low} \end{Bmatrix}$

This resistance range is used for impedance matching or used as buffer.

Difference Amplifier:



In the above given op-amp figure. Find the value of output voltage in term of V_1 and V_2.

Soln. By the VGP condition $V_p = V_n = V$.

For the upper loop, $\frac{V_1 - V}{R_1} = \frac{V - V_0}{R_2}$ ... (i)

For the lower loop, $\frac{V_2 - V}{R_1} = -\frac{V}{R_2}$ ... (ii)

$$\Rightarrow \frac{V_2}{R_1} = V\left(\frac{1}{R_1} - \frac{1}{R_2}\right) \Rightarrow V\left(\frac{R_2 - R_1}{R_1 R_2}\right)$$

$$\Rightarrow V = \frac{V_2 . R_2}{(R_2 - R_1)} \quad \text{... (A)}$$

Now putting the value of equation (A) in equation (i)

$$\boxed{V_0 = \frac{R_2}{R_1}(V_2 - V_1)}$$

for ideal subtractor circuit CMRR is ∞

Super Position, Principle: Let V_1 be at ground, then $V_2 = \left(1 + \frac{R_2}{R_1}\right)V$

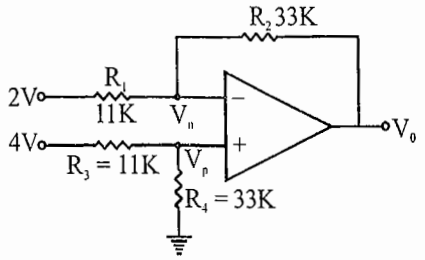
$$V = \frac{R_2 V_2}{R_1 + R_2} \quad \therefore V_{02} = \left(1 + \frac{R_2}{R_1}\right).\frac{R_2 V_2}{R_1 + R_2}$$

$$\Rightarrow V_{02} = \frac{(R_1 + R_2)}{R_1}.\frac{R_2 V_2}{(R_1 + R_2)}; \; V_{02} = \frac{R_2}{R_1} V_2$$

Now, when V_2 be at ground, then, $V_{01} = -\frac{R_2}{R_1} V_1; V_0 = V_{01} + V_{02}$

Total $\boxed{V_0 = \frac{R_2}{R_1}(V_2 - V_1)}$

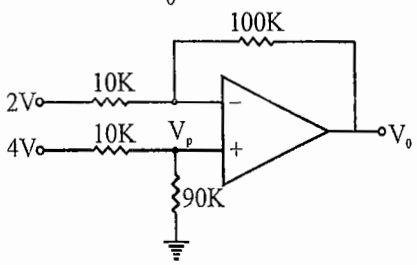
10. In the given op-amp circuit. Find the output voltage V_0?



Soln. $V_0 = 3(4 - 2)$, $V_0 = 6$ volt

Hence, $\frac{R_2}{R_1} = \frac{R_4}{R_3}$, then $V_0 = \frac{R_2}{R_1}(V_1 - V_2)$ or $V_0 = \frac{R_4}{R_3}(V_1 - V_2)$

11. In the given op-amp circuit. Find the value of V_0.

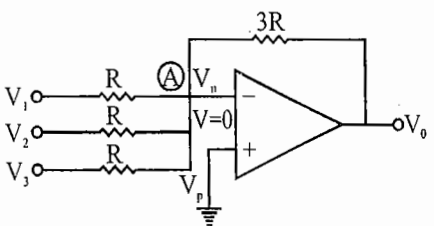


Soln. Firstly, considering first inverting loop, $V_{01} = -\frac{R_f}{R_1}V_i \Rightarrow \frac{-100}{10} \times 2 = -20V$

Now, considering non-inverting loop $V_P = \frac{4 \times 90}{90+10} \Rightarrow \frac{360}{100} \Rightarrow 3.6V$

$\Rightarrow V_{02} = \left(1 + \frac{100}{10}\right)3.6 \Rightarrow 39.6 \quad \therefore V_0 = (39.6 + (-20V)) \Rightarrow 19.6 Volt$

Adder:

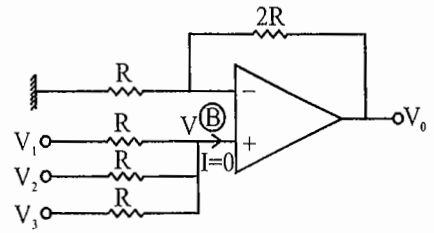


Soln: By VGP $\Rightarrow V_n = V_p = 0$

KCL at point A $\frac{V_1}{R} + \frac{V_2}{R} + \frac{V_3}{R} = \frac{0 - V_0}{3R} \Rightarrow \boxed{V_0 = -3(V_1 + V_2 + V_3)}$

So, the above op-amp is working as a inverting adder.

For the given op-amp circuit. Find the value of output voltage.

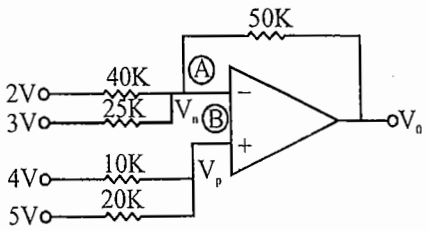


Soln. KCL at point B $\frac{V_1 - V}{R} + \frac{V_2 - V}{R} + \frac{V_3 - V}{R} = 0$ or $\boxed{V = \frac{1}{3}(V_1 + V_2 + V_3)}$

$\therefore V_0 = \left(1 + \frac{2R}{R}\right)V \Rightarrow V_0 = (1+2).\frac{1}{3}(V_1 + V_2 + V_3)$ $\boxed{V_0 = (V_1 + V_2 + V_3)}$

So, this is non-inverting adder.

12. In the given op-amp figure. Find the output voltage.



Soln. By VGP condition (Virtual Ground Position) ($V_p = V_n$)

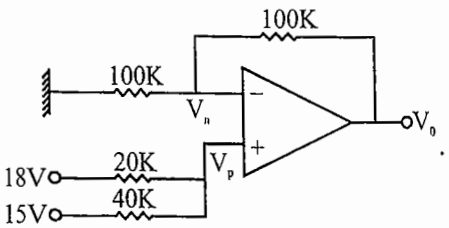
Let $V_p = V_p = V$.

Now, KCL at point B, $\frac{4 - V_p}{10} + \frac{5 - V_p}{20} = 0 \Rightarrow V_p = \frac{13}{3} Volt$

Now, KCL at point A, $\frac{2 - V_n}{40} + \frac{3 - V_n}{25} = \frac{V_n - V_0}{50}$, $\frac{2}{40} + \frac{3}{25} = \frac{V_n}{40} + \frac{V_n}{25} + \frac{V_n}{50} - \frac{V_0}{50}$

Now putting the value of V_n, $\frac{2}{40} + \frac{3}{25} = \frac{13}{120} + \frac{13}{75} + \frac{13}{150} - \frac{V_0}{50} \Rightarrow V_0 = 9.9V$ $\because V_n = V_p$

13.



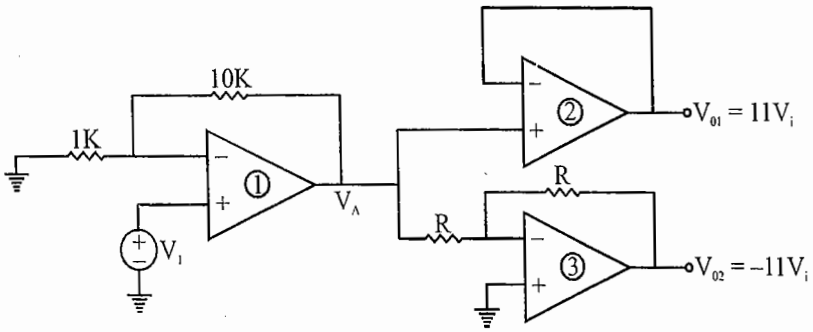
In the above given op-amp circuit, find output voltage.

Soln. $V_p = V_n = V$ (By VGP)

KCL at positive terminal, $\frac{18 - V}{20} + \frac{15 - V}{40} = 0 \Rightarrow V = \frac{41}{3} Volt$.

KCL at positive terminal, $\Rightarrow \frac{0 - \frac{41}{3}}{100K} = \frac{\frac{41}{3} - V_0}{100} \Rightarrow V_0 = \frac{82}{3} Volt$

14. For the given op-amp circuits. Find $\frac{V_{01}}{V_{02}}$.



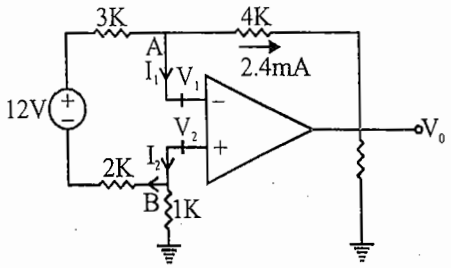
Soln. For the op-amp ... (1), this is non-inverting amplifier.

$V_A = \left(1+\frac{10}{1}\right)V_i = 11V_i$ $\Rightarrow$ Op-amp (2) is working like buffer, $V_{01} = 11V_i$

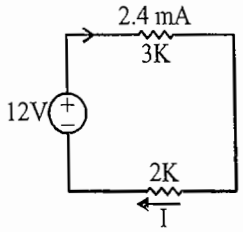
$\Rightarrow$ Op-amp (3) is working like inverting amplifier, $V_{02} = \frac{-R}{R}11V_i = -11V_i$

$\Rightarrow \frac{V_{01}}{V_{02}} = -\frac{11V_i}{11V_i} = -1$

15. In the given op-amp circuit find output voltage.



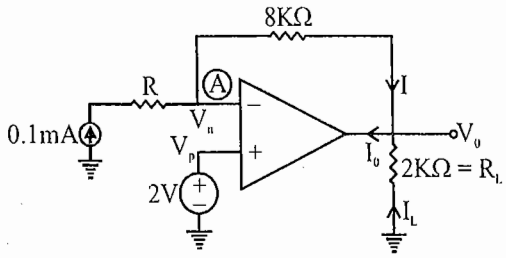
Soln. Because $I_1 = I_2 \Rightarrow V_1 - V_2 = 0$



$I = \frac{12}{5} = 2.4mA; V_B = 0 - 2.4\times 1 = -2.4V$, $V_A = -2.4V$;

$\Rightarrow \frac{-2.4 - V_0}{4} = 2.4 \Rightarrow \boxed{V_0 = -12.0V}$

16. In the given op-amp circuit find V_0 and I_0.

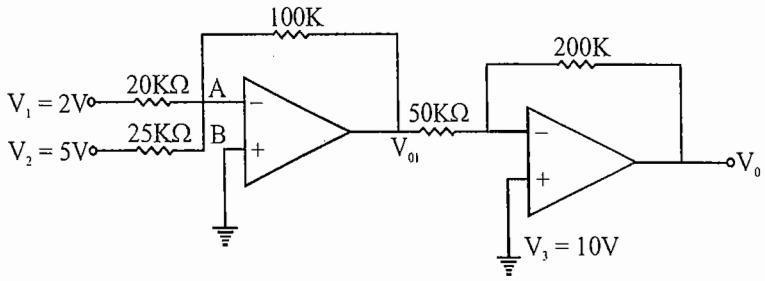


Soln: By VGP $\rightarrow$ $V_n = V_p = 2V$

Now, KCL at point A

$$0.1 = \frac{2-V_0}{8} \Rightarrow V_0 = -2.8Volt\,,\ I_L = \frac{2.8}{R_L} = 1.4mA\,,\ I_0 = 1.4 + 0.1 = 1.5\text{mA}$$

17. In the given op-amp figure. Find the output voltage.

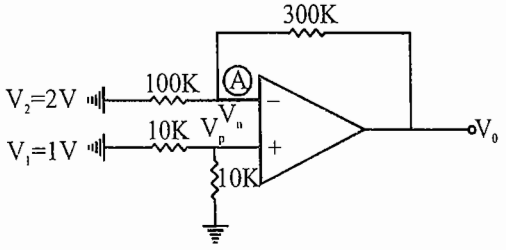


Soln. By VGP, $V_B = V_A = 0$, Now, KCL at point A, $\frac{2}{20} + \frac{5}{25} = \frac{0-V_0}{100} \Rightarrow V_{01} = -30Volt$

Now, KCL at second OP-amplifier $\frac{10-(-30)}{50} = \frac{V_0-10}{200}\,;\frac{40}{50} = \frac{V_0-10}{200}$

$\therefore V_0 = 1T_0\,Volt$

18. In the given Op-amp circuit. Find V_0?



Soln. $V_p = \frac{10\times1}{10+10} = 0.5V$, By VGP condition, $V_n = V_p = 0.5V$

Now, KCL at point A, $\Rightarrow \frac{2-0.5}{150} = \frac{0.5-V_0}{300} \Rightarrow V_0 = -2.5Volt$

19.

Soln.

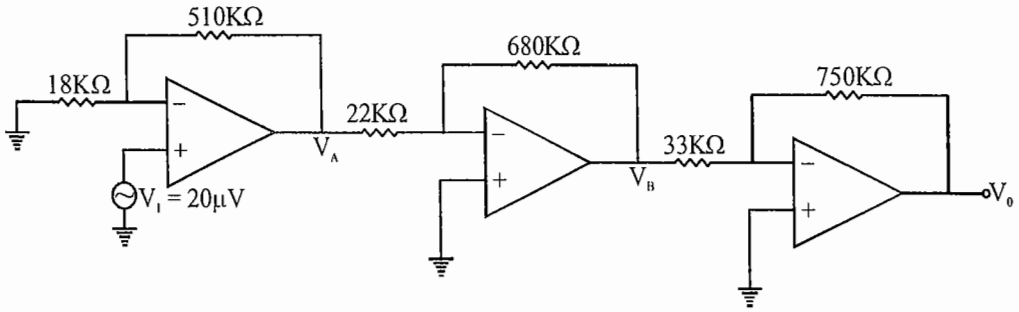
20.

Soln.

21.

Soln.

19. In the given Op-amp circuit. Find output voltage.

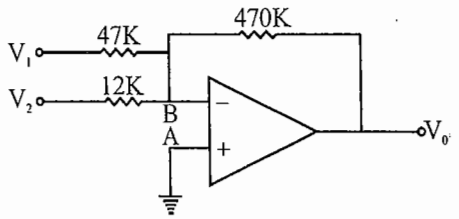


Soln. We will 1st calculate V_A, $\frac{20\times10^{-6}-0}{18}=\frac{V_A-20\times10^{-6}}{510}$

$$\Rightarrow 20\times10^{-6}\left[\frac{1}{18}+\frac{1}{510}\right]=\frac{V_A}{510};V_A=\frac{528}{18}\times20\times10^{-6},\ V_A=5.86\times10^{-4}Volt$$

Similarly on solving, $V_B=\frac{-680}{22}\times5.86\times10^{-4}V$, $V_B=-0.081Volt$, $V_0 = 0.409$ Volt

20. Calculate the output voltage for the circuit with input $V_1 = 40mV$, $V_2 = 20mV$.

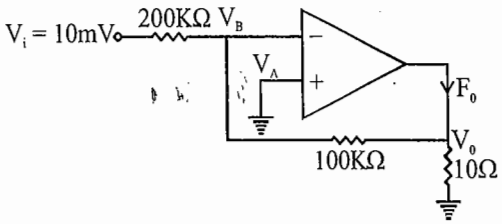


Soln. $V_A = V_B = 0$, Now applying KCL in inverting loop

$$\frac{V_1-0}{47}+\frac{V_2-0}{12}=\frac{0-V_0}{470},\ \Rightarrow\frac{40}{47}+\frac{20}{12}=-\frac{V0}{470}\Rightarrow V_0=\frac{-(40\times12+20\times47)\times470}{47\times12}$$

$$\Rightarrow\therefore V_0=\frac{-(480+940)\times5}{6}=\frac{7100}{6}=-1183.93mV\ \Rightarrow V_0=-1.183Volt$$

21. Calculate the output current I_0 in the given circuit.



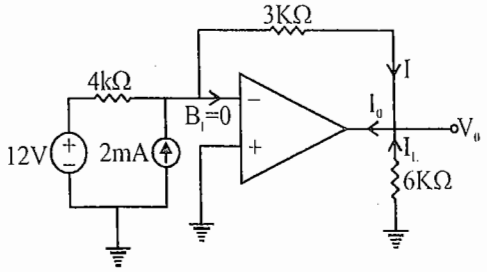
Soln. Potential at A and B points are equal by VGP. i.e. $V_A = V_B = 0$

Now applying KCL in inverting loop

$$\frac{V_i-0}{200}=\frac{0-V_0}{100K}\Rightarrow V_0=\frac{10\times100\times10^{-3}\times10^3}{200}V_0\Rightarrow 5V$$

Now, $I_0=\frac{5}{10}+\frac{5}{100k\Omega}=0.5+0.00005\simeq0.5A$

22. In the given Op-amp circuit. Find I_0 and V_0?

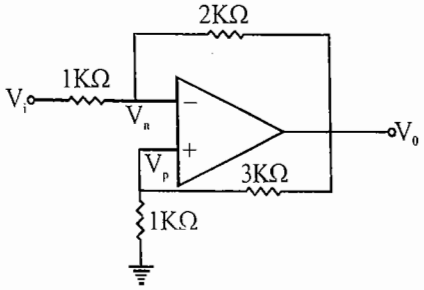


Soln. Applying KCL at point B, $2\times10^{-3}+\frac{12}{4K}=\frac{0-V_0}{3K}$

$$\Rightarrow 2\times10^{-3}+3\times10^{-3}=\frac{-V_0}{3K}\Rightarrow V_0=-(15Volt)$$

$$I_L=\frac{V_0}{6}=2.5m\,Amp,\quad I=\frac{0+15}{3K}=5mA,\quad I_0=I+I_L\Rightarrow 7.5mA$$

23. In the given circuit find voltage gain $\frac{V_0}{V_i}$.

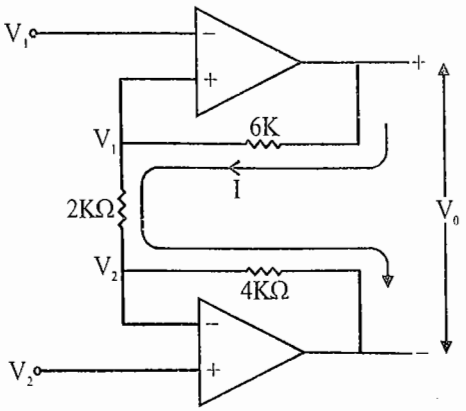


Soln. In the non-inverting loop applying KCL let $V_p = V_n = V$

In the $\frac{0-V}{1}=\frac{V-V_0}{3}\Rightarrow V_0=4V,\boxed{V=\frac{V_0}{4}}$.

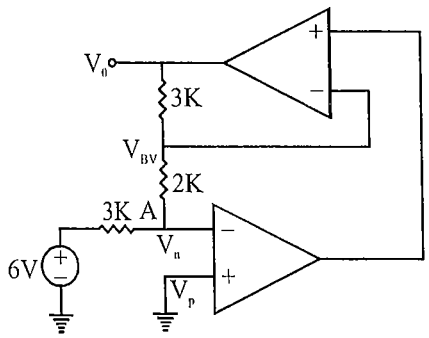
In the inverting loop applying KCL, $\frac{V_i-V}{1}=\frac{V-V_0}{2}\Rightarrow V_i-\frac{V_0}{4}=\frac{\frac{V_0}{4}-V_0}{2}\Rightarrow\boxed{\frac{V_0}{V_i}=-8}$

24. In the given circuit. Find $\frac{V_0}{V_1-V_2}$?



Soln. $V_0=6I+2I+4I=12I;\ V_1-V_2=2I\quad\therefore\frac{V_0}{V_1-V_2}=\frac{12I}{2I}=6$

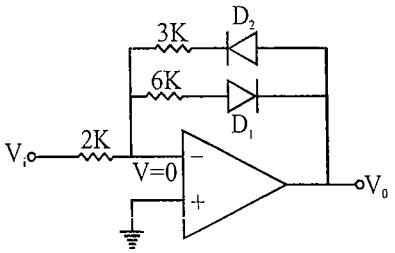
25. In the given circuit find V_0?



Soln. $V_n = V_p = 0\{VGP\}$, Now, KCL at point A, $\frac{6-0}{3} = \frac{0-V_B}{2} \Rightarrow V_B = -4V$

Now, KCL at point B, $\frac{0-V_B}{2} = \frac{V_B - V_0}{3} \Rightarrow \because V_B = -4V$, $\frac{4}{2} = \frac{-4-V_0}{3} \Rightarrow \boxed{V_0 = -10V}$

26. In the circuit calculate the output voltage V_0?



(i) If $V_i = 3V$, then V_0? (ii) If $V_i = -3V$, then V_0?

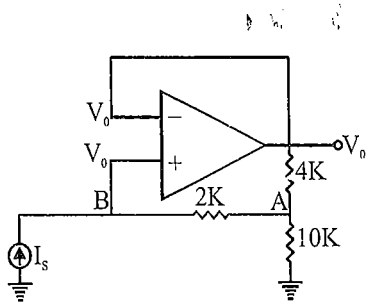
Soln. (i) When $V_i = 3V$, diode D_1 will on, Now KCL in D_1 loop

$$\frac{3-0}{2} = \frac{0-V_0}{6} \Rightarrow V_0 = -9Volt$$

(ii) When $V_i = -3V$, diode D_2 will on, Now, KCL in D_2 loop

$$\frac{V_i - 0}{2} = \frac{0-V_0}{3} \Rightarrow -\frac{3}{2} = -\frac{V_0}{3} \Rightarrow V_0 = 4.5Volt$$

27. In the given circuit calculate $\frac{V_0}{I_S}$.



Now, KCL at point A.

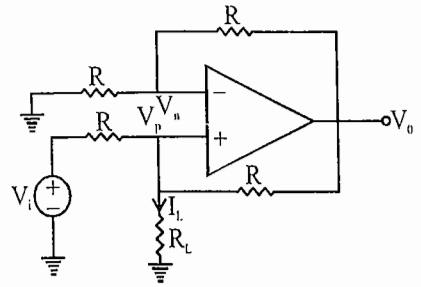
$$\frac{V-V_0}{4} + \frac{V-V_0}{2} + \frac{V}{10} = 0 \Rightarrow 5(V-V_0) + 10(V-V_0) + 2V = 0$$

$$\Rightarrow 5V - 5V_0 + 10V - 10V_0 + 2V = 0 \Rightarrow 17V = 15V_0 \Rightarrow V = \frac{15V_0}{17}$$

Now, KCL at point A

$$\frac{V_0 - V}{2} + (-I_S) = 0 \Rightarrow V_0 - V - 2I_S = 0 \Rightarrow V_0 - \frac{15V_0}{17} = 2I_S \Rightarrow \frac{2V_0}{17} = 2I_S \Rightarrow \frac{V_0}{I_S} = 17$$

28. In the given circuit find value of I_L.



Soln. By VGP, $V_n = V_p = V$. Firstly, KCL in non-inverting terminal

$$\frac{V_i - V}{R} = I_L + \frac{V - V_0}{R} \quad \text{... (i)}$$

Similarly, KCL in inverting terminal

$$\frac{0 - V}{R} = \frac{V - V_0}{R} \Rightarrow V_0 = 2V \Rightarrow V = \frac{V_0}{2} \quad \text{... (ii)}$$

Now, putting value of (ii) in equation (i)

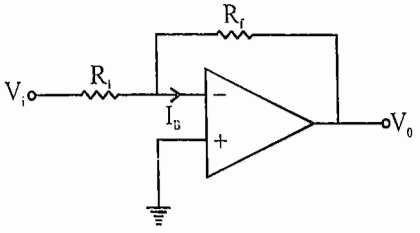
$$\frac{V_i - \frac{V_0}{2}}{R} = I_L + \frac{\frac{V_0}{2} - V_0}{R}, \; V_i - \frac{V_0}{2} = I_L R + \frac{V_0}{2} - V_0 \Rightarrow \boxed{I_L = \frac{V_i}{R}}$$

DC Characteristic of Op-amp:

(i) Input bias current (For DC analysis)

(ii) Input offset current

(iii) Input offset voltage



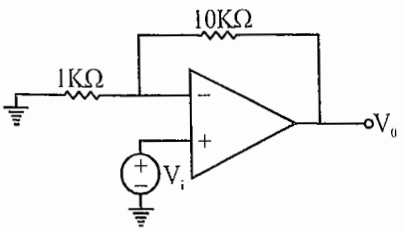
(i) Input bias current $= \frac{|I_B^+| + |I_B^-|}{2}$. Let $|I_B^+| = |I_B^-|$, $0 - V_0 = |I_B^-| R_f$; $\boxed{V_0 = |I_B^-| R_f}$

To compensate effect of input bias current R_{comp} is used. $\therefore \boxed{R_{comp} = R_1 \| R_f}$

(ii) Input offset current; $I_{OS} = |I_B^+| - |I_B^-|$, $V_0 = R_f I_{OS} \rightarrow$ output if $V_i = 0$, due to input offset current.

(iii) Input offset voltage; $V_{OS} = V_1 - V_2$, output to input offset; $V_0 = \left(1 + \frac{R_f}{R_1}\right) V_{OS}$.

29.



Calculate I_L, Given V_{OS} = 10mV, $|I_B^-|$ = 300nA, I_{OS} = 100pA.

Find (a) Calculate maximum output voltage due to V_{OS} and I_B^-. (b) Calculate R comperate.

(c) Calculate output voltage if R_{comp} is connected.

Soln. (i) If we are considering input bias current then $I_{OS} = 0$, as we have already assumed $|I_B^+| = |I_B^-|$.

(ii) If R_{comp} is connected, then input bias current will not considered, only I_{OS} will be considered.

If R_{comp} is connects then for zero input = zero output.

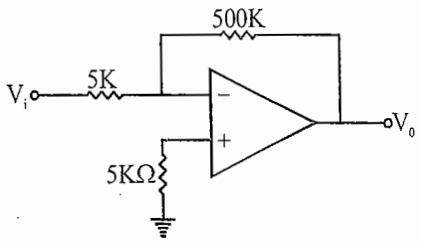
(a) $V_0 = \left(1+\frac{R_f}{R_1}\right).V_{OS} + R_f.I_B^- = \left(1+\frac{10}{1}\right).10 + 10.300nA = 110 + 3mV = 113mV$

(b) $R_{comp} = R_1 \,||\, Rf = \frac{10}{11}K\Omega$

(c) $V_0 = \left(1+\frac{R_f}{R_1}\right).V_{OS} + R_f I_{OS} = \left(1+\frac{10}{1}\right)\times 10mV + 10K\times 100\,pA$

$= 110mV + 0.001mV = 110.001mV$

30. If input offset voltage = 4mV, input offset current = 150nA, input bias current = 300nA.



Soln. $V_0 = \left(1+\frac{R_f}{R_1}\right)V_{OS} + R_f.I_{OS} = \left(1+\frac{500}{5}\right).4mV + 500K\times 150nA = 101 \times 4 + 75$

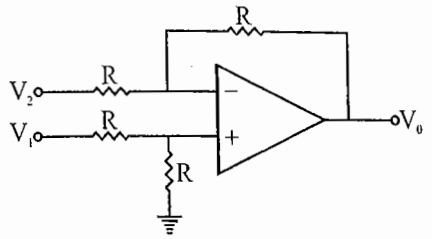
$= 404 + 75 = 479$mvolt.

Calculation of CMRR

$\boxed{CMRR = \frac{A_d}{A_C}}$ A_d = differential mode gain, A_C = Common mode gain

$\boxed{V_0 = A_d V_d + A_C V_C}$ $V_d = V_1 - V_2$, $V_C = \frac{V_1+V_2}{2}$, $A_d = \left.\frac{V_0}{V_d}\right|_{V_C=0}$, $A_C = \left.\frac{V_0}{V_C}\right|_{Vd=0}$

31. In the given circuit. Find the value of CMRR?



Soln. $V_0 = \frac{R}{R}(V_1 - V_2)$, $V_0 = (V_1 - V_2)$ $\therefore V_d = V_1 - V_2, \Rightarrow A_d = 1$

For A_C, $V_1 = V_2 . \Rightarrow A_C = 0$ $\therefore CMRR = \frac{1}{0} = \infty$

32. In the op-amp circuit, CMRR = 40dB and A_d = 50dB. Find A_C.

Soln. Here, CMRR = Common Mode Rejection Ratio

A_d = Difference Mode gain, A_C = Common Mode gain

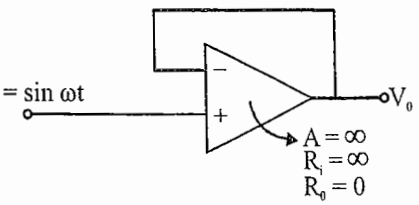
CMRR and A_d are given in dB. First off all we will change it in normal value.

40dB = 20 $\log_{10}$ CMRR

$\Rightarrow$ CMRR = $(10)\frac{40}{20} = 10^2 = 100$ $\Rightarrow$ 50dB = 20$\log_{10}$ A_d

$\Rightarrow$ $A_d = 10^{2.5} = 316.22$ $\Rightarrow$ CMRR = $\frac{A_d}{A_C}$ $\Rightarrow$ $A_C = \frac{A_d}{CMRR} \Rightarrow \frac{316.27}{100}$

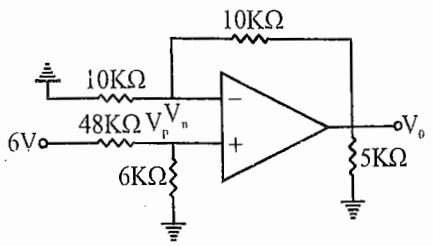
$A_C = 3.16$

Slew Rate: 

33. What is the maximum value of input voltage given to an voltage follower so, that there is no distortion (Slew rate is given).

Soln: $V_0 = V_m \sin \omega t$, Slew Rate = $Vm.\omega \cos \omega t$, S.R. = $Vm.\omega$ $\therefore V_m = \frac{S.R}{2\pi f}$

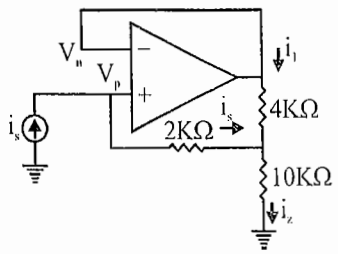
34. For the circuit shown below the value of V_0 is



(a) $\frac{4}{3}$V (b) $-\frac{2}{3}$V (c) $\frac{2}{3}$V (d) $-\frac{4}{3}$V

Soln. $V_p = \frac{6\times 6}{48+6} = \frac{2}{3}V$, $V_0 = \left(1+\frac{R_f}{R_1}\right)V_p = \left(1+\frac{10}{10}\right).\frac{2}{3} = (2)\times\frac{2}{3} = \frac{4}{3}$

35. For the circuit shown below the input resistance is

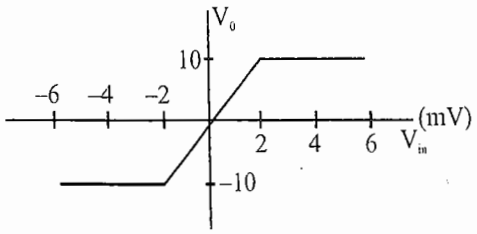


(a) $38K\Omega$ (b) $17K\Omega$ (c) $25K\Omega$ (d) $47K\Omega$

Soln. Since op-amp is ideal, $V_n = V_p, 2k\,i_s = 4k\,i_1 \Rightarrow i_s = 2i_1, V_s = 2k\,i_s + 10k\,i_2, i_2 = i_s + i_1$

$$V_s = 2k\,i_s + 10k(i_s + i_1) \because i_1 = \frac{i_s}{2} \Rightarrow V_s = 2k\,i_s + 10k\left(i_s + \frac{i_s}{2}\right) \Rightarrow \frac{V_s}{i_s} = 17K = R_{in}$$

36. The voltage transfer characteristic of an operation amplifier is shown in figure. What are the values of gain and offset voltage for this op-amp.



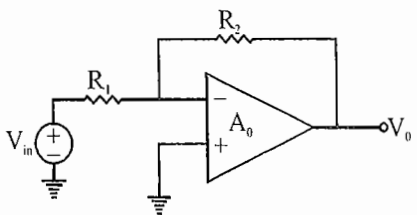
(a) 10, 1mV (b) 7500, –1mV (c) 20, 2mV (d) 7500, –2mV

Soln. $V_0 = A_V(V_{in} + V_{OS})$, $V_{OS} \rightarrow$ Offset Voltage, $A_V \rightarrow$ Voltage Gain

$$A_V = \frac{dV_0}{dV_{in}} = \frac{10-(-5)}{(2-0)mV} = 7500$$, When $V_0 = 0$, $V_{in} = -V_{OS}$

Offset voltage is $V_{OS} = -V_{in} / V_0 = 0 = -1mV$

37. An inverting operational amplifier shown in figure has an open gain of 1000 and closed loop gain of 4, gain error is

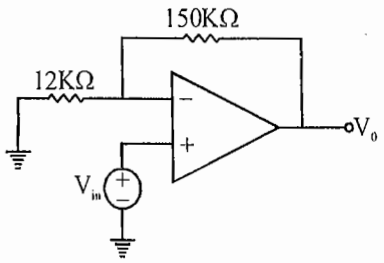


(a) 0.4% (b) 0.5% (c) 2.5% (d) 2%

Soln. Gain error is given as $\Delta g = \frac{1}{A_0}\left(1+\frac{R_2}{R_1}\right)$, $A_0 = 1000$ (Open loop gain)

$\frac{R_2}{R_1} = 4$ (Closed loop gain), $\Delta g = \frac{1}{1000}(1+4) = 0.5\%$

38. In the following non-inverting amplifier. The op-amp has an open loop gain of 86dB, gain error is



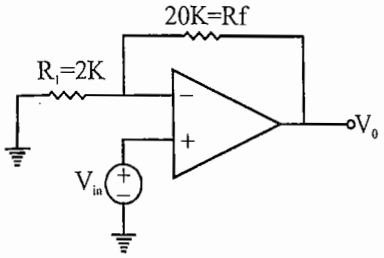
(a) 0.0125% (b) 0.13% (c) 0.930% (d) 0.0675%

Soln. Gain error for non-inverting amplifier is given by $\Delta g = \frac{1}{A_0}\left(1+\frac{R_2}{R_1}\right)$

where $A_0 \rightarrow$ open loop gain $20\log_{10} A_0 = 86$(given) $A_0 \simeq 20,000$, $R_2 = 150K\Omega$, $R_1 = 12K\Omega$

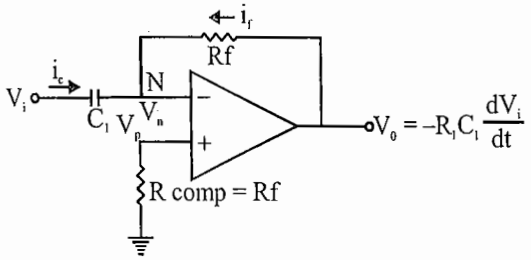
So, gain error is $\Delta g = \frac{1}{20,000}\left(1+\frac{150}{2}\right) = 6.75\times10^{-4}$ or $\Delta g = 0.0675\%$

39. Op-Amp of a given figure has open loop gain of 45. What is closed loop gain of an op-amp.



Soln. For non-inverting $A_{CL} = \frac{\left(1+\frac{R_f}{R_1}\right)}{1+\frac{\left(1+\frac{R_f}{R_1}\right)}{A_{OL}}} \Rightarrow \frac{\left(1+\frac{20}{2}\right)}{1+\frac{\left(1+\frac{20}{2}\right)}{45}} = \frac{11}{1+\frac{11}{45}} = \frac{4\times11}{56} \Rightarrow 8.95$

Differentiator:



By VGP, $V_p = V_n = 0$, Now, KCL at point N, $i_C = C_1\frac{d}{dt}(V_i - V_N) = C_1\frac{dV_i}{dt}$, this is far capacitor current.

For feedback resistor Rf. $i_f = \frac{V_0}{R_f} \Rightarrow C_1\frac{dV_i}{dt} + \frac{V_0}{R_f} = 0 \Rightarrow \boxed{V_0 = -RfC_1\frac{dV_i}{dt}}$

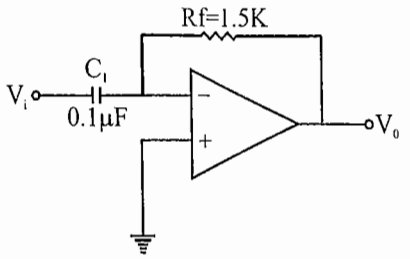
We may now write the magnitude of gain A of the differentiator as,

$|A| = \left|\frac{V_0}{V_i}\right| = |-J\omega RfC_1| = \omega RfC_1$ or $|A| = \frac{f}{f_a}$ where $\boxed{f_a = \frac{1}{2\pi RfC_1}}$

40.

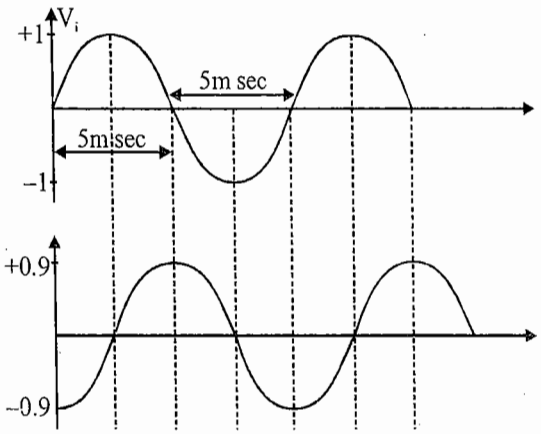
Soln.

40. In the given differentiator, if $V_i = \sin(2\pi \times 10^2 t)$. Draw wave form of V_0.

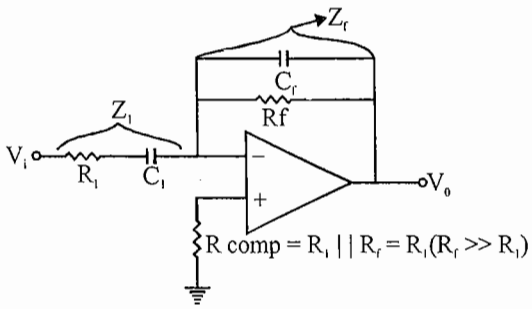


Soln. $V_0 = -CR_f \frac{dV_i}{dt}$, $V_0 = -0.1\times10^{-6}\times1.5\times10^3.\cos(2\pi\times10^2 t).2\pi\times10^2$

$V_0 = -3\pi\times10^{-2}\cos(2\pi\times10^2 t) = -0.09\cos(2\pi\times10^2 t)$



Practical Differentiator:

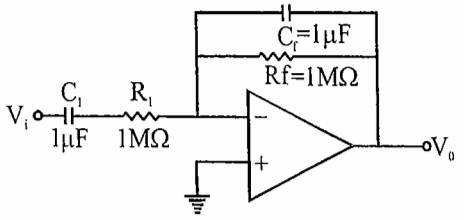


This is inverting op-amp: $\frac{V_{0(s)}}{V_{i(s)}} = -\frac{Z_f}{Z_i} = -\frac{SR_fC_1}{(1+SRf(f)(1+SC_1R_1)}$

For $R_fC_f = R_1C_1$, we get $\frac{V_{0(S)}}{V_{i(S)}} = -\frac{SR_fC_1}{(1+SR_1C_1)^2} = -\frac{SR_fC_1}{\left(1+j\frac{f}{f_b}\right)^2}$

Where, $\boxed{f_b = \frac{1}{2\pi R_1C_1}}$

41. In the given practical differentiator circuit. Find output voltage. If $V_i = \sin t$

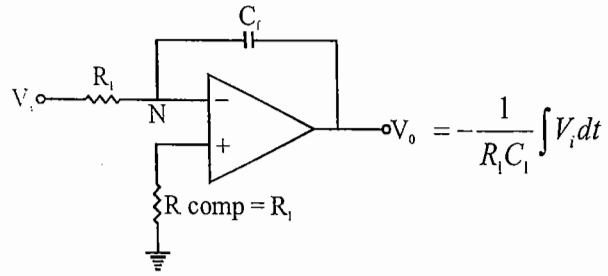


Soln. $\frac{V_{0(s)}}{V_{i(S)}} = \frac{-SRfC_f}{(1+SR_1C_1)^2} \Rightarrow \frac{V_{0(S)}}{V_{i(S)}} = \frac{-S}{(1+S)^2}, S = J\omega, S^2 = -\omega^2 = -1$

$\left|\frac{V_{0(S)}}{V_{i(S)}}\right| = \frac{1}{(1+S^2+2S)} = \frac{1}{1-1+2j} = \frac{-j}{2} \quad \therefore V_0 = \frac{1}{2}\sin(t-90°) \Rightarrow V_0 = -\frac{1}{2}\cos t$

42.

Integrator:



$V_0 = -\frac{1}{R_1C_1}\int V_i dt$

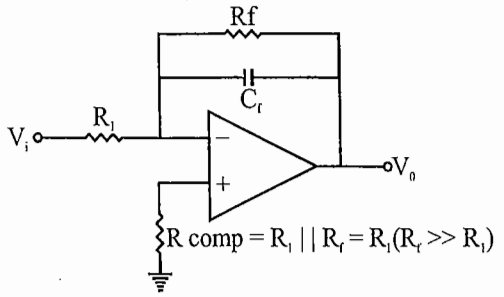
Soln.

By KCL at node, N, $\frac{V_i}{R_1} + C_f\frac{dV_0}{dt} = 0 \Rightarrow \frac{dV_0}{dt} = -\frac{1}{R_1C_f}V_i$

43.

Integrating both sides, we get, $\int_0^t dV_0 = -\frac{1}{R_1C_f}\int_0^t V_i dt \Rightarrow \boxed{V_0 = -\frac{1}{R_fC_f}\int_0^t v_i dt}$

Practical Integrator Circuit: (Lossy Integration)



Soln.

44.

Soln.

45.

The nodal equation at the inverting input terminal of the op-amp $\frac{V_{i(S)}}{R_1} + SC_fV_{0(S)} + \frac{V_{0(S)}}{R_f} = 0.$

For which we have, $V_{0(S)} = -\frac{1}{SR_1C_f + R_1/R_f}V_{i(S)}$ or $\boxed{\frac{V_{0(S)}}{V_{i(S)}} = \frac{-\frac{R_f}{R_1}}{1+SC_fR_f}}$

If R_f is large, the lossy integrator application the ideal integrator.

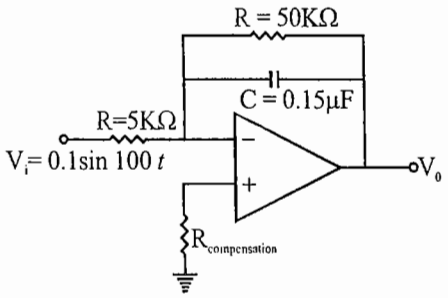
$$|A| = \left|\frac{V_0}{V_i}\right| = \frac{1}{\sqrt{\omega^2 R_1^2 C_f^2 + R_1^2 / R_f^2}} = \frac{R_f / R_1}{\sqrt{1+(\omega R_f C_f)^2}}$$

The break frequency $(f = f_a)$ at which the gain is 0.707 (R_f / R_1) (or – 3dB below its value of R_f/R_1).

$$\sqrt{1+(\omega R_f C_f)^2} = \sqrt{2}$$

Solving for $f = f_a$, we get $\boxed{f_a = \frac{1}{2\pi R_f C_f}}$

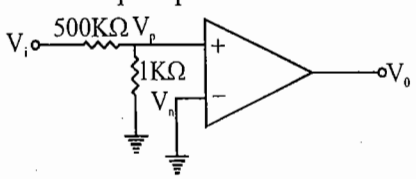
42. In the integrator circuit, find the value of output voltage?



Soln. $\frac{V_{0(S)}}{V_{i(S)}} = \frac{-R_f / R_1}{1+SR_fC_f} = \frac{-10}{1+j\times100\times50\times0.15\times10^{-6}} = \frac{-10}{1+0.75J}$

$V_{0(S)} = 0.8\sin(100t+\phi)$, where $\phi = 143.14$, $V_m = 0.8$

43. For the circuit shown below the output voltage V_0 is 2.5 V_g in response with to input voltage V_i = 5V. the finite open loop differential gain of the op-amp.



(a) 5×10^4 (b) 250.5 (c) 2×10^4 (d) 501

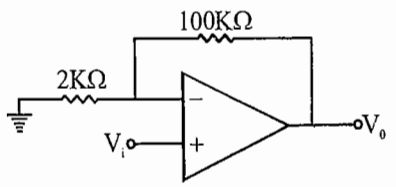
Soln. $V_p = \frac{V_i \times 1}{500+1}$, $V_0 = \frac{A_{od}V_i}{501} \Rightarrow (2.5)(501) = A_{od(S)} \Rightarrow A_{od} = 250.5$

44. If open loop gain is A_{od} = 999, then closed loop gain is

(a) –0.999 (b) 0.999 (c) 1.001 (d) –1.001

Soln. $A_{od}(V_i - V_0) = V_0, A_{od} = 999, \frac{V_0}{V_i} = \frac{A_{od}}{1+A_{od}} = \frac{999}{1+999} = 0.999$

45. The op-amp shown below has a very poor open-loop voltage gain of 45 but is otherwise ideal. The closed-loop gain of amplifier is



(a) 20 (b) 4.5 (c) 4 (d) 5

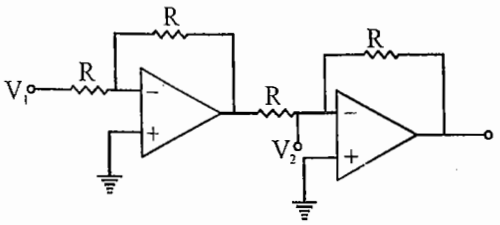
Soln. A closed loop gain $A_{CL} = \frac{V_0}{V_i} = \frac{A_{od}}{1 + A_{od}\beta}$, $\beta = \frac{2K}{8K + 2K} = 0.2$,

$$A_{CL} = \frac{45}{1 + (45)(0.2)} = 4.5$$

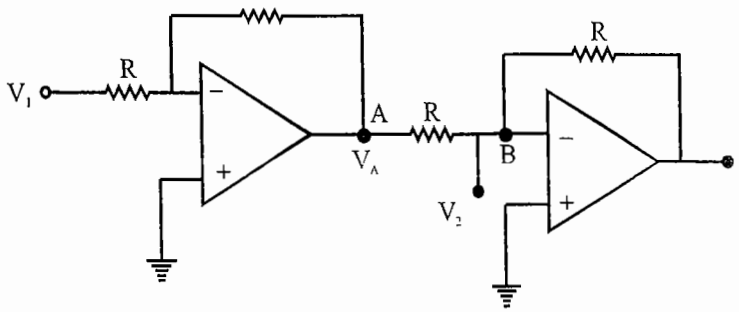
46. The circuit shown is based on ideal operational amplifiers. It acts as a **[GATE 2007]**

(a) subtractor (b) buffer amplifier

(c) adder (d) divider



Soln.



Let the voltage at the point A is VA

$$\therefore \quad \frac{V_1 - 0}{R} = \frac{0 - V_A}{R}$$

$$\Rightarrow \quad V_A = -V_1$$

Due to virtual ground the voltage at the point B will be zero.

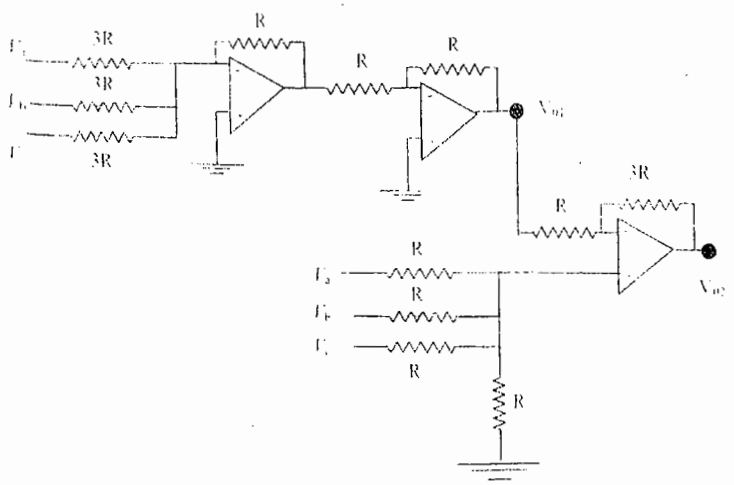
$$\therefore \quad \frac{V_A - 0}{R} = \frac{0 - V_0}{R} \Rightarrow \frac{-V_0}{R} = -\frac{V_1}{R} \Rightarrow V_0 = +V_1$$

Therefore, it a buffer amplifier.

Correct option is (b)

Statement for Linked Answer Q.47 and Q.48:

The following circuit contains three operational amplifiers and resistors **[GATE 2008]**



47.

Soln.

48.

Soln.

49.

Soln.

47. The output voltage at the end of second operational amplifier V_{01} is

(a) $V_{01} = 3(V_a + V_b + V_c)$ (b) $V_{01} = -\frac{1}{3}(V_a + V_b + V_c)$

(c) $V_{01} = \frac{1}{3}(V_a + V_b + V_c)$ (d) $V_{01} = \frac{4}{3}(V_a + V_b + V_c)$

Soln. The out at the end of first op-amp is given by

$$V = -\frac{R}{3R}(v_a + v_b + v_c) = -\frac{1}{3}(v_a + v_b + v_c)$$

$$\therefore \quad v_{01} = -\frac{R}{R}\left[-\frac{1}{3}(v_a + v_b + v_c)\right] = \frac{1}{3}(v_a + v_b + v_c)$$

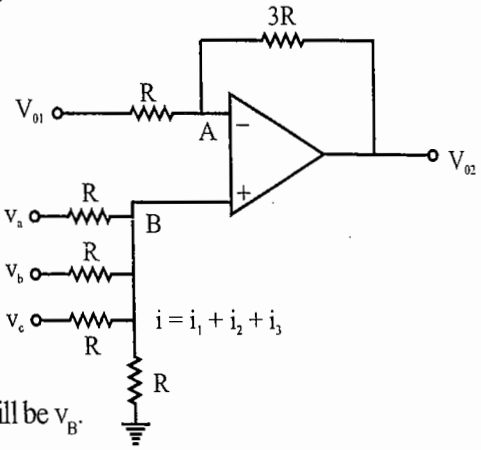
Correct option is (c)

48. The output V_{02} (at the end of third op-amp) of the above circuit is

(a) $V_{02} = 2V(V_a + V_b + V_c)$ (b) $V_{02} = 2(V_a + V_b + V_c)$

(c) $V_{02} = -\frac{1}{2}(V_a + V_b + V_c)$ (d) zero

Soln. Let the voltage at the point B is V_B.



$$\therefore \quad i_1 + i_2 + i_3 = \ell$$

$$\Rightarrow \quad \frac{v_a - v_B}{R} + \frac{v_b - v_B}{R} + \frac{v_c - v_B}{R} = \frac{v_B - 0}{R}$$

$$\Rightarrow \quad 4v_B = (v_a + v_b + v_c)$$

$$\Rightarrow \quad v_B = \frac{1}{4}(v_a + v_b + v_c)$$

Due to virtual ground the voltage at the point A will be v_B.

$$\therefore \quad \frac{v_{01} - v_B}{R} = \frac{v_B - v_{02}}{3R}$$

$$\Rightarrow \quad 3v_{01} - 3v_B = v_B - v_{02}$$

$$\Rightarrow \quad v_{02} = 4v_B - 3v_{01} = 4 \times \frac{1}{4}(v_a + v_b + v_c) - 3 \times \frac{1}{3}(v_a + v_b + v_c) = 0$$

Correct option is (d)

49. The Common Mode Rejection Ratio (CMRR) of a differential amplifier using an operational amplifier is 100 dB. The output voltage for a differential input of 200 μV is 2 V. The common mode gain is

(a) 10 (b) 0.1 (c) 30 dB (d) 10 dB **[GATE 2009]**

Soln. For differential amplifier, $V_0 = A \propto V_d$

$$\Rightarrow \quad 2 = A_d \times 200 \times 10^{-6}$$

$$\Rightarrow \quad A_d = 10^4$$

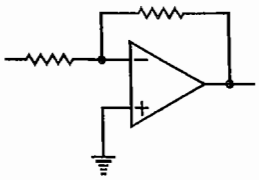
We know, CMRR = $20 \log \frac{A_d}{A_c} = 100\ dB$.

$$\Rightarrow \quad \frac{A_d}{A_c} = 10^5 \Rightarrow A_c = 10^{-1} = 0.1$$

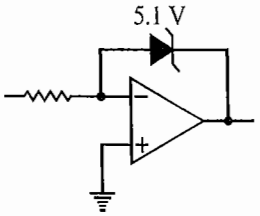
Correct option is (b)

50. In the of the following circuits, negative feedback does not operate for a negative input. Which one is it ? The opamps are running from +15 V supplies. **[GATE 2010]**

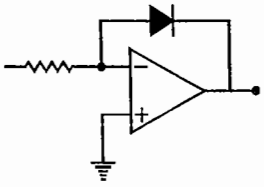
(a)



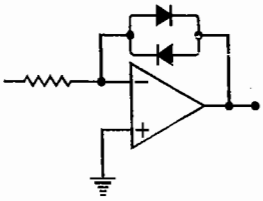
(b)



(c)



(d)

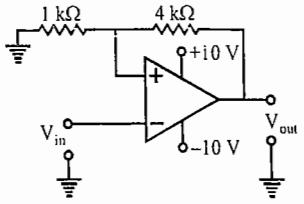


Soln.

Soln. Since diode does not conduct in reverse bias. So, the circuit given in option (c) does not operate for a negative feedback.

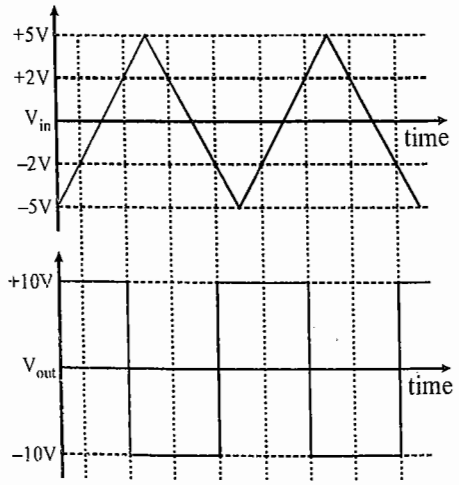
Correct option is (c)

51. Consider the following circuit. **[GATE 2011]**

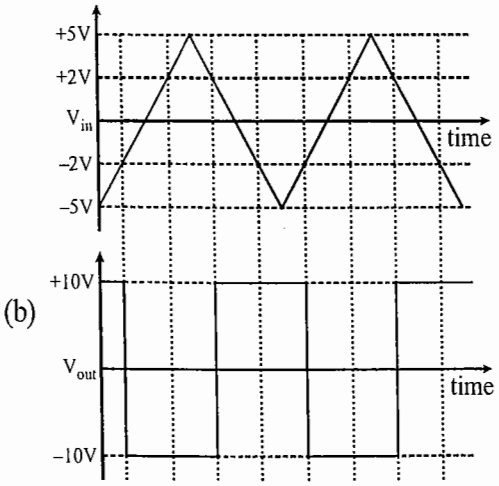


Which of the following correctly represents the output V_{out} corresponding to the input V_{in} ?

(a)

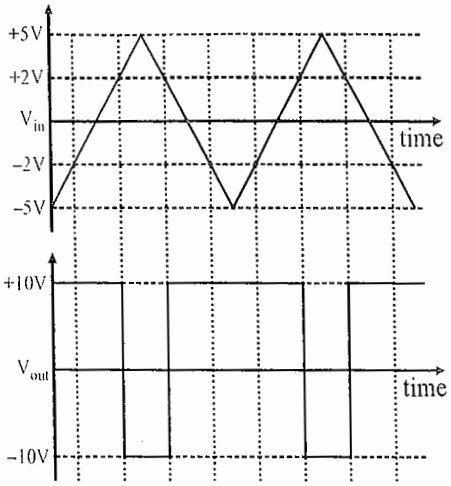


(b)

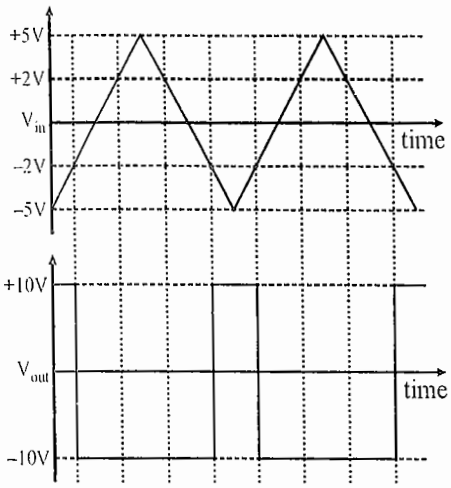


52.

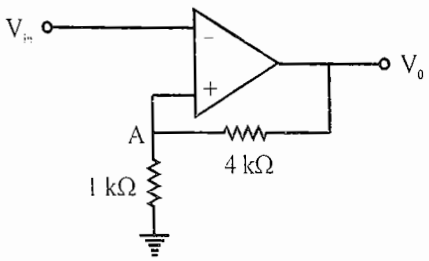
(c)



(d)

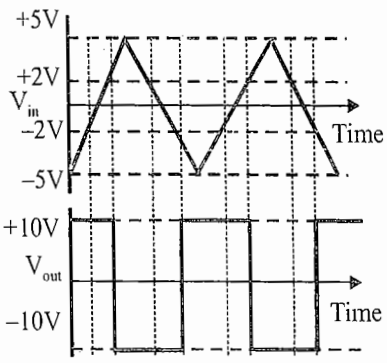


Soln.



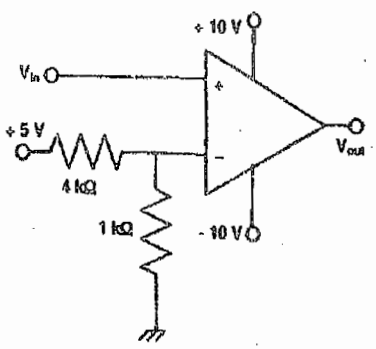
Let output is $+V_{sat}$. So, the voltage at A is $V_A = \frac{V_0}{5} \times 1 = \frac{10}{5} = 2$ volt

So, it input voltage $V_i \propto 2$ volt then output will be $V_0 = +10V$ when $V_i > 2$ the output will be negative $V_0 = -10$ volt



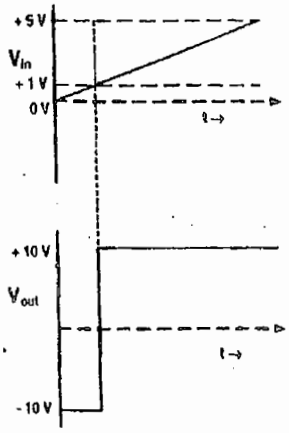
Correct option is (a)

52. Consider the following OP-AMP circuit. **[GATE 2012]**

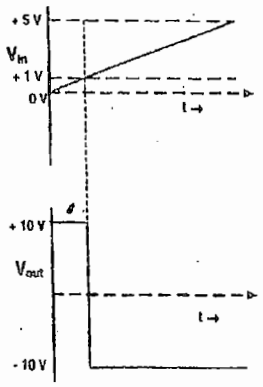


53. Which one of the following correctly represents the output V_{out} corresponding to the input V_{in} ?

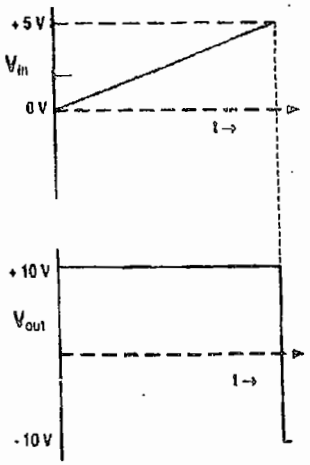
(a)



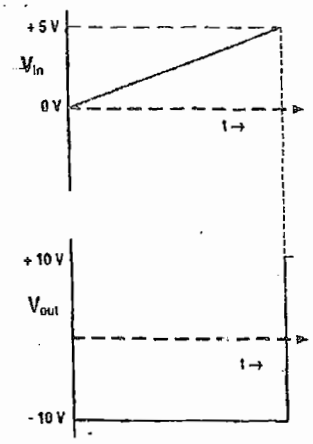
(b)



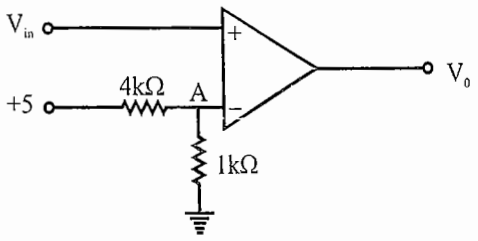
(c)



(d)



Soln.



The voltage the point A is V_A.

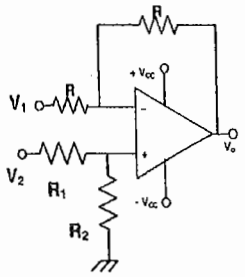
$$\therefore \quad V_A = \frac{5}{5} \times 1 = 1 \text{ volt}$$

if $V_i > I$ then output will be +10 volt

if $V_i < 1$ then output will be –10 volt.

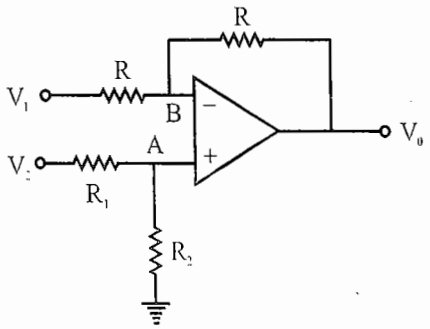
Correct option is (a)

53. In the following circuit, for the output voltage to $V_0 = (-V_1 + V_2/2)$ the ratio R_1/R_2 is



(a) 1/2 (b) 1 (c) 2 (d) 3 **[GATE 2012]**

Soln.



The voltage at the point is $V_A = \dfrac{V_2 R}{R_1 + R_2}$

Due to vertual ground the voltage at the B will be V_A.

$$\therefore \quad \frac{V_1 - \dfrac{V_2 R_2}{R_1 + R_2}}{R} = \frac{\dfrac{V_2 R_2}{R_1 + R_2} - V_0}{R}$$

$$\Rightarrow \quad V_1 - \frac{2V_2 R_2}{R_1 + R_2} = -V_0 \quad \Rightarrow V_0 = \frac{2V_1 R_2}{R_1 + R_2} - V_1 \Rightarrow V_0 = \frac{2V_1 R_2}{R_1 + R_2} - V_1$$

Now, $V_0 = \left(-V_1 + \dfrac{V_2}{2}\right)$

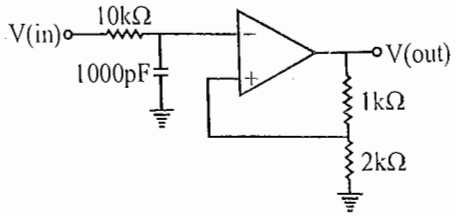
$$\therefore \quad -V_1 + \frac{V_2}{2} = \frac{2V_2 R_2}{R_1 + R_2} - V_1$$

$$\Rightarrow \quad \frac{R_2}{R_1 + R_2} = \frac{1}{4} \Rightarrow \frac{R_1 + R_2}{R_2} = 4 \Rightarrow \frac{R_1}{R_2} = 3$$

Correct option is (d)

Statement for Linked Answer Q.54 and Q.55:

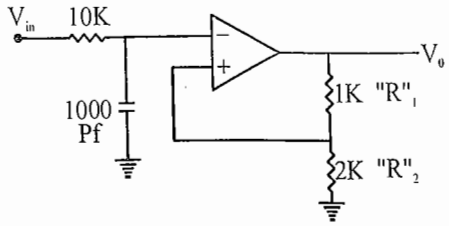
Consider the following circuit **[GATE 2013]**



54. For this circuit the frequency above which the gain will decrease by $20dB$ per decade is

(a) 15.9 kHz (b) 1.2 kHz (c) 5.6 kHz (d) 22.5 kHz

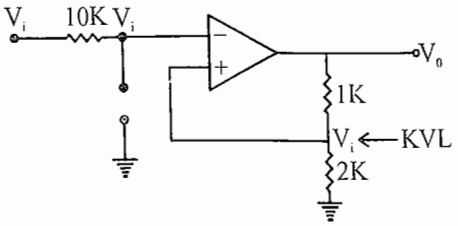
Soln.



at $f = 0$ capacitor open

at $f \to \infty$ capacitor short

CKT for $f = 0$, capacitor open



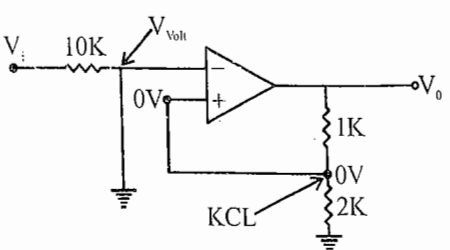
$$\frac{V_i - V_0}{1} + \frac{V_i - 0}{2} = 0$$

$$V_i + \frac{V_i}{2} = V_0, \quad \frac{3V_i}{2} = V_0$$

$$\boxed{\frac{V_0}{V_i} = \frac{3}{2}}$$

CKT for $f \to \infty$

Capacitor short



$$\frac{0-V_0}{1}+\frac{0-0}{2}=0$$

$$\boxed{V_0=0}$$

Hence given circuit is "LPF"

Now finding Transfer function of "CKT"

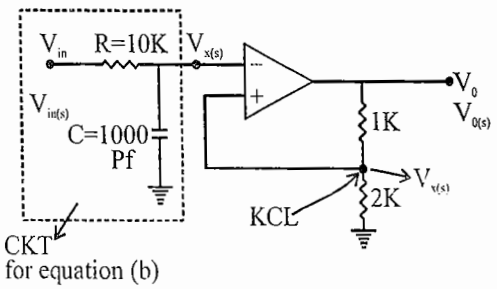
$$\frac{V_x(s)-0}{2}+\frac{V_x(s)-V_0(s)}{1}=0$$

$$\frac{V_x(s)}{2}+V_x(s)=V_0(s)$$

$$\frac{3V_x(s)}{2}=V_0(s)$$

$$V_0(s)=\frac{3}{2}V_x(s) \qquad \text{... (a)}$$

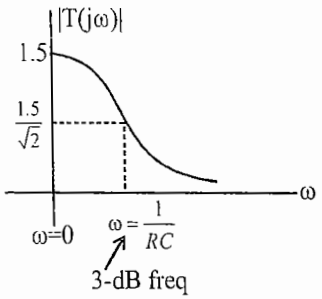
$$V_{x(s)}=\frac{V_{in(s)}\times\frac{1}{CS}}{R+\frac{1}{CS}} \qquad \text{.... (b)}$$



Put value $V_{x(s)}$ from (b) equation to equation (a)

$$V_{0(s)}=\frac{3}{2}\left[\frac{1}{1+RCS}\right]\cdot V_{in(s)}$$

$$\frac{V_{0(s)}}{V_{in(s)}}=\frac{1.5}{1+RCS}=T_{(s)}$$

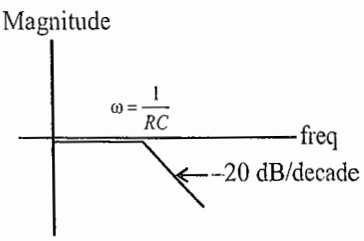


$$T(j\omega)=\frac{1.5}{1+j\omega RC}$$

Magnitude plot

$$|T(j\omega)|=\frac{1.5}{\sqrt{1+\omega^2R^2C^2}}$$

At : $\omega=\frac{1}{RC}$ magnitude reduced by factor of $\frac{1}{\sqrt{2}}$ times



$$20\log\frac{1}{\sqrt{2}}=-3dB$$

Bode plot of $\frac{1}{1+RCS}$ "LPF"

$\omega = \frac{1}{RC} \Rightarrow R \& C$ are mention in solution regarding CKT "*b*"

$$f = \frac{1}{2\pi RC}, \quad f = \frac{1}{2\pi \times 10 \times 10^3 \times 1000 \times 10^{-12}}$$

$$\boxed{f = 15.91 KHz}$$

Correct option is (a)

55. At 1.2 kHz the closed loop gain is

(a) 1 (b) 1.5 (c) 3 (d) 0.5

Soln. ∵ We know

$$\frac{V_{0(s)}}{V_{i(s)}} = \frac{1.5}{1+RCS} = T_{(S)}$$

$$T_{(S)} = \frac{1.5}{1+RCS}, \quad T_{(j\omega)} = \frac{1.5}{1+j\omega RC}$$

Magnitude $|T(j\omega)| = \frac{1.5}{\sqrt{1+\omega^2 R^2 C^2}}$

$$|T(jf)| = \frac{1.5}{\sqrt{1+(2\pi f)^2 R^2 C^2}}$$

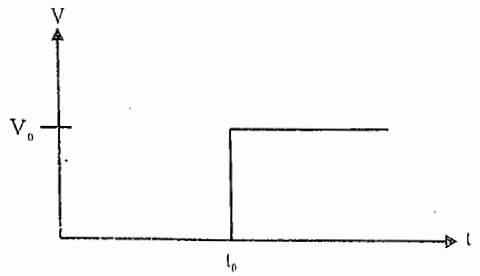
$$\left|T(j1.2\times10^3)\right| = \frac{1.5}{\sqrt{1+(2\pi\times1.2\times10^3)^2 R^2 C^2}}$$

Put $f = 1.2\times10^3$ Put $R = 10\times10^3\Omega$, $C = 1000\times10^{-12} F$

$$\boxed{\left|T(j\cdot1.2\times10^3)\right| = 1.495 \cong 1.5}$$

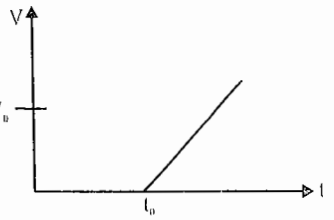
Correct option is (b)

56. The input given to be an ideal OP-AMP integrator circuit is **[GATE 2014]**

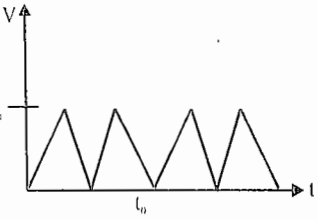


The correct output of the integrator circuit is

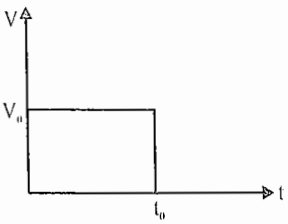
(a)



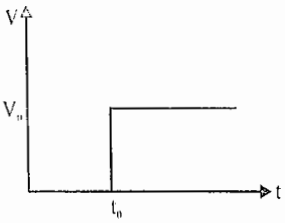
(b)



(c)



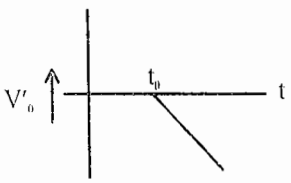
(d)



Soln. We know the output of the integer circuit is given by

$V'_0 = 0 \qquad t \le t_0$

$V'_0 = -\frac{1}{RC} \int V_0 dt = -\frac{1}{RC} V_0 t + C$

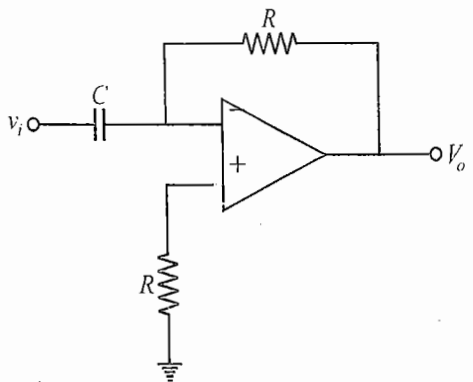


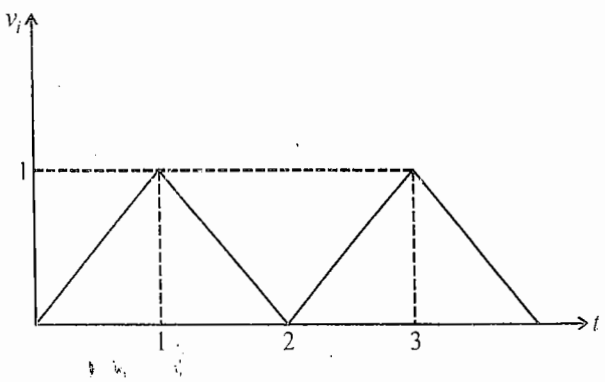
At $t = t_0 \quad V'_0 = 0$

$\therefore \qquad C = \frac{1}{RC} V_0 t_0$

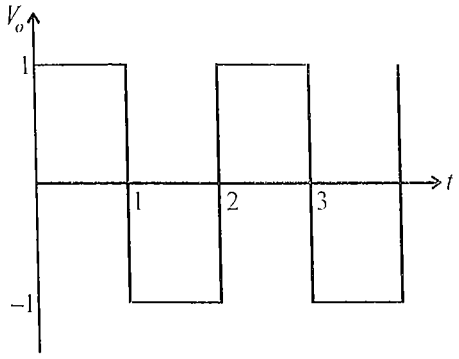
$\therefore \qquad V'_0 = \frac{1}{RC}(V_0 t_0 - V_0 t) = \frac{V_0}{RC}(t_0 - t) \qquad t > t_0$

57. Consider the circuit shown in the figure, where $RC = 1$. For an input signal V_i shown below, choose the correct V_0 from the options: **[GATE 2015]**

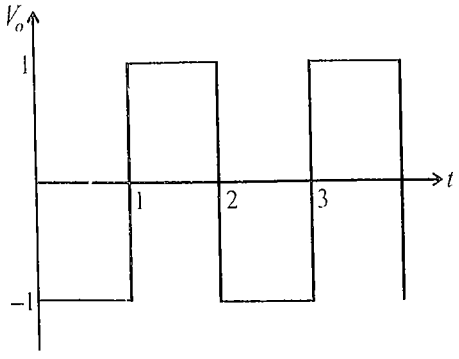




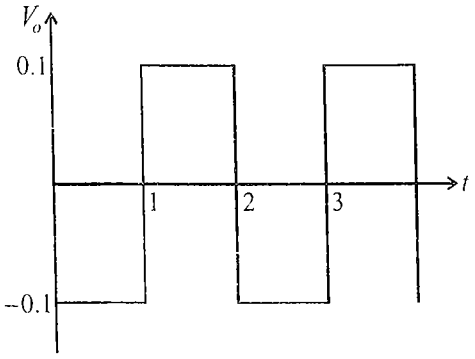
(a)



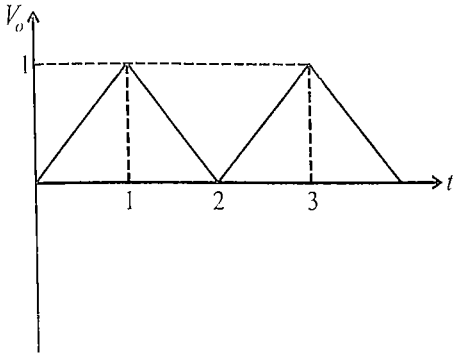
(b)



(c)



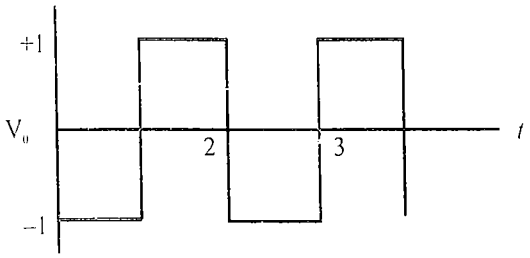
(d)



Soln. $\frac{d}{dt}(v_i C) = \frac{0 - V_0}{R}$

$$\Rightarrow \quad V_0 = -RC\left(\frac{dV_i}{dt}\right) = -RC\frac{d}{dt}(t) \quad t < 1$$

$$= -1 \qquad (\because RC = 1)$$



And $V_0 = -\frac{d}{dt}(2 - t) = +1 \qquad 1 < t < 2$

Correct option is (b)

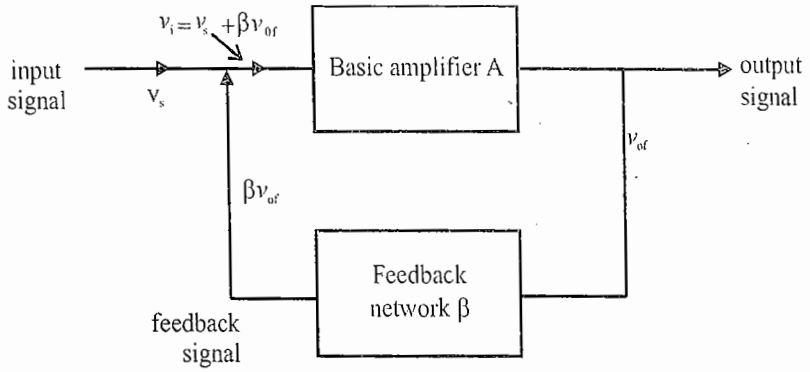
Chapter 7

Feedback & Oscillator Circuits

If a part of the output signal is returned and superposed on the input signal. This process of energy transfer from the output to input is known as feedback amplifier.

Principle of a feedback amplifier:

The given figure is a simple block diagram of a generalised feedback amplifier. In the absence of the feedback network the input signal v_s is amplified to an output signal.



$v_0 = Av_s$ where A is the gain with out feedback. A is also called open loop gain. In presence of the feedback. Network a fraction β of the output voltage v_{of} is feedback to the input such that the effect of effective input becomes $v_i = v_s + \beta v_{of}$. The quantity β is known as the feedback ratio.

The basic amplifier and feedback network may introduce phase changes. Hence, A and β are in general, complex and the feedback voltage βv_{of} may be in phase or out of phase with the input voltage. Therefore, the output of an amplifier with feedback is

$$v_{of} = Av_i = A\left(v_s + \beta v_{of}\right)$$

Or, $$v_{of}\left(1 - \beta A\right) = Av_s$$

Therefore, overall gain with feedback is

$$A_f = \frac{v_{of}}{v_s} = \frac{A}{1 \pm \beta A}$$

$$\boxed{A_f = \frac{A}{1 \pm \beta A}}$$

where the – sign is for positive feedback and + sign is for negative feedback.

Types of feedback connection:

There are four basic feedback arrangements

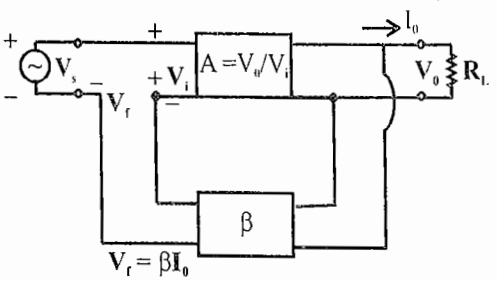
(1) Voltage -series feedback (Figure-a)

(2) Voltage - shunt feedback (Figure-b)

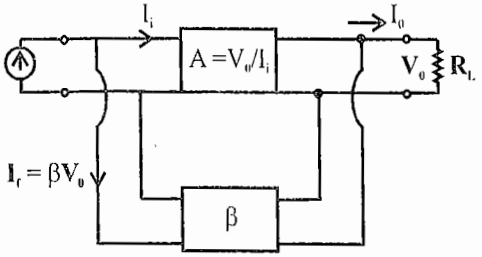
(3) Current series feedback(Figure-c)

(4) Current shutn feedback (Figure-d)

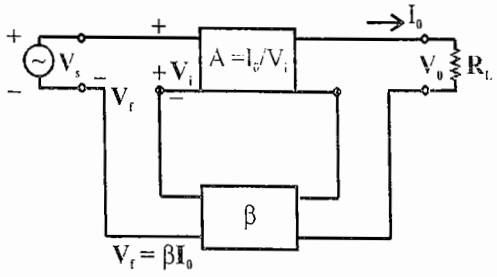
(a)



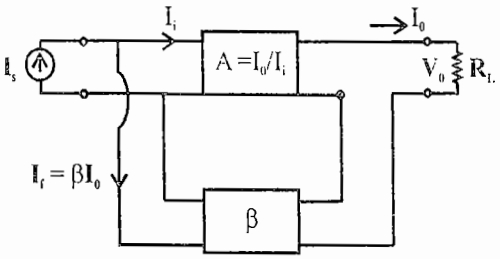
(b)



(c)

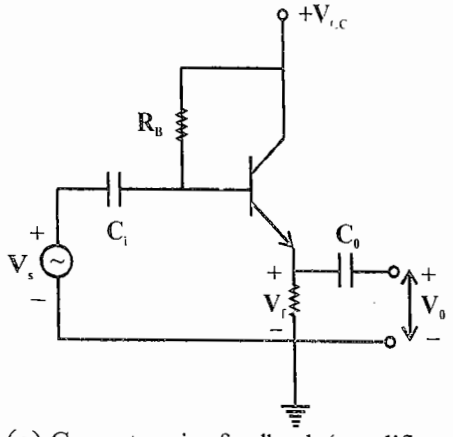


(d)

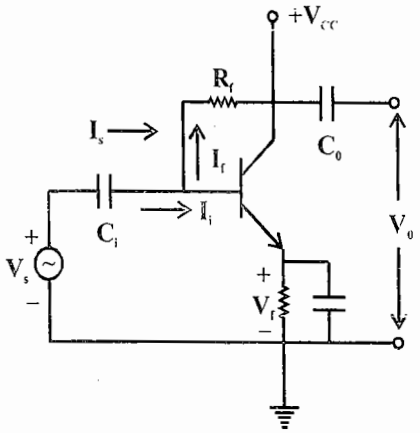


Some practical feedback circuit:

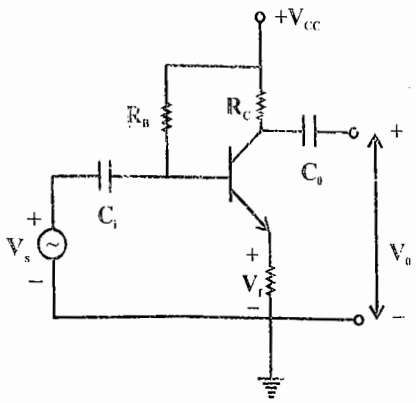
(a) Voltage-series feedback (Emitter follower)



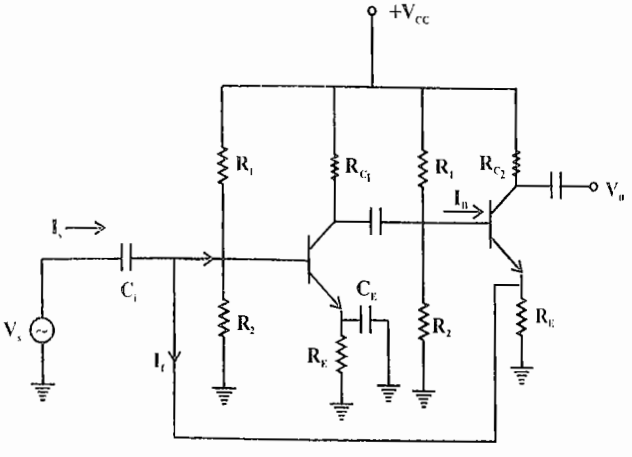
(b) Voltage-shunt feedback (CE amplifier)



(c) Current-series feedback (amplifier with unbypassed emitter resistance)



(d) Current-shunt feedback



Effects of negative feedback:

Though the negative feedback reduces the gain of an amplifier, at the cost of this reduced gain it can improve many important characteristics of the amplifier as stated below.

1. Stability of gain:

The percentage change in gain with feedback

$$\boxed{\frac{dA_f}{A_f} = -\frac{dA}{A}\frac{1}{1+\beta A}}$$

So, it smaller than the percentage change in gain without feedback.

2. Reduction of phase distortion:

$$\phi_f = \phi_0 - \frac{\beta|A|\sin\phi_0}{1+\beta|A|\cos\phi_0}$$

3. Increase in bandwidth:

Due to negative feedback.

Upper half-power frequency become

$$f'_2 = f_2(1+A\beta)$$

and lower half power frequency

$$f'_1 = \frac{f_1}{1+A\beta}$$

4. Effect of feedback on input impedance:

The series input of negative feedback signal increase the input resistance,

$$R_{if} = R_i(1+\beta A)$$

The shunt input of negative feedback signal decrease the input resistance

$$\boxed{R_{if} = \frac{R_i}{1+\beta A}}$$

5. Effect of feedback on output impedance:

The negative voltage feedback decrease the output impedance

$$R_{0f} = \frac{R_0}{1+\beta A}$$

The negative current feedback increase the output impedance,

$$R_{0f} = R_0(1+\beta A)$$

Oscillator:

- An oscillator is a non-linear electronics device consisting of active and passive circuit elements which can generate senusoidal or other periodic waves at a desired frequency
- It delivers output voltage without any external input signal. Input signal is provided by the circuit noise.
- It converted d.c. power from the supply source to the output a.c. power
- A great variety of oscillator circuits have been developed. If the output waveform is senusoidal then it is called sunusoidal oscillator on the other hand, a non-senusoidal oscillator produces square wave, triangular wave, swatooth waves, pulses etc.

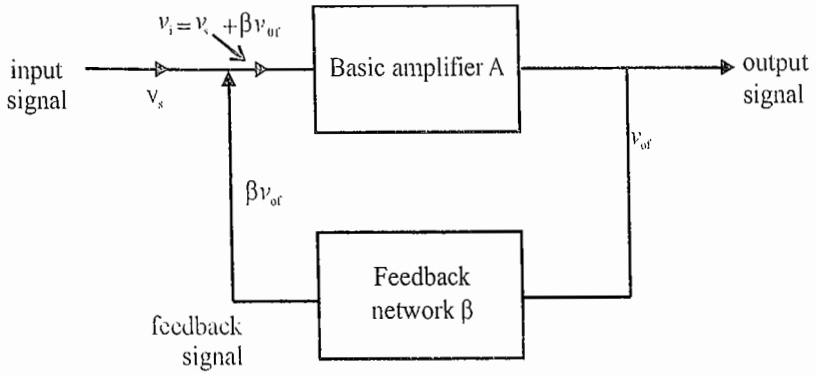
Barkhausen Criterion for oscillator:

From the block diagram of a feedback amplifier we can write the output

$$v_{0f} = Av_i = A(v_s + \beta v_0 f)$$

So, overall gain,

$$A_f = \frac{v_{0f}}{v_s} = \frac{A}{1 - A\beta}$$



if $A\beta = 1$ then gain becomes infinite. That is an output is obtained without any external input signal. The amplifier then turns into an oscillator.

The condition $\beta A = 1$ is called Barkhausen criterion of oscillator. The condition implies that loop gain $|A\beta| = 1$ and the overall phase shift around the loop is zero or an integral multiple of 2π. In this case feedback voltage become equal to the external signal both amplitude and phase.

*** Please read the following oscillator from any electronics book.**

(i) RC-Phase shift oscillator
(ii) Wien bridge oscillator
(iii) Hartley oscillator
(iv) Colpitts oscillator

SOLVED PROBLEMS

1. An amplifier of gain 1000 is made into a feedback amplifier by feeding 9.9 % of its output voltage in series with the input opposing. If $f_L = 20$ Hz and $f_H = 200$ kHz for the amplifier without feedback, then due to the feedback **[GATE 2009]**

(a) the gain decreases by 10 times
(b) the output resistance increases by 10 times
(c) the f_H increases by 100 times
(d) the input resistance decreases by 100 times

Soln. $A = 1000, \beta = \dfrac{9.9}{100}$

$$\therefore \quad A_f = \frac{A}{1+\beta A} = \frac{1000}{1+\frac{90}{1000}\times 1000} = \frac{1000}{100} = 10$$

Therefore, gain decreases by 100 times.
Due to series input of negative feedback. The input resistance increase by a factor

$$(1+\beta A) = \left(1+\frac{99}{1000}\times 1000\right) = 100$$

And out put impedance decrease by $\dfrac{1}{100}$ times.

Higher cut off frequency due to negative feedback increase by $(1+\beta A) = 1+\dfrac{99}{1000}\times 1000 = 100$

Correct option is (c)

Chapter 8

Digital Electronics

Boolean Algebra:

$(1)\ A+A=A,\quad (2)\ A+1=1,\ (3)\ A+0=A,\quad (4)\ A+\overline{A}=1,\quad (5)\ A.A=1,\quad (6)\ A.1=A$

$(7)\ A.0=0,\quad (8)\ A.\overline{A}=0,\quad (9)\ \overline{\overline{A}}=A,\quad (10)\ A+A.B=A,\quad (11)\ A(A+B)=A$

$(12)\ A.(\overline{A}+B)=AB,\quad (13)\ A+\overline{A}B=A+B,\quad (14)\ \overline{A}+AB=\overline{A}+B,\quad (15)\ A(\overline{A}+B)=\overline{A}+\overline{B}$

Note: $A+BC=(A+B)(A+C)$

Boolean Law:

(1) Commutative Law: $A+B=B+A, AB=B.A$

(2) Associative Law: $A+(B+C)=(A+B)+C,\ A.(B.C)=(A.B).C$

(3) Distributive Law: $A+B.C=(A+B)(A+C),\ A.(B+C)=AB+AC$

(4) Demorgan's Law: $\overline{A.B}=\overline{A}+\overline{B},\ \overline{A+B}=\overline{A}.\overline{B}$

SOLVED PROBLEMS

1. The Boolean expression $(X+Y)(X+\overline{Y})(\overline{X}+Y)$ is equivalent to

(a) $\overline{X}Y$ (b) $X\overline{Y}$ (c) XY (d) $\overline{X}\overline{Y}$

Soln. $(X+\overline{Y})(\overline{X}+Y)=XY+\overline{X}\overline{Y}$

$\Rightarrow (X+Y)(X+\overline{Y})(\overline{X}+Y)=(X+Y)(XY+\overline{X}\overline{Y})\ =\ XY+XY=XY$

2. Given that $AB+\overline{A}C+BC=AB+\overline{A}C$, then $(\overline{A}+C)(B+C)(A+B)$ is equivalent to

(a) $(\overline{A}+B)(A+C)$ (b) $(A+B)(\overline{A}+C)$ (c) $(A+\overline{B})(\overline{A}+C)$ (d) $(A+\overline{B})(\overline{A}+\overline{C})$

Soln. According to Consensus theorem. Correct option **(b)**

3. Expression $A+\overline{A}B+\overline{A}\overline{B}C+\overline{A}\overline{B}\overline{C}D+\overline{A}\overline{B}\overline{C}\overline{D}E$ would be similar to

(a) $A+\overline{A}B+CD+E$ (b) $A+B+CDE$

(c) $A+BC+CD+DE$ (d) $A+B+C+D+E$

Soln. $F=A+\overline{A}B+\overline{A}\overline{B}C+\overline{A}\overline{B}\overline{C}(D+\overline{D}E)$

$=\ A+\overline{A}B+\overline{A}\overline{B}(C+\overline{C}(D+E))\ =\ A+\overline{A}(B+\overline{B}(C+D+E))\ =\ A+B+C+D+E$

Complement and Dual of Expression: For calculating dual of a expression multiply is replaced by plus sign, while plus sign is replaced by multiply. After calculating dual primed variable are replaced by unpaired. Variable while unprimed by primed variables.

4. Calculate dual complement of given expression $Y(A,B,C) = A\bar{B}C + \bar{A}B\bar{C}$

$Y_D(A,B,C) = (A+\bar{B}+C)(\bar{A}+B+\bar{C})$, $\bar{Y}(A,B,C) = (\bar{A}+B+\bar{C})(A+\bar{B}+C)$

Minterms: For n variables we have 2^n minterms. Here each minterm is obtained by from AND operation of n variables of n variables with each variable being primed if corresponding bit of binding number is zero unprimed if corresponding bit is 1. Sum of all minterms is always equal to 1.

Minterms far No. 110 is $AB\bar{C}$.

Maxterms: It is nothing but simply complement of minterm and each minterm is complement of maxterm.

Maximum term for 011 is Maxterm for number 110 is $\bar{A}+\bar{B}+C$.

SOP $\rightarrow$ SUM OF PRODUCT, POS $\rightarrow$ PRODUCT OF SUM

Examples:

f(A, B, C) = $\sum(0, 3, 5, 6, 7)$ ..... SOP, f(A, B, C) = $\pi(0, 3, 5, 6, 7)$ ..... POS

5. f(A, B, C) = $\sum(0, 5, 6)$ ..... POS

Soln. $m_0 + m_5 + m_6 = \bar{A}\bar{B}\bar{C} + A\bar{B}C + AB\bar{C}$

6. f(A, B, C) = $\pi(0, 2, 4, 7)$ ..... SOP = $M_0M_2M_4M_7$

$= (A+B+C)(A+\bar{B}+C)(\bar{A}+B+C)(\bar{A}+\bar{B}+\bar{C})$

Deriving sum of product (SOP) expression from the truth table

Derive a minterm expression for the following table

Input			**Output**
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

$Y = \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}\bar{C} + AB\bar{C}$

Deriving product of sum (POS) expression from a truth table

Derive a Maxterm expression for the following truth table

Input			**Output**
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

$Y = (A+B+C)(A+\bar{B}+C)(\bar{A}+B+\bar{C})(\bar{A}+\bar{B}+\bar{C})$

KARNAUGH MAP

Combination Logic Circuit: It is a method of simplication of boolean alzebra. It can minimize number of gates and number of terms. At the same time it minimizes number of litercals. But at the same time result of K-Map is not unique. Simplification of K-map can be give different results. Maurice karnaugh devised a graphical technique to simplify Boolean expression for a two variable realization. This technique can be used for any number of variables.

Paring in K-Map: In case of *n*-variables K-Map if number of terms in a pair are 2^m then number of terms in simplified expression are (n – m). From the fore going we see that a pair (group of two) reduces to one variable a quad eliminates 2 variables, an octet eliminates 3 variables in case of 4 variables K-map.

Methods of Solving Problems by K-Map:

1. Write a interm of Boolean expression from the truth table.
2. Place the 1's on the appropriate squares of the K-map.
3. Circle the isolated 1's which do not form adjacencies
4. Loop pairs of adjancencies
5. Loop any octet.
6. Loop any quad that contains one or more 1's which have not already been looped.
7. Simplify by dropping terms that contain a variable and its complement within the loop.
8. Or the remaining terms (one term per loop) and write the simplified minterm Boolean expression.

3-Variable K-Map: A 3 variables expression will be $2^3 = 8$ squares. In this 2 variables will be on one side of the fail and one below. It can be drawn horizontally or vertically.

AB \ C	$\bar{C}$	C
$\bar{A}\bar{B}$ 00	0	1
$\bar{A}B$ 01	2	3
AB 11	6	7
$A\bar{B}$ 10	4	5

	AB	$\bar{A}\bar{B}$	$\bar{A}B$	AB	$A\bar{B}$
		00	01	11	10
0	$\bar{C}$	0	2	6	4
1	C	1	3	7	5

4-Variable K-Map: A four variable Boolean function is *f*(A, B, C, D). Its K-map will be with 16 squares.

AB \ CD	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

In 4-Variable Map

1. 8 adjacent squares yield a single variable.
2. 4 adjacent squares yield a two variable term
3. 2 adjacent squares yield a three variables term
4. Individual cells yield a four variable term.

7. $f(X_1, X_2, X_3, X_4) = \Sigma(0,2,3,5,7,8,9,10,11) + \Sigma dc(4,15)$. A function with don't care condition is as follows. The minimized expression for this function is

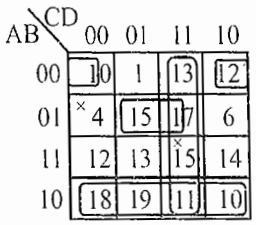
(a) $a\bar{b} + \bar{b}\,\bar{d} + cd + \bar{a}\,\bar{b}\,\bar{c}$

(b) $a\bar{b} + \bar{b}\,\bar{d} + cd + \bar{a}bd$

(c) $a\bar{b} + \bar{b}\,\bar{d} + \bar{b}c + \bar{a}bd$

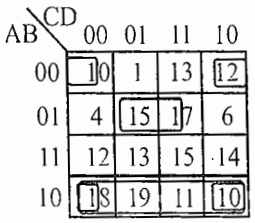
(d) Above all

Soln. The K-map is as shown below:



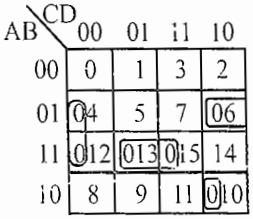
$f = A\bar{B} + CD + \bar{A}BD + \bar{B}\bar{D}$

If we take $\bar{c}\,\bar{d}$ instead cd, with $\bar{a}\,b$ then, $f = A\bar{B} + CD + \bar{B}\bar{D} + \bar{A}B\bar{C}$



$f = a\bar{b} + \bar{b}d + \bar{b}c + \bar{a}bd$

8. Minimize the 4-variable expression using K-Map, $f(A,B,C,D) = \pi(4,6,10,12,13,15)$.



$f(A,B,C,D) = (\bar{A} + \bar{B} + \bar{D}).(\bar{B} + C + D).(A + \bar{B} + D).(\bar{A} + B + \bar{C} + D)$

Use of don't care Condition: When the output for input is immaterial whether a 1 or 0, we put on X or *d* in the K-map and call it don't care condition. Such functions are incompletely specified functions. Output may be specified for only a combination of input leaving the rest undecided. For instance in four variable input, output may be specified for some say upto m_{10} leaving the rest unspecified either 0 or 1 such an expression is expressed as

9. In a certain application four input A, B, C, D are Feb to logic circuit, producing an output which operates a relay. The relay turns on when $f(A,B,C,D) = 1$ for the following states of the inputs (A B C D): 0000, 0010, 0101, 0110, 1101 and 1110 states 1000 and 1001 do not occur and far the remaining states the relay is off. The minimized Boolean expression F is

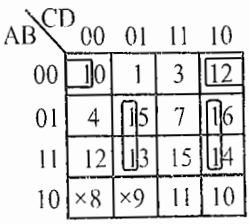
(a) $\bar{A}C\bar{D} + BC\bar{D} + B\bar{C}D$

(b) $\bar{B}\bar{C}D + BC\bar{D} + \bar{A}C\bar{D}$

(c) $ABD + \bar{B}C\bar{D} + \bar{B}\bar{C}D$

(d) $\bar{A}\bar{B}\bar{D} + B\bar{C}D + BC\bar{D}$

Soln. The K-Map is as follows:



$\bar{A}\bar{B}\bar{D} + B\bar{C}D + BC\bar{D}$

10. $f(A,B,C,D) = \pi(4,5,6,7,8,12) + d(1,2,3,9,11,14)$

AB \ CD	00	01	11	10
00	0	×1	×3	×2
01	04	05	07	06
11	012	13	15	×14
10	08	×9	×11	10

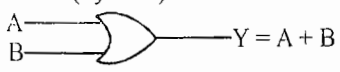
$f(A,B,C,D) = (A+\bar{B})(C+D+\bar{A})$

Logic Gates: Positive Logic: logic 0 = 0V, logic 1 = 5V

Negative Logic: logic 1 = 0V, logic 0 = 5V.

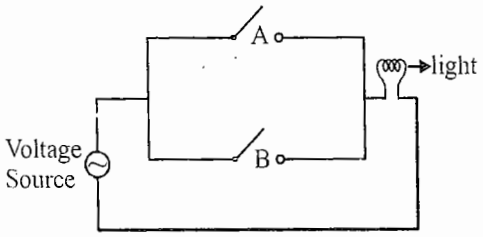
Logic-Gates: There are the most basic and most important building blocks of any digital system including computers. Three logic gates are AND, OR and NOT gates. These three gates together can be used to construct the logic circuit for any given logic or boolean expression.

OR Gates: $\boxed{Y = A+B}$ (Symbol)



It is a logic circuit with 2 or more than two inputs and one output.

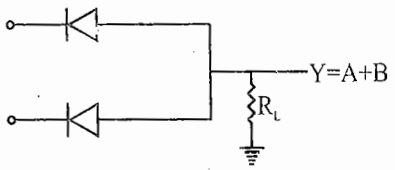
Switching Circuit of OR Gate:



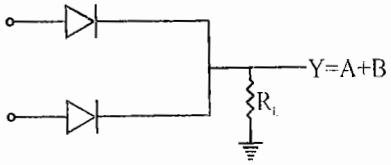
Truth Table for OR gate:

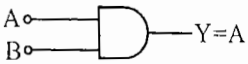
A	B	$Y = A+B$
0	0	0
0	1	1
1	0	1
1	1	1

(1) Negative Logic or Gate:



(2) Positive Logic or Gate:

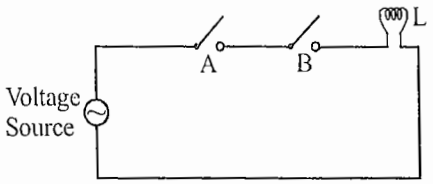


AND Gate: $\boxed{Y = A.B}$ 

{Symbol of AND Gate}

It is a logic circuit having two or more than two input and one output.

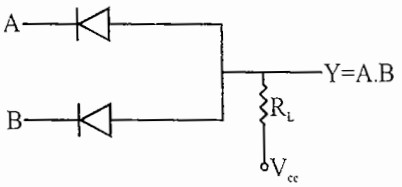
Switching Circuit of AND Gate:



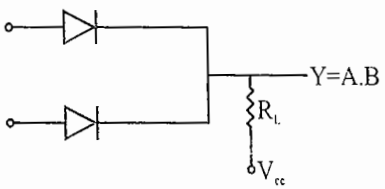
Truth Table:

A	B	$Y = A.B$
0	0	0
0	1	0
1	0	0
1	1	1

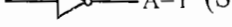
(1) Positive logic AND gate:



(2) Negative logic AND gate:



Note: Negative logic OR gate is same as positive logic AND gate and vice-versa while positive logic OR gate is same as negative logic AND gate and vice-versa.

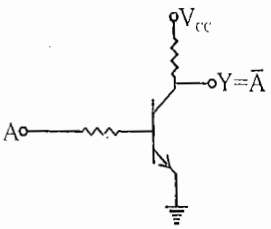
NOT Gate: $\boxed{Y = \bar{A}}$ 

(Symbol NOT Gate)

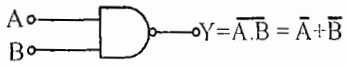
It is one input and one output logic gate whose output is always the complement of the Input.

Truth Table:

A	$Y=\bar{A}$
0	1
1	0

Switch Circuit of NOT Gate: 

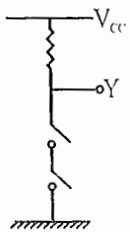
NAND Gate: NAND stands for NOT-AND. An AND gate followed by a NOT circuit makes it a NAND gate. The truth table of a NAND gate is obtained from truth table of an AND gate by complementing the output entries.



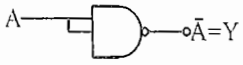
Input		Output
A	B	NAND
0	0	1
0	1	1
1	0	1
1	1	0

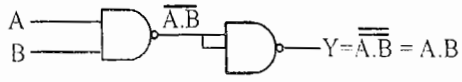
When both inputs are high in a NAND gate the output is low. NAND gate gives zero output only in high input condition.

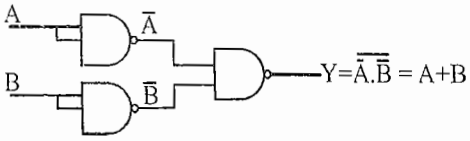
Switching Circuit of NAND Gate:



The NAND gate is called an universal gates as all functions OR, AND, NOT can be realized from it.

NOT: 

AND: 

OR: 

NOR Gate: NOR stands for NOT-OR. Thus the NOR Gate output is obtained by complementing the output of OR gate. Thus output of NOR gate logic 1 when all its input are logic 0. For all other cases the output is logic 0. NOR gate also called as universal gate because all the gates can be designed by this gate.

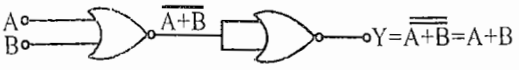
Input		Output
A	B	NOR
0	0	1
0	1	0
1	0	0
1	1	0

Output of NOR will gate be high when all of its input are low.

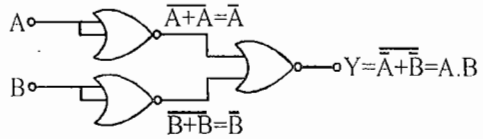
NOR gates as universal Gate:

OR, NOT, AND can be derived using only NOR gate.

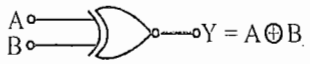
NOT: 

OR: 

AND:



EXOR Gate: The output of 2 input EX-OR gate is logic 1 when the two inputs are unequal and output is logic 0 when two inputs are equal.



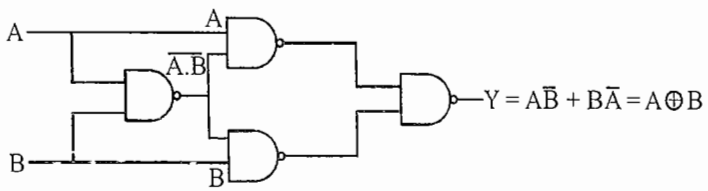
Truth Table of EX-OR Gate:

Input		**Output**
A	B	XOR
0	0	0
0	1	1
1	0	1
1	1	0

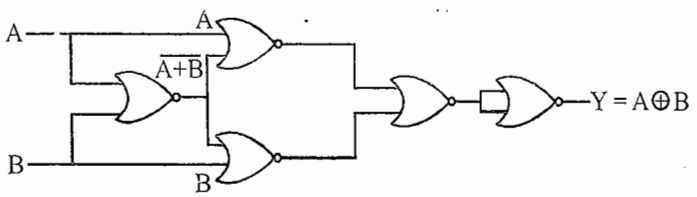
The symbol $\oplus$ means the terms are XORed together. $Y = A\bar{B} + \bar{A}B$ is boolean expression for EX-OR.

Implementation of EX-OR gate with 2 input NAND and NOR gate:

Using NAND Gate:



Using NOR Gate:



Application of EX-OR Gate:

1. XOR Gate can be used as an inequality comparator.
2. It can also be used as controlled inverter.
3. It can be used for complemeting in adder circuit.
4. XOR is an important logic gate used in arithmetic operations, code conversion, and in error detector and correction circuit.

EX-NOR Gate: The output of the XOR Gate is connected to an inverter and the output taken.

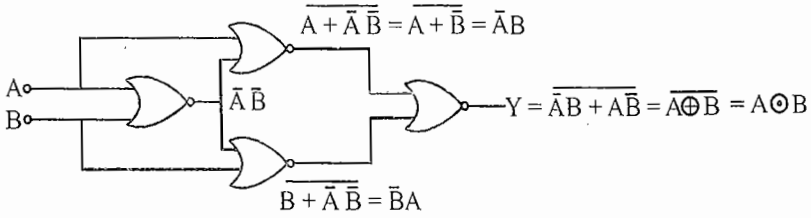
Example:

Truth Table:

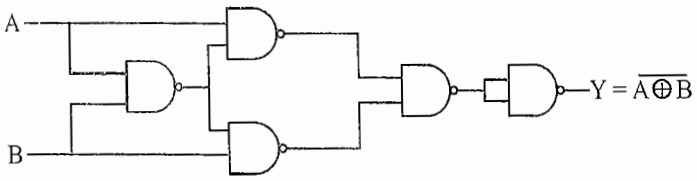
Input		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

So, If XOR is an odd number detector then XNOR is an even number detector.

Implementation of EX-NOR gate with 2 input NOR and NAND gate.



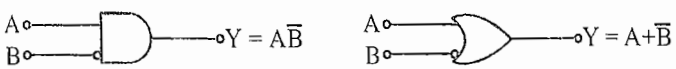
Using NOR Gate



Using NAND Gate

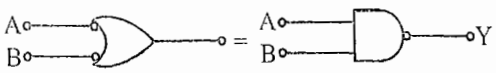
Logic gate	*No. of NAND gate used*	*No. of NOR gate used*
NOT	1	1
AND	2	3
OR	3	2
EX – OR	4	5
EX – NOR	5	4
NOR	4	1
NAND	1	4

Inhibitor: If one of the inputs to an AND or OR gate is inverted it becomes an INHIBITOR. An inhibitor is also known as AND-NOT or OR-NOT gate.



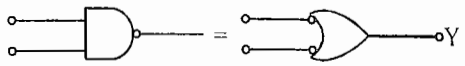
If we add on inverter at the output only the outputs get inverted. How ever, if we invert the input, the gate functions change.

1. If both the inputs to one OR gate are inverted, the gate becomes a NAND gate.



2. If both the inputs to an NAND gate are inverted, the gate becomes a NOR gate.

If we invert both inputs and outputs.



If we invert both inputs and outputs.

3. An AND gate becomes as OR gate.

4. An OR gate becomes an AND gate.

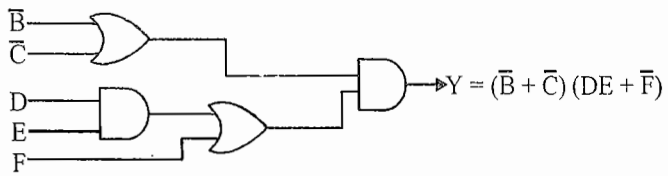
Design of a Boolean expression by minimum number of NAND gate.

1st Step: Write boolean expression is form of AND and OR gate.

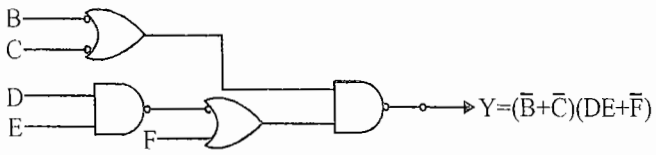
2nd Step: Place a bubble at the output of each AND gate and place a bubble at each input of OR gate.

3rd Step: NOT followed by NOT means original literal.

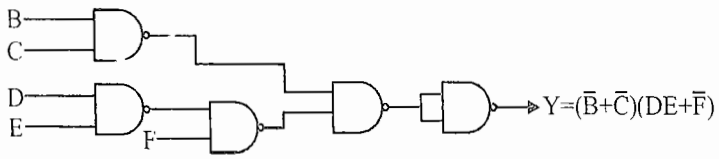
11. Design $Y = (\overline{B} + \overline{C})(DE + \overline{F})$ by use of minimum number of 2 input NAND gates.



Put bubble at input of OR gate and at the output of AND gate.



Invert OR is NAND gate AND-invert is NAND gate



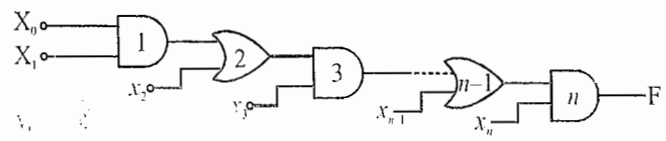
Design of a boolean expression by minimum number of NOR gate:

1st Step: Write boolean expression in form of OR and AND gate.

2nd Step: Place a bubble at the output of gates, place a bubble at each of the inputs of AND gate.

3rd Step: NOT followed by NOT means original literal.

12. In the network shown below f can be written as



(a) $x_0x_1x_3x_5 + x_2x_4x_5 \ldots\ldots x_{n-1} + \ldots\ldots\ldots x_{n-1}x_n$

(b) $x_0x_1x_3x_5 + x_2x_4x_5 \ldots\ldots x_n + \ldots\ldots\ldots x_{n-1}x_n$

(c) $x_0x_1x_3x_5 \ldots\ldots x_n + x_2x_3x_5 \ldots\ldots x_n + \ldots\ldots + x_{n-1}x_n$

(d) $x_0x_1x_3x_5 \ldots\ldots x_{n-1} + x_2x_3x_5 \ldots\ldots x_n + x_{n-1}x_{n-2} + x_n$

Soln. Output of gate 1 is x_0x_1

Output of gate 2 is $x_0x_1 + x_2$

Output of gate 3 is $(x_0x_1 + x_2)x_3 = x_0x_1x_3 + x_2x_3$

Output of gate 4 is $x_0x_1x_3x_5 + x_2x_3 + x_4$

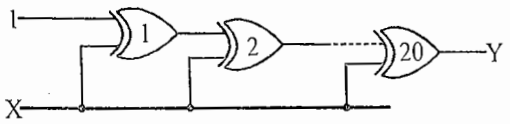
Output of gate 5 is $x_0x_1x_3x_5 + x_2x_3x_5 + x_4x_5$

So, output of gate n would be

$x_0x_1x_3x_5.....x_n + x_2x_3x_5.....x_n + x_4x_5x_7.....x_n + x_{n-1}x_n$.

Correct answer is (c)

13. If the input to the digital circuit shown below consisting of a cascade of 20 XOR gates is X, then the output Y is equal to.



(a) X (b) $\bar{X}$ (c) 0 (d) 1

Correct answer is (d)

Soln. Output of 1st XOR = $\bar{X}1 + X\bar{1} = \bar{X}$, Output of 2nd XOR = $\bar{X}\bar{X} + XX = 1$

So after 4, 6, 8, ... 20XOR output will be 1.

14. If A = 0 in logic expression

$Z = [A + EF + \bar{B}C + D][A + \bar{D}\bar{E} + \bar{B}C + \bar{D}\bar{E}]$. then

(a) $Z = 0$ (b) $Z = 1$ (c) $Z = \bar{B}C$ (d) $Z = B\bar{C}$

Soln. $Z = [A + \bar{B}C + D + EF][A + \bar{B}C + \bar{D}(\bar{E} + \bar{F})] = \underbrace{[A + \bar{B}C}_{x} + \underbrace{EF + D]}_{y}\underbrace{[A + \bar{B}C}_{x} + \underbrace{\overline{D + EF]}}_{y}$

$= (x + y)(x + \bar{y}) = X = A + B\bar{C}$ for $A = 0$, $Z = B\bar{C}$

Correct answer is (d)

15. The simplified form of a logic function

$Y = A(B + C(\overline{AB + AC}))$

$= AB + AC(\overline{AB + AC}) = AB + AC(\overline{AB}.\overline{AC}) = AB + AC((\bar{A} + \bar{B}).(\bar{A} + \bar{C}))$

$= AB + AC(\bar{A} + \bar{A}\bar{C} + \bar{B}\bar{A} + \bar{B}\bar{C}) = AB$

(a) $\bar{A}\bar{B}$ (b) AB (c) $\bar{A}B$ (d) $A\bar{B}$

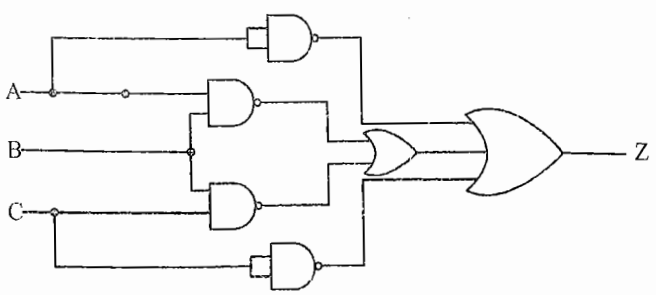
Correct answer is (b)

16. If $X\bar{Y} + \bar{X}Y = Z$, then $X\bar{Z} + \bar{X}Z$ is equal to

(a) $\bar{Y}$ (b) Y (c) 0 (d) 1

Soln. $X\bar{Z} + \bar{X}Z = X(\overline{X\bar{Y}} + \overline{\bar{X}Y}) + \bar{X}(X\bar{Y} + \bar{X}Y) = X(XY + \bar{X}\bar{Y}) + \bar{X}Y = XY + \bar{X}Y = Y$

17. In the following circuit the output z is



(a) $\overline{A}+\overline{B}+\overline{C}$ (b) $\overline{ABC}$ (c) $\overline{AB}+\overline{BC}+\overline{AC}$ (d) Above all

Soln. $Z=\overline{A}+(\overline{AB}+\overline{BC})+\overline{C} = \overline{A}+(\overline{A}+\overline{B}+\overline{B}+\overline{C})+\overline{C} = \overline{A}+\overline{B}+\overline{C}$

$\overline{ABC} = \overline{A}+\overline{B}+\overline{C}$

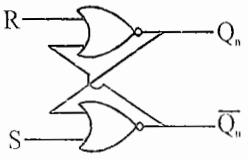
$\overline{AB}+\overline{BC}+\overline{AC} = \overline{A}+\overline{B}+\overline{B}+\overline{C}+\overline{A}+\overline{C} = \overline{A}+\overline{B}+\overline{C}$

FLIP-FLOP

Digital output are required to be generated in accordance with sequence in which input signals are received, which is not possible with the combinational circuit generated should depend on present and past history of input. Such circuit is called as sequential circuit.

Sequential Circuit

SR-Latch:

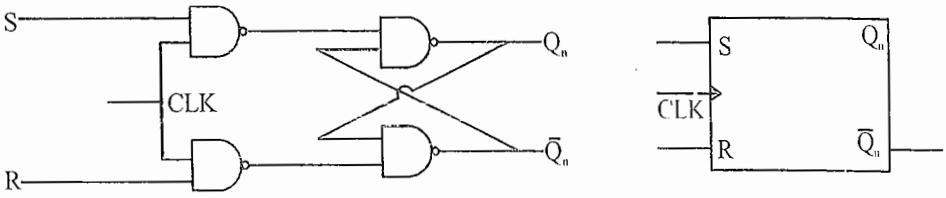


Truth Table:

CLK	R	S	Q_{n+1}
1	0	0	Q_n
1	0	1	1
1	1	0	0
1	1	1	*Invalid*
0	X	X	Q_n

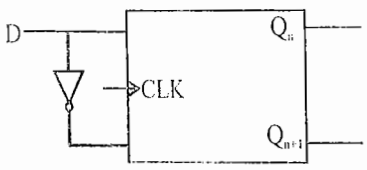
X : Input either 0 or 1

S-R Flip Flop with NAND Gate:



D-Flip Flop (Delay):

When S = D, $\overline{R}=D$, Now SR becomes D type Flip Flop.

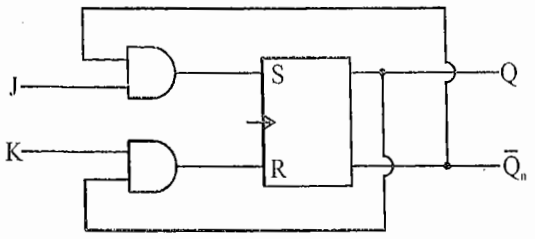


Truth Table

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

J-K Flip Flop:

$S = J(\bar{Q}_n)$; $R = K(Q_n)$



J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

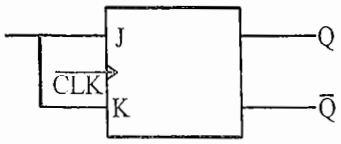
→ Toggle State

19.

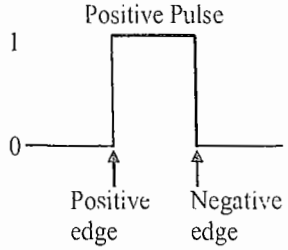
Note: Problem in JK flip flop is race around condition.

T-type (Toggle) Flip Flop: J = K = T then T = Flip Flop.

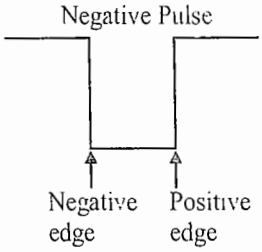
Soln.



Input	Q_{n+1}
0	Q_n
1	$\bar{Q}_n$



(Fig.1)



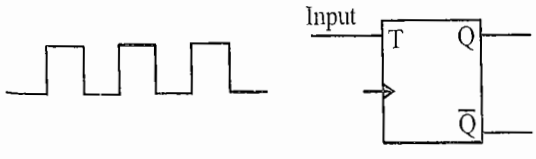
(Fig.2)

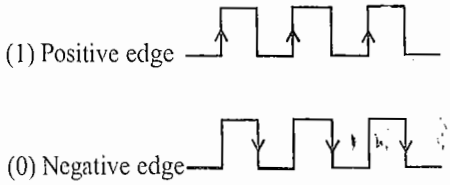
20.

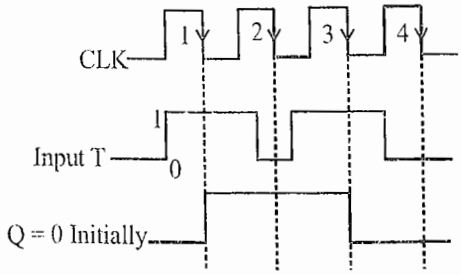
A clock pulse may be either positive or negative. A positive clock source remains at 0 during the interval between pulses and goes 0 to 1 during the occurrence of a pulse. The pulse goes through two signal transitions; from 0 to 1 and return from 1 to 0.9n figure 1 and 2, positive transition is defined as the positive edge and the negative transition as the negative edge.

Soln.

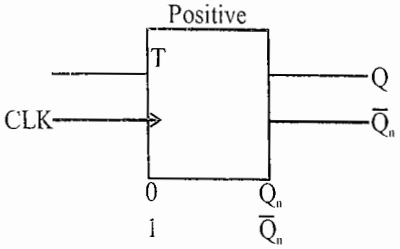
Time Diagram Representation:



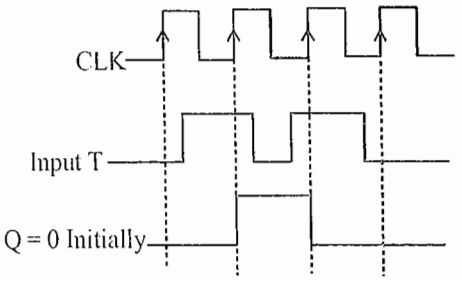




21.

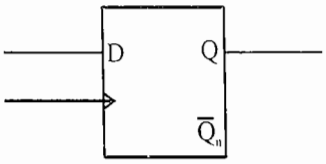


If we take positive edge:

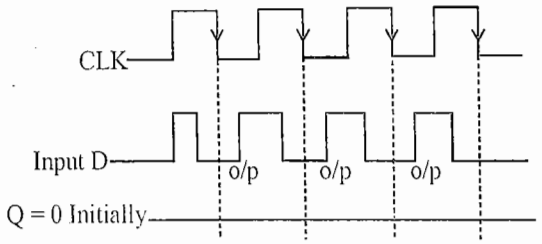


19. For negative edge draw the time diagram of D Flip-Flop?

Soln.



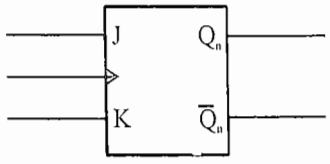
For negative edge draw time diagram of D type flip flop.



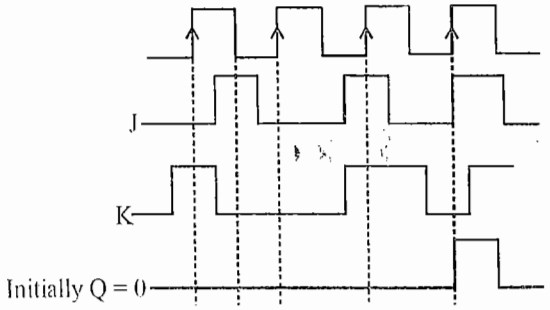
If D is high then output is high. If D is low output is low.

20. For the positive clock pulse find the timing diagram of JK flip flop.

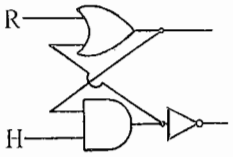
Soln.



Time diagram of above flip flop.



21. Consider a latch circuit shown in figure below, which of the following let of input is invalid for circuit.



(a) R = 0, H = 0 (b) R = 0, H = 1 (c) R = 1, H = 1 (d) R = 1, H = 0

Soln.

R	H	Q	Q or Q^{n+1}
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	X
1	0	1	X
1	1	0	1
1	1	1	1

Counters

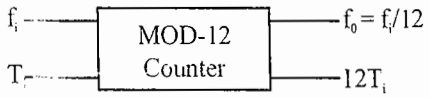
1. Asynchronous or ripple or serial
2. Synchronous or parallel or fast
3. (i) Ring counter (ii) Twisted tail or thomson or mobious (Type of shift registers)

1. **Asynchronous Counter:** No, common clock-clock is output of previous flip-flop.
2. In synchronous counter common clock is used.

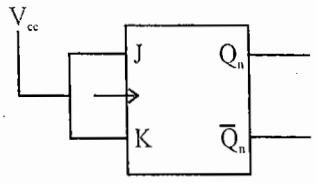
22. What is meaning of MOD-12 counter $\Rightarrow$ number of states are 12.

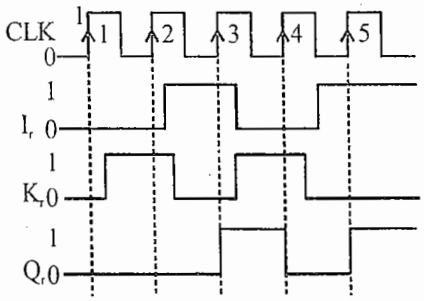
1. 0–11 $\rightarrow$ 12 states
2. 2–13 $\rightarrow$ 12 states
3. 3–14 $\rightarrow$ 12 states
4. 1–12 $\rightarrow$ 12 states

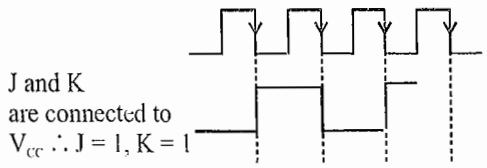
MOD 12 means divide by 12.



Asynchronous Counter:







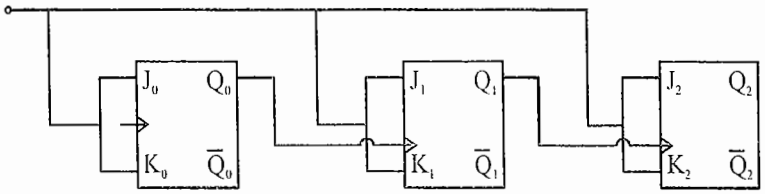
Note:

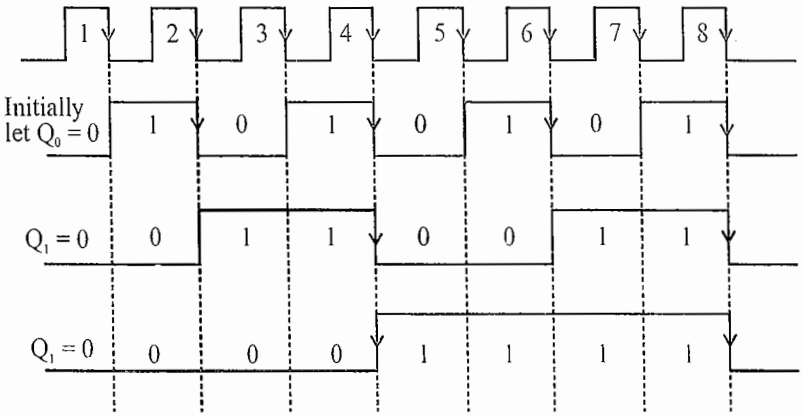
1. Total number of flip-flop required for Mod-N counter $N = 2^n$.
2. 3 bit means MOD-8 counter $\Rightarrow$ MOD $8 = 2^3$ means 3 Flip-Flop required.
3. 4 bit $\rightarrow$ 16 MOD $\rightarrow 2^4 \rightarrow$ 4 Flip Flop required

23.

Soln.

MOD-8 Asychronous Counter:



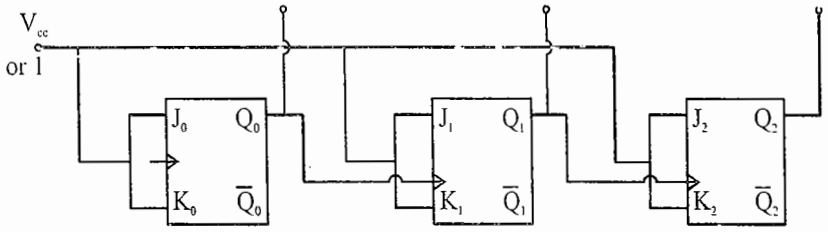


Truth Table

CLK	Q_2	Q_1	Q_0
1	0	0	0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0
6	1	0	1
7	1	1	0
8	1	1	1

Edge → Positive → (i) up counter (ii) Down counter

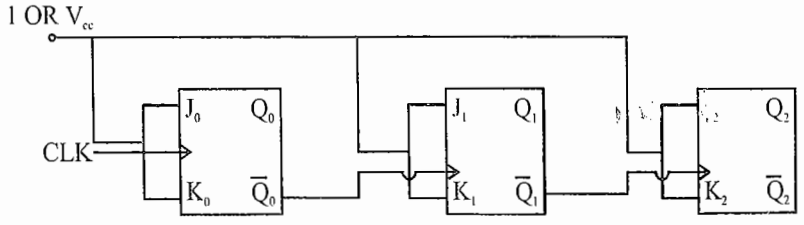
Edge → Negative → (i) up counter (ii) Down counter



Q_2, Q_1, Q_0 are standard output

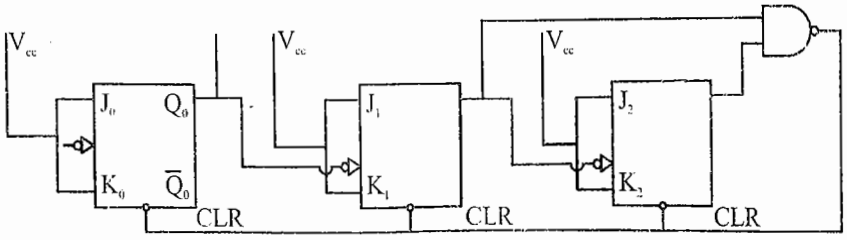
Case (i): If the output is of first flip-flop is given as circuit to next flip-flop it will act as up counter.

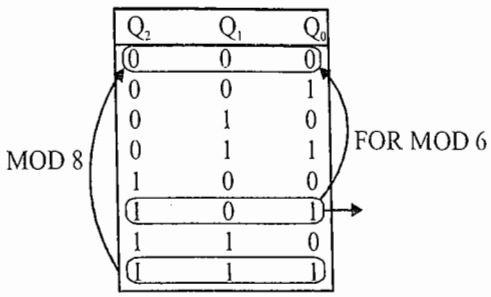
Case (ii): If $\bar{Q}$ of 1st flip flop is given as circuit to next flip-flop it will act as down counter.



23. Design MOD-6 UP Counter:

Soln.





Design gate in such a manner that 110 goes to 000 we use NAND gate for MOD-6. NAND gate output will clear all flip-flops.

25.

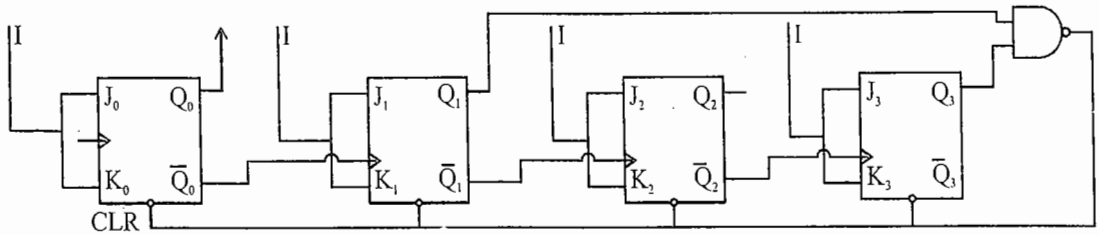
Synchronous Counter:

(i) Common clock is there (ii) There are fast

Widely used If MOD is in form of 2N then design is simple. If MOD is not in form of 2N then design by use of K-map.

Example: MOD-10 UP counter.

Soln.



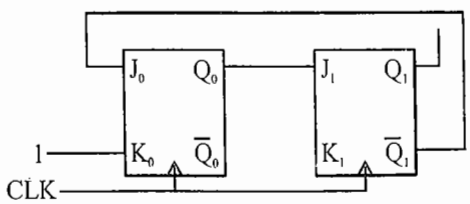
Truth Table

26.

Q_3	Q_2	Q_1	Q_0	
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	→ Remove

24. Find MOD of the counter:

Soln.



(a) 1 (b) 2 (c) 3 (d) 4

Soln. Module of counter $\rightarrow 3$, $J_0 = \bar{Q}_1$, $\bar{J}_1 = Q_0$, $K_0 = 1$, $K_1 = 1$

Let initially counter is at $\begin{matrix} Q_1 & Q_0 \\ 0 & 0 \end{matrix}$

i.e. $J_0 = 1$ $J_1 = 0$

$K_0 = 1$ $K_1 = 1$

After one clock pulse

$Q_0 = 1,\ Q_1 = 0,\ J_0 = 1,\ J_1 = 1,\ K_0 = 1,\ K_1 = 1$

After two clock pulse

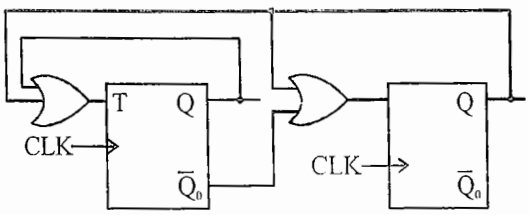
$Q_0 = 0,\ Q_1 = 1,\ J_0 = 0,\ J_1 = 0,\ K_0 = 1,\ K_1 = 1, Q_0 = 0, Q_1 = 1$

So reading

0	0	0	0
1	0	0	1
0	1	1	0
0	0	0	0

MOD-3 Counter

25. The circuit shown in figure below is



(a) a MOD-2 counter

(b) A MOD-3 counter

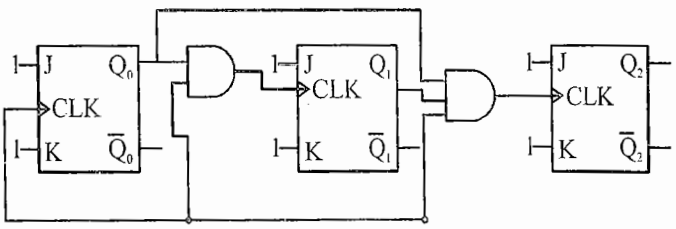
(c) Generate sequence 00, 10, 01, 01 ...

(d) Generate sequence 00, 10, 00, 00 ....

Soln. The truth table is shown below:

Present State		Flip Flop Input		Next State	
Q_A	Q_B	T_A	T_B	Q_A^+	Q_B^+
0	0	0	1	0	1
0	1	1	1	1	0
1	0	1	0	0	0
1	1	1	1	0	0

26. Consider a sequential circuit shown in figure. Initially all the flip-flop are reset output $Q_0\ Q_1\ Q_2$ after 5^{th} clock pulse is

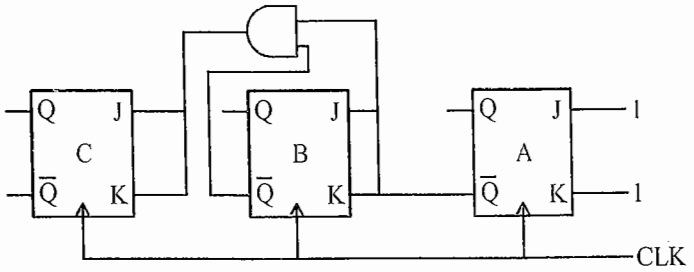


(a) 100 (b) 101 (c) 110 (d) 111

Soln. This is a 3 bit counter, so the output sequence is

CLK	Q_2	Q_1	Q_0
Initially	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

27. The counter shown in figure below is a



(a) MOD-8 up counter
(b) MOD-8 down counter
(c) MOD-6 up counter
(d) MOD-6 down counter

Soln.

FFC	*FFB*	*FFA*	
$JK\overline{C}$	$JK\overline{B}$	$JK\overline{A}$	$C^+B^+A^+$
111	111	111	111
000	000	110	110
000	110	111	101
000	001	110	100
111	111	111	011
001	000	110	010
001	110	111	001
000	001	110	000

SHIFT REGISTER

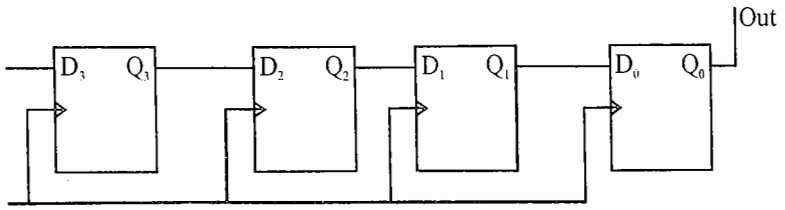
Register's are group of flip-flop.

To store *n*-bits *n*-bits *n*-flip-flop are required in register.

Depending upon input and output registers can be classified as

(1) SISO [Serial input serial output]
(2) SIPO [Serial input parallel out]
(3) PISO [Parallel in serial output]
(4) PIPO [Parallel input parallel output]

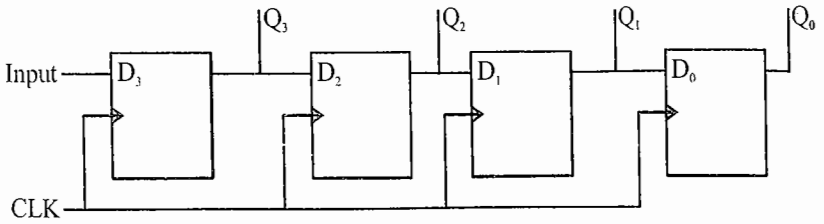
4-Bit SISO



To provide *n*-bit data out $(n-1)$ click pulse required.

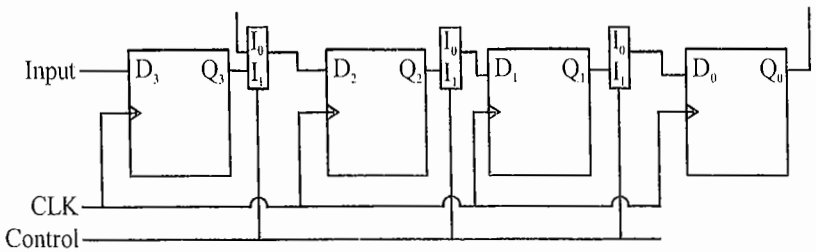
To store *n*-bit data *n*-click pulse required.

SIPO (4-Bit)



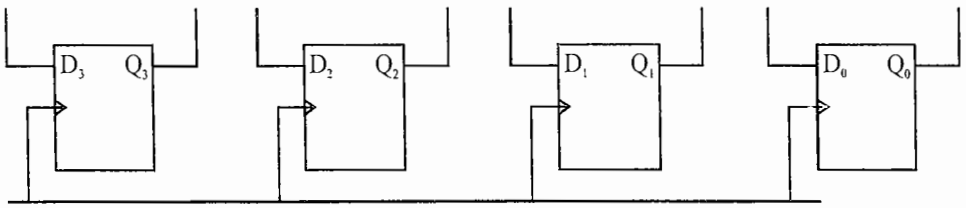
To provide *n*-bit data in *n*-clk pulse required, to provide parallel out no circuit pulse required.

PISO

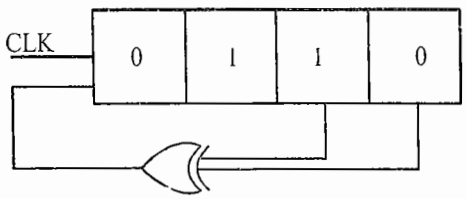


Control 0 → Parallel input, Control 1 → Serial output

PIPO

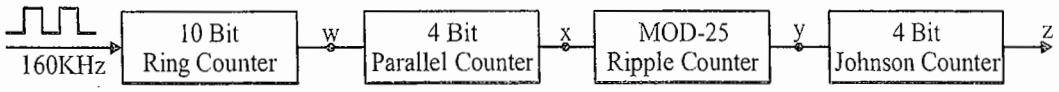


28. Initial contents of 4-bit SIPO, ring shift register, shown in figure is 0110. After 3 clock pulses are applied, what are contents of shift register.



Soln. After 1st clock → 1011, 2nd clock → 0101, 3rd clock → 1010.
So content are 1010.

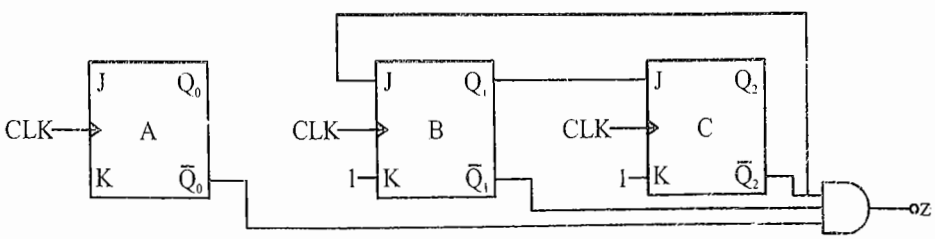
29. The frequency of the pulse at Z in the N/W. Show in figure below is



(a) 10Hz (b) 160Hz (c) 40Hz (d) 5Hz

Soln. 10-bit ring counter is a MOD-10, so it divides the 160 KHz input by 10. Therefore, w = 16KHz. The four bit parallel counter is a MOD-16. Thus, the frequency at x = 1 KHz, the MOD - 25 ripple counter produces a frequency at y = 40Hz. (1Khz / 25 = 40Hz). The four bit Johnson counter is a MOD-8. This the frequency at z = 5 Hz.

30. Consider a sequential circuit using three J-K flip-flop and one AND gate shown in figure output of the circuit becomes '1' after every N-clock cycle. The value of N is



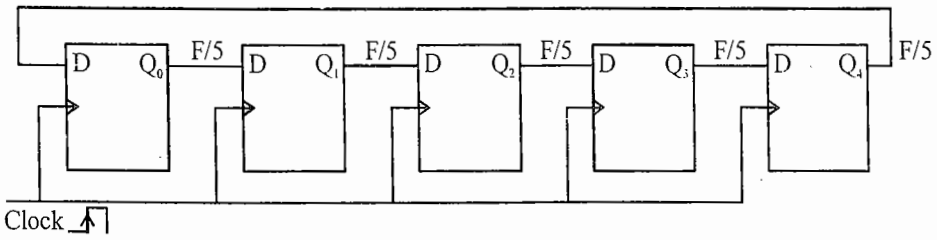
(a) 4 (b) 7 (c) 8 (d) 6

Soln. Let initially output is 1, then

CLK	Q_2	Q_1	Q_0	Z
Initially	0	0	0	1
1	1	1	0	0
2	0	0	1	0
3	1	0	0	0
4	0	1	0	0
5	1	0	1	0
6	0	0	0	

Ring Counter:

Design MOD-5 ring counter. After each 10 steps is reads again 0000.



Ring counter is shift register with feedback applied last flip-flop output Q to input of first flip flop.

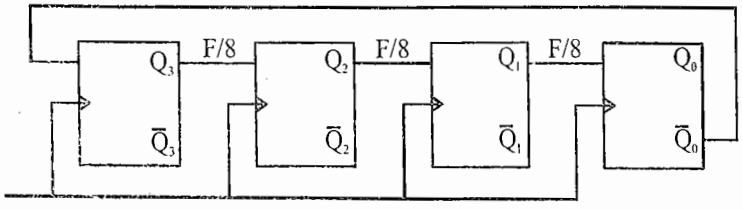
Ring counter is one bit is logic one and it will rotate with clock.

In n-bit ring counter number of use state is n.

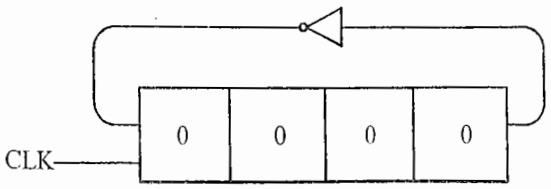
Number of unused states in n-bit ring counter is $2^n - n$.

CLK	Q_4	Q_3	Q_2	Q_1	Q_0	
0	0	0	0	0	0	
1	1	0	0	0	0	
2	0	1	0	0	0	
3	0	0	1	0	0	5 State
4	0	0	0	1	0	
5	0	0	0	0	1	
6	1	0	0	0	0	
7	0	1	0	0	0	
8	0	0	1	0	0	5 State
9	0	0	0	1	0	
10	0	0	0	0	1	

Johnson Counter or (Twisted Ring Counter) or Switch Tail Counter or Creeping Counter or Mobies Counter or Walking Counter.



Equivalent Circuit:



Truth Table :

CLK	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
8	0	0	0	0

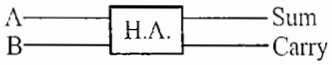
In Johnson counter with *n*-flip-flop maximum possible states are 2n states or maximum uses states.

Unused states are $2^n - 2n$.

50% duty cycle.

When a Johnson counter is working in uses state the operation frequency $f/2n$.

1. Half Adder:

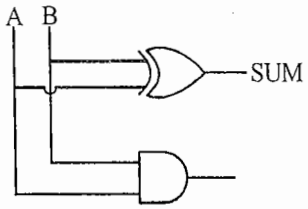


2. Truth Table:

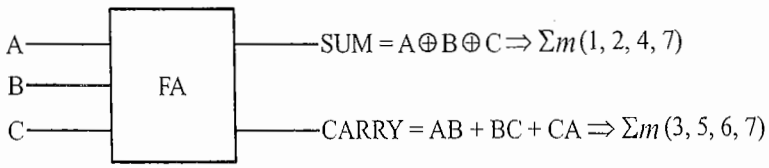
A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Logical expression SUM = $\bar{A}B + A\bar{B} = A \oplus B$, Carry = $A.B$

3. Logic Diagram:



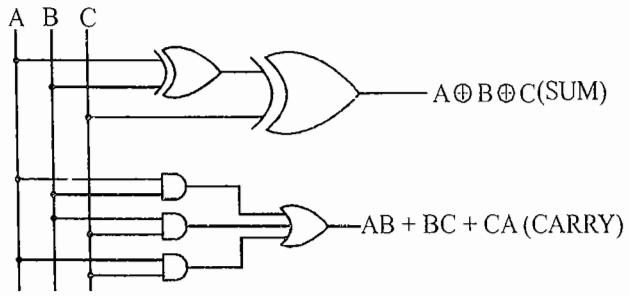
Full Adder:



Truth Table

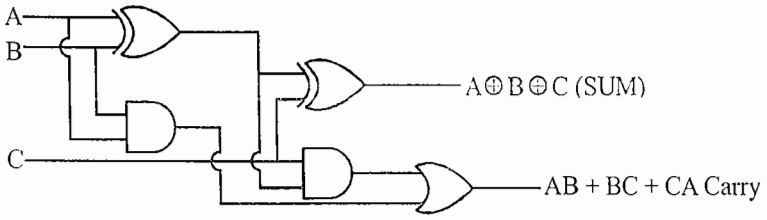
A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Logic Diagram:

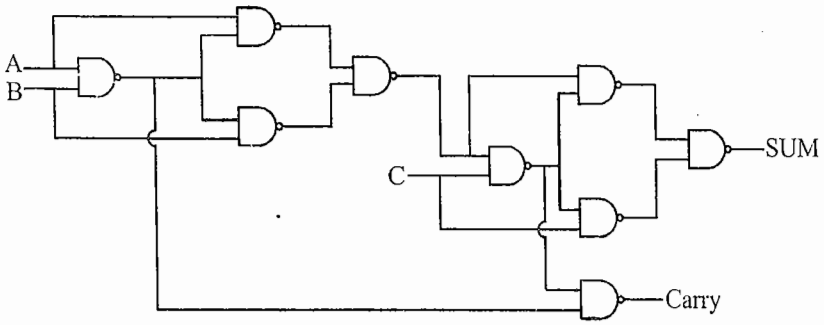


Note: In full adder, if all logic gates have same delay then to provide sum of carry output it require minimum 2 tpd delay.

Now Full Adder Using Half Adder: FA = 2HA + 1 OR gate

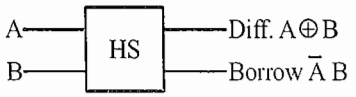


Full Adder Using NAND Gate:



9-NAND gate needed for FA circuit.

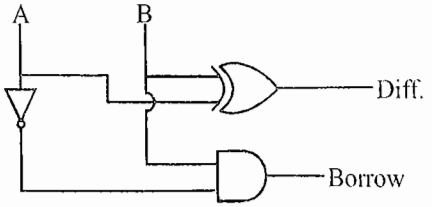
Half Subtractor:



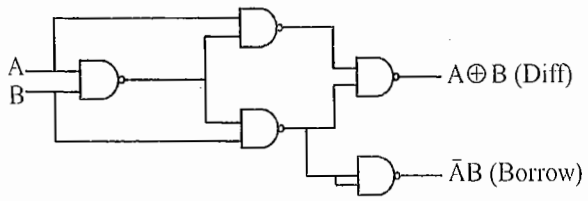
Truth Table:

A	B	Diff.	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

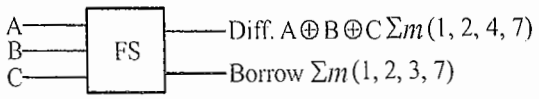
Logic Diagram:



HS Using NAND Gate:



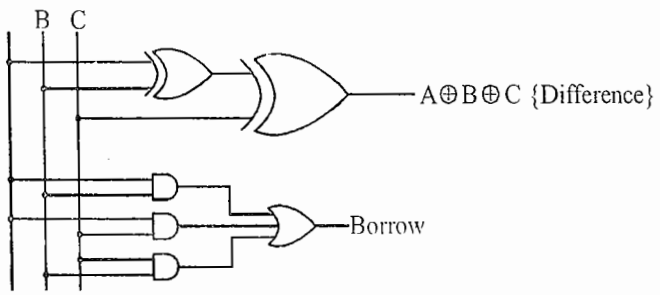
Full Subtractor:



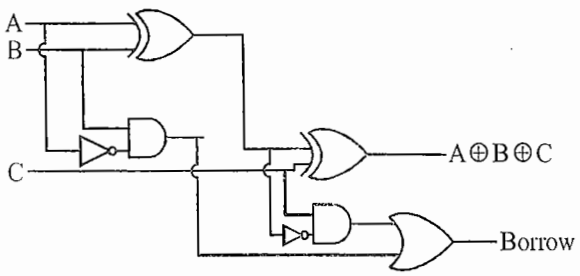
Truth Table:

A	B	C	Diff.	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Logic Circuit:

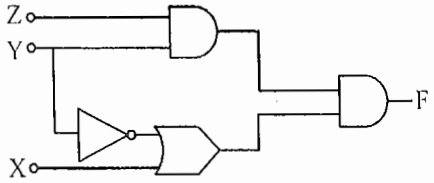


Full Subtracter Using Half Subtractor:



FS = 2HS + 1 OR gate

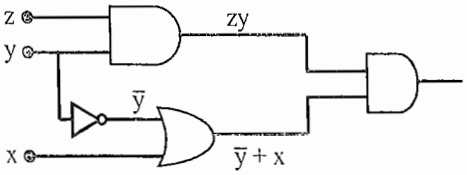
31. Identify the function F generated by the logic network shown **[GATE 2007]**



(a) $F=(X+Y)Z$ (b) $F=Z+Y+\bar{Y}X$

(c) $F=ZY(Y+X)$ (d) $F=XYZ$

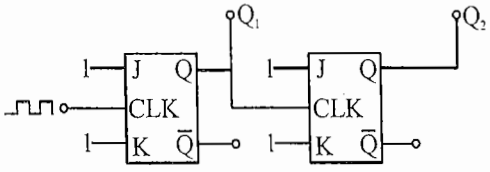
Soln.



$zy(\bar{y}+x)=xyz=F$

Correct option is (d)

32. In the circuit shown, the ports Q_1 and Q_2 are in the state $Q_1=1$, $Q_2=0$. The circuit is now subjected to two complete clock pulses. The state of these ports now becomes **[GATE 2007]**



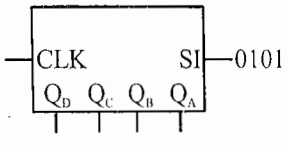
(a) $Q_2=1$, $Q_1=0$ (b) $Q_2=0$, $Q_1=1$

(c) $Q_2=1$, $Q_1=1$ (d) $Q_2=0$, $Q_1=0$

Soln. Since, j and k both are high. So, after giving clock pulse output will be complement.
Therefore, after first clock pulse Q_1 will be zero and Q_2 will be one and after second clock pulse Q_1 will be one and Q_2 will be one.

Correct option is (c)

33. The registers Q_D, Q_C, Q_B and Q_A shown in the figure are initially in the state 1010 respectively. An input sequence SI = 0101 is applied. After two clock pulses, the state of the shift registers (in the same sequence Q_D Q_C Q_B Q_A) is **[GATE 2007]**



(a) 1001 (b) 0100

(c) 0110 (d) 1010

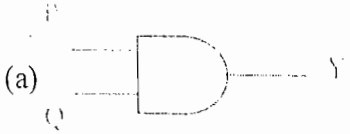
Soln.

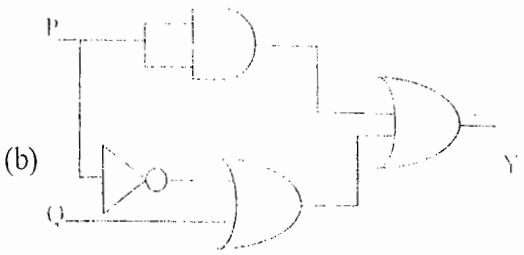
Clock pulse	Input	Q_A	Q_B	Q_C	Q_D
1	0	1	0	1	0
2	1	0	1	0	1
3	0	1	0	1	0

Correct option is (d)

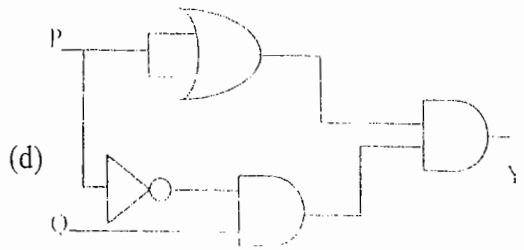
34. The simplest logic gate circuit corresponding to the Boolean expression, $Y = P + \bar{P}Q$ is

[GATE 2008]

(a) 

(b) 

(c) 

(d) 

Soln. We have, $y = P + \bar{P}Q = P \cdot 1 + \bar{P}Q = P(1+Q) + \bar{P}Q = P + PQ + \bar{P}Q = P + (P + \bar{P})Q = P + Q$

This is OR gate.

Correct option is (c)

35. An analog voltage V is converted into 2-bit binary number. The minimum number of comparators required and their reference voltages are

[GATE 2008]

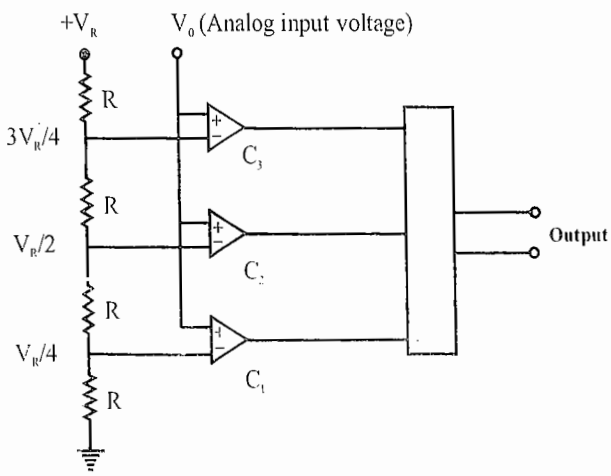
(a) $3, \left(\frac{V}{4}, \frac{V}{2}, \frac{3V}{4}\right)$

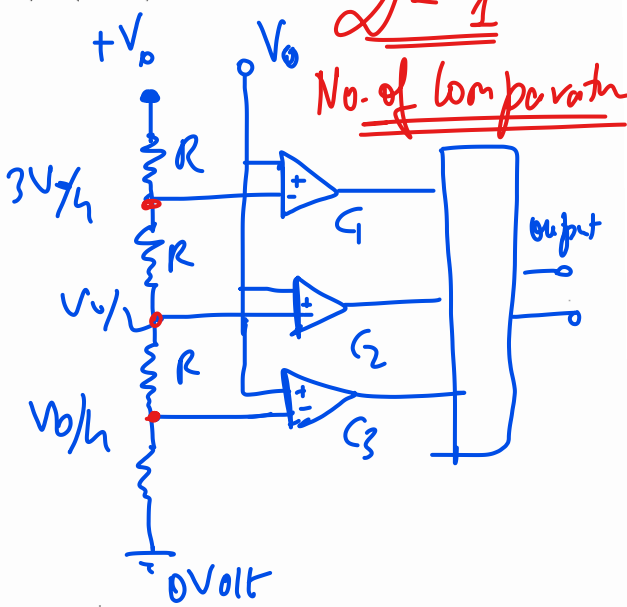
(b) $3, \left(\frac{V}{3}, \frac{2V}{3}, V\right)$

(c) $4, \left(\frac{V}{5}, \frac{2V}{5}, \frac{3V}{5}, \frac{4V}{5}\right)$

(d) $4, \left(\frac{V}{4}, \frac{V}{2}, \frac{3V}{4}, V\right)$

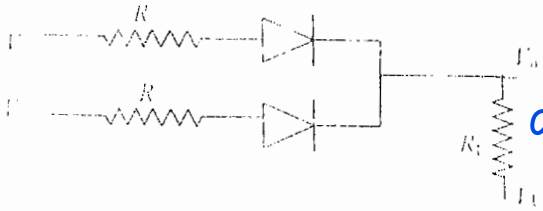
Soln. The components are required for an 2-bit converter is $(2^n - 1) = (2^2 - 1) = (4 - 1) = 3$





Correct option is (a)

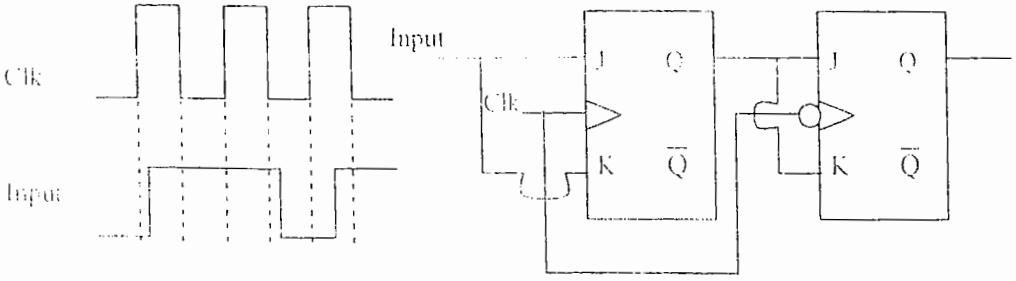
36. The following circuit (where $R_L >> R$) performs the operation of **[GATE 2008]**



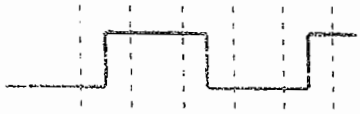
(a) OR gate for a negative logic system
(b) NAND gate for a negative logic system
(c) AND gate for a positive logic system
(d) AND gate for a negative logic system

Soln. OR (+ve) logic gate
AND (–ve) duality property.
Correct option is (d)

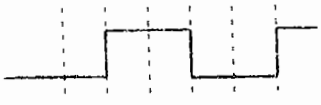
37. In the T type master-slave JK flip flop is shown along with the clock and input waveforms. The Q_n output of flip-flop was zero initially. Identify the correct output waveform. **[GATE 2008]**



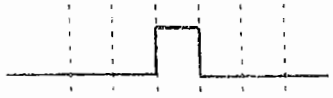
(a)



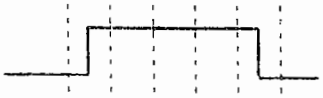
(b)



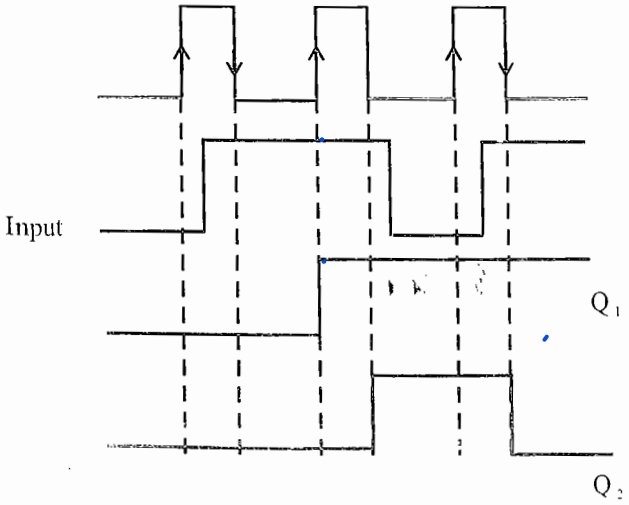
(c)



(d)



Soln.

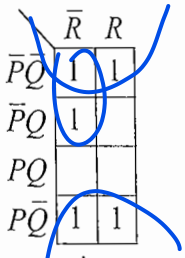


Truth table of T-flip-flip

input	output
0	Q_n
1	$\overline{Q}_n$

Statement for Linked Answer Q. 38 and Q.39 :

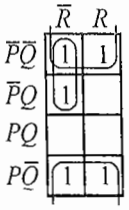
The Karnaugh map of a logic circuit is shown below: **[GATE 2009]**



38. The minimized logic expression for the above map is

(a) $Y = \bar{P}\bar{R} + \bar{Q}$ (b) $Y = \bar{Q} \cdot PR$ (c) $Y = \bar{Q} + PR$ (d) $Y = Q \cdot \overline{PR}$

Soln.

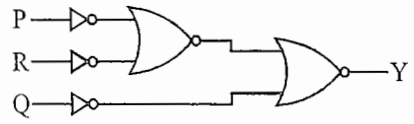


$y = P\bar{Q} + \bar{P}\bar{R} + P\bar{Q} = \bar{Q} + \bar{P}\bar{R}$

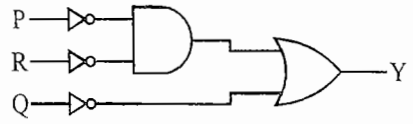
Correct option is (a)

39. The corresponding logic implementation using gates is given as :

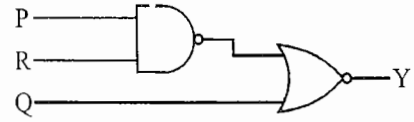
(a)



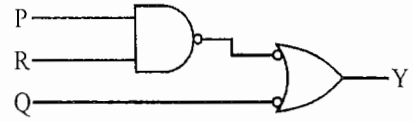
(b)



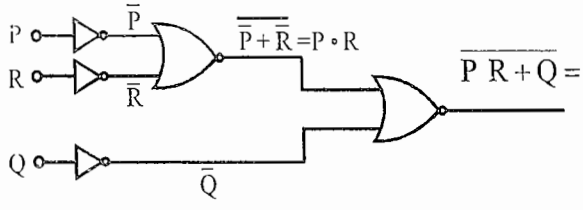
(c)



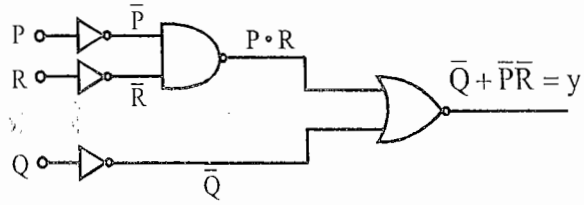
(d)



Soln.



$\overline{P\,R + Q} = \bar{Q} \cdot (\bar{P} + \bar{R}) = y$



Correct option is (b)

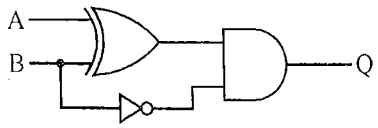
40. The voltage resolution of a 12-bit digital to analog converter (DAC), whose output varies from –10 V to +10 V is, approximately **[GATE 2010]**

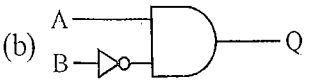
(a) 1 mV (b) 5 mV (c) 20 mV (d) 100 mV

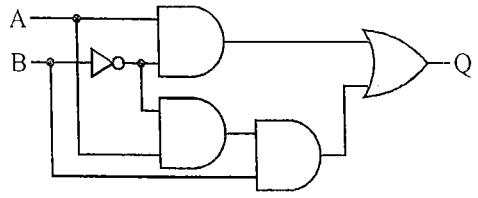
Soln. $\text{Resolution} = \dfrac{\text{full scale output voltage}}{\text{number of steps}} = \dfrac{20}{2^{12}} \simeq 5\,mV$

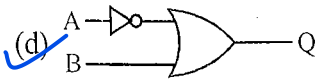
Correct option is (b)

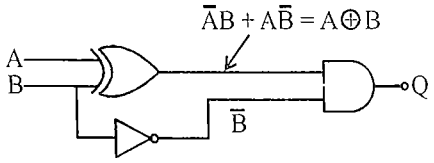
41. For any set of inputs A and B, the following circuits give the same output Q, except one. Which one is it ? **[GATE 2010]**

(a) 

(b) 

(c) 

(d) 

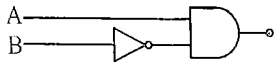
Soln. (a) 

$$Q = [A \oplus B] \cdot B$$

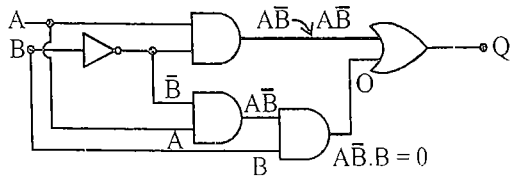
$$Q = [\bar{A}B + A\bar{B}]B$$

$$Q = \bar{A}B\bar{B} + A\bar{B} \cdot B \qquad \because x \cdot \bar{x} = 0$$

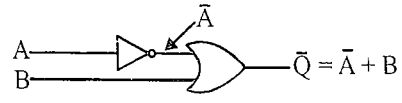
$$\boxed{Q = A\bar{B}} \qquad \because x \cdot x = x$$

(b) 

$Q = \boxed{A\bar{B}}$

(c) 

$\boxed{Q = A\bar{B}}$

(d) 

Q of (d) CKT is different rest all are same i.e. $A\bar{B}$

Correct option is (d)

42. The following Boolean expression **[GATE 2011]**

$Y = A \cdot \bar{B} \cdot \bar{C} \cdot \bar{D} + \bar{A} \cdot B \cdot \bar{C} \cdot D + \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot D + \bar{A} \cdot \bar{B} \cdot C \cdot D + \bar{A} \cdot B \cdot C \cdot D + A \cdot \bar{B} \cdot \bar{C} \cdot D$

can be simplified to

(a) $\bar{A} \cdot \bar{B} \cdot C + A \cdot \bar{D}$ (b) $\bar{A} \cdot B \cdot \bar{C} + A \cdot \bar{D}$ (c) $A \cdot \bar{B} \cdot \bar{C} + \bar{A} \cdot D$ (d) $A \cdot \bar{B} \cdot C + \bar{A} \cdot D$

Soln. $y = A\bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C}D + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}CD + \bar{A}BCD + A\bar{B}\bar{C}D$

$$= \bar{A}\bar{C}D\left(B + \bar{B}\right) + \bar{A}CD\left(\bar{B} + B\right) + A\bar{B}\bar{C}\left(D + \bar{D}\right)$$

$$= \bar{A}\bar{C}D + \bar{A}CD + A\bar{B}\bar{C}$$

$$= \bar{A}D\left(\bar{C} + C\right) + A\bar{B}\bar{C} = A\bar{B}\bar{C} + \bar{A}D$$

Correct option is (c)

43. A voltage regulator has ripple rejection of –50dB. If input ripple is 1mV, what is the output ripple voltage in μ V? The answer should be up to two decimal places _____ **[GATE 2013]**

Soln. ripple $_{dB} = -50$ dB

$20 \log [\text{ripple}] = -50$

$[\text{ripple}]_{\text{regulation}} = 3.162 \times 10^{-3}$

$$\text{Ripple regulation} = \frac{\text{o/p voltage}}{\text{i/p voltage}}$$

$$3.162 \times 10^{-3} = \frac{\text{o/p voltage}}{1 \times 10^{-3}}$$

$$\boxed{\text{o/p voltage} = 3.162\,\mu\text{v}}$$

44. What should be the clock frequency of a 6-bit A/D converter so that its maximum conversion time is $32\mu s$?

[GATE 2013]

(a) 1 MIz (b) 2 MHz (c) 0.5 MHz (d) 4 MHz

Soln. 6-bit A to D converter

C_T : Conversion time maximum = 32 μ sec

Note: Not mention which type of A/D converter

$\boxed{C_T = nTc}$ $\boxed{C_T = 2^n Tc}$

nT_c $2^n T_c$

Flash type (faster) > Successive approximation > Counter type > Dual slope OR Integrating type (Slower)

$C_T = 2^n Tc$, n : 6 bit

$32 \times 10^{-6} = 2 \times T_c$

$$T_c = \frac{1}{2} \times 10^{-6}$$

$$\boxed{f_c = \frac{1}{T_c} = \frac{2}{10^{-6}} = 2MHz}$$

Correct option is (b)

45. The minimum number of flip-flops required to construct a mod-75 counter is _____

[GATE 2014]

Soln. Let n number flip-flop is require for mod - 75 counter

$\therefore \quad 2^n = 75$

$\Rightarrow \quad n \simeq 7$

46. In order to measure a maximum of 1 V with a resolution of 1mV using a n-bit A/D converter, working under the principle of ladder network, the minimum value of n is _____ **[GATE 2014]**

Soln. We know resolution of n bit ADC is given by

$$\text{resolution} = \frac{\text{full scale of output}}{\text{number of step}}$$

$$\Rightarrow \quad 1\,mV = \frac{1V}{2^n}$$

$$\Rightarrow \quad 2^n = \frac{1V}{1\,mV} = 1000$$

$$\therefore \quad n = 10$$

Correct answer is (10)

47. Which one of the following DOES NOT represent an exclusive OR operation for inputs A and B?

[GATE 2015]

(a) $(A+B)\overline{AB}$ (b) $A\overline{B} + B\overline{A}$ (c) $(A+B)(\overline{A}+\overline{B})$ (d) $(A+B)AB$

Soln. (a) $y = (A+B)\overline{AB} = (A+B)(\overline{A}+\overline{B}) = \overline{A}B + \overline{B}A$ *X – OR gate*

(b) $y = \overline{A}B + A\overline{B}$ is XOR gate

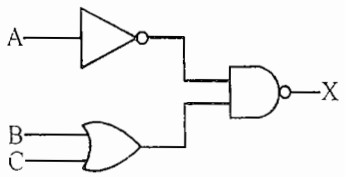
(c) $y = (A+B)(\overline{A}+\overline{B}) = \overline{A}B + A\overline{B}$ is XOR gate

(d) $y = (A+B)(AB) = AB + AB = AB$ is not X-OR gate

Correct optino is (d)

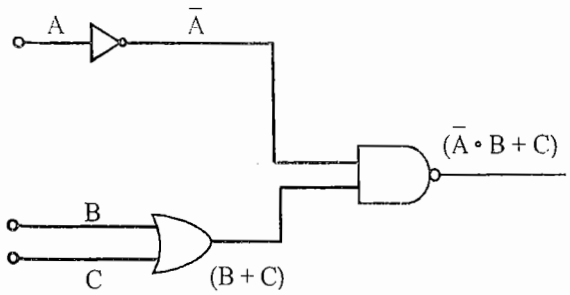
48. For the digital circuit given below, the output X is

[GATE 2016]



(a) $\overline{\overline{A}+B\cdot C}$ (b) $\overline{\overline{A}\cdot(B+C)}$ (c) $\overline{A}\cdot(B+C)$ (d) $A+\overline{(B\cdot C)}$

Soln.



Correct option is (b)

Chapter 9

Microprocessor

→ It is an electronic chip that have computing and decision making ability.

→ It is an integrated electronic chip that fetch instruction from memory execute then and provide result.

Bus: It is group of parallel combination of metal wires that is used interface two different devices.

Main memory is also called as RAM

Program is always stored in RAM.

ROM system software is stored.

Micro Controller: It is the example of ASIC design (Application specific integrated chip).

Machine Language: Commands written in the form of binary pattern such language is called as machine language.

Assembly Language: It commands written in the form of English language than, it is called as "Mnemonics" such type of language is called as Assembly language.

LANGUAGE:

Low Level Language: Assembly language and machine language are low level languages.

High Level Language: Ex. C, C^{++}, JAVA etc.

Compiler: Read whole program at once and produce its object code that is executed by microprocessor. It is only a software.

Interpreter: Read one instruction at one time and produce it to be the object that is executed by microprocessor.

Microprocessor	Bit of Microprocessor	Technology used
4004	4	P MOS
8008	8	N MOS
8080	8	N MOS
8085	8	N MOS
8086	16	C MOS

8085 is improved version of 8080.

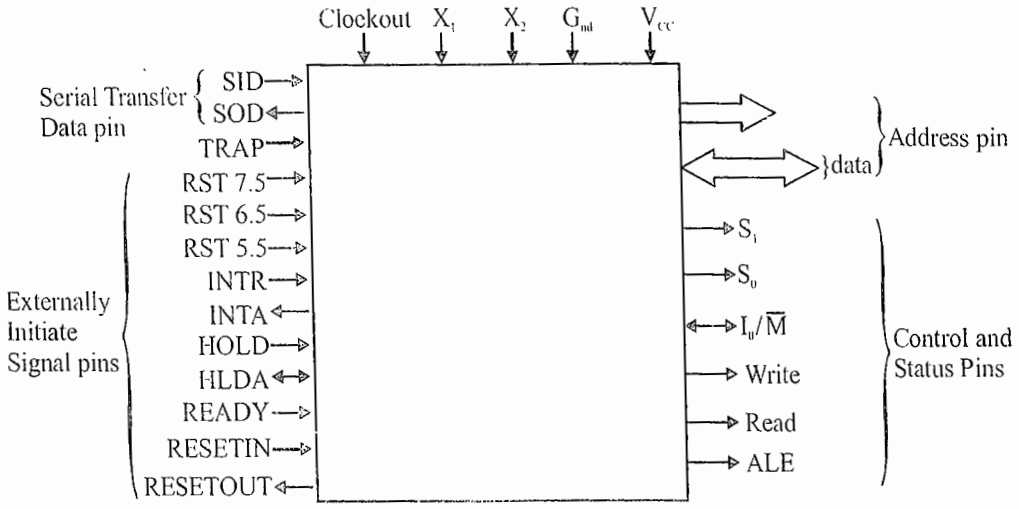
Numbers of bits executed by microprocessor at a time is also called 1 machine cycle.

Size of ALU is known as size of accumulator called is bits of processor.

Speed of Processor: $\boxed{S \propto \frac{1}{\text{Execution Time}} \propto f}$

8085 Architecture:

- It is a 40p in I_C, Pin number 20 is ground pid
- Number chip enable is available.



Interrupts:

(1) Trap (2) RST 7.5 (3) RST 6.5 (4) RST 5.5 (5) INTR

Internal Architecture:

1. ALU (Arithmetic Logic Unit)
   (a) accumulator (b) Resistors (c) Register array
2. Timing and control
3. Interrupt control circuit

Registers:

1. General purpose registers: B, C, D, E, H, L all are 8 bits.
2. Special purpose registers

(a) HL pair used as memory pointer

(b) USER register/general purpose register

(c) Accumulator register {8 bit}

(d) States register (flag resister's) (8 bit)

(e) Stack pointer (16 bit)

(f) Program counter (PC) (16 bit)

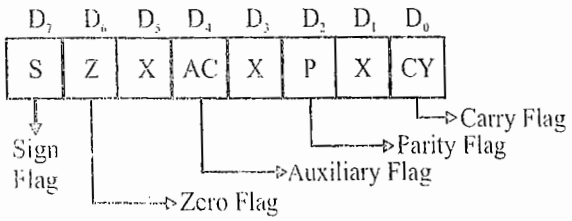
User not Accessible:

(a) Temporary register (8 bits)

(b) Interrupt register (8 bit)

(c) Latches (16 bits)

Status Register / Flag Register:



Accumulator Register: 8-bit special type of registers. It performs arithmetic and logic operations.

Addressing Mode's:

(a) Register Addressing Mode: Address of data given in form of register in the instruction.

MOV B, C, XRA, B

(b) Direct Addressing Mode: If address of data directly given in the instruction ≅ direct addressing mode Ex: IN 25H.

(c) Immediate Addressing Mode: Ex. MVI B, 2FH

(d) Indirect Register Addressing Mode: Ex. MOV B, M

(e) Implicit / Implied Addressing Mode:

If address of data not required in the instruction then it is called as implicit addressing mode.

Ex. NOP, CMA, HLT.

Few Instruction Sets:

(1) ADD:

Ex. ADD R→any register A, B, C, D, E, H, L, M

[A] ← [A] + [R], [ ]→ Content of register.

(2) ADI, 8 bit data: [A] ← [A] + 8 bit data

(3) SUBR: [A] ← [A] – [R]

(4) SUIR: [A] ← [A] -8 bits data

(5) INR, R: [R] ← [R] + $1_{(LSB)}$

(6) DCR, R: [R] ← [R] - $I_{(LSB)}$

Logical Instructions:

1. **AND R:** [A]←[A] AND [R]
2. **ORA, R:** [A]←[A] OR [R]
3. **XRA, R:** [A] ← [A]⊕[R]

CMA: Complement of Accumulator Register: [A]←[$\bar{A}$]

HLT: Halt of stop execution.