Kuldeep Singh

ELECTRONICS

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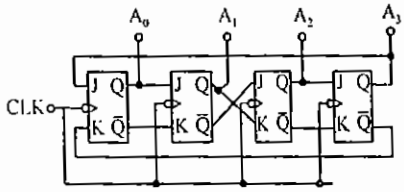
CSIR-UGC-NET Previous Years' Questions

1. A counter consists of four flip-flops connected as shown in the figure. **[NET Dec. 2011]**



If the counter is initialized as $A_0\ A_1\ A_2\ A_3 = 0110$, the state after the next clock pulse is

(a) 1000 (b) 0001 (c) 0011 (d) 1100

2. If one of the inputs of a J-K flip flop is high and the other is low, then the outputs Q and $\bar{Q}$

(a) oscillate between low and high in race-around condition **[NET Dec. 2013]**

(b) toggle and the circuit acts like a T flip flop

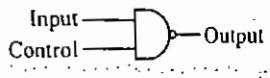
(c) are opposite to the inputs

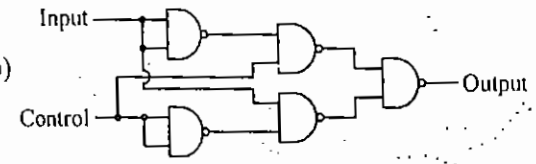
(d) follow the inputs and the circuit acts like an R-S flip flop

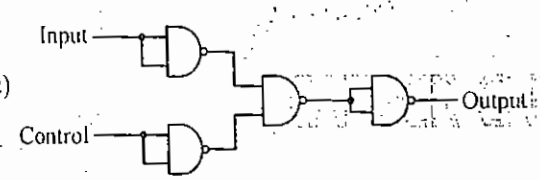
3. A 4-variable switching function is given by $f = \Sigma(5,7,8,10,13,15) + d(0,1,2)$, where d is the do-not-care-condition. The minimized form of f in sum of products (SOP) form is **[NET Dec. 2013]**

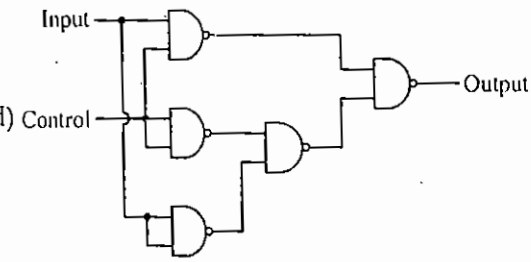
(a) $\bar{A}\bar{C} + \bar{B}\bar{D}$ (b) $A\bar{B} + C\bar{D}$ (c) $AD + BC$ (d) $\bar{B}\bar{D} + BD$

4. Which of the following circuits behaves as a controlled inverter? **[NET June 2015]**

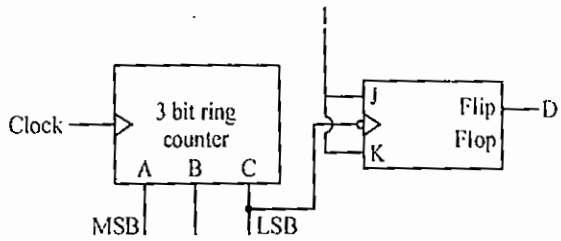
(a)


(b)


(c)


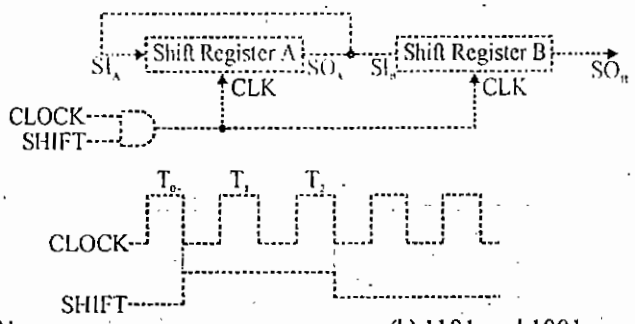
(d)


5. For the logic circuit given below, the decimal count sequence and the modulus of the circuit corresponding to A B C D are **[NET June 2015]**



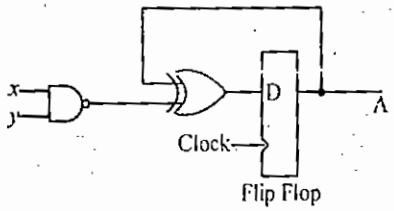
(a) $8 \to 4 \to 2 \to 1 \to 9 \to 5$ (mod 6) (b) $8 \to 4 \to 2 \to 9 \to 5 \to 3$ (mod 6)
(c) $2 \to 5 \to 9 \to 1 \to 3$ (mod 5) (d) $8 \to 5 \to 1 \to 3 \to 7$ (mod 5)

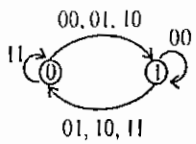
6. In the schematic figure given below, the initial values of 4 bit shift registers A and B are 1011 and 0010 respectively. The values of SO_A and SO_B after the pulse T_2 are respectively. **[NET Dec. 2015]**

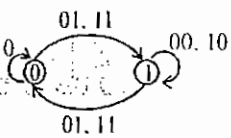


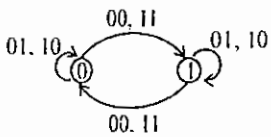
(a) 1110 and 1001 (b) 1101 and 1001
(c) 1101 and 1100 (d) 1110 and 1100

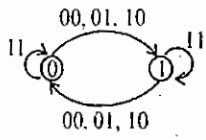
7. The state diagram corresponding to the following circuit is **[NET Dec. 2015]**



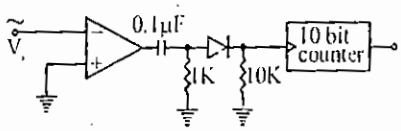
(a) 

(b) 

(c) 

(d) 

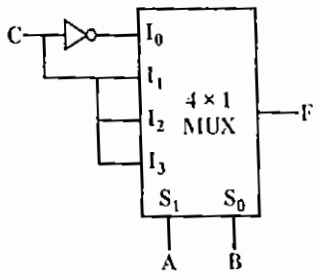
8. A sinusoidal signal of peak to peak amplitude 1 V and unknown time period is input to the following circuit for 5 seconds duration. If the counter measures a value $(3E8)_{H}$ in hexadecimal then the time period of the input signal is **[NET Dec. 2015]**



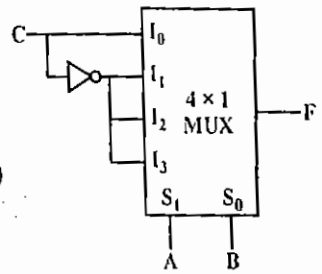
(a) 2.5 ms (b) 4 ms (c) 10 ms (d) 5 ms

9. Which of the following circuits implements the Boolean function $F(A, B, C) = \Sigma(1, 2, 4, 6)$? [NET Dec. 2016]

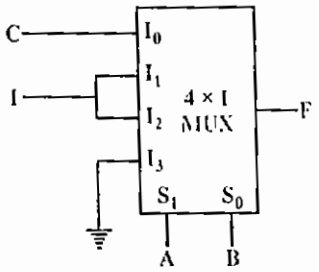
(a)



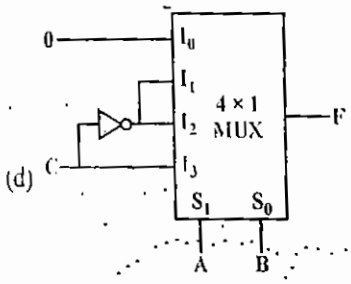
(b)



(c)

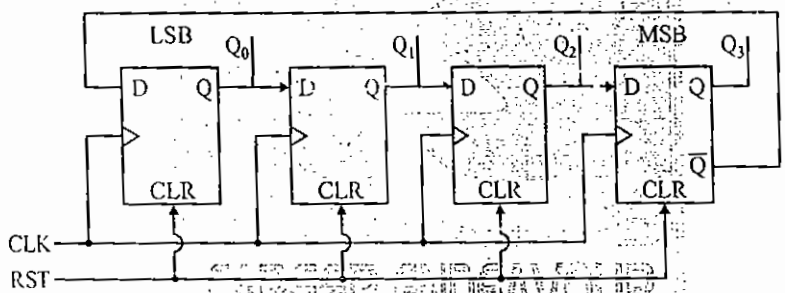


(d)



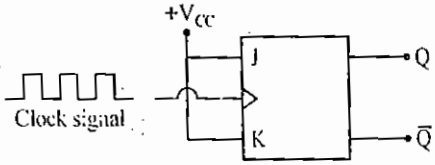
10. A 2 × 4 decoder with an enable input can function as a [NET June 2017]
(a) 4 × 1 multiplexer (b) 1 × 4 demultiplexer
(c) 4 × 2 encoder (d) 4 × 2 priority encoder

11. The circuit below comprises of D-flip flops. The output is taken from Q_3, Q_2, Q_1 and Q_0, as shown in the figure.



The binary number given by the string $Q_3\,Q_2\,Q_1\,Q_0$ changes for every clock pulse that is applied to the CLK input. If the output is initialized at 0000, then the corresponding sequence of decimal numbers that repeats itself, is [NET Dec. 2017]
(a) 3, 2, 1, 0 (b) 1, 3, 7, 14, 12, 8
(c) 1, 3, 7, 15, 12, 14, 0 (d) 1, 3, 7, 15, 14, 12, 8, 0

12. In the following JK flip-flop circuit, J and K inputs are tied together to $+V_{CC}$. If the input is a clock signal of frequency f, the frequency of the output Q is [NET June 2018]



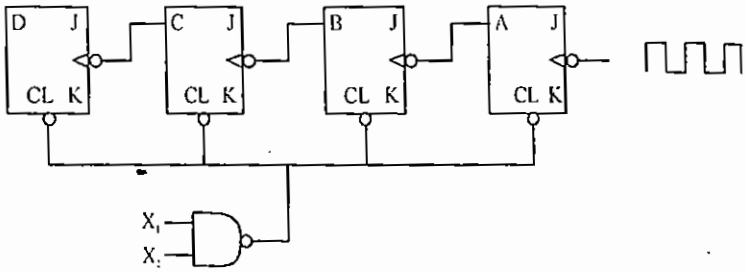
(a) f (b) $2f$ (c) $4f$ (d) $f/2$

ANSWER KEY

1. (b)	2. (d)	3. (d)	4. (b)	5. (b)	6. (d)	7. (d)
8. (d)	9. (b)	10. (b)	11. (d)	12. (d)		

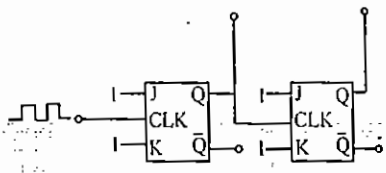
GATE Previous Years' Questions

1. A ripple counter designed with JK flip-flops provided with CLEAR (CL) input is shown in the figure. In order that this circuit functions as a MOD-12 counter, the NAND gate input (X_1 and X_2) should be



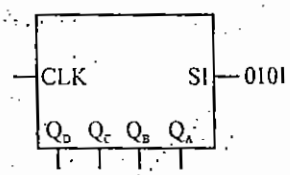
(a) A and C (b) A and D (c) B and D (d) C and D [GATE 2006]

2. In the circuit shown, the ports Q_1 and Q_2 are in the state $Q_1 = 1, Q_2 = 0$. The circuit is now subjected to two complete clock pulses. The state of these ports now becomes [GATE 2007]



(a) $Q_2 = 1, Q_1 = 0$ (b) $Q_2 = 0, Q_1 = 1$ (c) $Q_2 = 1, Q_1 = 1$ (d) $Q_2 = 0, Q_1 = 0$

3. The registers Q_D, Q_C, Q_B and Q_A shown in the figure are initially in the state 1010 respectively. An input sequence SI=0101 is applied. After two clock pulses, the state of the shift registers (in the same sequence $Q_D\ Q_C\ Q_B\ Q_A$) is: [GATE 2007]



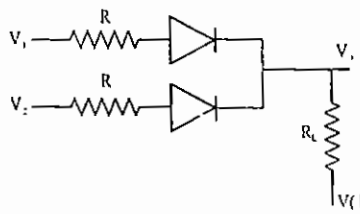
(a) 1001 (b) 0100 (c) 0110 (d) 1010

4. An analog voltage V is converted into 2-bit binary number. The minimum number of comparators required and their reference voltages are [GATE 2008]

(a) $3, \left(\frac{V}{4}, \frac{V}{2}, \frac{3V}{4}\right)$ (b) $3, \left(\frac{V}{3}, \frac{2V}{3}, V\right)$

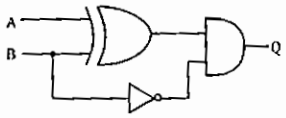
(c) $4, \left(\frac{V}{5}, \frac{2V}{5}, \frac{3V}{5}, \frac{4V}{5}\right)$ (d) $4, \left(\frac{V}{4}, \frac{V}{2}, \frac{3V}{5}, V\right)$

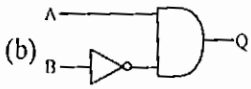
5. The following circuit (where $R_L >> R$) performs the operation of [GATE 2008]

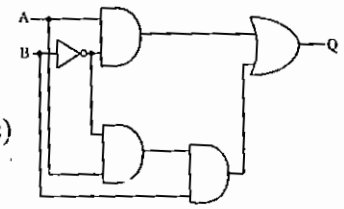


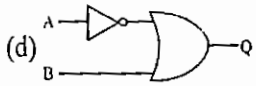
(a) OR gate for a negative logic system (b) NAND gate for a negative logic system.
(c) AND gate for a positive logic system. (d) AND gate for a negative logic system.

6. For any set of inputs, A and B, the following circuits give the same output Q, except one. Which one is it? [GATE 2010]

(a) 

(b) 

(c) 

(d) 

7. The following Boolean expression [GATE 2011]

$Y = A \cdot \bar{B} \cdot \bar{C} \cdot \bar{D} + \bar{A} \cdot B \cdot \bar{C} \cdot D + \bar{A} \cdot \bar{B} \cdot C \cdot D + \bar{A} \cdot \bar{B} \cdot \bar{C} \cdot D + \bar{A} \cdot B \cdot C \cdot D + A \cdot \bar{B} \cdot \bar{C} \cdot D$

can be simplified to .

(a) $\bar{A} \cdot \bar{B} \cdot C + A \cdot \bar{D}$ (b) $\bar{A} \cdot B \cdot \bar{C} + A \cdot \bar{D}$ (c) $A \cdot \bar{B} \cdot \bar{C} + \bar{A} \cdot D$ (d) $A \cdot \bar{B} \cdot C + \bar{A} \cdot D$

ANSWER KEY

1. (d) 2. (c) 3. (a) 4. (a) 5. (d) 6. (d) 7. (c)

TIFR Previous Years' Questions

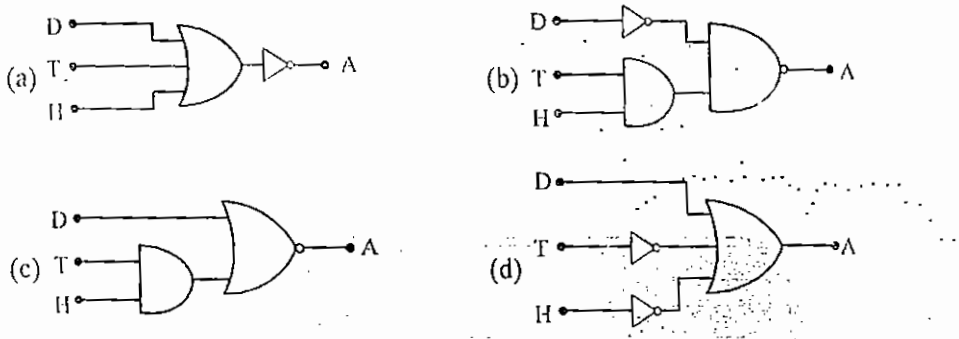
1. A control circuit needs to be designed to save on power consumption by an air-conditioning unit A in a windowless room with a single door. The room is fitted with the following devices: **[TIFR 2014]**

   (1) A temperature sensor T, which is enabled (T = 1) whenever the temperature falls below a pre-set value;

   (2) A humidity sensor H, which is enabled (H = 1) whenever the humidity falls below a certain pre-set value;

   (3) A sensor D on the door, which is triggered (D = 1) whenever the door opens

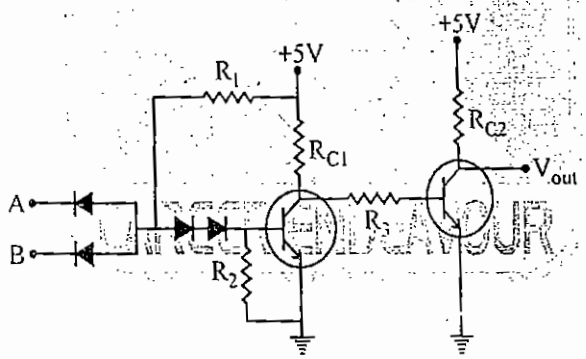
   Which of the following logical circuits will turn the air-conditioning unit off (A = 0) whenever the door is opened or when the both temperature and humidity are below their pre-set values?



2. To measure the voltage in the range 0 – 5 V with a precision of 5 mV, the minimum number of bits required in a digital voltmeter is **[TIFR 2015]**

   (a) 9 (b) 10 (c) 11 (d) 12

3. Which digital logic gate is mimicked by the following diode and silicon transistor circuit? **[TIFR 2017]**

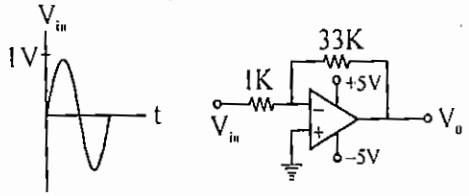


ANSWER KEY

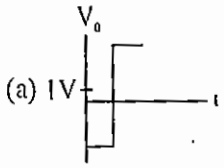
1. (c) 2. (b) 3. (AND gate)

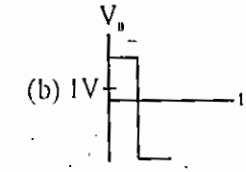
CSIR-UGC-NET Previous Years' Questions

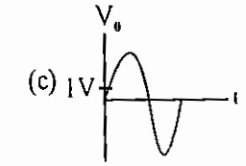
1. For the OP-AMP circuit shown in the figure below, which is the correct output waveform?

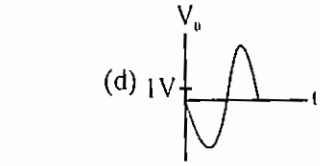


[NET Dec. 2010]

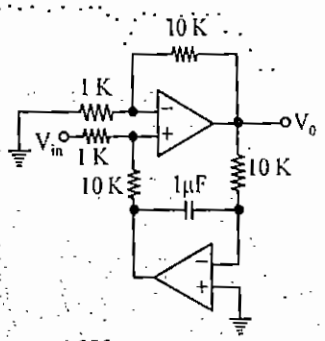
(a) 

(b) 

(c) 

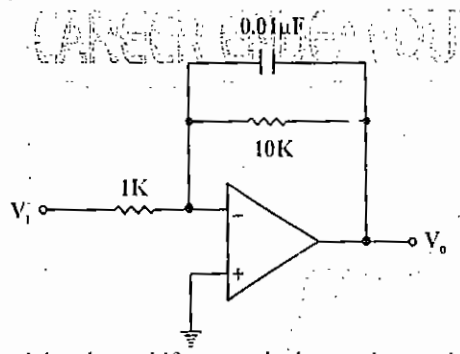
(d) 

2. A time varying signal V_{in} is fed to an op-amp circuit with output signal V_0 as shown in the figure below. The circuit implements a [NET June 2011]



(a) High pass filter with cutoff frequency 16 Hz.
(b) High pass filter with cutoff frequency 100 Hz
(c) Low pass filter with cutoff frequency 16 Hz
(d) Low pass filter with cutoff frequency 100 Hz.

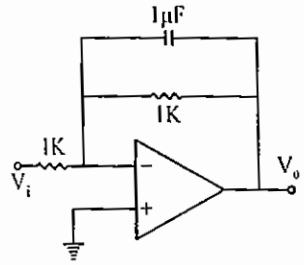
3. In the op-amp circuit shown in the figure, V_i is a sinusoidal input signal of frequency 10 Hz and V_0 is the output signal. [NET Dec. 2012]



The magnitude of the gain and the phase shift, respectively, are close to the values

(a) $5\sqrt{2}$ and $\frac{\pi}{2}$ (b) $5\sqrt{2}$ and $\frac{-\pi}{2}$ (c) 10 and zero (d) 10 and π

4. Consider the op-amp circuit shown in the figure. [NET Dec. 2013]

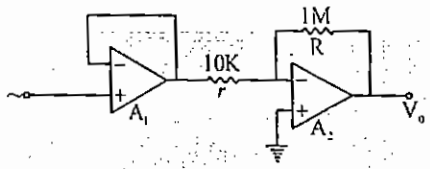


If the input is a sinusoidal wave $V_i = 5\sin(1000t)$, then the amplitude of the output V_0 is

(a) $\frac{5}{2}$ (b) 5 (c) $\frac{5\sqrt{2}}{2}$ (d) $5\sqrt{2}$

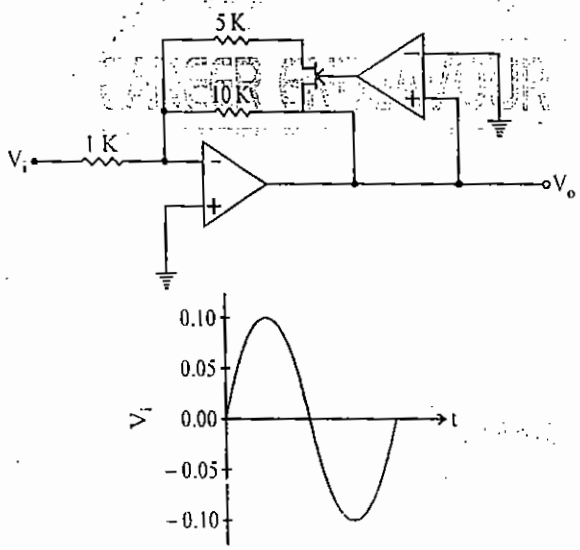
5. Consider the amplifier circuit comprising of the two op-amps A_1 and A_2 as shown in the figure

If the input ac signal source has an impedance of $50k\Omega$, which of the following statements is true?

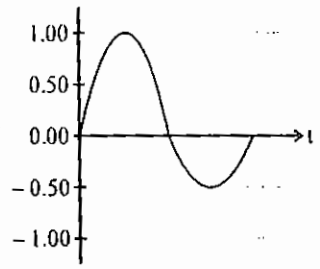


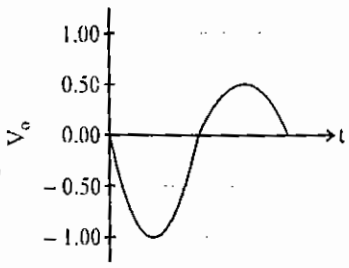
(a) A_1 is required in the circuit because the source impedance is much greater than r [NET Dec. 2014]
(b) A_1 is required in the circuit because the source impedance is much less than R
(c) A_1 can be eliminated from the circuit without affecting the overall gain
(d) A_1 is required in the circuit if the output has to follow the phase of the input signal

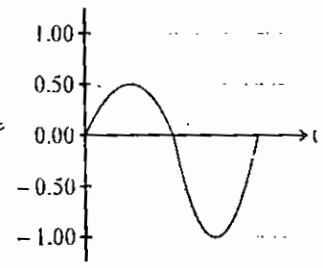
6. For the circuit and the input sinusoidal waveform shown in the figures below, which is the correct waveform at the output? [NET June 2015]

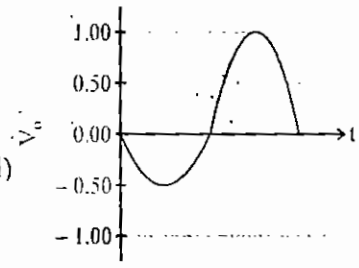


(The time scales in all the plots are the same).

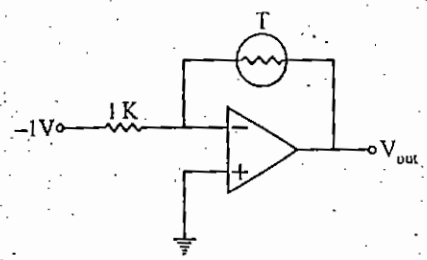
(a)


(b)


(c)


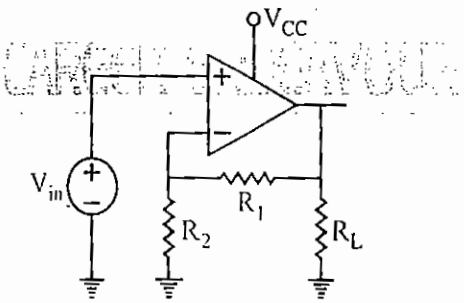
(d)


7. In the circuit given below, the thermistor has a resistance 3 kΩ at 25°C. Its resistance decreases by 150Ω per °C upon heating. The output voltage of the circuit at 30°C is **[NET June 2015]**



(a) –3.75 V (b) –2.25 V (c) 2.25 V (d) 3.75 V

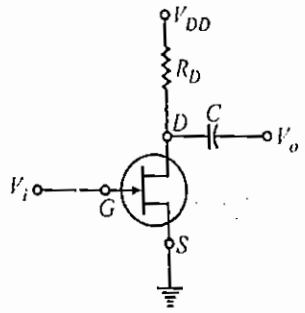
8. In the circuit below, the input voltage V_i is 2 V, $V_{cc} = 16$ V, $R_2 = 2$ kΩ and $R_L = 10$ kΩ.



The value of R_1 required to deliver 10 mW of power across R_L is **[NET Dec. 2016]**

(a) 12 kΩ (b) 4 kΩ (c) 8 kΩ (d) 14 kΩ

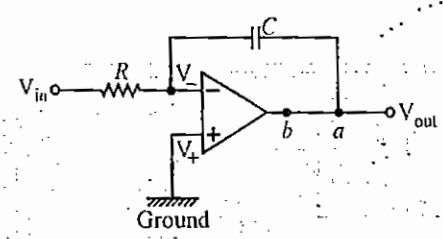
9. In the n-channel JFET shown in figure below, $V_i = -2V$, $C = 10\,pF$, $V_{DD} = +16\,V$ and $R_D = 2\,k\Omega$.



If the drain D-source S saturation current I_{DSS} is 10 mA and the pinch-off voltage V_P is –8V, then the voltage across points D and S is [NET June 2017]

(a) 11.125 V (b) 10.375 V (c) 5.75 V (d) 4.75 V

10. The gain of the circuit given below is $-\frac{1}{\omega RC}$. [NET June 2017]



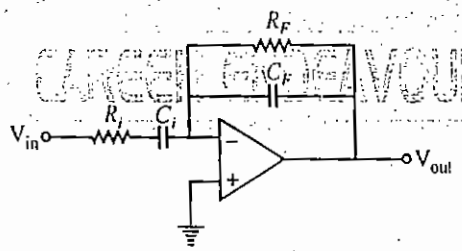
The modification in the circuit required to introduce a dc feedback is to add a resistor

(a) between a and b (b) between positive terminal of the op-amp and ground

(c) in series with C (d) parallel to C

11. In the following operational amplifier circuit $C_{in} = 10\,nF$, $R_{in} = 20\,k\Omega$, $R_F = 200\,k\Omega$ and $C_F = 100\,pF$.

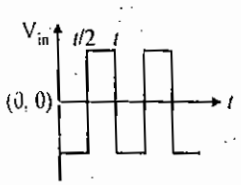
The magnitude of the gain at a input signal frequency of 16 kHz is [NET June 2017]

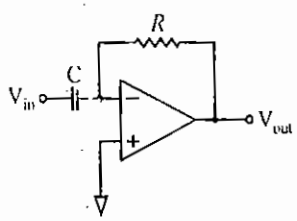


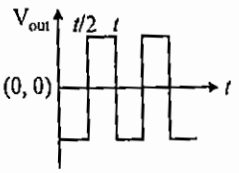
(a) 67 (b) 0.15 (c) 0.3 (d) 3.5

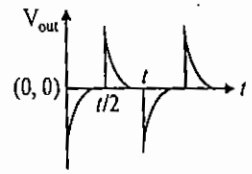
12. The input V_i to the following circuit is a square wave as shown in the following figure : [NET June 2018]

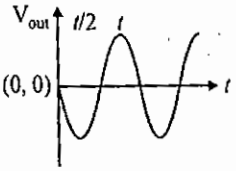
Which of the waveforms V_o best describes the output?

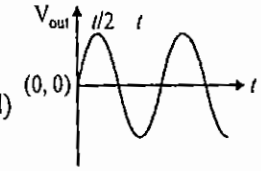




(a) 

(b) 

(c) 

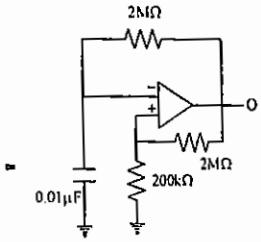
(d) 

ANSWER KEY

1. (a)	2. (a)	3. (b)	4. (c)	5. (a)	6. (b)	7. (c)
8. (c)	9. (d)	10. (d)	11. (4.45)	12. (b)		

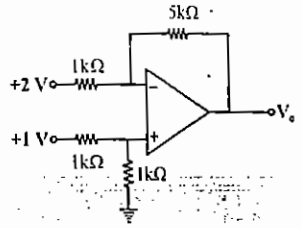
GATE Previous Years' Questions

1. A bistable multivibrator with a saturation voltage ±5V is shown in the diagram. The positive and negative threshold at the inverting terminal for which the multivibrator will switch to the other state are **[GATE 2003]**



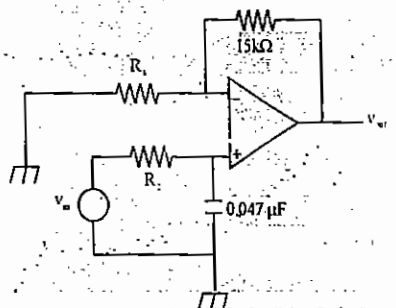
(a) ±5/11 V (b) ±10/11 V (c) ±5 V (d) ± 11V

2. The output V_0 of the ideal OP-AMP circuit shown in the figure is: **[GATE 2005]**



(a) –7V (b) –5 V (c) 5 V (d) 7 V

3. The low-pass active filter shown in the figure has a cut-off frequency of 2kHz and a pass band gain of 1.5. The values of the resistors are **[GATE 2006]**

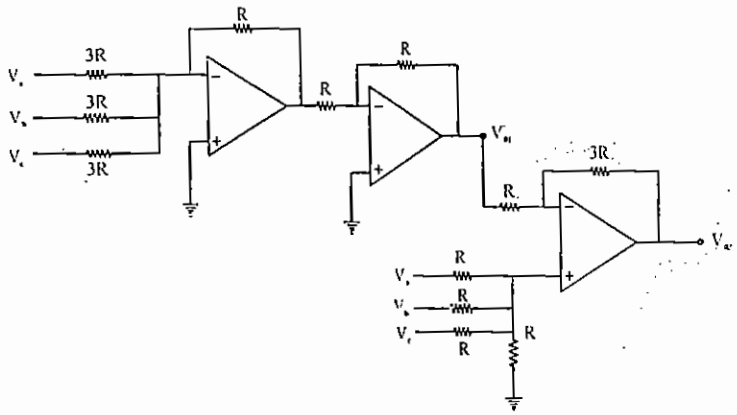


(a) $R_1 = 10k\Omega; R_2 = 1.3\ k\Omega$ (b) $R_1 = 30k\Omega; R_2 = 1.3\ k\Omega$

(c) $R_1 = 10k\Omega; R_2 = 1.7\ k\Omega$ (d) $R_1 = 30k\Omega; R_2 = 1.7\ k\Omega$

Statement for Linked Answer Q.4 and Q.5 **[GATE 2008]**

The following circuit contains three operational amplifiers and resistors.



4. The output voltage at the end of second operational amplifier V_{01} is:

(a) $V_{01} = 3(V_a + V_b + V_c)$ (b) $V_{01} = -\frac{1}{3}(V_a + V_b + V_c)$

(c) $V_{01} = \frac{1}{3}(V_a + V_b + V_c)$ (d) $V_{01} = \frac{4}{3}(V_a + V_b + V_c)$

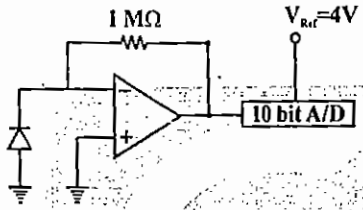
5. The output V_{02} (at the end of third OP-AMP) of the above circuit is:

(a) $V_{02} = 2(V_a + V_b + V_c)$ (b) $V_{02} = 3(V_a + V_b + V_c)$

(c) $V_{02} = -\frac{1}{2}(V_a + V_b + V_c)$ (d) Zero.

Statement for Linked Q.6 and Q.7 **[GATE 2010]**

Shown in the figure is a circuit to measure light intensity and convert it to a digital signal. The photodiode P has a responsivity of 0.1 A per watt of incident light intensity. The Op-amp converts the induced photocurrent to a voltage which is digitized by the 10-bit A/D converter with a reference voltage of 4 V.



6. For a light intensity of 25 μW incident on the photodiode, the voltage output of the OP-AMP is:

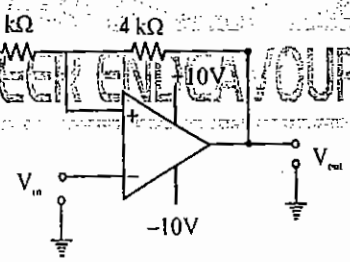
(a) 0.25 V (b) 1.0 V (c) 4.0 V (d) 2.5 V

7. The range of light intensity which can be measured by this set up is:

(a) 100 mW to 100 μW (b) 100 nW to 100 μW

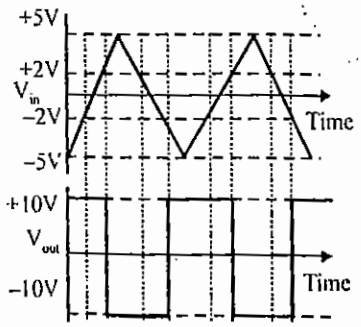
(c) 40 mW to 40 μW (d) 40 nW to 40 μW

8. Consider the following circuit **[GATE 2011]**

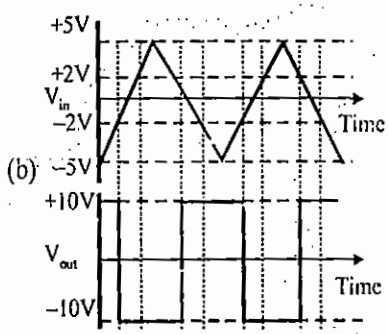


Which of the following represents the output V_{out} corresponding to the input V_{in}?

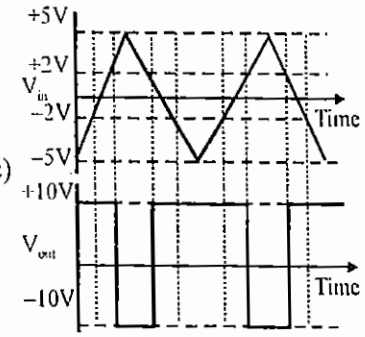
(a)



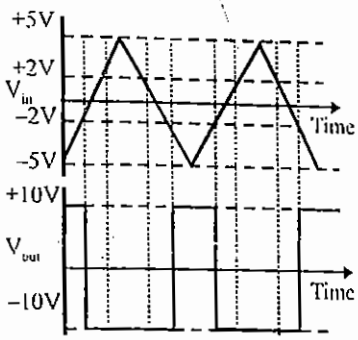
(b)



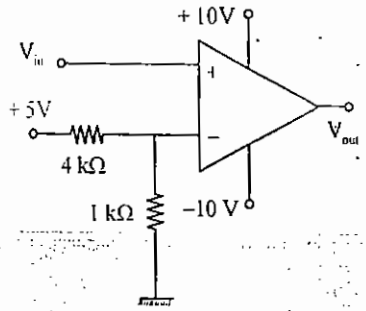
(c)



(d)

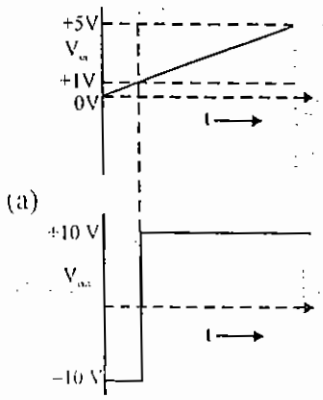


9. Consider the following OP-AMP circuit. **[GATE 2012]**

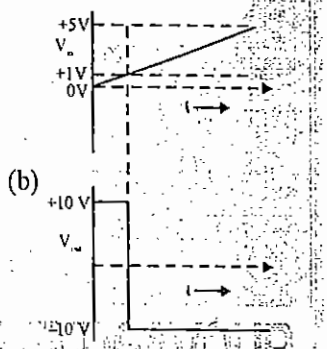


Which one of the following correctly represents the output V_{out} corresponding to the input V_{in} ?

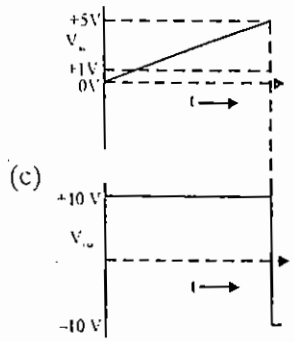
(a)



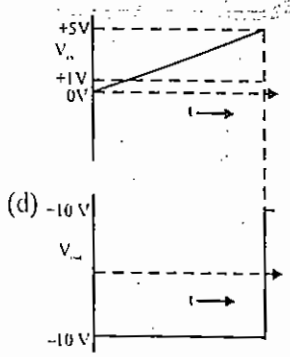
(b)



(c)

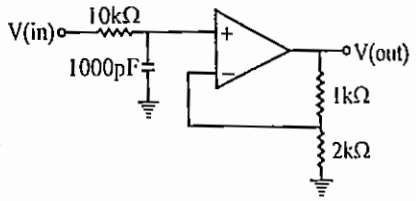


(d)



Statement for Linked Answer Q. 10 and Q. 11 : **[GATE 2013]**

Consider the following circuit



10. For this circuit the frequency above which the gain will decrease by 20*dB* per decade is
(a) 15.9 kHz (b) 1.2 kHz (c) 5.6 kHz (d) 22.5 kHz

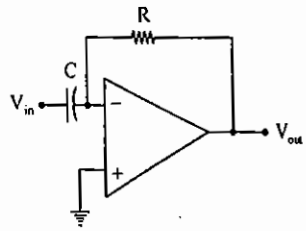
11. At 1.2 kHz the closed loop gain is
(a) 1 (b) 1.5 (c) 3 (d) 0.5

ANSWER KEY

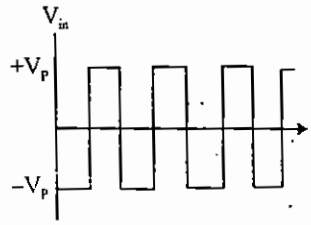
1. (a)	**2. (a)**	**3. (d)**	**4. (c)**	**5. (d)**	**6. (d)**	**7. (d)**
8. (a)	**9. (a)**	**10. (a)**	**11. (b)**			

TIFR Previous Years' Questions

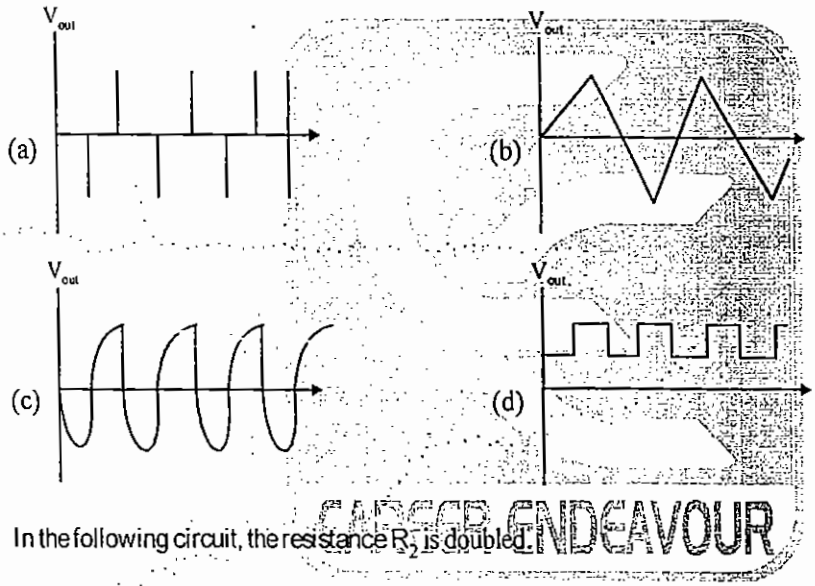
1. Consider the following circuit : **[TIFR 2012]**



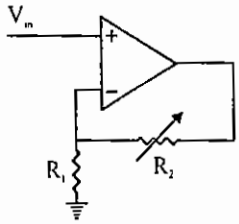
If the waveform given below is fed in at V_{in}



then the waveform at the output V_{out} will be



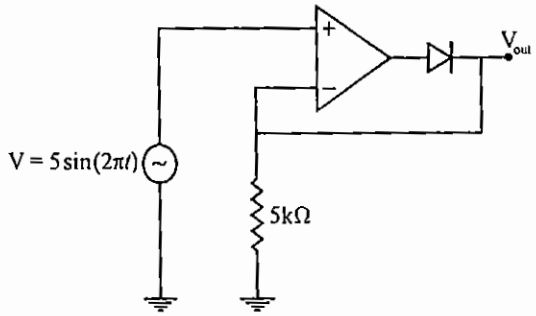
2. In the following circuit, the resistance R_2 is doubled. **[TIFR 2014]**



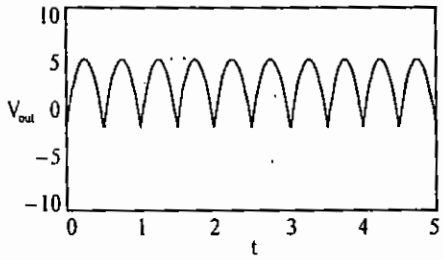
It follows that the current through R_2.

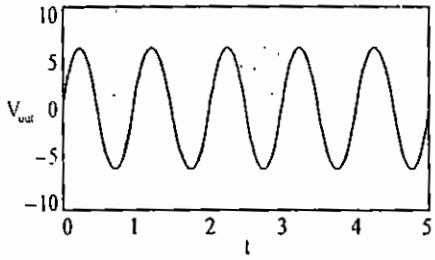
(a) remains the same
(b) is halved
(c) is doubled
(d) is quadrupled.

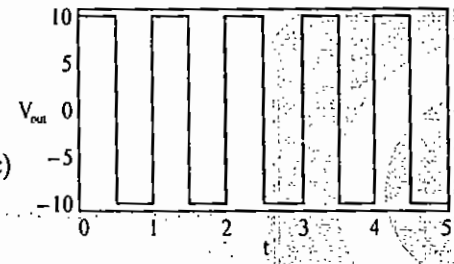
3. In the circuit shown below, the op-amp is powered by a bipolar supply of ±10 V. **[TIFR 2015]**

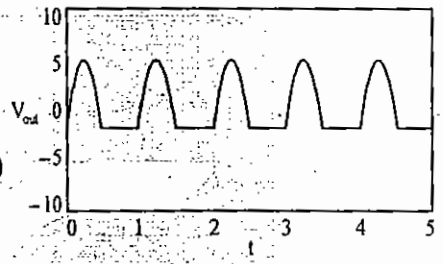


Which one of the following graphs represents V_{out} correctly?

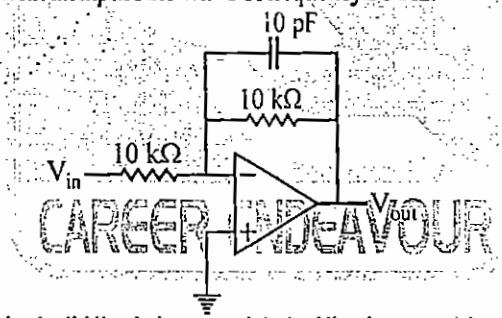
(a)


(b)


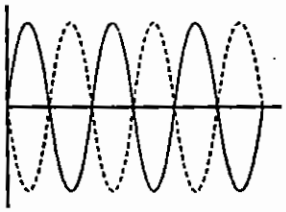
(c)


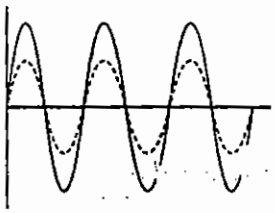
(d)


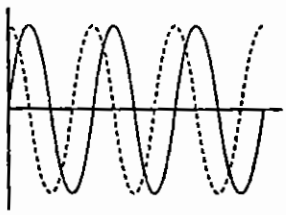
4. The following circuit is fed with an input sine wave of frequency 50 Hz.

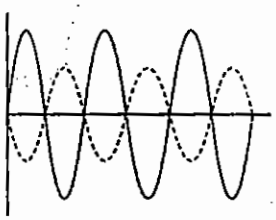


Which of the following graphs (solid line is input and dashed line is output) best represent the correct situation?

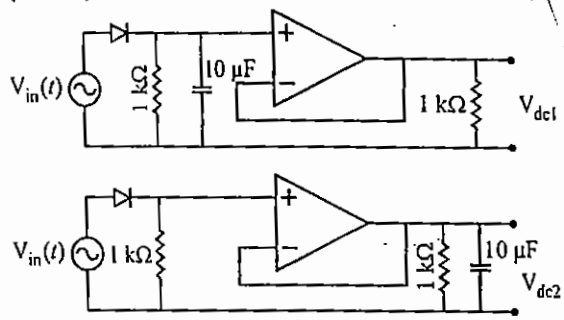
(a)


(b)


(c)


(d)


5. A signal $V_{in}(t) = 5\sin(100\pi t)$ is sent to both the circuits sketched below : **[TIFR 2018]**

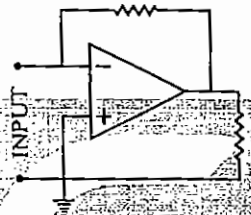


In the DC output voltage of the top circuit has a value V_{dc1} and the bottom circuit has a value V_{dc2}, then which of the following statements about the relative value of V_{dc1} and V_{dc2} is correct?

(a) $V_{dc1} > V_{dc2}$ (b) $V_{dc1} < V_{dc2}$

(c) $V_{dc1} = V_{dc2}$ (d) It will depend on the slew rate of the op-amp.

6. Consider the circuit shown on the right, which involves on op-amp and two resistors, with an input voltage marked INPUT. **[TIFR 2018]**



Which of the following circuit components, when connected across the input terminals, is most likely to create a problem in the normal operation of the circuit?

(a) A voltage source with very high Thevenin resistance.

(b) A current source with a very high Norton resistance.

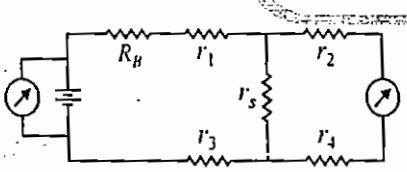
(c) A voltage source with a very low Thevenin resistance.

(d) A current source with a very low Norton resistance.

7. Which one of the following circuits, constructed only with resistors and voltmeters, will allow you to obtain the correct value of resistance r_s using the voltmeter readings? Note that the value of R_B is known while r_1, r_2, r_3, r_4 and r_s are all unknown. **[TIFR 2018]**

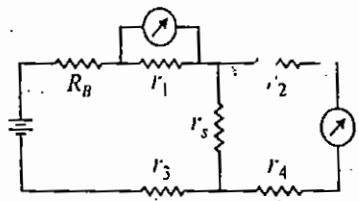
[Assume that the voltmeters and resistance are ideal].

(a)

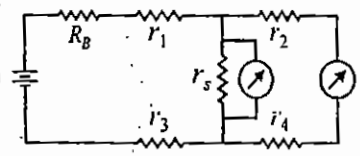


(b)

(c)



(d)

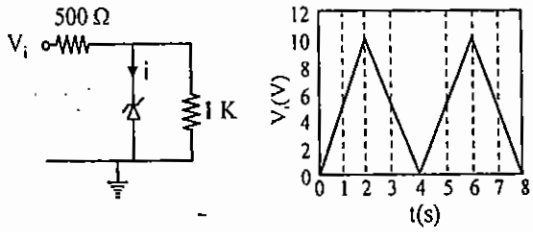


ANSWER KEY

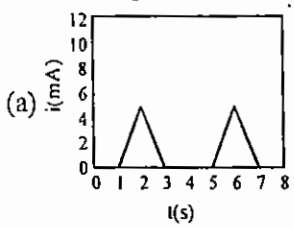
1. (a)	2. (a)	3. (d)	4. (a)	5. (b)	6. (*)	7. (b)

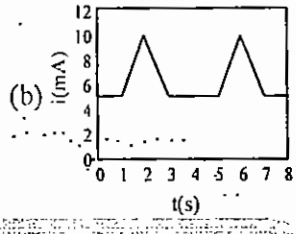
CSIR-UGC-NET Previous Years' Questions

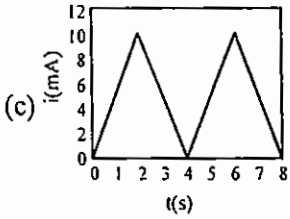
1. The figure below shows a voltage regulator utilizing a Zener diode of breakdown voltage 5V and a positive triangular wave input of amplitude 10V. **[NET Dec. 2011]**

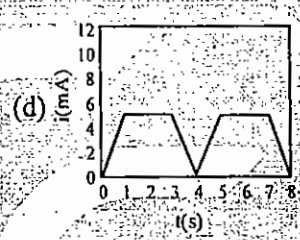


For $V_i > 5V$, the Zener regulates the output voltage by channeling the excess current through it self. Which of the following waveforms shows the current 'i' passing through the Zener diode?

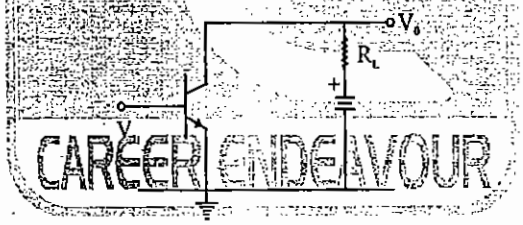








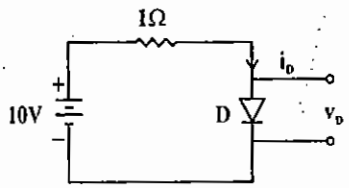
2. The transistor in the given circuit has $h_{fe} = 35$ and $h_{ie} = 1000\Omega$. If the load resistance $R_L = 1000\Omega$, the voltage and current gain are, respectively. **[NET June 2012]**



(a) –35, –35 (b) 35, 35 (c) 35, 0.97 (d) 0.98, 35

3. A diode D as shown in the circuit as an i–v relation which can be proximated by **[NET Dec. 2012]**

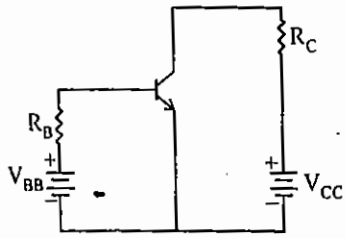
$$i_D = \begin{cases} v_D^2 + 2v_D, & \text{for } v_D > 0 \\ 0, & \text{for } v_D \le 0 \end{cases}$$

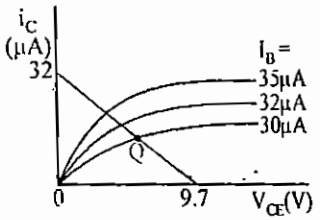


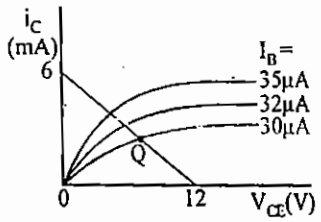
The value of v_D in the circuit is:

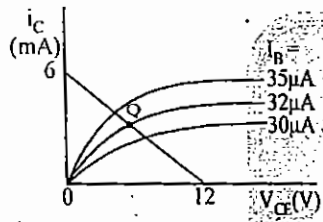
(a) $\left(-1+\sqrt{11}\right)V$ (b) 8V (c) 5V (d) 2V

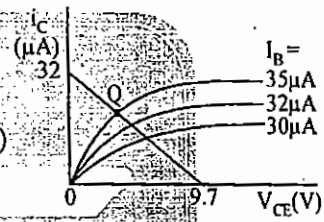
4. A silicon transistor with built-in voltage 0.7V is used in the circuit shown, with $V_{BB} = 9.7V$, $R_B = 300k\Omega$, $V_{CC} = 12V$ and $R_C = 2k\Omega$. Which of the following figures correctly represents the load line and the quiescent Q point? **[NET June 2013]**



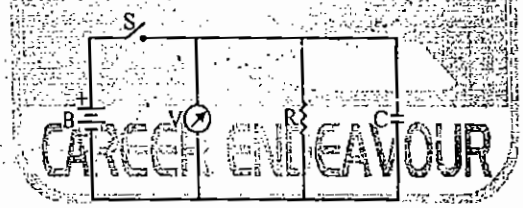
(a)


(b)


(c)


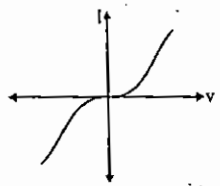
(d)


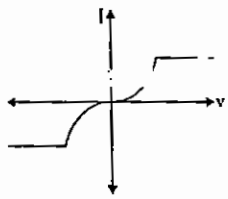
5. The insulation resistance R of an insulated cable is measured by connecting it in parallel with a capacitor C, a voltmeter, and battery B as shown. The voltage across the cable dropped from 150V to 15V, 1000 seconds after the switch S is closed. If the capacitance of the cable is 5μF, then its insulation resistance is approximately **[NET June 2013]**

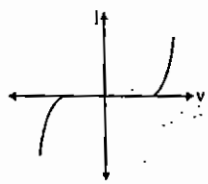


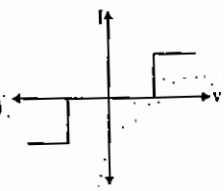
(a) $10^9\Omega$ (b) $10^8\Omega$ (c) $10^7\Omega$ (d) $10^6\Omega$

6. Two identical Zener diodes are placed back to back in series and are connected to a variable DC power supply. The best representation of the I-V characteristics of the circuit is **[NET Dec. 2013]**

(a)


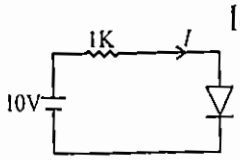
(b)


(c)


(d)


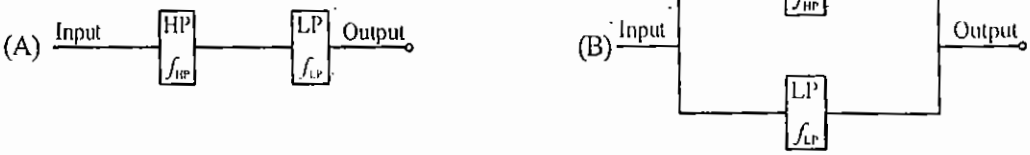
7. The I-V characteristics of the diode in the circuit is given by [NET Dec. 2014]

$$I = \begin{cases} (V-0.7)/500 & \text{for } V \geq 0.7 \\ 0 & \text{for } V < 0.7 \end{cases}$$



where V is measured in volts and I is measured in amperes.
The current I in the circuit is
(a) 10.0 mA (b) 9.3 mA (c) 6.2 mA (d) 6.7 mA

8. Consider a Low Pass (LP) and a High Pass (HP) filter with cut-off frequencies f_{LP} and f_{HP}, respectively, connected in series or in parallel configurations as shown in the Figures A and B below.



Which of the following statements is correct? [NET Dec. 2014]

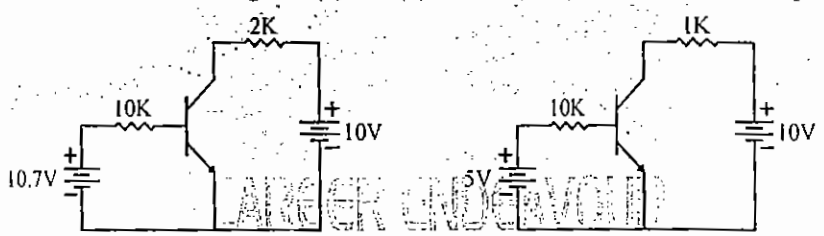
(a) For $f_{HP} < f_{LP}$, A acts as a Band Pass filter and B acts as a Band Reject filter

(b) For $f_{HP} > f_{LP}$, A stops the signal from passing through and B passes the signal without filtering.

(c) For $f_{HP} < f_{LP}$, A acts as a Band Pass filter and B passes the signal without filtering

(d) For $f_{HP} > f_{LP}$, A passes the signal without filtering and B acts as a Band Reject filter

9. Consider the circuits shown in Figures (a) and (b) below. [NET June 2015]



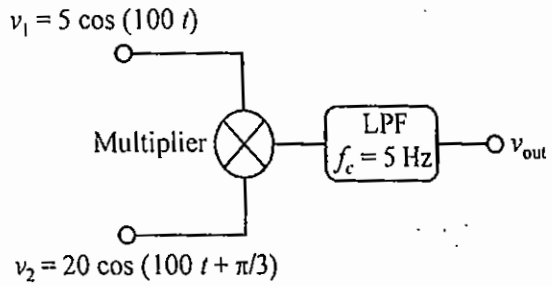
If the transistors in Figures (a) and (b) have current gain (β_{dc}) of 100 and 10 respectively, then they operate in the
(a) active region and saturation region respectively
(b) saturation region and active region respectively
(c) saturation region in both cases
(d) active region in both cases

10. If the reverse bias voltage of a silicon varactor is increased by a factor of 2, the corresponding transition capacitance [NET Dec. 2015]

(a) increases by a factor of $\sqrt{2}$ (b) increases by a factor of 2

(c) decreases by a factor of $\sqrt{2}$ (d) decreases by a factor of 2

11. Two sinusoidal signals are sent to an analog multiplier of scale factor 1 V^{-1} followed by a low pass filter (LPF).



If the roll-off frequency of the LPF is $f_c = 5$ Hz, the output voltage V_{out} is **[NET Dec. 2016]**

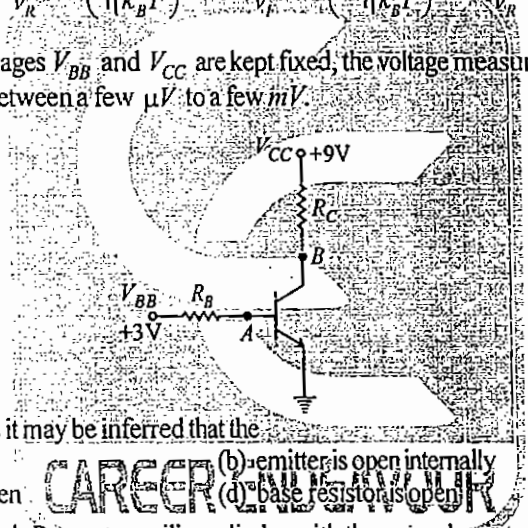
(a) 5 V (b) 25 V (c) 100 V (d) 50 V

12. Let I_0 be the saturation current, η the ideality factor and v_F and v_R the forward and reverse potentials, respectively, for a diode. The ratio R_R/R_F of its reverse and forward resistances R_R and R_F respectively, varies as (In the following k_B is the Boltzmann constant, T is the absolute temperature and q is the charge).

[NET June 2017]

(a) $\frac{v_R}{v_F}\exp\left(\frac{qv_F}{\eta k_B T}\right)$ (b) $\frac{v_F}{v_R}\exp\left(\frac{qv_F}{\eta k_B T}\right)$ (c) $\frac{v_R}{v_F}\exp\left(-\frac{qv_F}{\eta k_B T}\right)$ (d) $\frac{v_F}{v_R}\exp\left(-\frac{qv_F}{\eta k_B T}\right)$

13. In the circuit below the voltages V_{BB} and V_{CC} are kept fixed, the voltage measured at B is a constant, but that measured at A fluctuates between a few μV to a few mV. **[NET Dec. 2017]**

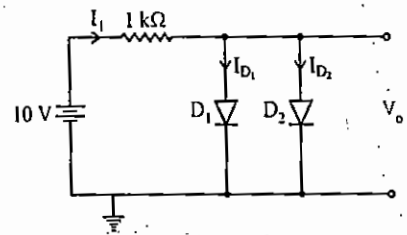


From these measurements it may be inferred that the

(a) base is open internally (b) emitter is open internally

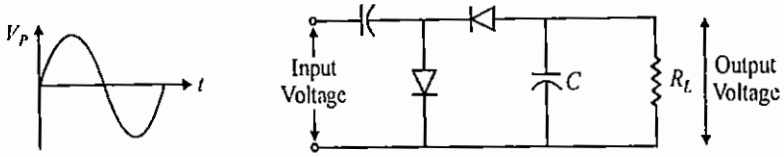
(c) collector resistor is open (d) base resistor is open

14. In the circuit below, D_1 and D_2 are two silicon diodes with the same characteristics. If the forward voltage drop of a silicon diode is 0.7 V, then the value of the current $I_1 + I_{D_1}$, is **[NET Dec. 2017]**



(a) 18.6 mA (b) 9.3 mA (c) 13.95 mA (d) 14.65 mA

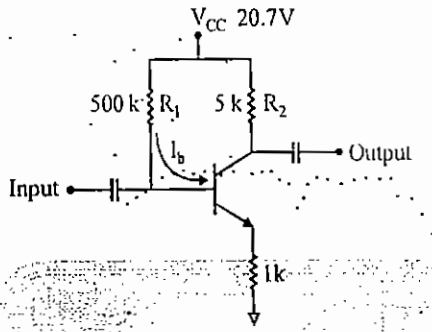
15. A sinusoidal signal with a peak voltage V_P and average value zero, is an input to the following circuit.



Assuming ideal diodes, the peak value of the output voltage across the load resistor R_L, is

(a) V_P (b) $V_P/2$ (c) $2V_P$ (d) $\sqrt{2}V_P$ **[NET June 2018]**

16. In the following circuit, the value of the common-emitter forward current amplification factor β for the transistor is 100 and V_{BE} is 0.7 *V*. **[NET June 2018]**



The base current I_B is

(a) 40 μA (b) 30 μA (c) 44 μA (d) 33 μA

17. Two signals $A_1 \sin(\omega t)$ and $A_2 \cos(\omega t)$ are fed into the input and the reference channels, respectively, of a lock-in amplifier. The amplitude of each signal is 1 V. The time constant of the lock-in amplifier is such that any signal of frequency larger than ω is filtered out. The output of the lock-in amplifier is **[NET June 2018]**

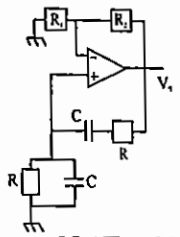
(a) 2V (b) 1V (c) 0.5V (d) 0V

ANSWER KEY

1. (a)	2. (a)	3. (d)	4. (b)	5. (b)	6. (c)	7. (c)
8. (c)	9. (b)	10. (c)	11. (b)	12. (a)	13. (d)	14. (c)
15. (c)	16. (d)	17. (d)				

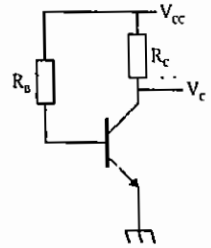
GATE Previous Years' Questions

1. What should be the values of the components R and R_2 such that the frequency of the Wien Bride oscillator is 300 Hz? [Given: C = 0.01 μF and R_1 = 12 kΩ] **[GATE 2004]**



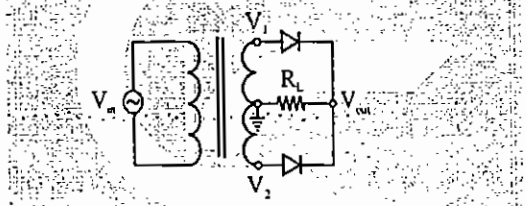
(a) R = 48kΩ and R_2 = 12kΩ (b) R = 26kΩ and R_2 = 24kΩ
(c) R = 530 kΩ and R_2 = 1 MΩ (d) R = 53kΩ and R_2 = 24kΩ

2 Calculate the collector voltage (v_c) of the transistor circuit shown in the figure **[GATE 2004]**
[Given: α = 0.96, I_{CBO} = 20μA, V_{BE} = 0.3V, R_B = 100kΩ, V_{CC} = +10V and R_C = 2.2kΩ]



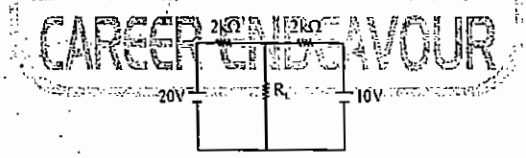
(a) 3.78 V (b) 3.82 V (c) 4.72 V (d) 9.7 V

3. For the rectifier circuit shown in the figure, the sinusoidal voltage (V_1 or V_2) at the output of the transformer has a maximum value of 10V. The load resistance R_L is 1 kΩ. If I_{av} is the average current through the resistor R_L the circuit corresponds to a. **[GATE 2005]**



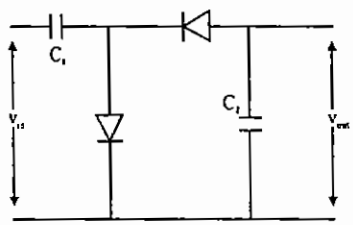
(a) Full wave rectifier with I_{av} = 20/π mA (b) Half wave rectifier with I_{av} = 20/π mA
(c) Half wave rectifier with I_{av} = 10/π mA (d) Full wave rectifier with I_{av} = 10/π mA

4. In the circuit shown in the figure the Thevenin voltage V_{Th} and Thevenin resistance R_{Th} as seen by the load resistance R_L (=1kΩ) are respectively. **[GATE 2005]**



(a) 15V, 1 kΩ (b) 30 V, 4 kΩ
(c) 20 V, 2 kΩ (d) 10V, 5 kΩ.

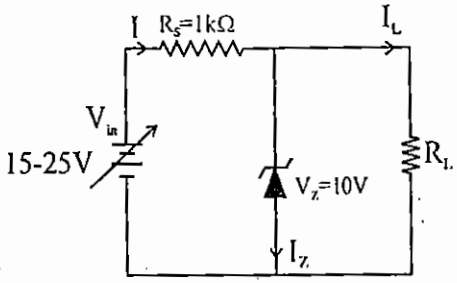
5. A sinusidal input voltage v_{in} of frequency ω is fed to the circuit shown in the figure, where $C_1 >> C_2$. If v_{in} is the peak value of the input voltage, then output voltage (v_{out}) is: **[GATE 2006]**



(a) $2v_{in}$ (b) $2v_0 \sin \omega t$ (c) $\sqrt{2}v_{in}$ (d) $\frac{V_{in}}{2}\sin \omega t$

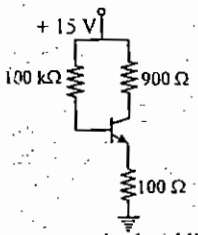
6. The largest analog output voltage from a 6-bit digital to analog converter (DAC) which produces 1.0 V output for a digital input of 010100, is: [GATE 2006]
(a) 1.6 V (b) 2.9 V (c) 3.15 V (d) 5.0 V

7. Pick the correct statement based on the below circuit. [GATE 2009]

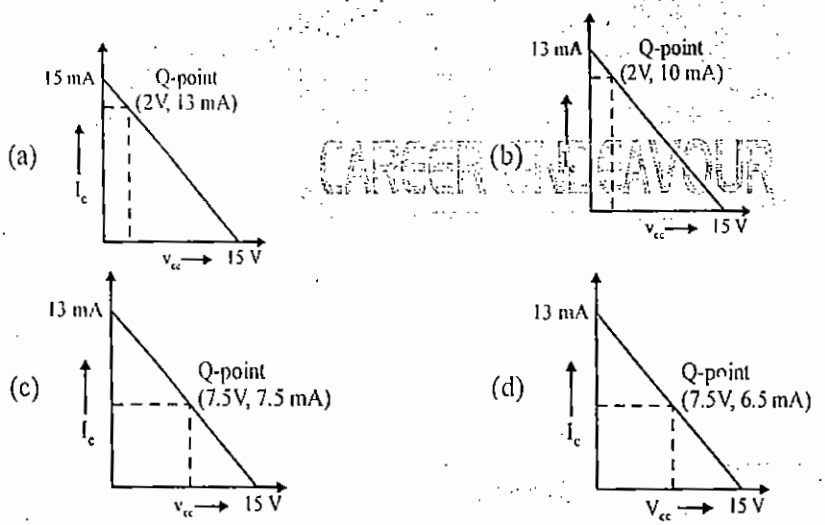


(a) The maximum Zener current, $I_{Z(max)}$, when $R_L = 10k\Omega$ is 15mA
(b) The minimum Zener current, $I_{Z(min)}$, when $R_L = 10k\Omega$ is 5mA
(c) With $V_{in} = 20V$, $I_L = I_Z$, when $R_L = 2k\Omega$
(d) The power dissipated across the Zener when $R_L = 10k\Omega$ and $V_{in} = 20V$ is 100 mW.

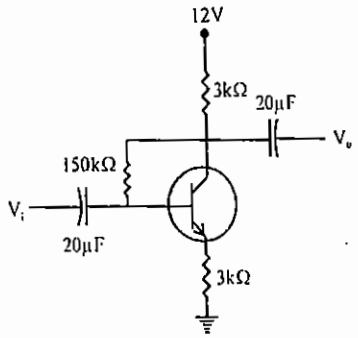
8. Consider the following circuit in which the current gain β_{dc} of the transistor is 100. [GATE 2012]



Which one of the following correctly represents the load line (collector current I_c with respect to collector-emitter voltage V_{CE}) and Q-point of this circuit?

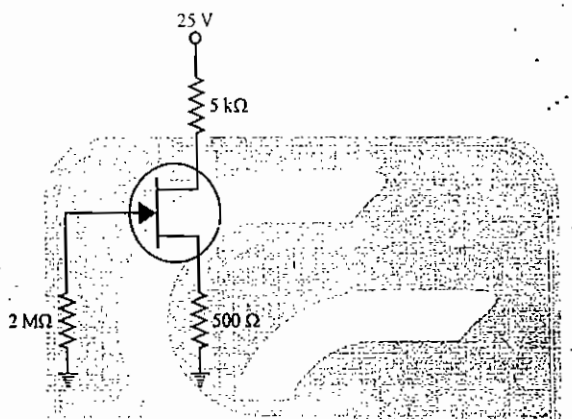


9. The current gain of the transistor in the following circuit is $\beta_{dc} = 100$. The value of collector current I_C is _____ mA. [GATE 2014]



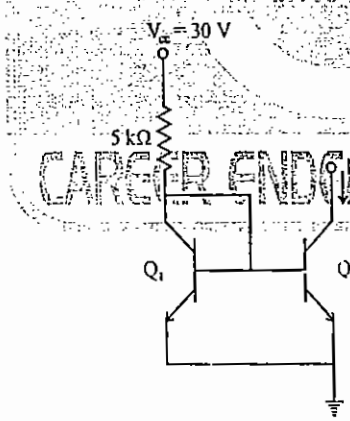
10. In order to measure a maximum of 1 V with a resolution of 1 mV using a n-bit A/D converter, working under the principle of ladder network, the minimum value of n is _____ [GATE 2014]

11. In the given circuit, the voltage across the source resistor is 1 V. The drain voltage (in V) is _____



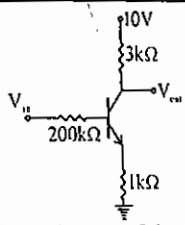
[GATE 2015]

12. In the simple current source shown in the figure, Q_1 and Q_2 are identical transistors with current gain $\beta = 100$ and $V_{BE} = 0.7\,V$ [GATE 2015]

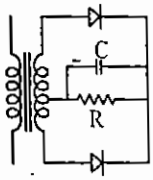


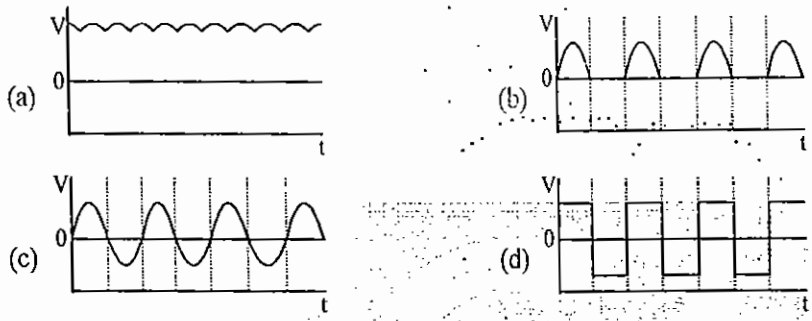
The current I_0 (in mA) is_____(upto two decimal places)

13. For the transistor shown in the figure, assume V_{BE} = 0.7V and β_{dc} = 100. If V_{in} = 5V, V_{out} (in Volts) is _____. (Give your answer upto one decimal place). [GATE 2016]

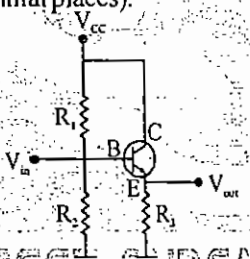


14. In the figure given below, the input to the primary of the transformer is a voltage varying sinusoidally with time. The resistor R is connected to the centre tap of the secondary. Which one of the following plots represents the voltage across the resistor R as a function of time? **[GATE 2017]**

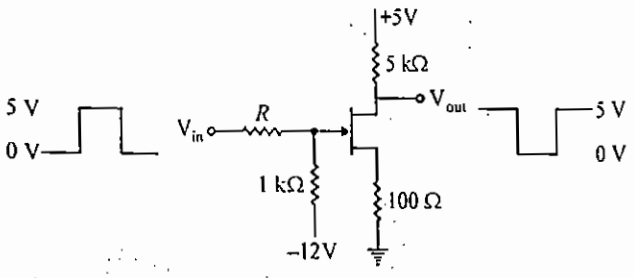




15. For the transistor amplifier circuit shown below with $R_1 = 10\ k\Omega$, $R_2 = 10\ k\Omega$, $R_3 = 1\ k\Omega$, and $\beta = 99$. Neglecting the emitter diode resistance, the input impedance of the amplifier looking into the base for small ac signal is _____ $k\Omega$. (up to two decimal places). **[GATE 2017]**



16. An n-channel FET having Gate-Source switch-off voltage $V_{GS(OFF)} = -2$ V is used to invert a 0 – 5 V square-wave signal as shown. The maximum allowed value of R would be _____ $k\Omega$ (up to two decimal places).



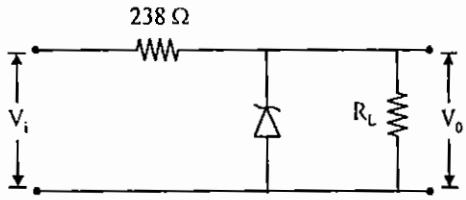
[GATE 2018]

ANSWER KEY

1. (d)	2. (b)	3. (a)	4. (a)	5. (a)	6. (c)	7. (c)
8. (a)	9. (1.4 -1.7)	10. (9.99–10.01)		11. ( )	12. (5.6 to 5.9)	
13. (5.5 to 5.9)		14. (a)	15. (4.75 to 5.01)		16. (0.70 to 0.73)	

TIFR Previous Years' Questions

1. The voltage regulator circuit shown in the figure has been made with a Zener diode rated at 15V, 200 mW. It is required that the circuit should dissipate 150 mW power across the fixed load resistor R_L

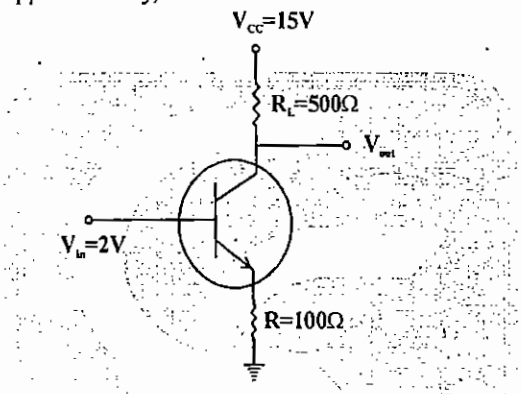


For stable operation of this circuit, the input voltage V_i must have a range **[TIFR 2012]**

(a) 17.5 V to 20.5 V (b) 15.5 V to 20.5 V
(c) 15.5 V to 22.5 V (d) 17.5 V to 22.5 V

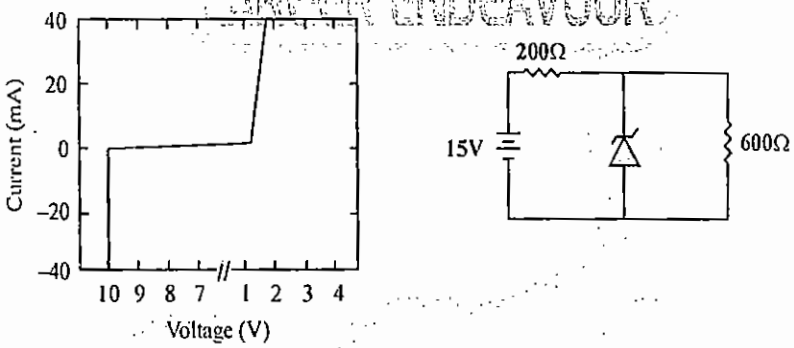
2. The circuit depicted on the right has been made with a silicon n-p-n transistor. **[TIFR 2013]**

Assuming that there will be a 0.7V drop across a forward-biased silicon p-n junction, the power dissipated across the transistor will be, approximately,



(a) 53 mW (b) 94 mW (c) 17 mW (d) 67 mW

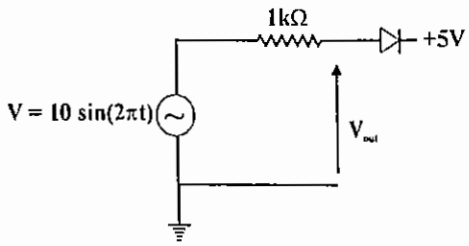
3. The figure on the right shows the current-voltage characteristics of a diode over a range of voltage and current where it is safe to operate the diode. **[TIFR 2013]**



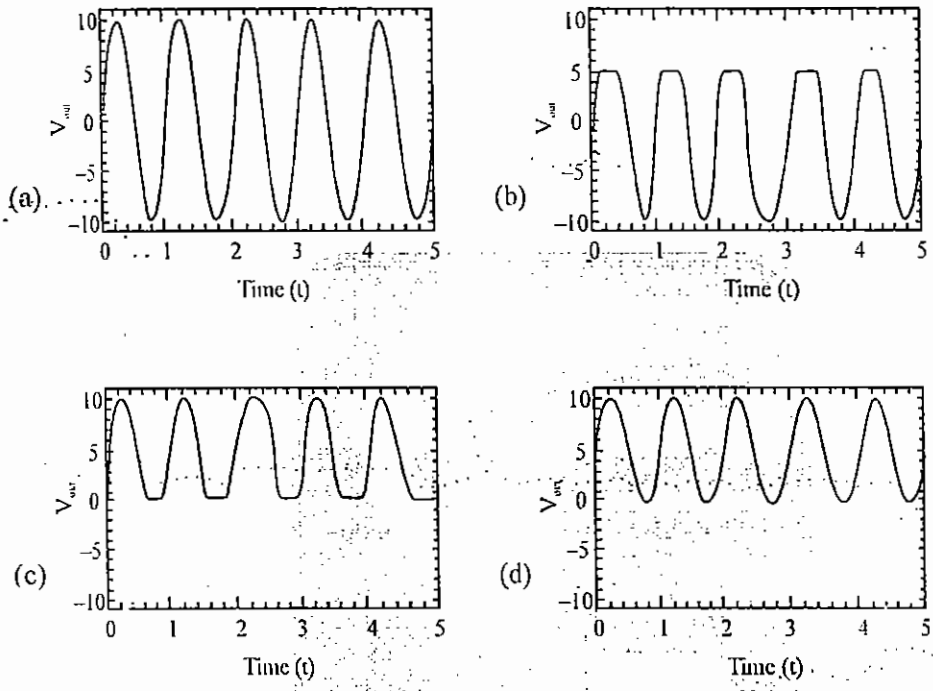
When this diode is used in the circuit on the extreme right, the approximate current, in mA, through the diode will be

(a) 0 (b) 8.3 (c) 16.7 (d) 25

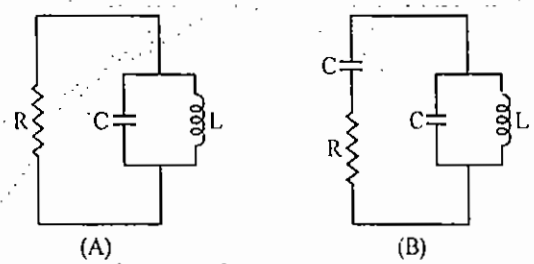
4. Consider the following circuit [TIFR 2014]



Which of the graphs given below is a correct representation of V_{out}?



5. Two LCR circuits (A) and (B) are shown below where $C_c \ll C$. At time $t = 0$, a charge Q is put on the capacitor C. [TIFR 2015]



Which of the following statements is correct?

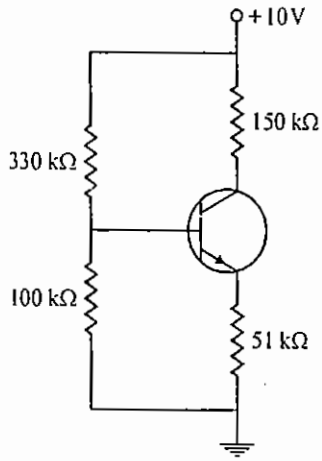
(a) The charge Q will decay faster in (A)

(b) The charge Q will decay faster in (B)

(c) The charge Q will decay at the same rate in (A) and (B)

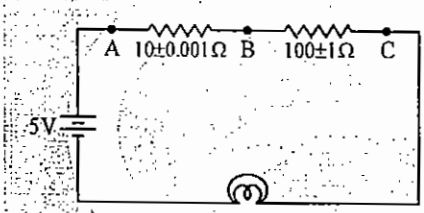
(d) The relative decay rates cannot be predicted without knowing the exact values of L, C, R and C_c

6. All resistors in the circuit on the right have a tolerance of ± 5%. [TIFR 2015]



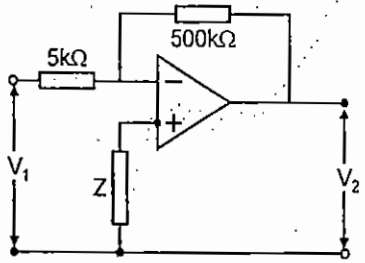
Assuming a diode drop of 0.7 V, which of the following is the lowest possible value of the collector voltage ?
(a) 3.1 V (b) 4.1 V (c) 4.7 V (d) 5.2 V

7. You are given the following circuit and two instruments : a voltmeter and an ammeter both with 0.001% accuracy in their readings. [TIFR 2015]



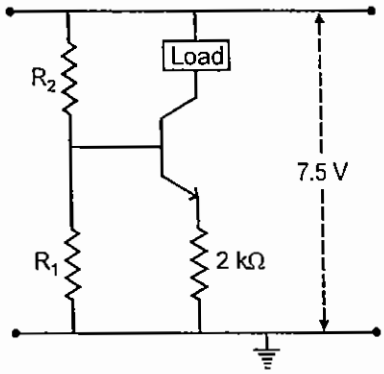
Which of the following methods will result in the most accurate reading for the current without interrupting the current in the circuit ?
(a) Use voltmeter to measure voltage across points B and C
(b) Use the ammeter to measure current at point B
(c) Use voltmeter to measure voltage across points A and B
(d) Use voltmeter to measure voltage across points A and C

8. In the generalized operational amplifier circuit shown on the right, the amp. has a very high input impedance ($Z > 50\ M\Omega$) and an open gain of 1000 for the frequency range under consideration. Assuming that the op. amp. draws negligible current, the voltage ratio V_2/V_1 is approximately [TIFR 2016]



(a) –190 (b) –190 (c) –90 (d) 80

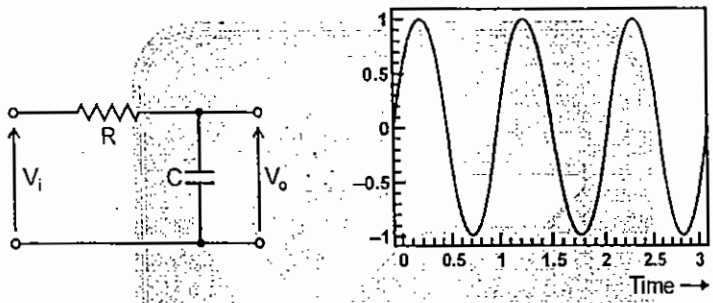
9. In the transistor circuit shown on the right, assume that the voltage drop between the base and the emitter is 0.5V. **[TIFR 2016]**



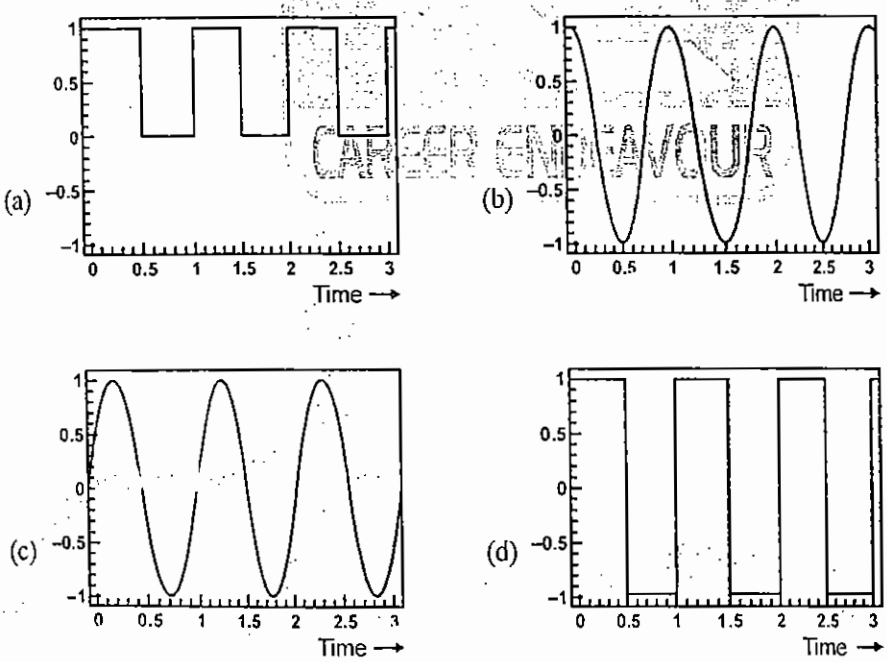
What will be the ratio of the resistances R_2/R_1, in order to make this circuit function as a source of constant current, $I = 1$ mA ?

(a) 4.5 (b) 3.0 (c) 2.5 (d) 2.0

10. For the circuit depicted on the right, the input voltage V_i is a simple sinusoid as shown below, where the time period is much smaller compared to the time constant of this circuit. **[TIFR 2016]**

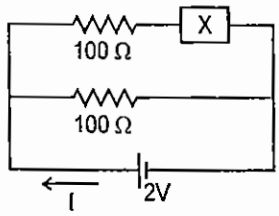


The voltage V_o across C is best represented by

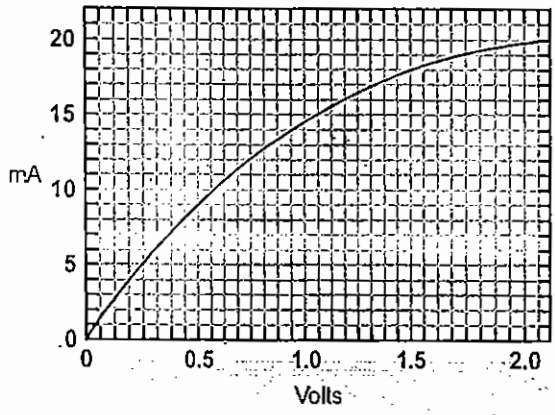


11. Consider a sawtooth waveform which rises linearly from 0 Volt to 1 Volt in 10 ns and then decays linearly to 0V over a period of 100 ns. Find the r.m.s. voltage in units of milliVolt? **[TIFR 2016]**

12. The circuit shown below contains an unknown device X.

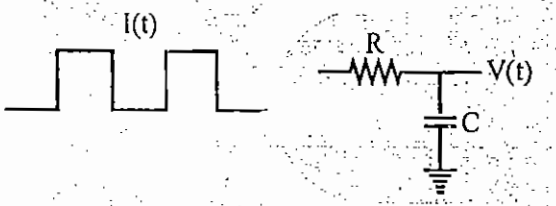


The current voltage characteristic of the device X were determined and are shown in the plot given below.



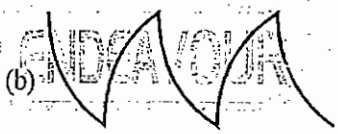
Determine the current I (in mA) flowing through the device X. [TIFR 2016]

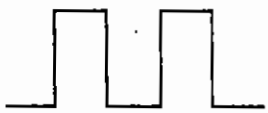
13. A current source produces a square wave $I(t)$ of 1.0 V peak-to-peak voltage and is used to drive the RC circuit shown below. [TIFR 2017]



Which of the following represents the correct voltage across the capacitor C ?

(a) 

(b) 

(c) 

(d) 

14. A signal is to be sent from a coaxial cable with impedance 40 Ω into a second coaxial cable with impedance 60 Ω. We can prevent reflection at the joint between the cables, by adding an impedance in parallel to the second cable. What should be the value, in units of Ohms (Ω), of that impedance ? [TIFR 2017]

ANSWER KEY

1. (a)	2. (b)	3. (b)	4. (b)	5. (a)	6. (c)	7. (c)
8. (c)	9. (d)	10. (b)	11. (Approx. 600)		12. (11 to 13)	
13. (d)	14. (120)					

1.

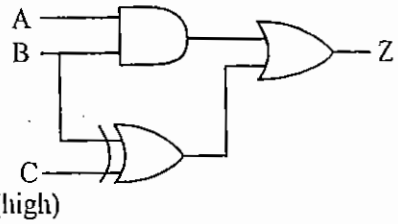
2

LEVEL-2

Solve Yourself

CSIR-UGC-NET Previous Years' Questions

1. Consider the digital circuit shown below in which the input C is always high (1). **[NET June 2011]**



The truth table for the circuit can be written as

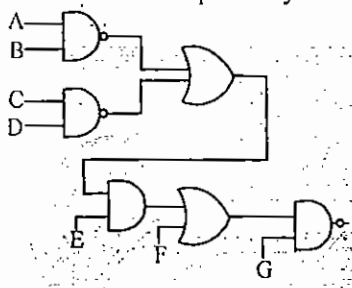
A	B	Z
0	0	
0	1	
1	0	
1	1	

The entries in the Z column (vertically) are

(a) 1011 (b) 0100 (c) 1111 (d) 1010

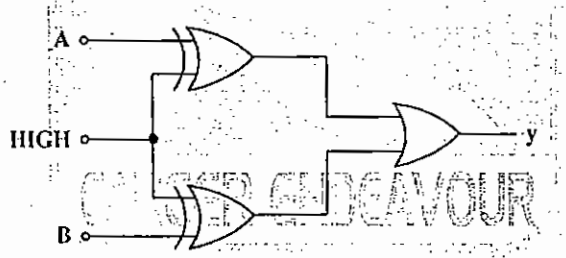
2. The output 0, of the given circuit in cases I and II, where **[NET June 2012]**

Case-I: A, B = 1; C, D ≠ 0; E, F = 1 and G = 0
Case-II: A, B ≠ 0; C, D = 0; E, F = 0 and G = 1 are respectively



(a) 1, 0 (b) 0, 1 (c) 0, 0 (d) 1, 1

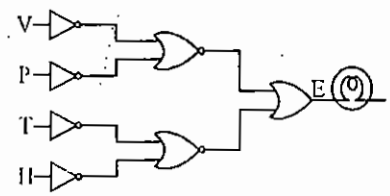
3. The logic circuit shown in the figure below **[NET Dec. 2012]**



implements the Boolean expression

(a) $y = \overline{A.B}$ (b) $y = \overline{A}.\overline{B}$ (c) $y = A.B$ (d) $y = A + B$

4. Four digital outputs V, P, T and H monitor the speed v, tyre pressure p, temperature t and relative humidity h of a car. These outputs switch from 0 to 1 when the values of the parameters exceed 85 km/hr, 2 bar, 40°C and 50%, respectively. A logic circuit that is used to switch ON a lamp at the output E is shown below. **[NET June 2013]**



Which of the following conditions will switch the lamp ON?

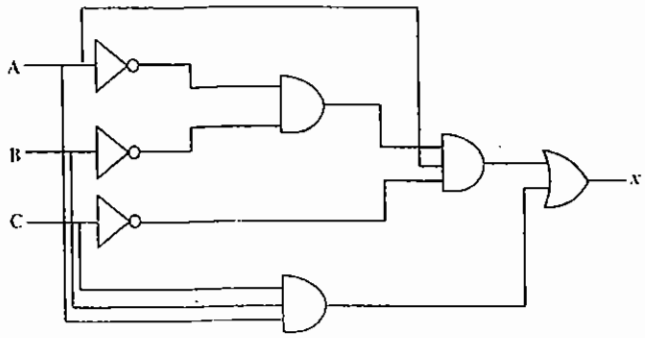
(a) $v < 85 km/hr, p < 2 bar, t > 40°C, h > 50\%$

(b) $v < 85km/hr, p < 2bar, t > 40°C, h < 50\%$

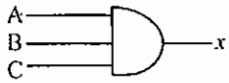
(c) $v > 85km/hr, p < 2bar, t > 40°C, h < 50\%$

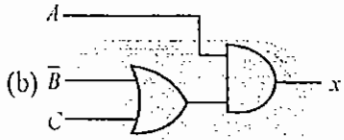
(d) $v > 85km/hr, p < 2bar, t < 40°C, h > 50\%$

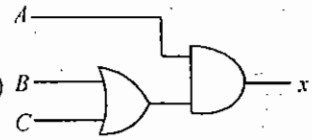
5. For the logic circuit shown in the figure below **[NET June 2014]**

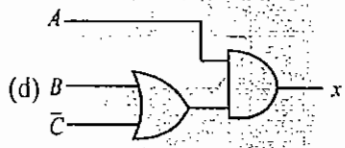


a simplified equivalent circuit is

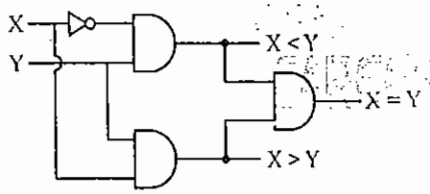
(a) 

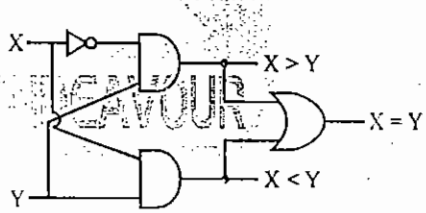
(b) 

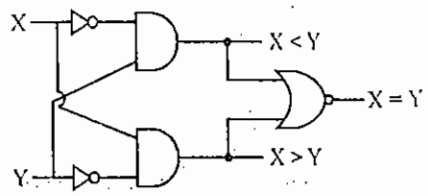
(c) 

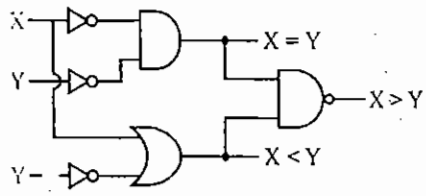
(d) 

6. In the figures below, X and Y are one bit inputs. The circuit which corresponds to a one bit comparator is **[NET June 2017]**

(a) 

(b) 

(c) 

(d) 

7. Which of the following gates can be used as a parity checker? **[NET June 2018]**

(a) an OR gate (b) a NOR gate

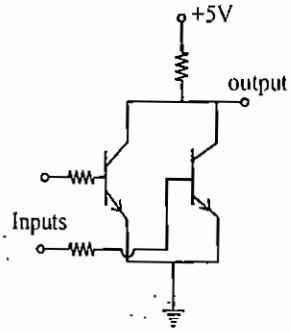
(c) an exclusive OR (XOR) gate (d) an AND gate

ANSWER KEY

1. (a)	2. (d)	3. (a)	4. (a)	5. (a)	6. (c)	7. (c)

GATE Previous Years' Questions

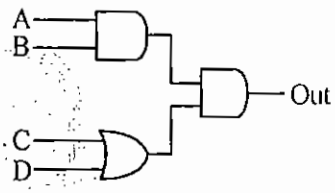
1. The circuit shown in figure below acts as a **[GATE 1997]**



(a) NOR gate (b) NAND gate
(c) AND gate (d) XOR gate

2. If the output of the logic circuit shown in the figure is 1, the input could be **[GATE 2000]**

(a) A = 1, B = 1, C = 1, D = 0
(b) A = 1, B = 1, C = 0, D = 0
(c) A = 1, B = 0, C = 1, D = 1
(d) A = 0, B = 1, C = 1, D = 1.



3. Which of the following options is true for a two input XOR gate? **[GATE 2002]**

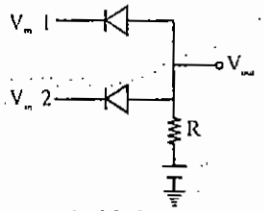
	Input		Output
	A	B	
(a)	0	1	1
(b)	1	0	0
(c)	0	0	1
(d)	1	1	1

4. Which of the given relations between the Boolean variables P and Q is NOT correct? (In the notation used here, P' denotes NOT P and Q' denotes NOT Q) **[GATE 2003]**

(a) $PQ' + PQ = P$ (b) $(PQ)' = P' + Q'$ (c) $PQ' = (P' + Q)'$ (d) $PQ' + Q = P$

5. A half-adder is a digital circuit with **[GATE 2004]**
(a) Three inputs and one output (b) Three inputs and two outputs
(c) Two inputs and one output (d) Two input and two outputs.

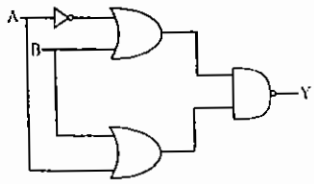
6. The circuit shown can be used as **[GATE 2005]**



(a) NOR gate (b) OR gate (c) NAND gate (d) AND gate

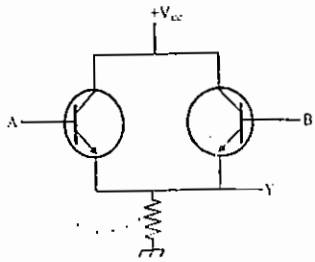
7. The Boolean expression: $B(A + B) + A.(\overline{B} + A)$ can be realized using minimum number of
(a) 1 AND gate (b) 2 AND gates (c) 1 OR gate (d) 2 OR gates. **[GATE 2005]**

8. In the given digital logic circuit, A and B form the input. The output Y is: **[GATE 2006]**



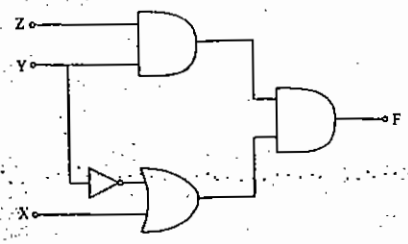
(a) $Y = \overline{A}$ (b) $Y = A\overline{B}$ (c) $Y = A + B$ (d) $Y = \overline{B}$

9. The circuit shown in the figure function as **[GATE 2006]**



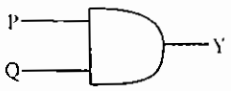
(a) an OR gate (b) an AND gate (c) a NOR gate (d) a NAND gate

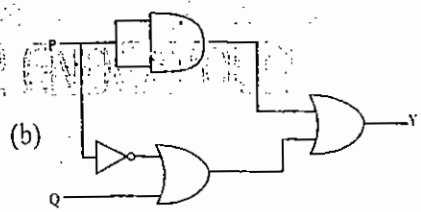
10. Identify the function F generated by the logic network shown **[GATE 2007]**

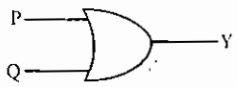


(a) $F = (X + Y)Z$ (b) $F = Z + Y + \overline{Y}X$ (c) $F = ZY(Y + X)$ (d) $F = XYZ$

11. The simplest logic gate circuit corresponding to the Boolean expression, $Y = P + PQ$ is:

(a) 

(b) 

(c) 

(d) None of these **[GATE 2008]**

Statement for Linked Q.12 and Q.13. **[GATE 2009]**

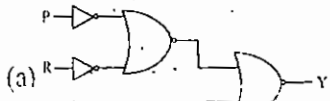
The Karnaugh map of a logic circuit is shown below:

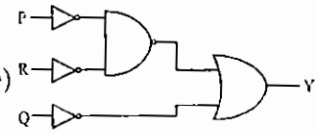
	$\bar{R}$	R
$\bar{P}\bar{Q}$	1	1
$\bar{P}Q$	1	
PQ		
$P\bar{Q}$	1	1

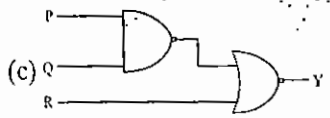
12. The minimized logic expression for the above map is:

(a) $Y = \bar{P}\bar{R} + \bar{Q}$ (b) $Y = \bar{Q}.PR$ (c) $Y = \bar{Q} + PR$ (d) $Y = Q.\overline{PR}$

13. The corresponding logic implementation using gates is given as:

(a) 

(b) 

(c) 

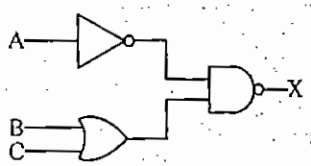
(d) None of the above

14. The minimum number of flip-flops required to construct a mod-75 counter is _____ **[GATE 2014]**

15. Which one of the following DOES NOT represent an exclusive OR operation for inputs A and B?

(a) $(A+B)\overline{AB}$ (b) $A\bar{B} + B\bar{A}$ (c) $(A+B)(\bar{A}+\bar{B})$ (d) $(A+B)AB$ **[GATE 2015]**

16. For the digital circuit given below, the output X is **[GATE 2016]**

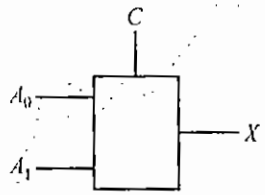


(a) $\overline{A + B \cdot C}$ (b) $\overline{\bar{A} \cdot (B+C)}$ (c) $\bar{A} \cdot (B+C)$ (d) $A + \overline{(B \cdot C)}$

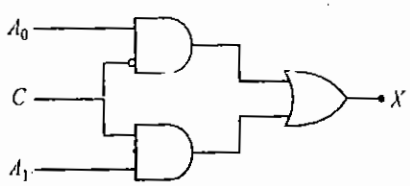
17. 20. The minimum number of NAND gates required to construct an OR gate is: **[GATE 2017]**

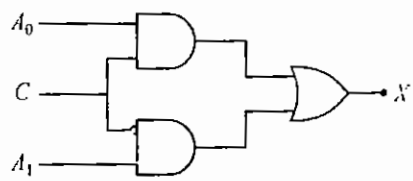
(a) 2 (b) 4 (c) 5 (d) 3

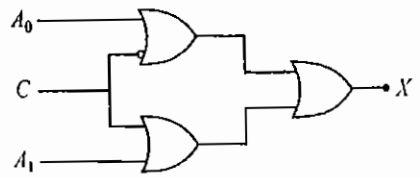
18. In a 2-to-1 multiplexer as shown below, the output $X = A_0$ if $C = 0$, and $X = A_1$ if $C = 1$.

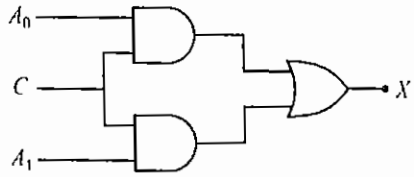


Which one of the following is the correct implementation of this multiplexer? **[GATE 2018]**

(a) 

(b) 

(c) 

(d) 

19. The logic expression $\bar{A}BC + \bar{A}\bar{B}C + AB\bar{C} + A\bar{B}\bar{C}$ can be simplified to **[GATE 2018]**

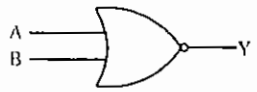
(a) A XOR C (b) A AND $\bar{C}$ (c) 0 (d) 1

ANSWER KEY

1. (a)	2. (a)	3. (a)	4. (d)	5. (d)	6. (d)	7. (c)
8. (d)	9. (a)	10. (d)	11. (d)	12. (a)	13. (d)	
14. (6.99 – 7.01)		15. (d)	16. (b)	17. (d)	18. (a)	19. (a)

TIFR Previous Years' Questions

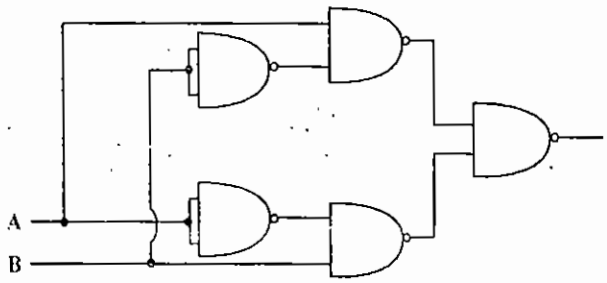
1. Consider the circuit shown below. **[TIFR 2012]**



The minimum number of NAND gates required to design this circuit is

(a) 6 (b) 5 (c) 4 (d) 3

2. The circuit shown below uses only NAND gates. Find the final output? **[TIFR 2013]**



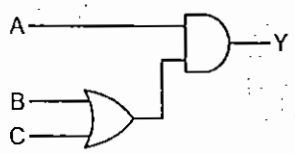
(a) A XOR B (b) A AND B (c) A OR B (d) A NOR B.

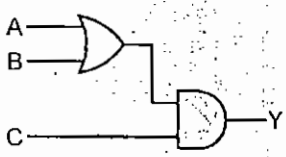
3. In a digital circuit for three input signals (A, B and C) the final output (Y) should be such that for inputs

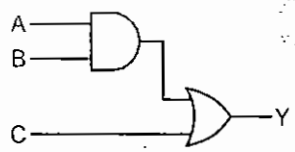
A	B	C
0	0	0
0	0	1
0	1	0

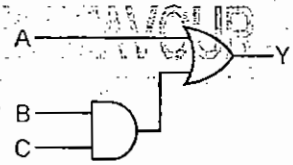
[TIFR 2016]

the output (Y) should be low and for all other cases it should be high. Which of the following digital circuits will give such output ?

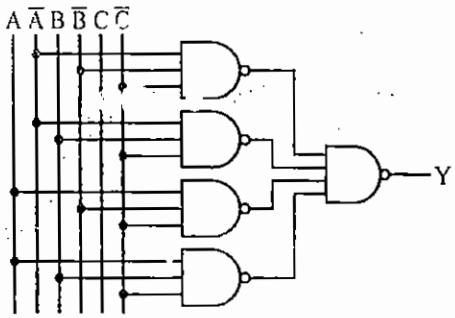
(a)


(b)


(c)


(d)


4. The output (Y) of the following circuit will be **[TIFR 2017]**



(a) $\bar{A} + B + \bar{C}$ (b) $\bar{A}$ (c) $\bar{B}$ (d) $\bar{C}$

5. For exact calculation and minimum complexity, two four-digit binary numbers can be added with [TIFR 2017]
   (a) 1 full adder and 3 half-adders (b) 2 full adders and 2 half-adders
   (c) 3 full adders and 1 half-adder (d) 4 full adders

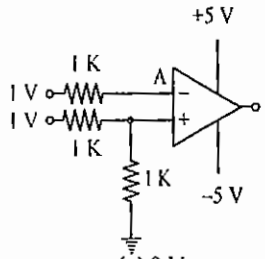
6. In Boolean terms, (A + B) (A + C) is equal to [TIFR 2018]
   (a) ABC (b) (A + B + C) (A + B)
   (c) A(B + C) (d) A + BC

ANSWER KEY

1. (c) 2. (a) 3. (d) 4. (d) 5. (c) 6. (d)

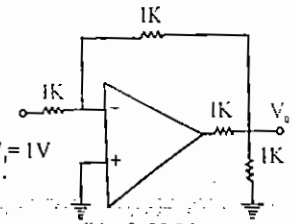
CSIR-UGC-NET Previous Years' Questions

1. In the operational amplifier circuit below, the voltage at point A is **[NET Dec. 2011]**



(a) 1.0 V (b) 0.5 V (c) 0 V (d) -5.0V

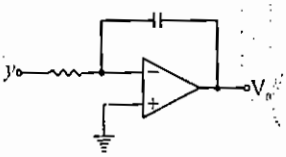
2. In the op-amp circuit shown in the figure below, the input voltage V_i is 1V. The value of the output V_o is:

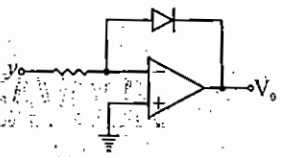


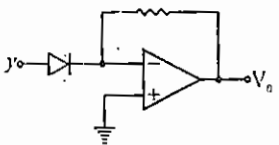
(a) –0.33 V (b) –0.50 V **[NET June 2012]**
(c) –1.00 V (d) –0.25 V

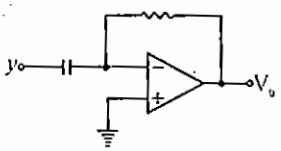
3. An op-amp based voltage follower **[NET June 2014]**
(a) is useful for converting a low impedance source into a high impedance source
(b) is useful for converting a high impedance source into a low impedance source
(c) has infinitely high closed loop output impedance
(d) has infinitely high closed loop gain

4. If the parameters y and x are related by $y = \log(x)$, then the circuit that can be used to produce an output voltage V_0 varying linearly with x is **[NET Dec. 2016]**

(a) 

(b) 

(c) 

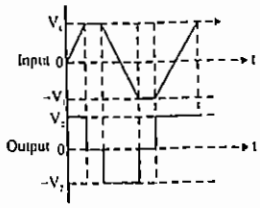
(d) 

ANSWER KEY

1. (a) 2. (c) 3. (b) 4. (c)

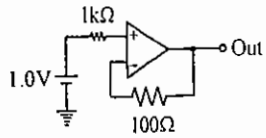
GATE Previous Years' Questions

1. The circuit for which the input and output waveforms are shown below is: **[GATE 1996]**



(a) Clipping circuit (b) Integrator (c) Differentiation (d) Schmitt trigger.

2. The output of the circuit on the right will be **[GATE 2000]**

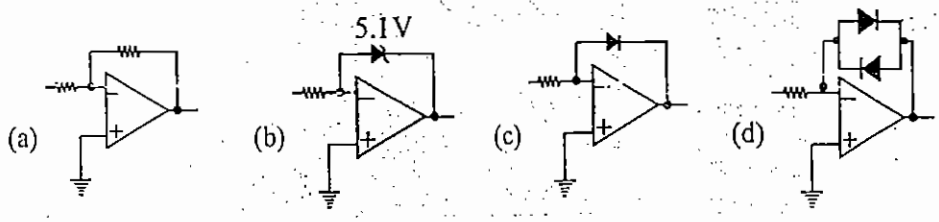


(a) 1V (b) 11V (c) −10V (d) 0 V

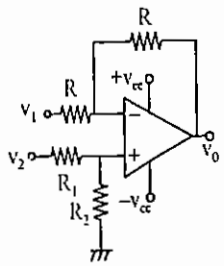
3. The inverting input terminal of an operational amplifier (OP-AMP) is shorted with the output terminal apart from being grounded. A voltage signal v_i is applied to the non-inverting input terminal of the op-amp. Under this configuration, the op-amp functions as. **[GATE 2004]**

(a) An open loop inverter (b) A voltage to current converter.
(c) A voltage follower (d) An oscillator.

4. In one of the following circuits, negative feedback does not operate for a negative input. Which one is it? The opamps are running from ±15V supplies. **[GATE 2010]**

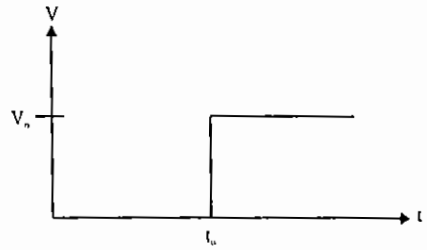


5. In the following circuit, for the output voltage to $V_0 = (-V_1 + V_2/2)$ the ratio R_1/R_2 is **[GATE 2012]**

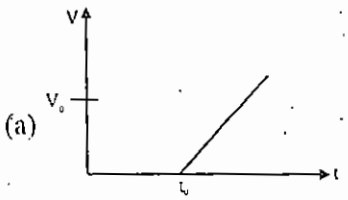


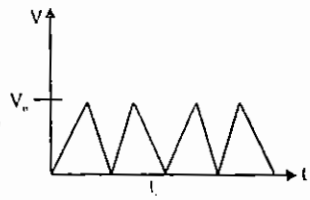
(a) 1/2 (b) 1 (c) 2 (d) 3

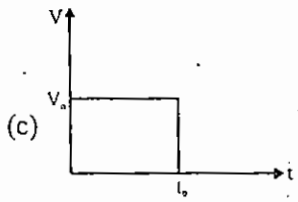
6. The input given to be an ideal OP-AMP integrator circuit is **[GATE 2014]**

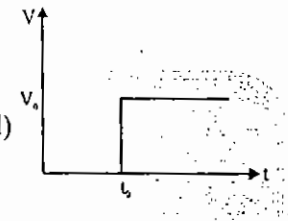


The correct output of the integrator circuit is (in magnitude form)

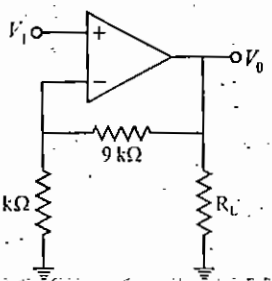
(a) 

(b) 

(c) 

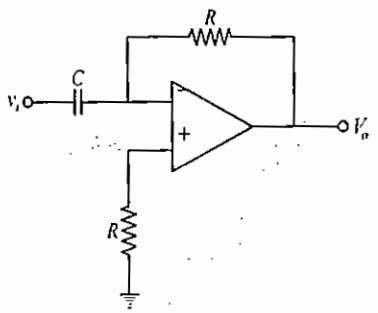
(d) 

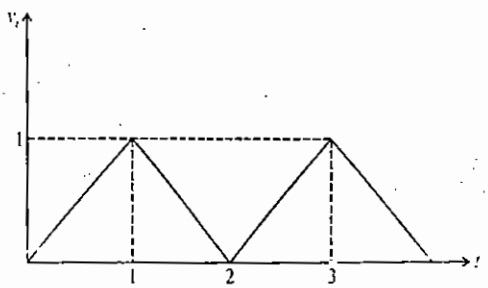
7. In the given circuit, if the open loop gain $A = 10^5$, the feedback configuration and the closed loop gain A_f are

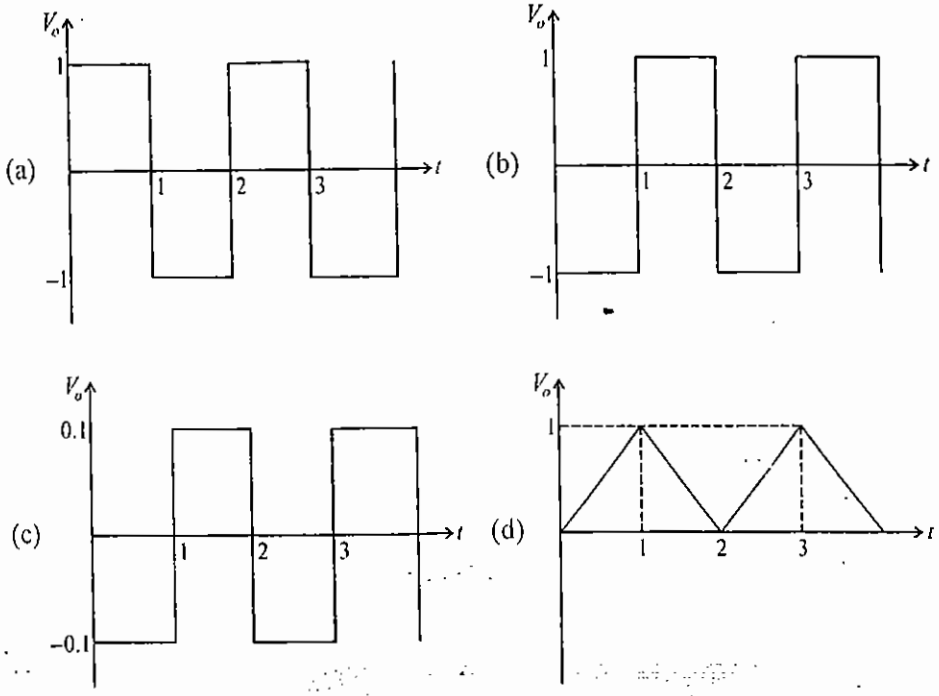


(a) series-shunt, $A_f = 9$ (b) series-series, $A_f = 10^4$ **[GATE 2015]**
(c) series-shunt, $A_f = 10$ (d) shunt-shunt, $A_f = 10$

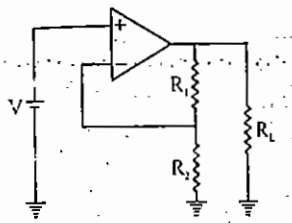
8. Consider the circuit shown in the figure, where RC = 1. For an input signal V_i shown below, choose the correct V_0 from the options: **[GATE 2015]**



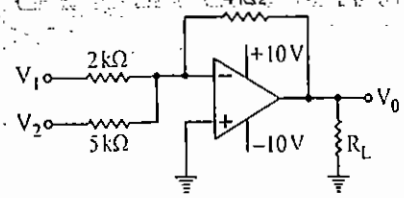




9. Consider an ideal operational amplifier as shown in the figure below with $R_1 = 5\ k\Omega$, $R_2 = 1\ k\Omega$, $R_L = 100\ k\Omega$. For an applied input voltage $V = 10\ mV$, the current passing through R_2 is _____ μA. (up to two decimal places). **[GATE 2017]**



10. For an operational amplifier (ideal) circuit shown below, **[GATE 2018]**



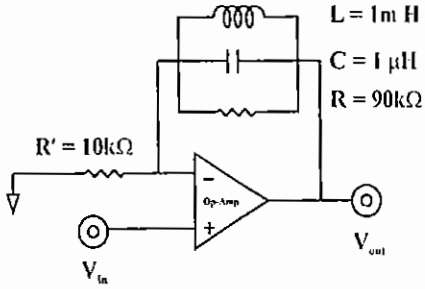
if $V_1 = 1\ V$ and $V_2 = 2\ V$, the value of V_0 is _____ V (up to one decimal place).

ANSWER KEY

1. (c)	2 (a)	3. (c)	4. (c)	5. (d)	6. (a)	7. (c)
8. (b)	9. (9.80 to 10.20)		10. (-3.5 to -3.7)			

TIFR Previous Years' Questions

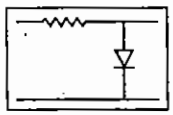
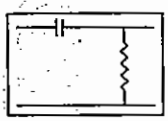
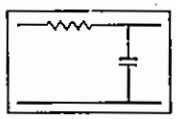
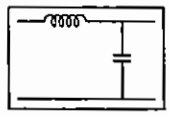
1. An input of 1.0 V DC is given to the ideal Op-Amp circuit depicted below. What will be the output voltage? [TIFR 2013]



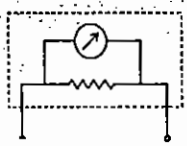
(a) 10.0 V (b) –9.0 V (c) 1.0 V (d) 0 V

2. The figure below shows an unknown circuit, with an input and output voltage signal. [TIFR 2018]

From the form of the input and output signals, one can infer that the circuit is likely to be

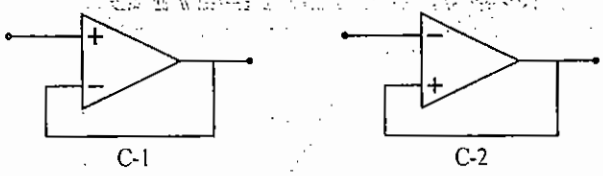
(a)  (b)  (c)  (d) 

3. A realistic voltmeter can be modelled as an ideal voltmeter with an input resistor in parallel as shown below.



Such a realistic voltmeter, with input resistance 1 kΩ, gives a reading of 100 mV when connected to a voltage source with source resistance 50 Ω. What will a similar voltmeter, with input resistance 1 MΩ, read in mV, when connected to the same voltage source? [TIFR 2018]

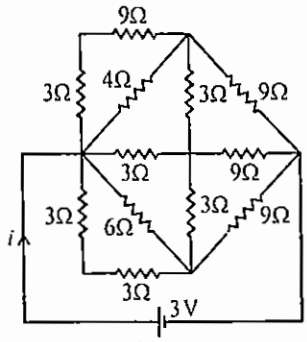
4. Consider the following circuits C-1 and C-2.



You can apply the golden rules of an ideal op-amp to [TIFR 2018]

(a) Only C-1 (b) Only C-2 (c) Both C-1 and C-2 (d) Neither C-1 nor C-2

5. The current i flowing through the following circuit is [TIFR 2018]



(a) 0.5 A (b) 0.6 A (c) 0.75 A (d) 1.0 A

ANSWER KEY

1. (c) 2. (b) 3. (105) 4. (a) 5. (c)

CSIR-UGC-NET Previous Years' Questions

1. A live music broadcast consists of a radio-wave of frequency 7 MHz, amplitude-modulated by a microphone output consisting of signals with a maximum frequency of 10 KHz. The spectrum of modulated output will be zero outside the frequency band **[NET Dec. 2012]**

(a) 7.00 MHz to 7.01 MHz (b) 6.99 MHz to 7.01 MHz
(c) 6.99 MHz to 7.00 MHz (d) 6.995 MHz to 7.005 MHz

2. An RC network produces a phase-shift of 30°. How many such RC networks should be cascaded together and connected to a Common Emitter amplifier so that the final circuit behaves as an oscillator?
(a) 6 (b) 12 (c) 9 (d) 3 **[NET June 2014]**

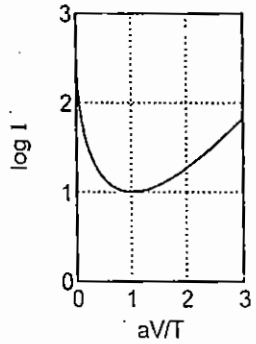
3. A junction is made between a metal of work function W_M, and a doped semiconductor of work function W_S with $W_M > W_S$. If the electric field at the interface has to be increased by a factor of 3, then the dopant concentration in the semiconductor would have to be **[NET Dec. 2014]**

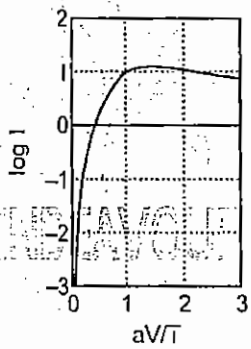
(a) increased by a factor of 9 (b) decreased by a factor of 3
(c) increased by a factor of 3 (d) decreased by a factor of $\sqrt{3}$

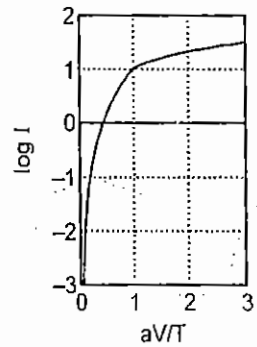
4. A large MOS transistor consists of N individual transistors connected in parallel. If the only form of noise in each transistor is $1/f$ noise, then the equivalent voltage noise spectral density for the MOS transistor is **[NET Dec. 2014]**

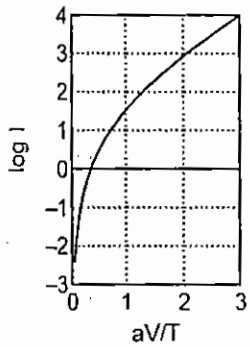
(a) $1/N$ times that of a single transistor (b) $1/N^2$ times that of a single transistor
(c) N times that of a single transistor (d) N^2 times that of a single transistor

5. The I-V characteristics of a device is $I = I_s\left[\exp\left(\frac{aV}{T}\right) - 1\right]$, where T is the temperature and a and I_s are constant independent of T and V. Which one of the following plots is correct for a fixed applied voltage V? **[NET Dec. 2016]**

(a)


(b)


(c)


(d)


6. The full scale voltage of an n-bit Digital-to-Analog Converter is V. The resolution that can be achieved in it is

(a) $\frac{V}{(2^n - 1)}$ (b) $\frac{V}{(2^n + 1)}$ (c) $\frac{V}{2^{2n}}$ (d) $\frac{V}{n}$ **[NET Dec. 2017]**

7. A Zener diode with an operating voltage of 10 V at 25 °C has a positive temperature co-efficient of 0.07% per °C of the operating voltage. The operating voltage of this Zener diode at 125 °C is **[NET Dec. 2017]**

(a) 12.0 V (b) 11.7 V (c) 10.7 V (d) 9.3 V

8. The full scale of a 3-bit digital-to-analog (DAC) converter is 7 V. Which of the following tables represents the output voltage of this 3-bit DAC for the given set of input bits ? **[NET June 2018]**

(a)

Input bits	Output voltage
000	0
001	1
010	2
011	3

(b)

Input bits	Output voltage
000	0
001	1.25
010	2.5
011	3.75

(c)

Input bits	Output voltage
000	1.25
001	2.5
010	3.75
011	5

(d)

Input bits	Output voltage
000	1
001	2
010	3
011	4

ANSWER KEY

1. (d) 2. (a) 3. (a) 4. (a) 5. (d) 6. (a) 7. (c)
8. (a)

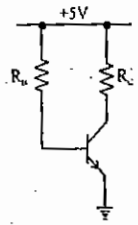
GATE Previous Years' Questions

1. A current amplifier is characterised by [GATE 1996]
   (a) low input impedance and high output impedance
   (b) high input impedance and low output impedance.
   (c) low impedance at both input and output terminals.
   (d) high impedance at both input and output terminals.

2. Which of the following characteristics DOES NOT belong to a common collector transistor amplifer? [GATE 1996]
   (a) Low voltage gain [≈] (b) High current gain.
   (c) High input impedance (d) High output impedance.

3. An amplifier has a voltage gain of 500 and an input impedance 20 KΩ, without any feedback. Now a negative feedback with $\beta = 0.1$ is applied. Its gain and input impedance with feedback will respectively be [GATE 1996]
   (a) 9.8 and 392 K ohms (b) 9.8 and 1020 K ohms
   (c) 50 and 1020 K ohms (d) 50 and 2 K ohms

4. In the circuit shown below, $R_B = 1\ k\Omega$ and $R_C = 100\Omega$. If the transistor $\beta(h_{FE})$ is 100, the current through R_C will be



   (a) ≈ 0.43 A (b) ≈ 50 mA [GATE 2000]
   (c) zero (d) Oscillating between 0 and 50 mA.

5. In an n-p-n transistor, the leakage current consists of [GATE 2001]
   (a) Electrons moving from the base to the emitter
   (b) Electrons moving from the collector to the base
   (c) Electrons moving from the collector to the emitter.
   (d) Electrons moving from the base to the collector.

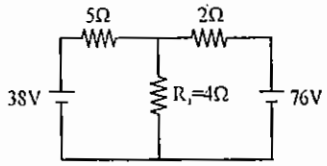
6. A field effect transistor is a [GATE 2004]
   (a) Unipolar device (b) Special type of bipolar junction transistor.
   (c) Unijunction device (d) Device with low input impedance

7. Which of the following statements is correct for a common emitter amplifier circuit? [GATE 2004]
   (a) The output is taken from the emitter
   (b) There is 180° phase shift between input and output voltages
   (c) There is no phase shift between input and output voltages
   (d) Both p-n juntions are forward biased.

8. A junction field effect transistor behaves as a [GATE 2005]
   (a) Voltage controlled current source (b) Voltage controlled voltage source
   (c) Current controlled voltage source (d) Current controlled current source

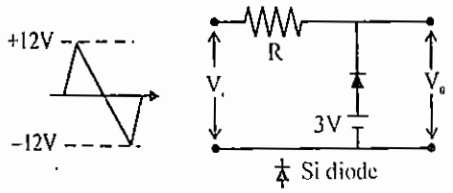
9. The high input impedance of field effect transistor (FET) amplifier is due to [GATE 2006]
   (a) The pinch-off voltage (b) Its very low gate current.
   (c) The source and drain being far apart (d) The geometry of the FET.

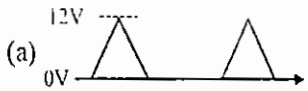
10. For the circuit shown, the potential difference (in Volts) across R_L is: **[GATE 2007]**

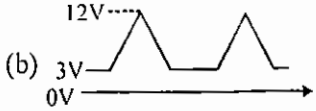


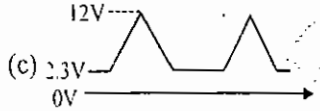
(a) 48 (b) 52 (c) 56 (d) 65

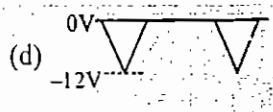
11. When an input voltage V_i of the form shown, is applied to the circuit given below, the output voltage V_0 is of the form. Vy(Si = 0.7 V) **[GATE 2007]**



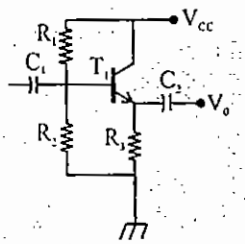
(a) 

(b) 

(c) 

(d) 

12. The circuit shown below **[GATE 2009]**

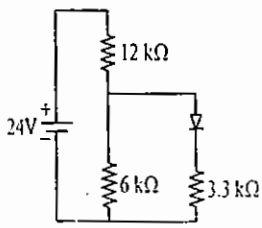


(a) Is a common-emitter amplifier (b) Uses a pnp transistor
(c) Is an osciliator (d) Has a voltage gain less than one.

13. An amplifier of gain 1000 is made into a feedback amplifier by feeding 9.9% of its output voltage in series with the input opposing. If f_L = 20 Hz and f_H = 200 kHz for the amplifier without feedback, then due to the feedback. **[GATE 2009]**

(a) The gain decreasse by 10 times (b) The outputresistance increases by 10 times
(c) The f_H increases by 100 times (d) The input resistance decreases by 100 times.

14. In the following circuit, the voltage drop across the ideal diode in forward bias condition is 0.7 V.



The current passing through the diode is **[GATE 2012]**

(a) 0.5 mA (b) 1.0 mA (c) 1.5 mA (d) 2.0 mA

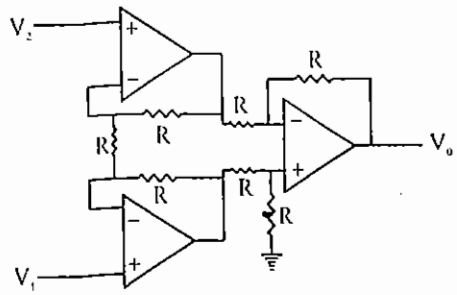
15. A low pass filter is formed by a resistance R and a capacitance C. At the cut-off angular frequency $\omega_c = \frac{1}{RC}$, the voltage gain and the phase of the output voltage relative to the input voltage respectively, are
(a) 0.71 and 45° (b) 0.71 and –45° (c) 0.5 and –90° (d) 0.5 and 90° **[GATE 2014]**

ANSWER KEY

1. (a)	2. (d)	3. (b)	4. (b)	5. (a)	6. (a)	7. (d)
8. (a)	9. (b)	10. (a)	11. (c)	12. (d)	13. (c)	14. (b)
15. (b)						

JEST Previous Years' Questions

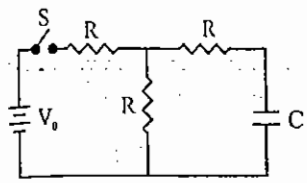
1. The classic three op-amp instrumentation amplifier configuration is shown below: **[JEST 2012]**



The op-amp are ideal and all resistors are of equal value R. The gain, defined as the output voltage V_0 divided by the differential input voltage $V_1 - V_2$, is equal to

(a) 2 (b) 3 (c) 4 (d) 6

2. A capacitor C is connected to a battery V_0 through three equal resistors R and a switch S as shown below:

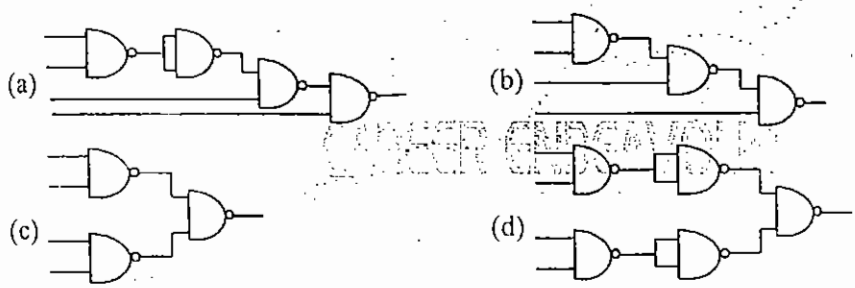


The capacitor is initially uncharged. At time t = 0, the switch S is closed. The voltage across the capacitor as a function of time 't' for t > 0 is given by **[JEST 2012]**

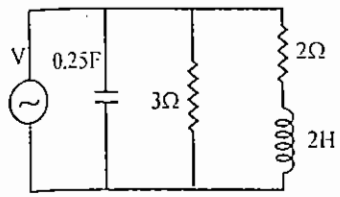
(a) $(V_0/2)(1-\exp)(-t/2RC)$ (b) $(V_0/3)(1-\exp)(-t/3RC)$

(c) $(V_0/3)(1-\exp)(-3t/2RC)$ (d) $(V_0/2)(1-\exp)(-2t/3RC)$

3. Which of the following circuits will act like a 4-input NAND gate? **[JEST 2014]**

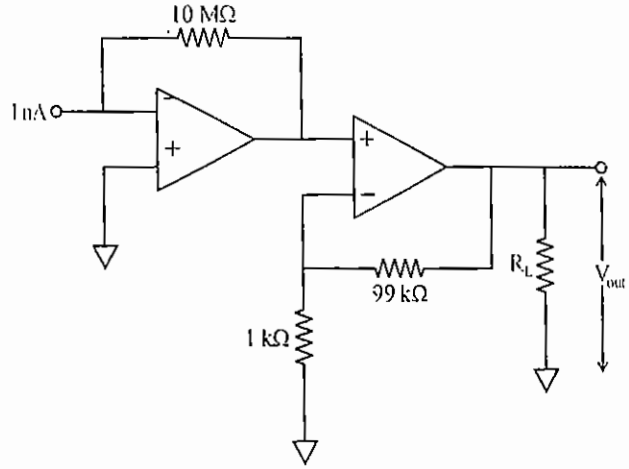


4. Find the resonance frequency (rad/sec) of the circle shown in the figure below **[JEST 2014]**



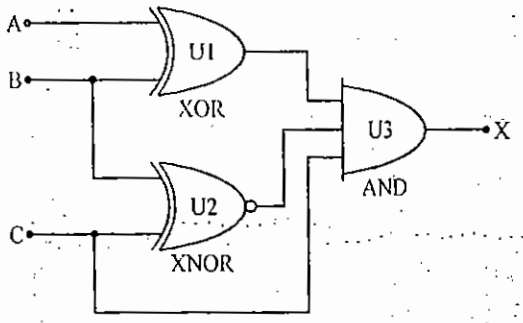
(a) 1.41 (b) 1.0 (c) 2.0 (d) 1.73

5. What is the voltage at the output of the following operational amplifier circuit? [JEST 2015]



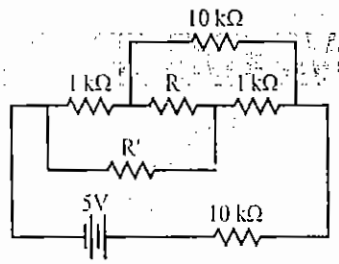
(a) 1 V (b) 1 mV (c) 1 μV (d) 1 nV

6. For the logic circuit shown in figure, the required input condition (A, B, C) to make the output (X) = 1 is,



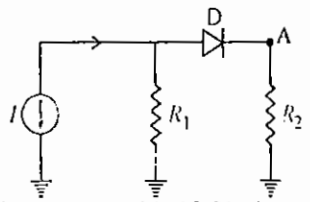
(a) 1, 0, 1 (b) 0, 0, 1 (c) 1, 1, 1 (d) 0, 1, 1 [JEST 2015]

7. It is found that when the resistance R indicated in the figure below is changed from 1 kΩ to 10 kΩ, the current flowing through the resistance R' does not change. What is the value of the resistor R'? [JEST 2016]



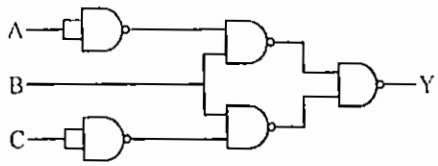
(a) 5 kΩ (b) 100 kΩ (c) 10 kΩ (d) 1 kΩ

8. Consider the circuit shown in the figure where $R_1 = 2.07$ kΩ and $R_2 = 1.93$ kΩ. Current source I delivers 10 mA current. The potential across the diode D is 0.7 V. What is the potential at A? [JEST 2017]



(a) 10.35 V (b) 9.65 V (c) 19.30 V (d) 4.83 V

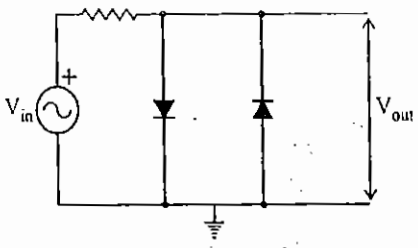
9. What is Y for the circuit shown below? [JEST 2017]

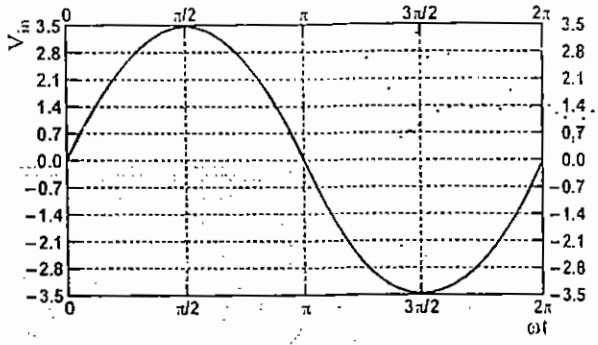


(a) $Y = \overline{(A+\bar{B})(\bar{B}+C)}$ (b) $Y = \overline{(A+\bar{B})(B+C)}$

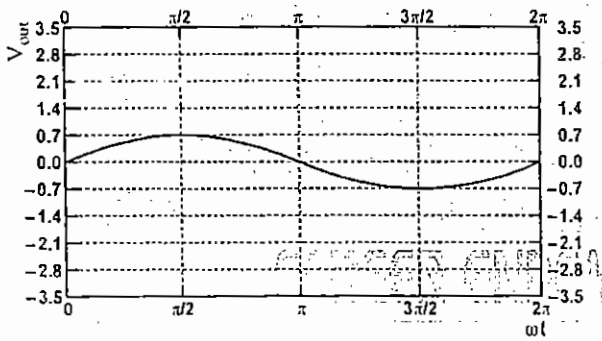
(c) $Y = \overline{(\bar{A}+B)(\bar{B}+C)}$ (d) $Y = \overline{(A+B)(\bar{B}+C)}$

10. In the following silicon diode circuit ($V_B = 0.7$ V), determine the output waveform (V_{out}) for the given input wave. [JEST 2017]

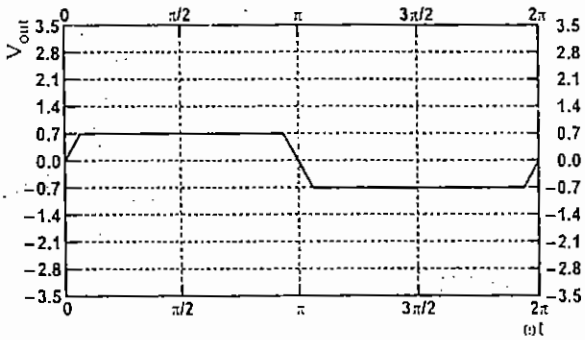




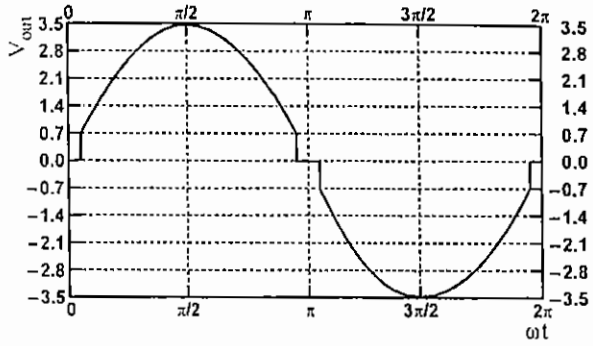
(a)



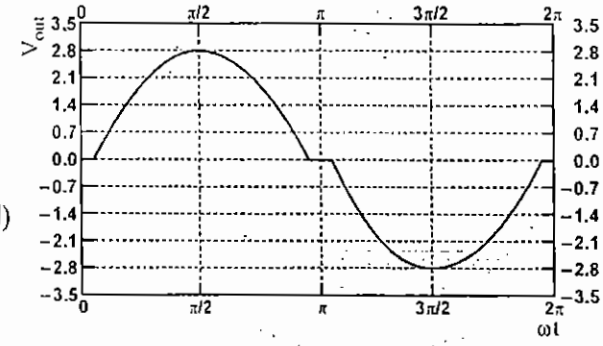
(b)



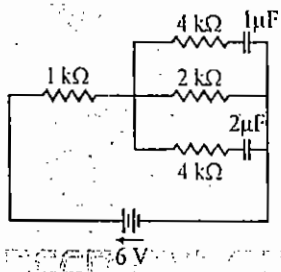
(c)



(d)

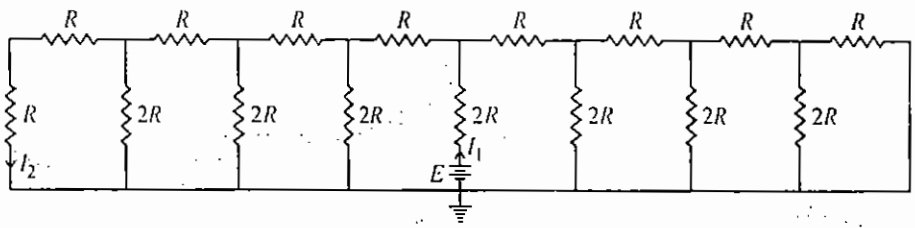


11. Consider the following circuit in steady state condition. Calculate the amount of charge stored in 1 μF and 2 μF capacitors respectively. **[JEST 2017]**

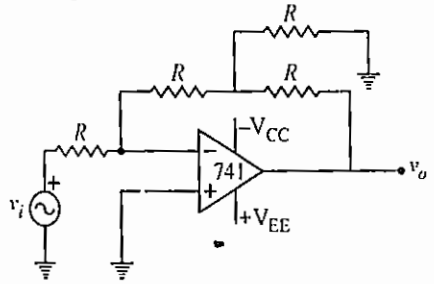


(a) 4 μC and 8 μC (b) 8 μC and 4 μC (c) 3 μC and 6 μC (d) 6 μC and 3 μC

12. For the circuit shown below, what is the ratio I_1/I_2 ? **[JEST 2017]**

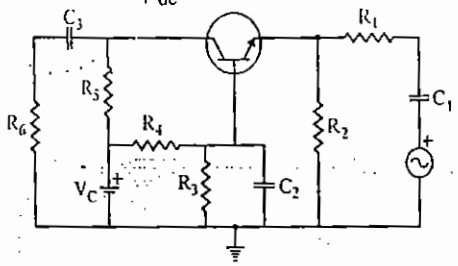


13. Consider a 741 operational amplifier circuit as shown below, where $V_{CC} = V_{EE} = +15V$ and $R = 2.2\,k\Omega$. If $v_i = 2\,mV$, what is the value of v_o with respect to the ground? **[JEST 2017]**



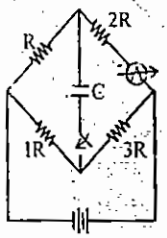
(a) $-1\,mV$ (b) $-2\,mV$ (c) $-3\,mV$ (d) $-4\,mV$

14. What is the DC base current (approximated to nearest integer value in μA) for the following *n-p-n* silicon transistor circuit, given $R_1 = 75\Omega$, $R_2 = 4.0\,k\Omega$, $R_3 = 2.1\,k\Omega$, $R_4 = 2.6\,k\Omega$, $R_5 = 6.0\,k\Omega$, $R_6 = 6.8\,k\Omega$, $C_1 = 1\,\mu F$, $C_2 = 2\,\mu F$, $V_C = +15\,V$ and $\beta_{dc} = 75$? **[JEST 2017]**

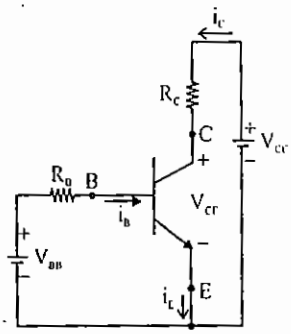


(a) 20 (b) 24 (c) 16 (d) 32

15. In the circuit shown below, the capacitor is initially uncharged. Immediately after the key K is closed, the reading in the ammeter is 27 mA. What will the reading (in mA) be a long time later? **[JEST 2018]**



16. Consider the transistor circuit shown in the figure. Assume $V_{BEQ} = 0.7V$, $V_{BB} = 6V$ and the leakage current is negligible. What is the required value of R_B in kilo-ohms if the base current is to be 4 μA? **[JEST 2018]**



ANSWER KEY

1. (b)	2. (d)	3. (d)	4. (b)	5. (a)	6. (d)	7. (b)
8. (b)	9. (a)	10. (b)	11. (a)	12. (16)	13. (–6)	14. (c)
15. (25.485mA)		16. (1325 kΩ)				