ANALOG AND DIGITAL ELECTRONICS

Unit Five

(Logic Families)

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Topics To be Covered

Lecture No.	Unit No.	Topics to be Covered	Syllabus from Books
01	Five	Standard TTL chara. : Speed, Power Dissipation, fan in, Fan out, Current and voltage parameter, noise margin, Operating temp.	Digital Electronics by R.P. Jain
02		Operation of TTL NAND gate, TTL configuration: Active pull-up, Wired AND, totem pole, open collector	
03		CMOS : CMOS Inverter, CMOS chara. CMOS configuration: Wired Logic, open drain o/p	
04		Interfacing : TTL to CMOS and CMOS to TTL Interfacing	

Agenda.

After the completion of this session you will be able to know

- Standard TTL chara. : Speed, Power Dissipation, fan in, Fan out, Current and voltage parameter, noise margin, Operating temp.
- Operation of TTL NAND gate,
- TTL configuration: Active pull-up, Wired AND, totem pole, open collector

Agenda.

After the completion of this session you will be able to know

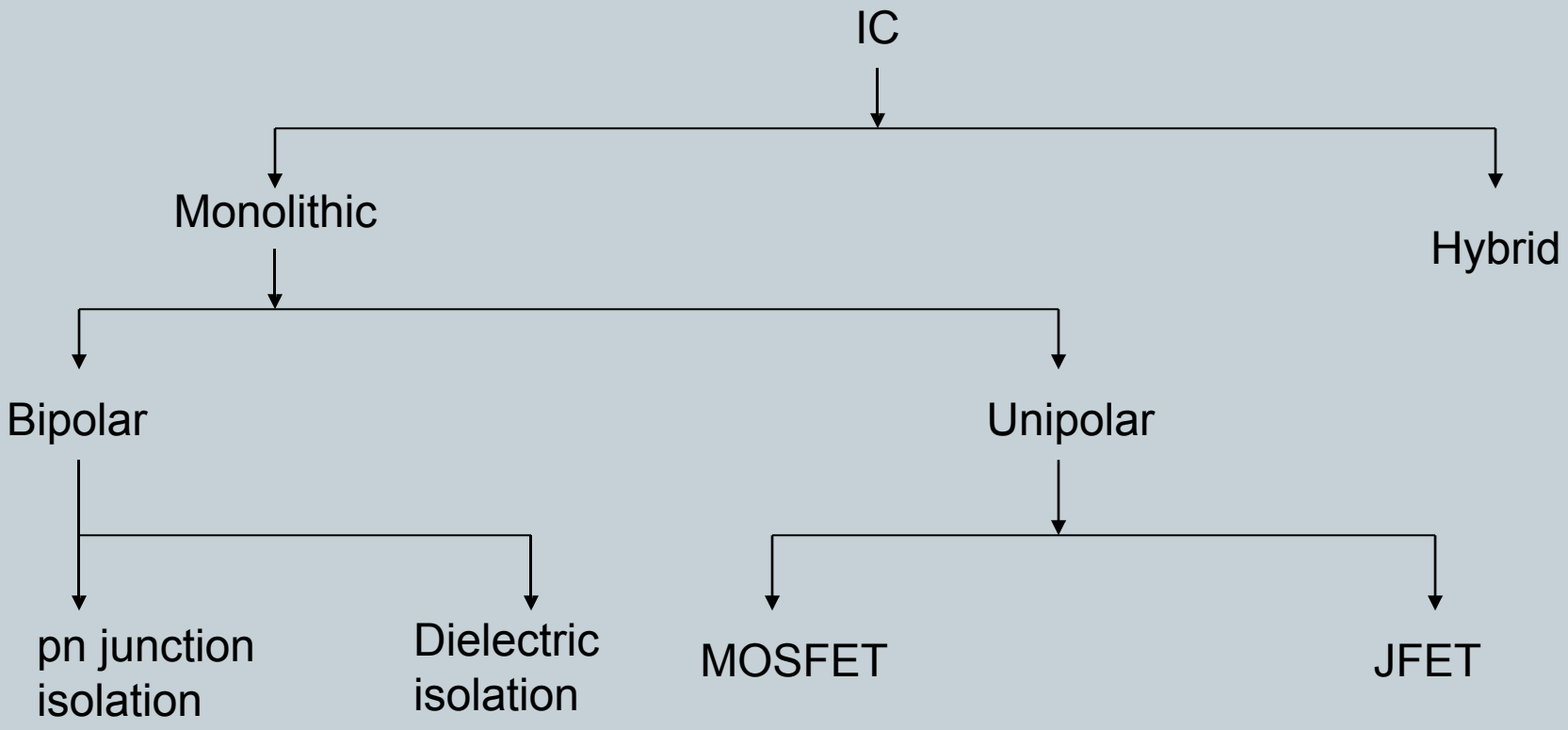
- CMOS : CMOS Inverter, CMOS chara.
- CMOS configuration: Wired Logic, open drain o/p
- Interfacing : TTL to CMOS and CMOS to TTL Interfacing

CMOS Reference books

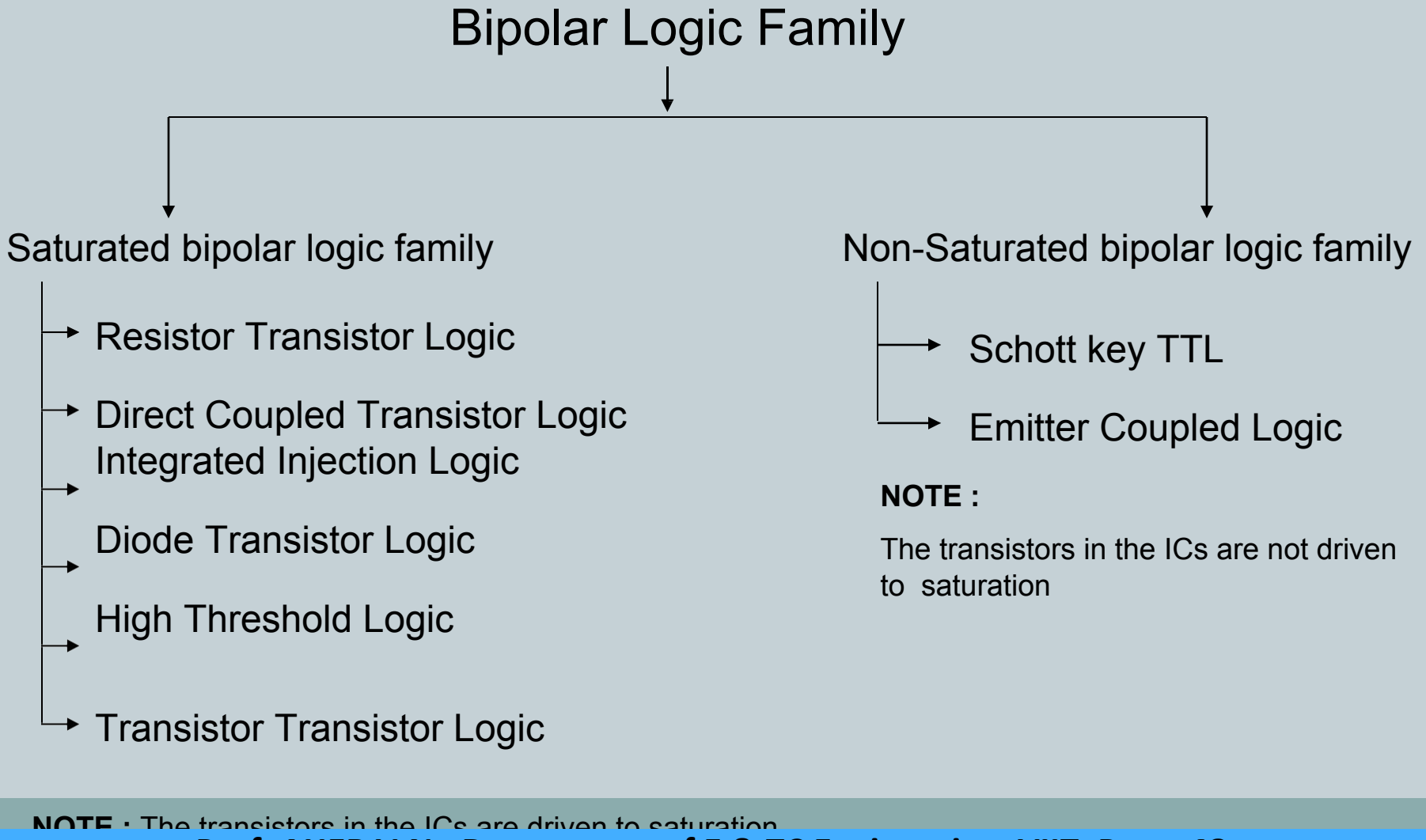
- List of Reference books

- 1. Analog CMOS Design by
  Razavi, McGraw Hill Publication
- 2. CMOS: Circuit Design, Layout , and Simulation by
  Boise, Baker, Lee, Prentice Hall Publication
- 3. Analog VLSI : Signal and Information Processing by
  Ismail and Feiz, McGraw Hill Publication

A group of compatible ICs with the same logic levels & supply voltages for performing various logic functions are fabricated using a special circuit configuration which is referred to as a **LOGIC FAMILY**.


IC
Monolithic
Hybrid
Bipolar
Unipolar
pn junction isolation
Dielectric isolation
MOSFET
JFET

Bipolar Logic Family



Unipolar Logic Family

- PMOS
- NMOS
- CMOS

NOTE :

Only MOSFETS are used widely in Unipolar Logic Families

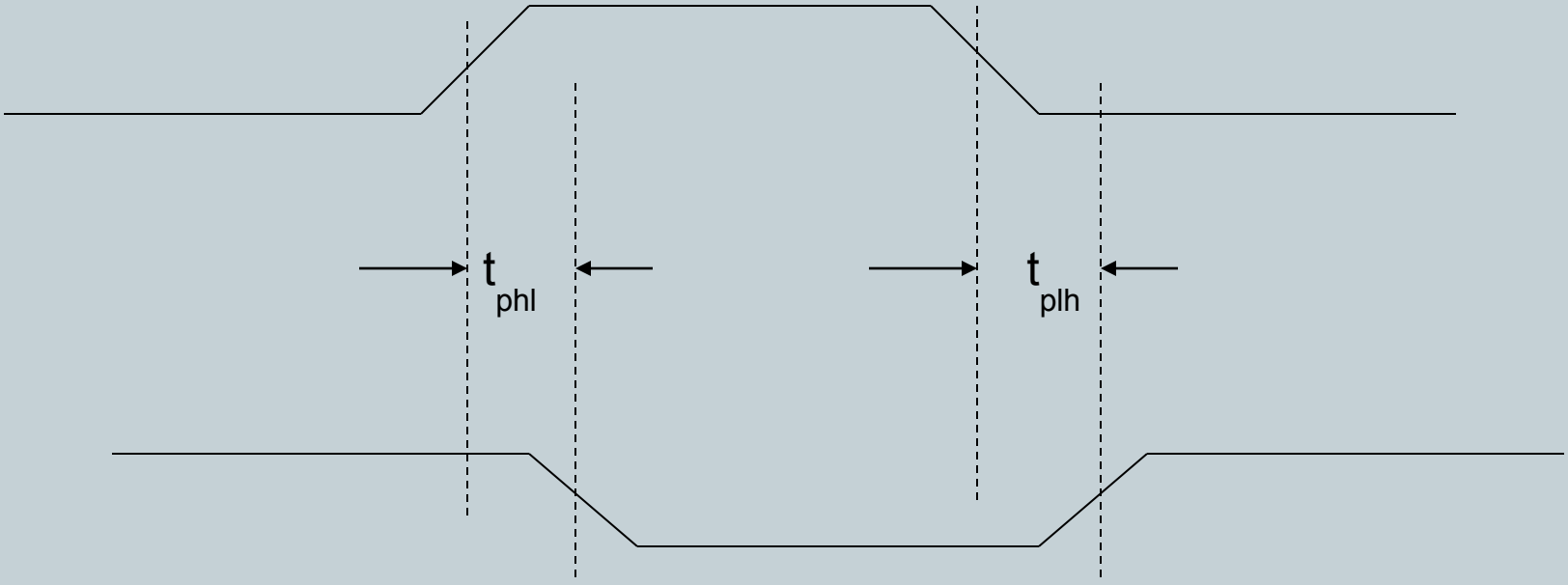
Classification of Integration

IC CLASS	INDIVIDUAL BASIC GATES GATES	NUMBER OF COMPONENTS
SSI SSI	<12 <12	<100 <100
MSI MSI	12 to 99 12 to 99	100 to 1000 100 to 1000
LSI LSI	100 to 1000 100 to 1000	1000 to 10000 1000 to 10000
VLSI VLSI	>1000 >1000	>10000 >10000

Parameters of Digital ICs

- Speed of operation
- Power dissipation
- Figure of merit
- Fanout
- Current and Voltage parameters
- Noise immunity
- Operating temperature range
- Power supply requirements
- Flexibility available

Speed of Operation



Speed of operation = ½ (t_{phl} + t_{plh})

Power Dissipation

Power dissipation = V_{cc} X I_{cc}

I_{cc} = ½ ($I_{cc}(0)$ + $I_{cc}(1)$)

Figure of Merit

- It is defined as the product of the propagation delay in ns and power dissipation in mW.

Fanout

- It is defined as the maximum number of similar gates that can be connected or driven by a gate.
- It is also called as “Loading Factor”.
- High Fanout is desirable.

Current and Voltage Parameters

- V_{ih}, V_{il}, V_{oh}, V_{ol}
- I_{ih}, I_{il}, I_{oh}, I_{ol}

- The suffix i represents i/p, o represents o/p, l represents low level logic, h represents high level logic

Noise Immunity

- Circuit's ability to tolerate noise signals is known as Noise Immunity.
- Quantitative measure of noise immunity is called as Noise figure or Noise margin.
- High Noise figure is desired.

Operating Temperature Range

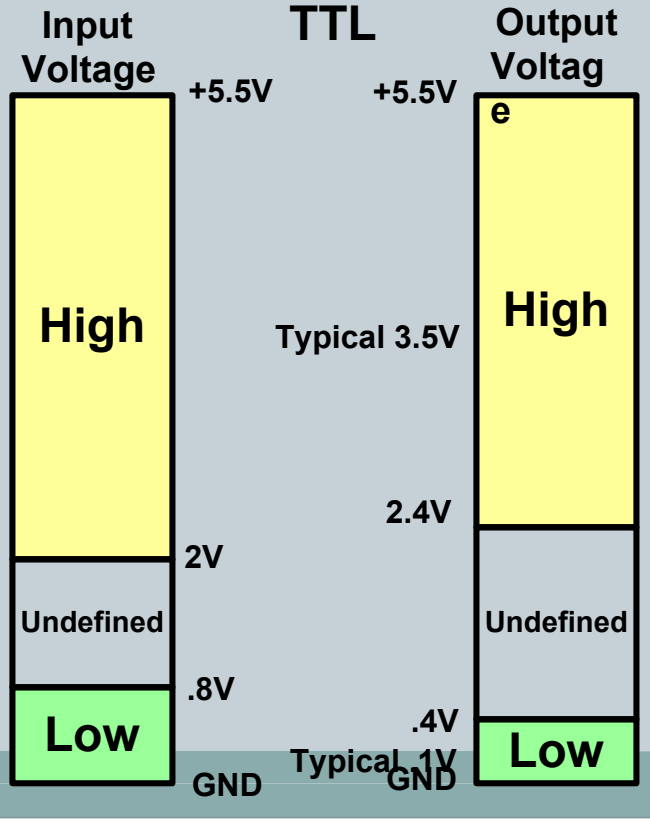
- Accepted temperature ranges are….

  → 0°C to +70°C for consumer & industrial applications.

  → -55°C to +125°C for military applications.

Logic Levels

- Voltage characteristics of TTL (Transistor-Transistor Logic) and CMOS ICs (Complimentary Metal Oxide Semiconductor Integrated Circuits)
  - Logical 0 (Low): Ground-.8V
  - Logical 1 (High): 2- 5.5V
  - Symbol:



TTL Configuration

- Transistor Transistor Logic (TTL)
  - Basic 2 input NAND gate (Diagram, operation)
- Wired Logic
  - (Diagram, operation)
- Open Collector
  - (Diagram, operation)
- TTL with Totem Pole
  - (Diagram, operation,limitation)

TTL Configuration cont.

- Three State Output TTL

  (Diagram, operation)

- Schottky TTL

  (symbol,circuit configuration, operation,types)

TTL Example SN74LS00

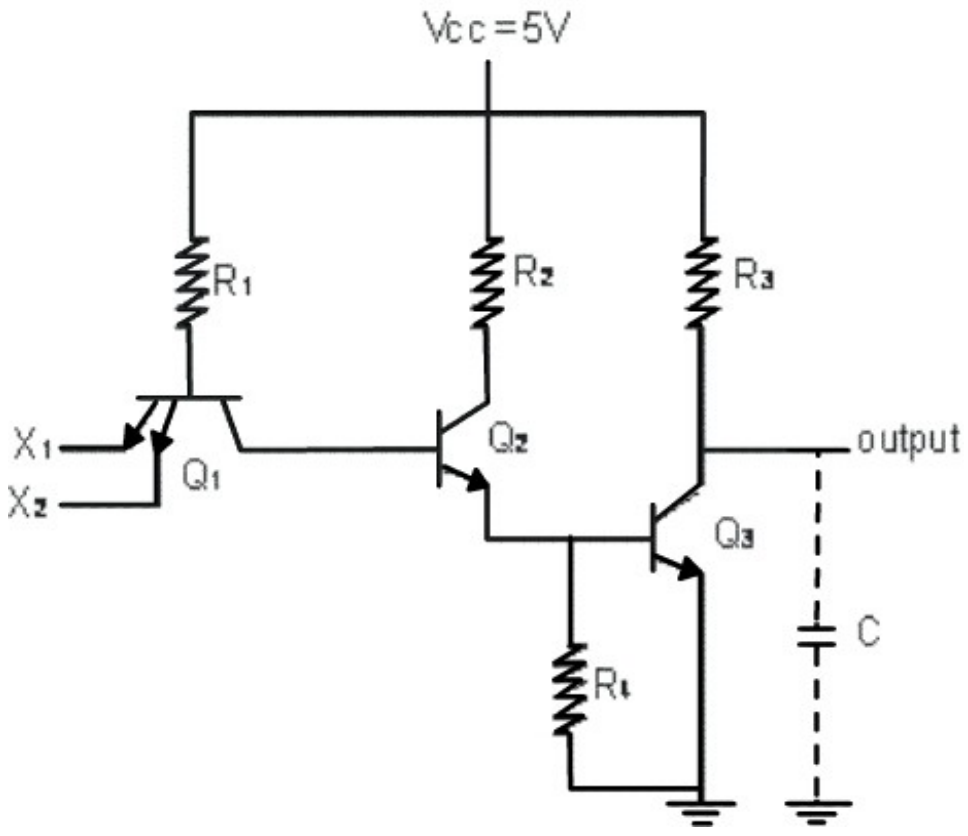
Recommended operating conditions

- V_{cc} supply voltage — $5V \pm 0.5\ V$
- Input voltages — $V_{IH} = 2V$, $V_{IL} = 0.8V$

TTL Example SN74LS00

- Output Voltage (worst) $V_{OH} = 2.7V$, $V_{OL} = 0.5V$
- Propagation delay $t_{pd} = 10\text{-}15$ ns
- Fan-out 20 TTL loads

TTL Basic NAND Gate



R1=4k Ω, R2=1.6kΩ, R3=4k Ω, R4=1k Ω,

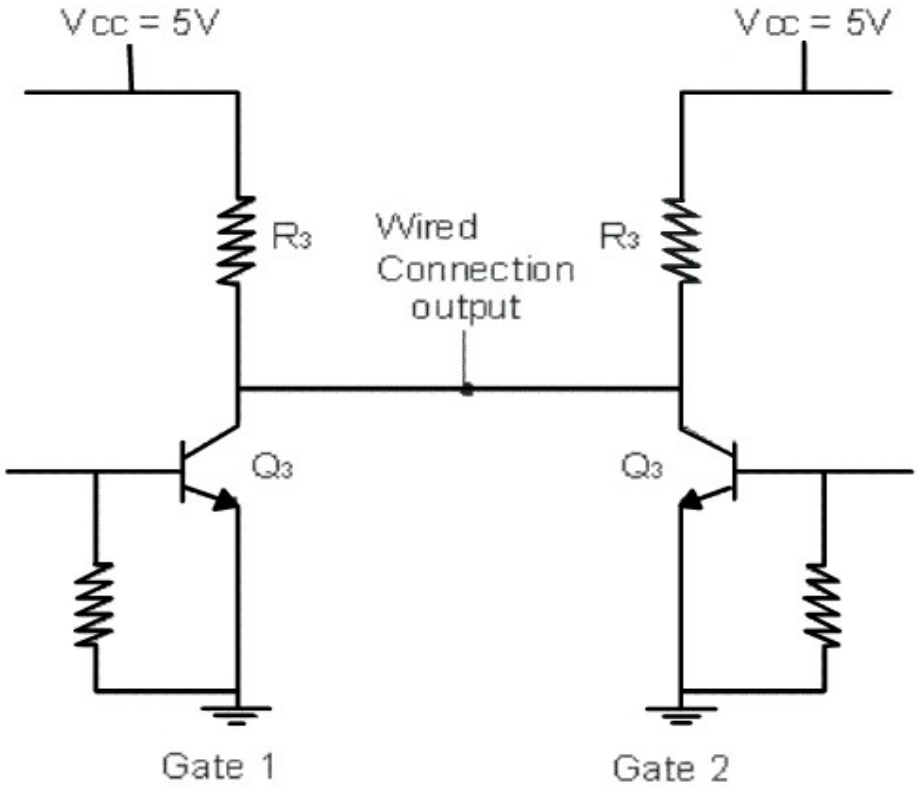
X1	X2	Q1	Q2	Q3	Vout
L	L	sat	off	off	H
L	H	sat	off	off	H
H	L	sat	off	off	H
H	H	iam	sat	sat	L

iam-inverted active mode

BC-forward biased

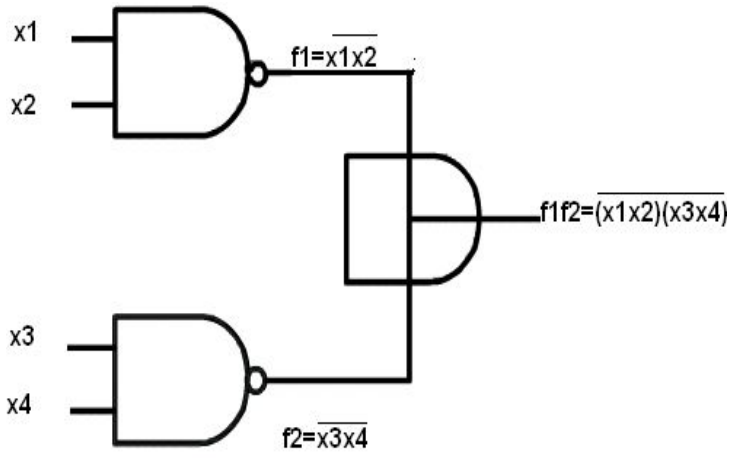
BE-reverse biased

Wired Logic



- It is possible to connect the outputs of some gates together to achieve the desired logic behaviour .
- This is called *Wired Logic*

Wired Logic Cont.

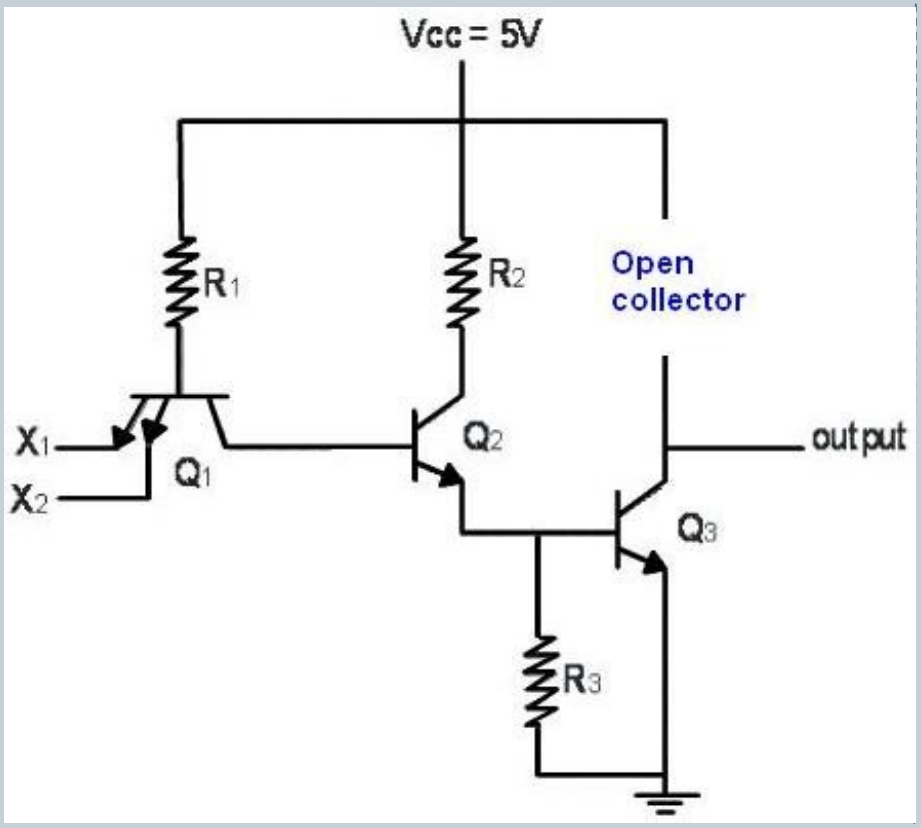


The outputs of the two NAND gates can be Wired together to achieve the desired logic.

The AND gate is implicit by the wired connection and is called the WIRED-AND connection

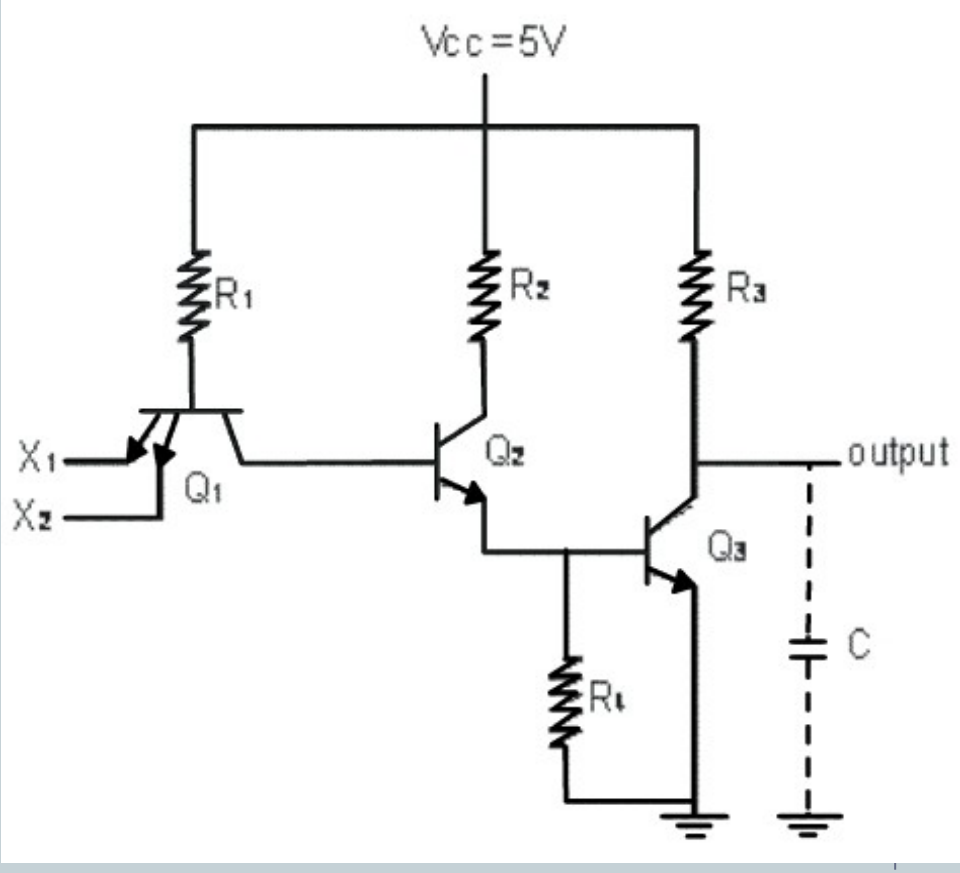
*Wired Logic increases the power dissipation.

Open Collector



- Hence open collector gates without R_3 are available and are called open collector TTL.
- A single collector resistor called passive pull up resistor must be connected externally.

Effect of Parasitic Capacitance



- Time constant for charging is R_3C when o/p changes L to H.
- Discharging time constant is $R_{Q3on}C$ when o/p changes from H to L.

Solution: an *active pull-up circuit* called totem pole

What is a totem pole?

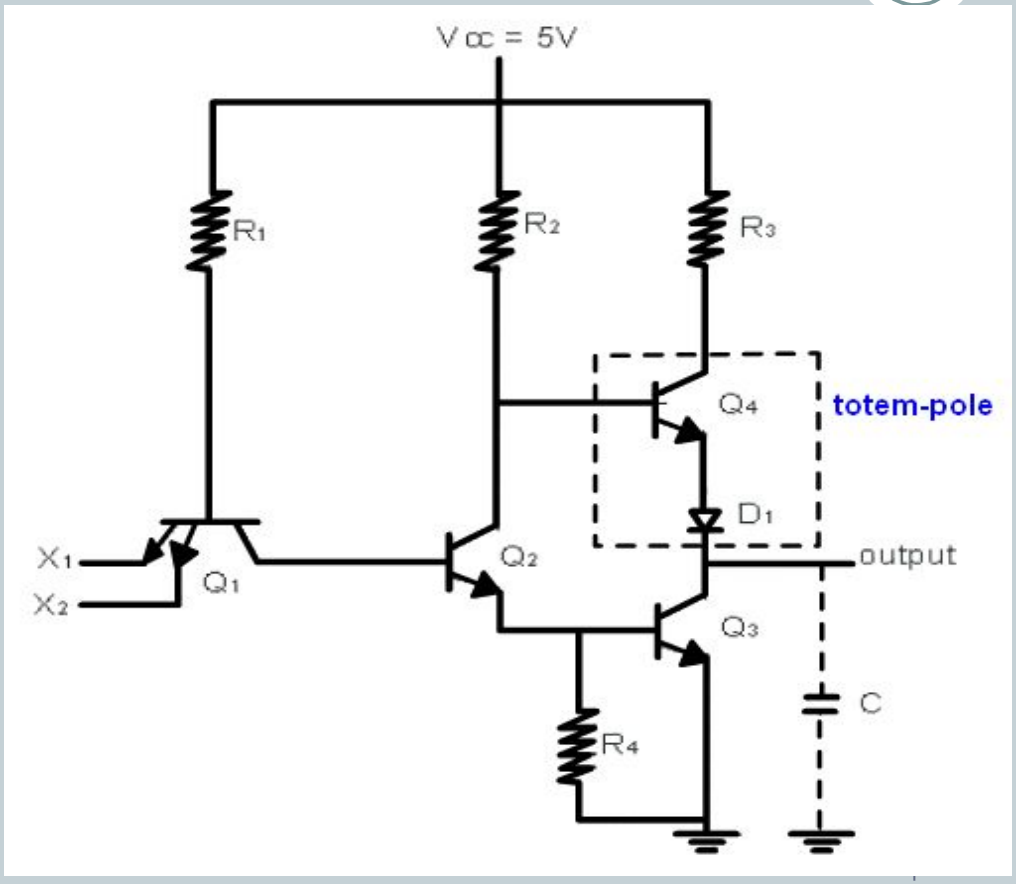
In art and history….

Totem poles are carved and painted vertical logs, constructed by many northwest coast native american indian people. The poles display mythological images, animal spirits whose significance is their association with the lineage.

Totem pole in TTL ?

- What is totem pole?
  - addition of an active pull up circuit in the output of a gate is called totem pole.
- Why totem pole?
  - To increase the switching speed of the gate which is limited due to the parasitic capacitance at the output.

Totem pole



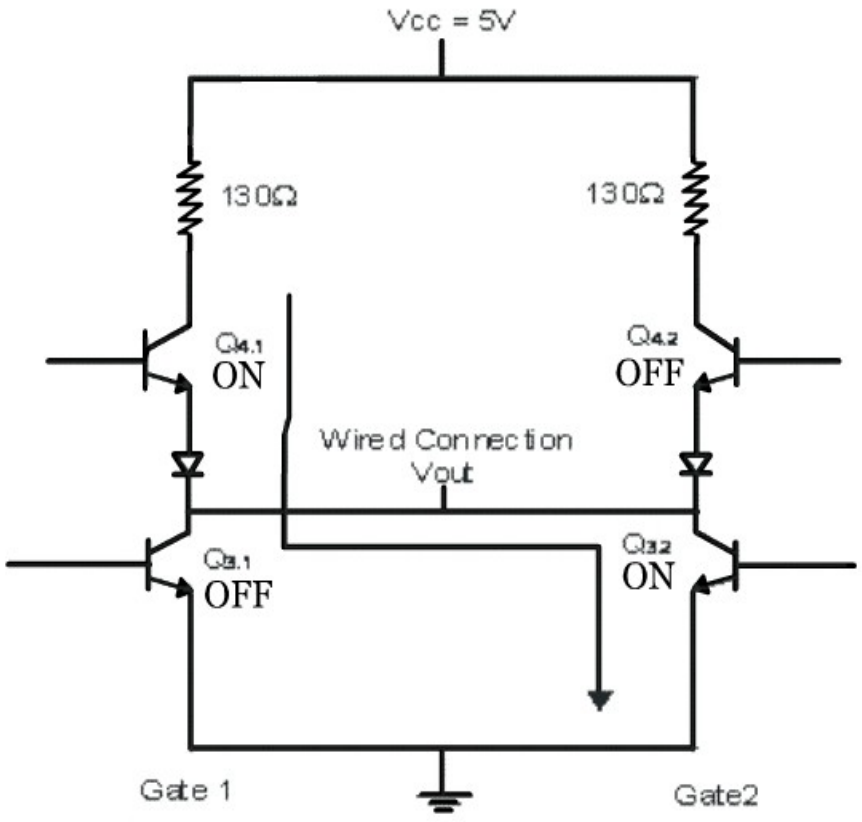
Requirement is :

R_3 (small)-for output transition L to H(small RC time const)

R_3(large) -for output transition H to L(low power dissipation)

R1=4k Ω, R2=1.6kΩ, R3=130Ω, R4=1k Ω,

Is Wired Totem pole Possible?



Disadvantage of Totem Pole- it does not permit wired logic.

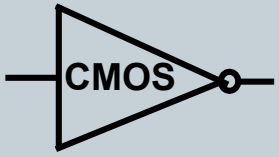
$Q_{3,1}$ -off , $Q_{4,2}$ -off

$Q_{3,2}$ -sat , $Q_{4,1}$ -normal active mode

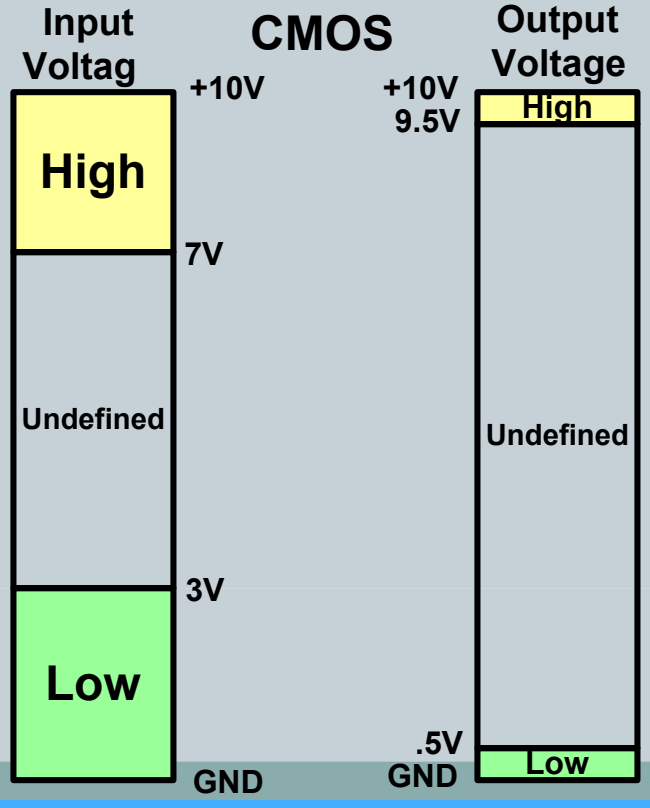
$Q_{3,2}$ –goes from sat to active. $V_{out} > V_{olmax}$

Logic Levels Cont.

- Voltage characteristics of CMOS logic families.
  - 4000 and 74C00 series.
    - Logical 0 (Low): Ground-.5V
    - Logical 1 (High): 7-10V
    - Symbol:

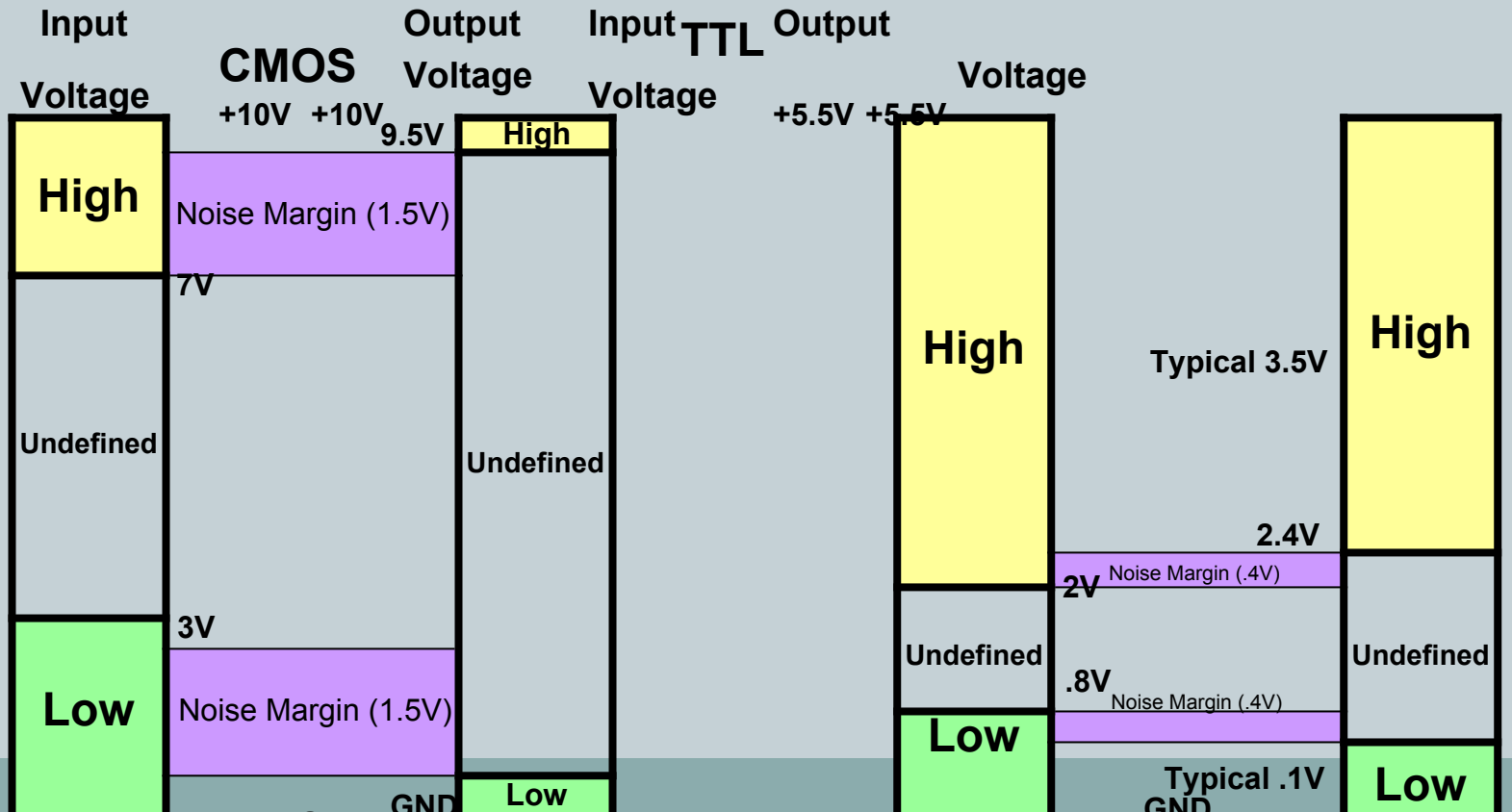


  - Advantages:
    1. Low power requirements
    2. Good noise immunity



Noise Levels

- Noise immunity (noise margin): Circuits insensitivity or resistance to undesired voltages or noise.
- Noise margin comparison: TTL vs. CMOS



Noise

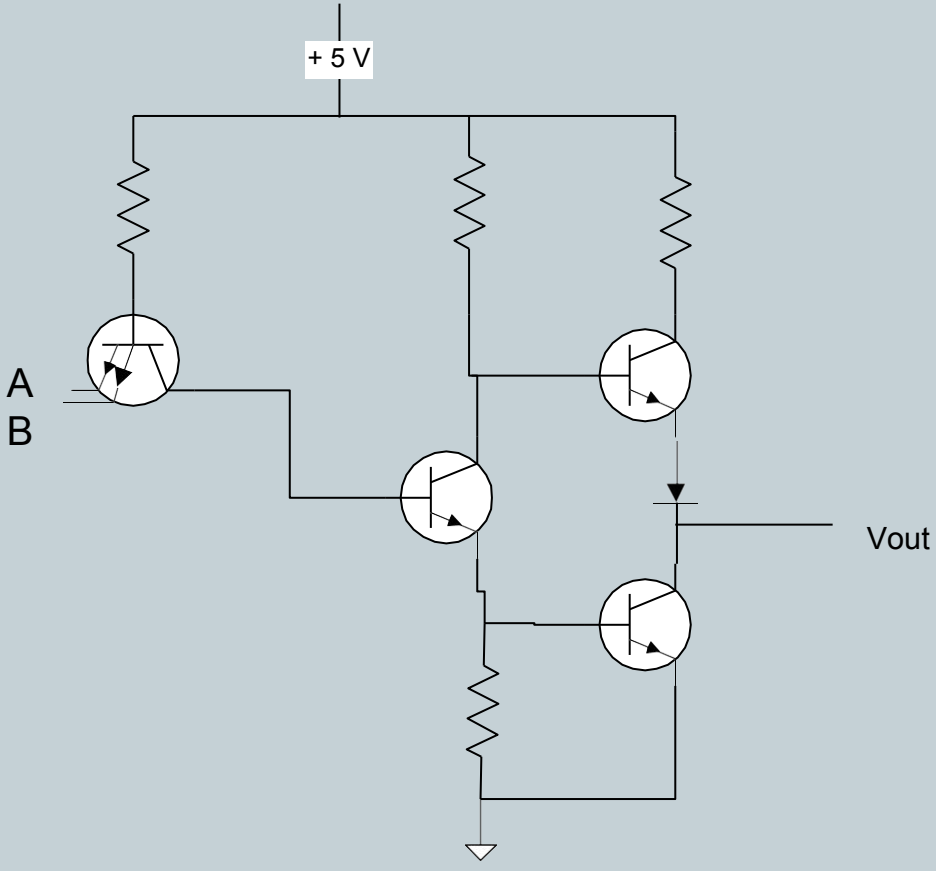
- In a digital circuit, noise is unwanted voltages.
- In actual practice, the noise is greater because the voltage must be increased to the switching threshold.
- Switching actually occurs in the undefined region. Varies widely by manufacturer, temperature and quality of chip.

Bipolar Logic Families

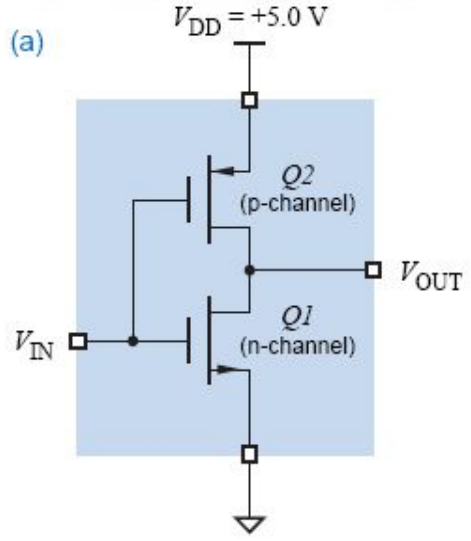
7400 series (5400 “mil spec”) 74 S - Schottky
74 LS - low power Schottky
74 AS - advanced Schottky
74 ALS - advanced low power Schottky 74 F - Fast TTL

Bipolar Logic Families

A Simplified TTL NAND Gate



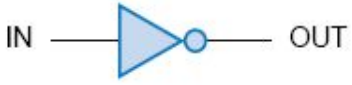
CMOS Inverter



(b)

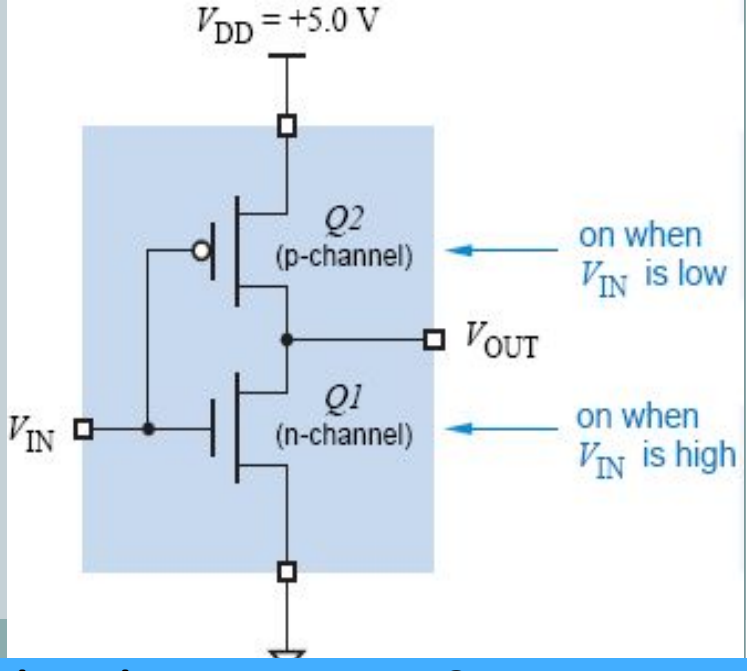
V_{IN}	Q1	Q2	V_{OUT}
0.0 (L)	off	on	5.0 (H)
5.0 (H)	on	off	0.0 (L)

(c)

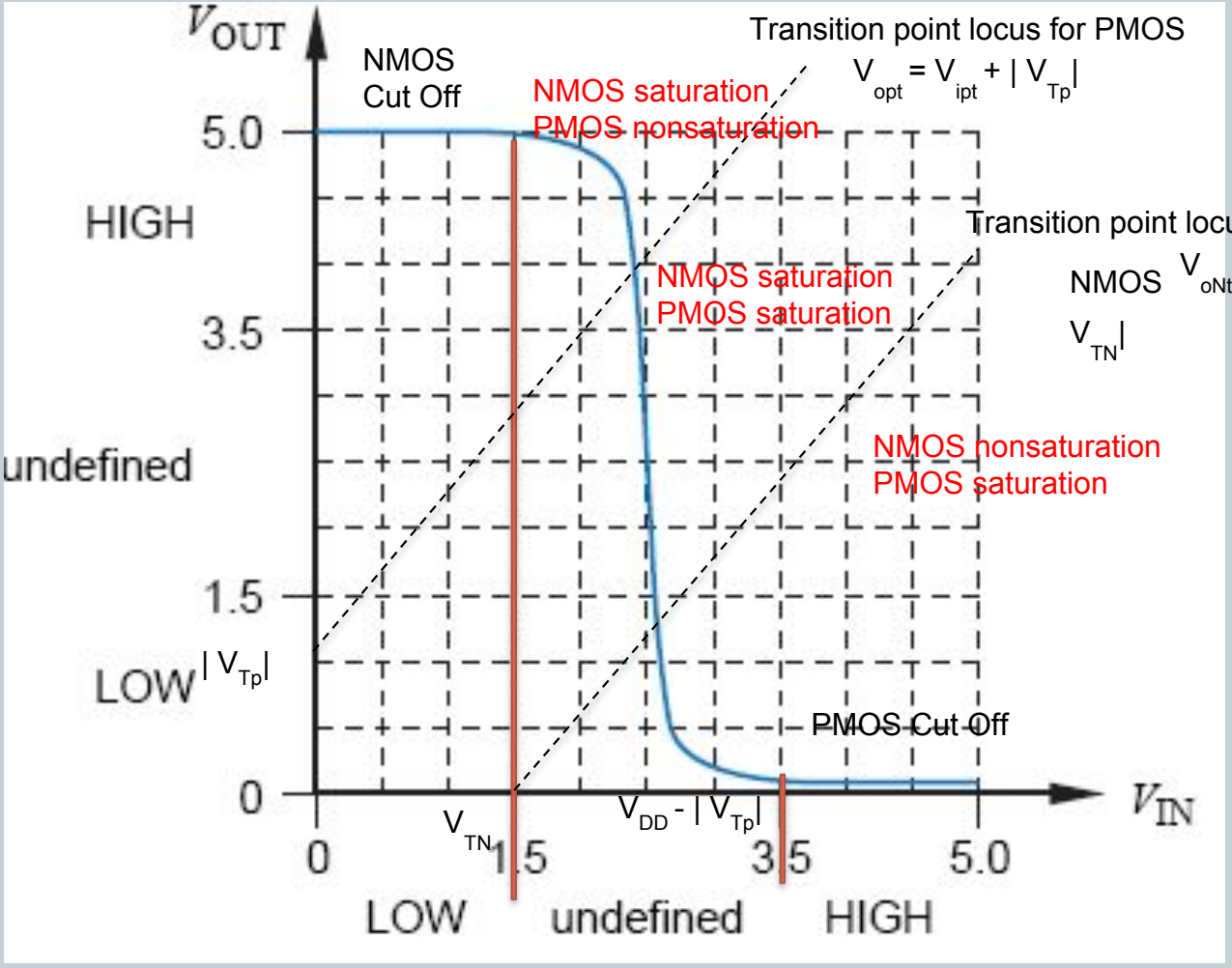


Symbol and Truth table for Inverter Circuit

Working of the Inverter Circuit



CMOS INVERTER Transfer Characterstics



CMOS INVERTER Transfer Characterstics

Continue....

The graph is divided in three regions as :

1) $V_{in} > V_{lt}$: NMOS saturated PMOS unsaturated in which Input Voltage at transition will be $V_{in} = V_{GSN} = V_{TN} +$

Finding V_{in} at transition point by equating two drain currents, $i_{DN} = i_{DP}$

$$K_N[V_{GSN} - V_{TN}]^2 = K_P[2(V_{SGP}+V_{TP})V_{SDP} - V^2]$$

$$V_{GSN} = V_I, V_{SGP} = V_{DD} - V_I, V_{SDP} = V_{DD} - V_O^{SDP}$$

2) $V_{in} = V_{lt}$: NMOS saturated, PMOS saturated in which

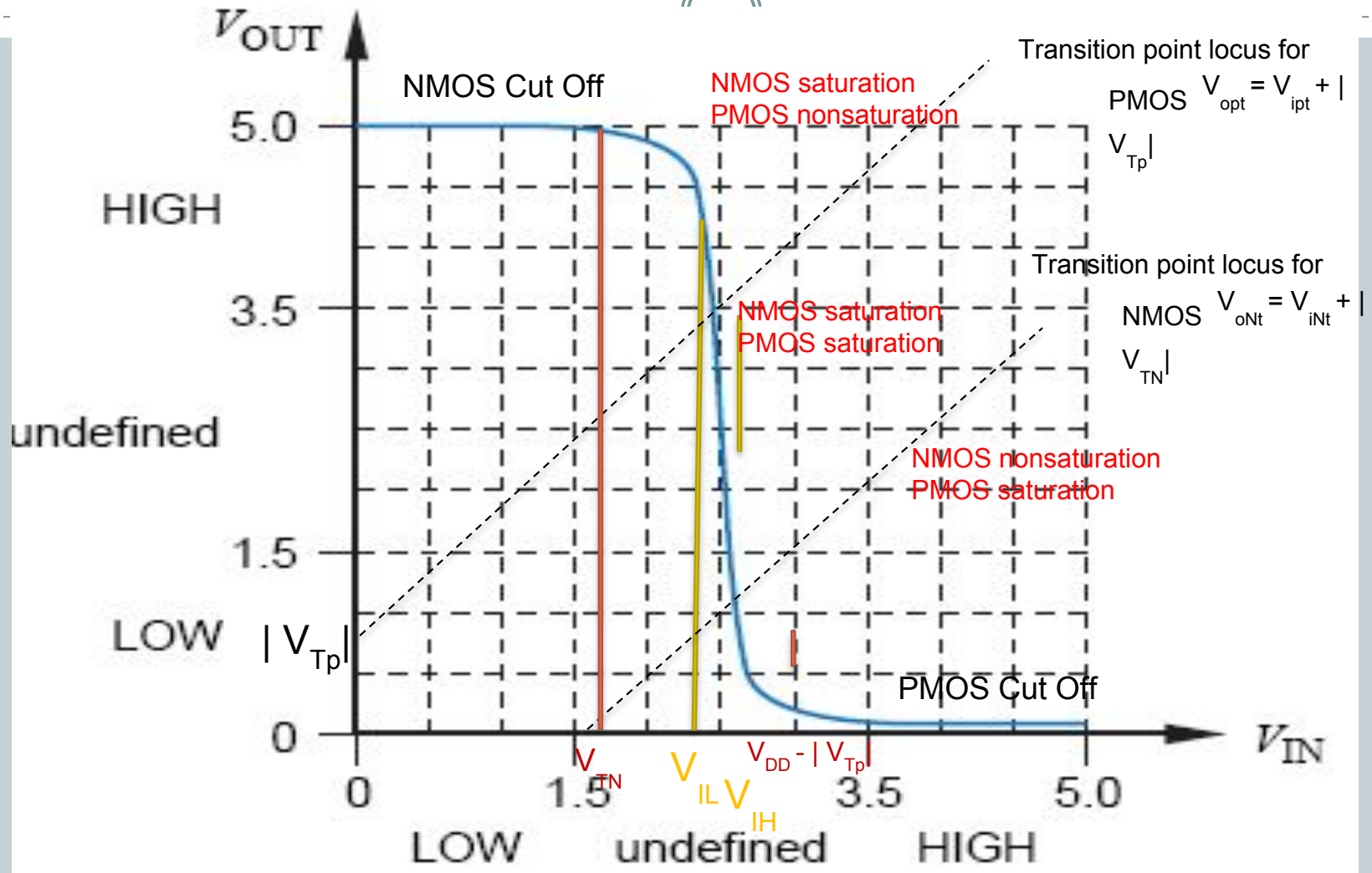
Finding V_{in} at transition point by equating two drain currents,

$$K_N[V_{GSN} - V_{TN}]^2 = K_P[V_{GSP} - V_{TP}]^2$$

1) $V_{in} < V_{lt}$: NMOS unsaturated, PMOS saturated in which

$$K_P[V_{GSP} - V_{TP}]^2 = K_N[2(V_{SGN}+V_{TN})V_{SDN} - V^2_{SDN}]$$

Noise Margin



Inverter gain is less than unity in the range of $V_{IL} \geq V_I$ & $V_I \leq V_{IH}$ o/p change slowly w.r.t. i/p

Noise Margin

Continue....

V_{IH} and V_{IL} determines the noise margin and are defined as the point at which

$$d_{VO}/d_{VI} = -1$$

Derivation for V_{IL} : when $V_I > V_{It}$ at the point V_{IL}

Equation 2 gives the relation between I/P and O/p. taking derivative of equation w.r.t. V_I

$$2K_N[V_I - V_{TN}] = K_P[-2(V_{DD}-V_O)-2(V_{DD}-V_I+V_{TP})dV_O/dV_I - 2(V_{DD}-V_O)(-dV_O/dV_I)$$

$$V_o = V_{OHU} = \tfrac{1}{2}(2V_I + V_{DD} - V_{TN} - V_{TP}) \quad \& \quad V_{IL} = V_{TN} + 3/8\,[V_{DD} + V_{TP} - V_{TN}]$$

$$NM_L = V_{IL} - V_{OLU}$$

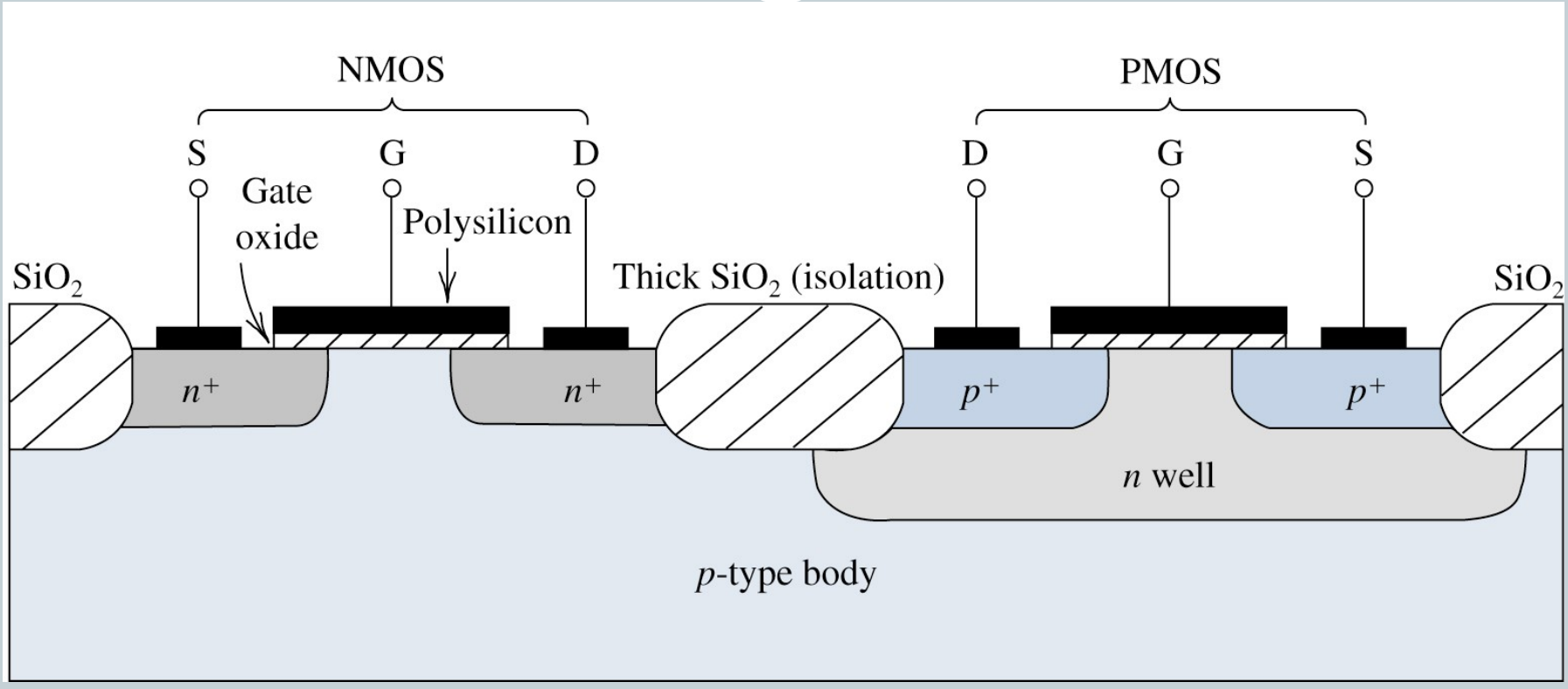
Derivation for V_{IH} : when $V_I < V_{It}$ at the point V_{IH}

$$K_N[2(V_I - V_{TN})\,dV_O/dV_I + 2V_O - 2V_O\,dV_O/dV_I] = 2K_P(V_{DD}-V_I+V_{TP}) - (1)$$

$$V_o = V_{OLU} = \tfrac{1}{2}(2V_I - V_{DD} - V_{TN} - V_{TP}) \quad \& \quad V_{IH} = V_{TN} + 5/8\,[V_{DD} + V_{TP} - V_{TN}]$$

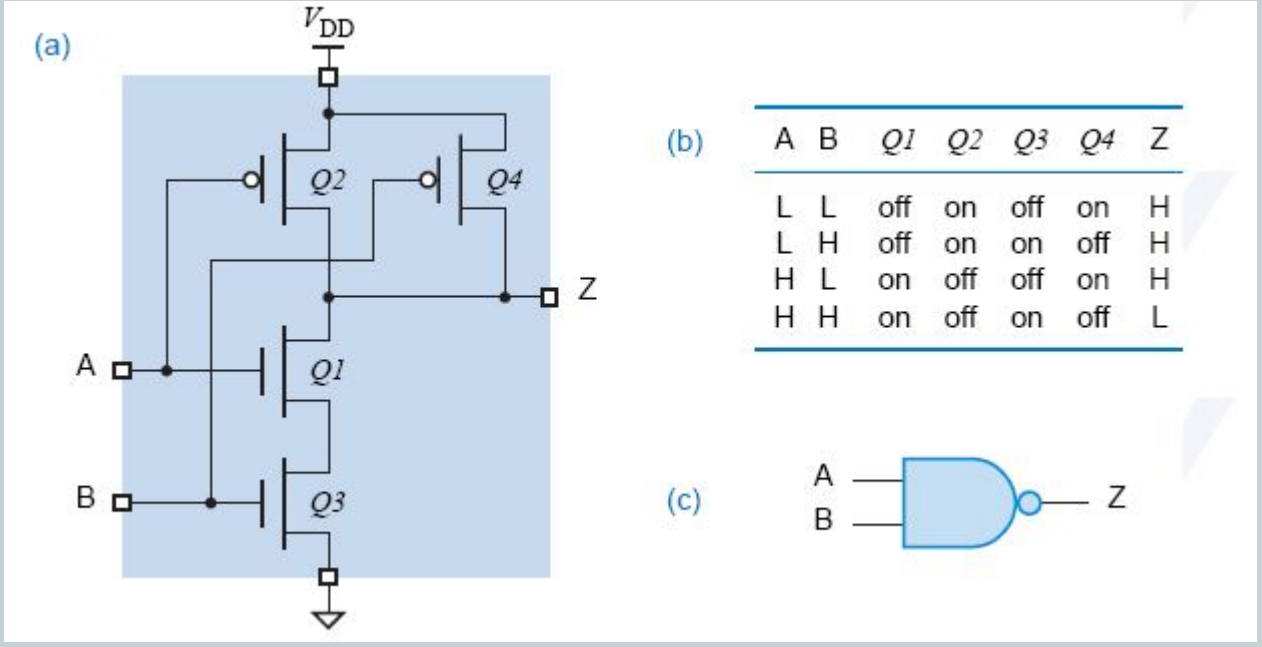
$$NM_L = V_{OHU} - V_{IH}$$

CMOS INVERTER CONSTRUCTION



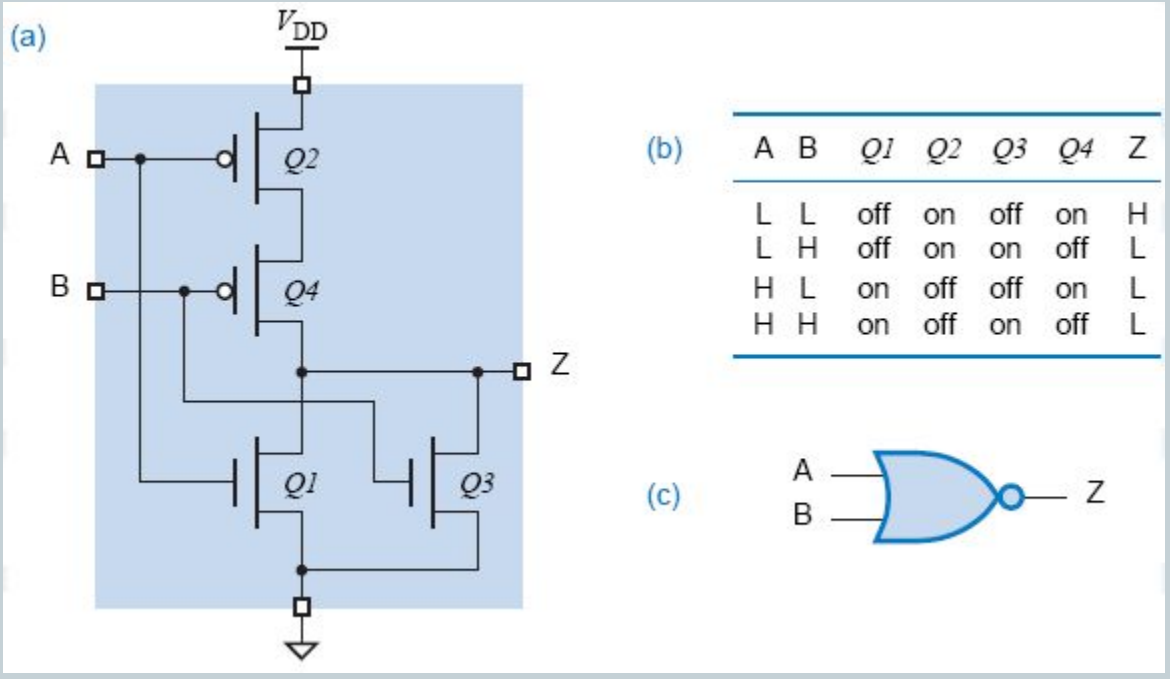
Cross section of a CMOS integrated circuit. Note that the PMOS transistor is formed in a separate *n-type region,*known as an *n well. Another arrangement is also possible in which an n-type body is used and the n device is formed in a p well.*

CMOS NAND GATE



A	B	Q1	Q2	Q3	Q4	Z
L	L	off	on	off	on	H
L	H	off	on	on	off	H
H	L	on	off	off	on	H
H	H	on	off	on	off	L

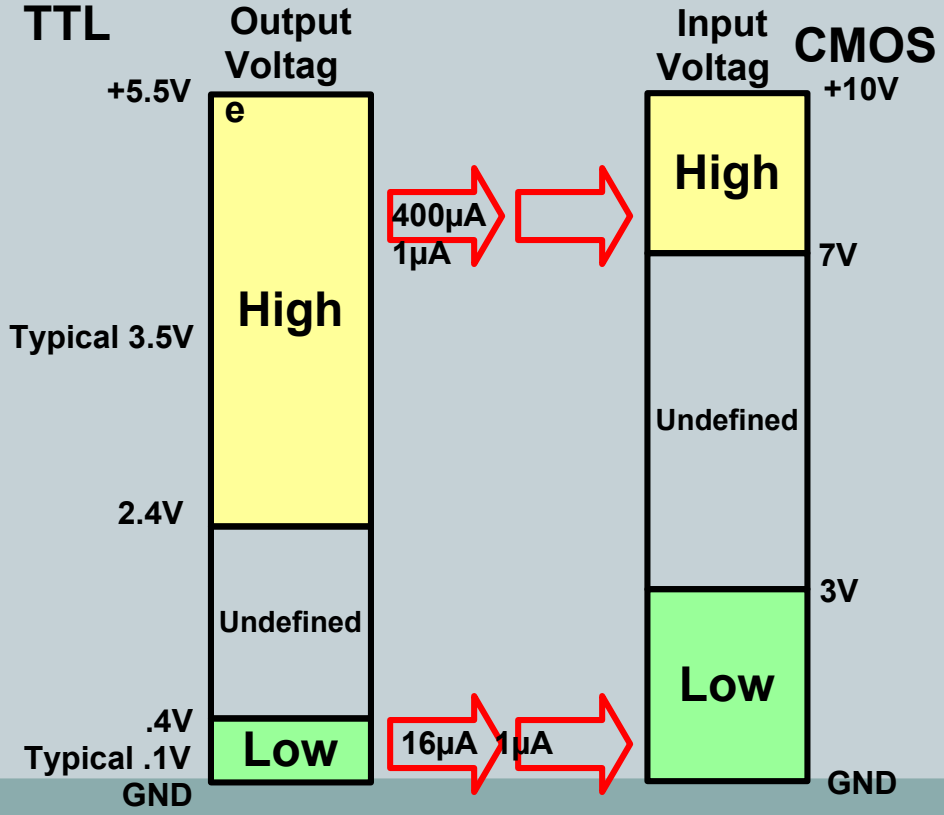
CMOS NOR GATE

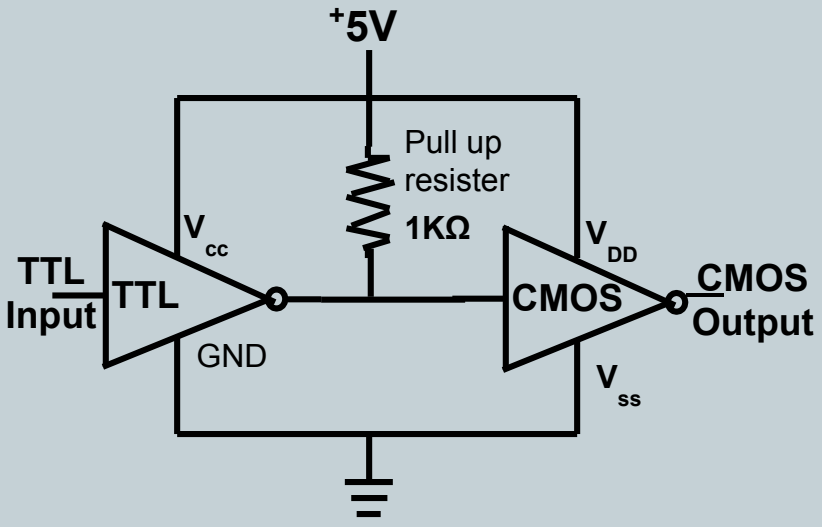


A	B	Q1	Q2	Q3	Q4	Z
L	L	off	on	off	on	H
L	H	off	on	on	off	L
H	L	on	off	off	on	L
H	H	on	off	on	off	L

Interfacing TTL and CMOS ICs

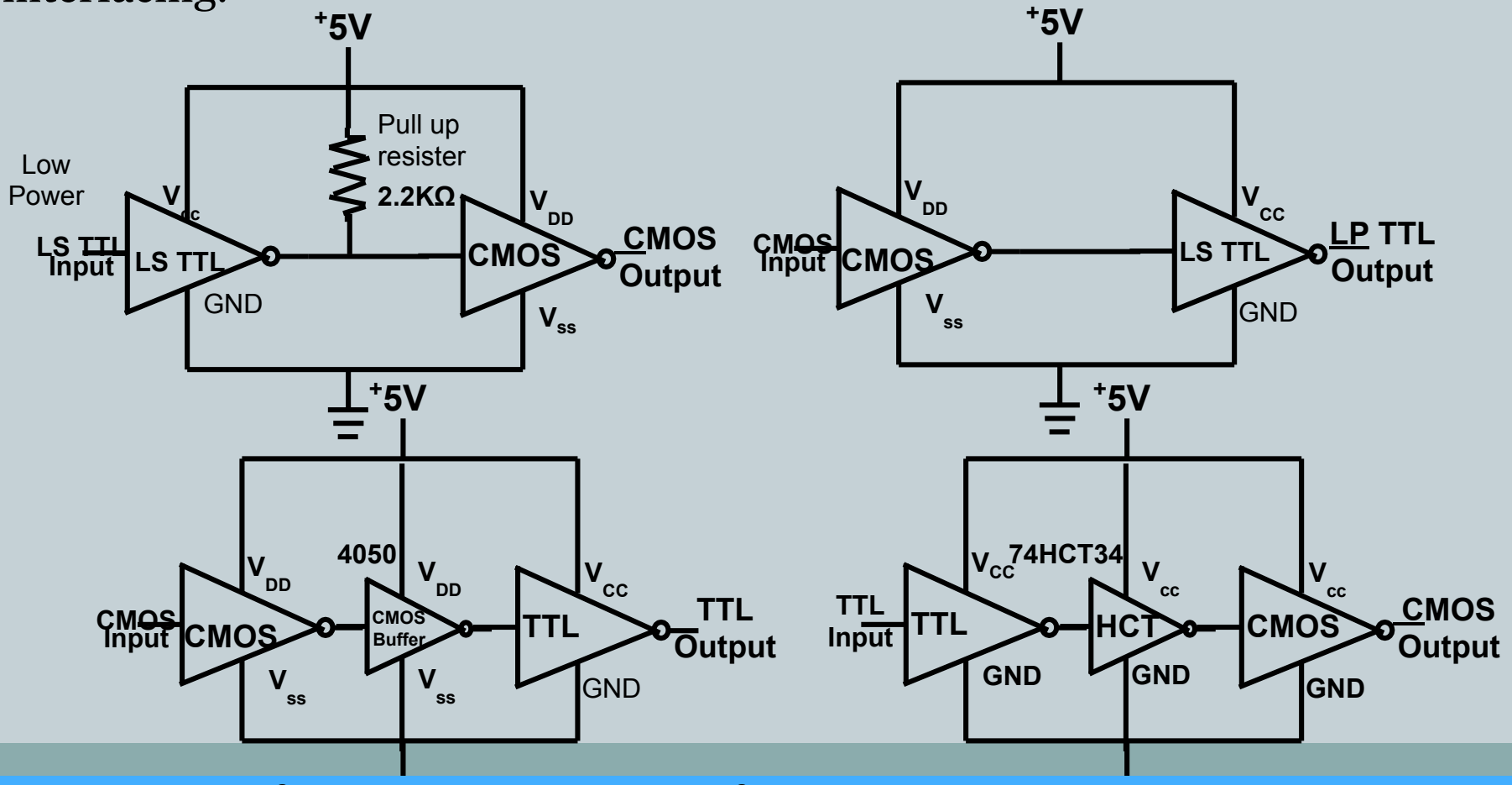
- TTL & CMOS logic levels (voltages) are different. Output TTL currents can drive CMOS input. A pull up resister is used on TTL output that does not fit in the high range CMOS input.





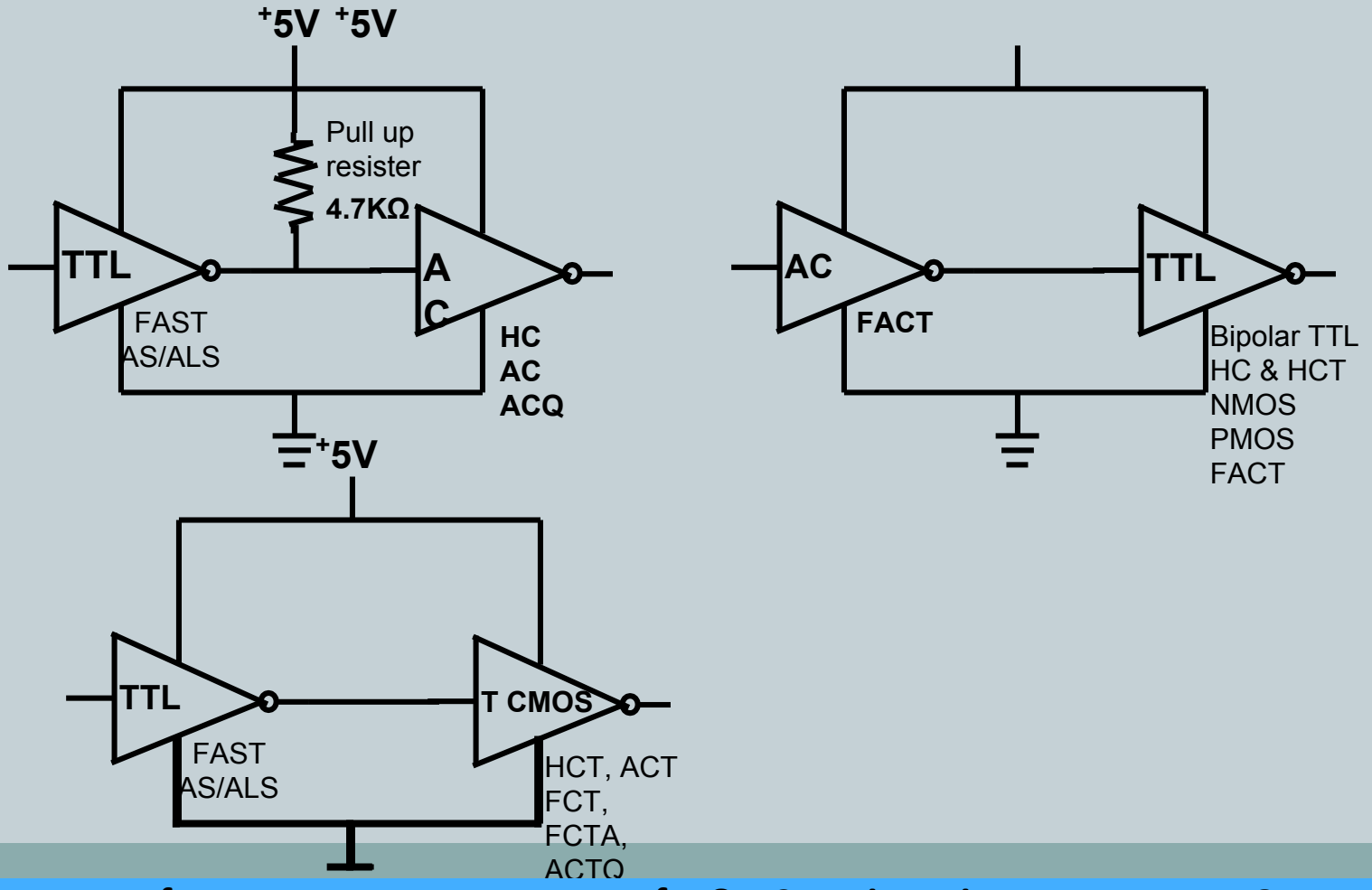
Interfacing TTL and CMOS Ics Cont.

- CMOS ICs cannot drive standard TTL ICs without special interfacing.



Interfacing TTL and CMOS Ics Cont.

FACT series CMOS ICs can drive TTL, CMOS, NMOS & PMOS ICs directly.



End of unit-5

THANK YOU ALL