Experiment 1
Characterization of a CMOS Inverter

Dhruv Ilesh Shah — 150070016

January 6, 2017

1 Overview

The CMOS inverter is one the simplest CMOS logic gate, and an essential component of all digital circuits. In this experiment, we characterize the CMOS inverter and observe its DC & AC behaviour. In particular, we observe the following.

→ DC Transfer Characteristics

→ Output Characteristics

→ Delay Characteristics

→ Delay variation with supply voltage

→ Current drawn by the Ring Oscillator

For transfer and output characteristics, IC *MM74C04* was used. The delay measurements and variations for a single CMOS inverter require very accurate instruments and hence, for the delay measurement tasks, a ring oscillator with *17* inverters was used. Variation of the period of oscillation with the load can be used to obtain a good estimate on the delay. The superposition of the switching currents of all the inverters is observed in the last part, as the total current drawn from the power source.

In Section 2 of this report, I present a brief overview of the experimental setup for the various sub-parts of the experiment performed. This is followed by the observations from the experiments, with figures of the waveforms wherever relevant. The answers to the assignment questions are also present.

2 Observations

Each part of the experiment essentially involves the CMOS inverter as the elementary unit. For this, I have used the IC *MM74C04* provided. The Opamp buffer (*TL072*) was introduced so that the DSO does not add extra load to the circuit during the act of measurement. Circuit layouts for the various parts of the experiment are shown below.

Components Used: MM74C04 ×4, TL072, Decoupling Capacitors (0.1μF) ×2, 20 KΩ potentiometer, resistors (1.2KΩ, 1Ω).

2.1 DC Transfer Characteristics

The most important characteristic of the CMOS inverter is the switching voltage V_{sw}. To find this, we must plot the transfer characteristics of the device. The circuit layout is as given below.

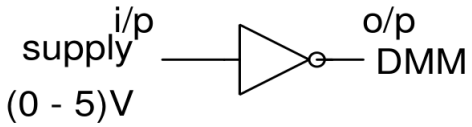


Figure 1: Observing the DC Transfer Characteristics

As we increase the input voltage from 0 to V_{DD}, the output is expected to fall from V_{DD} to 0.

$\mathbf{V_{in}}$	$\mathbf{V_{out}}$
0.3	5.01
1.3	5
1.4	4.99
1.6	4.96
1.7	4.91
1.9	4.8
2	4.64
2.1	4.53
2.19	4.28
2.2	4.08
2.215*	3.43
2.23*	2.16
2.245*	1.81
2.26*	1.34
2.275*	0.65
2.29	0.51
2.3	0.36
2.4	0.24
2.5	0.14
2.6	0.11
2.7	0.07
2.8	0.05
2.9	0.035
3	0.02
3.1	0.009
3.2	0.0036
3.5	0.0001

Table 1: DC Transfer Characteristics of the given CMOS inverter

The readings suggest a near ideal behaviour of the inverted with the $V_sw \approx 2.2V$. The behaviour can be better represented by plotting $\mathrm{V_{out}}$ versus $\mathrm{V_{in}}$ as shown in figure 2.

*Considering the least count of the Voltmeter, readings between 2.2V and 2.3V could not be obtained precisely, but the fall in V_{out} is very steep, and hence the interpolation was done. The values of V_{out} were not manipulated.

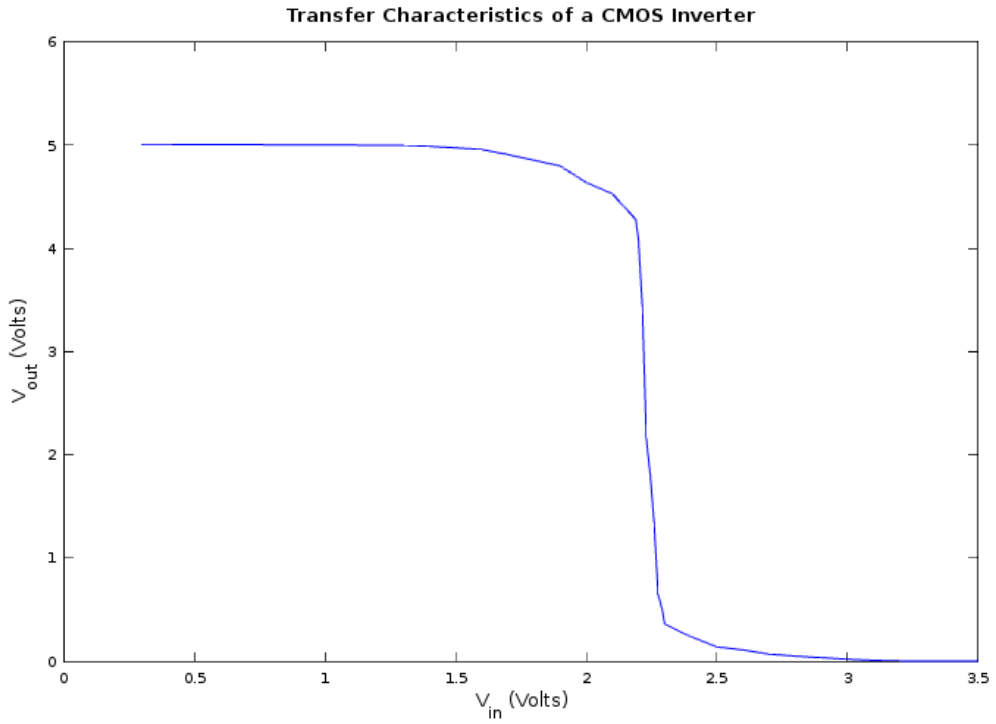


Figure 2

But we have

$$V_{sw} = \frac{\sqrt{\beta_p}(V_{DD} - V_t) + \sqrt{\beta_n}V_t}{\sqrt{\beta_p} + \sqrt{\beta_n}}$$

Substituting the values[1] gives $\frac{\beta_p}{\beta_n} \approx \frac{4}{9}$.

2.2 Output Characteristics

The CMOS inverter is used widely in many circuits, and hence it is very important to model the output characteristics of the device. The figures 4 and 5 represent the output characteristics of the device, measure according to the circuit arrangement below.

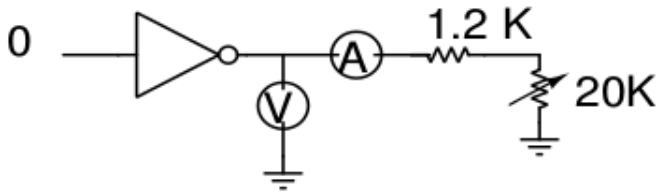


Figure 3: Ciruit Layout for observing output characteristics at *low input*

A similar layout was used for measuring the characteristics at high input.
The highly linear behaviour, with the change in the variable resistance suggests that the output impedance is largely constant.

[1] *(Here, I have used $V_t \approx 1V$)*

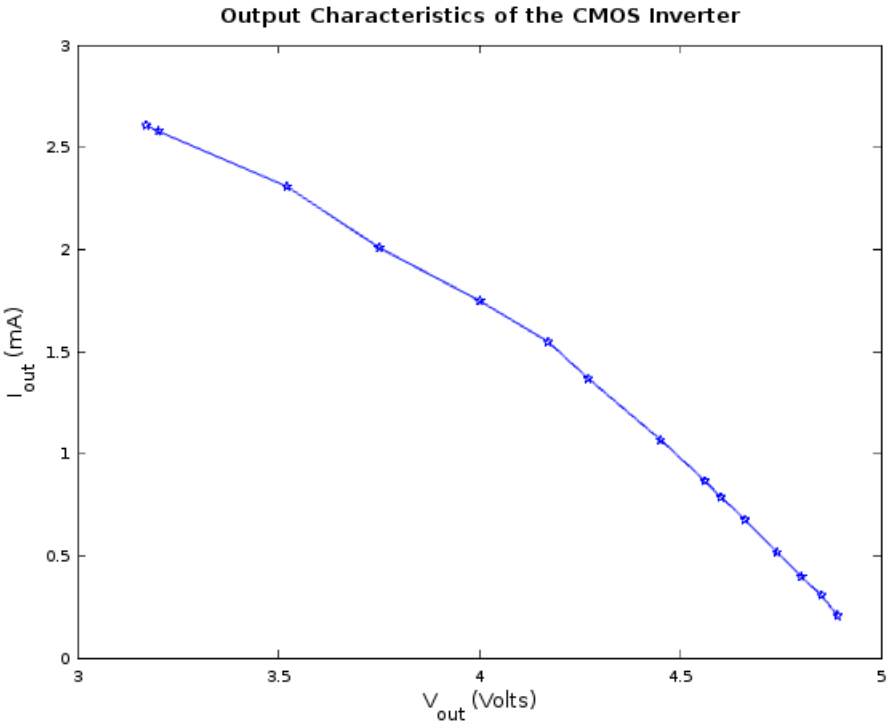


Figure 4: Output Characteristics with $V_{in} = 0$

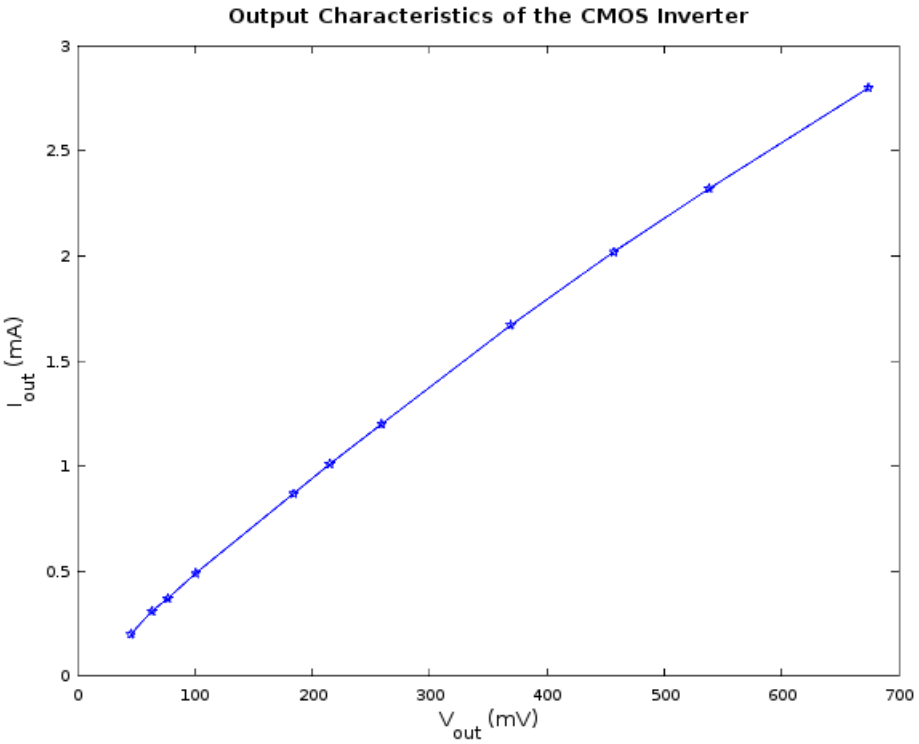


Figure 5: Output Characteristics with $V_{out} = V_{DD}$

Voltage (Volts)	Current (mA)
4.89	0.21
4.85	0.31
4.8	0.4
4.74	0.52
4.66	0.68
4.6	0.79
4.56	0.87
4.45	1.07
4.27	1.37
4.17	1.55
4	1.75
3.75	2.01
3.52	2.31
3.2	2.58
3.17	2.61

Table 2: Output Characteristics with $V_{in} = 0$

Voltage (mV)	Current (mA)
45.4	0.2
63.3	0.31
76.8	0.37
100.6	0.49
184.2	0.87
215	1.01
259	1.2
369	1.67
457	2.02
538	2.32
674	2.8

Table 3: Output Characteristics with $V_{out} = V_{DD}$

2.3 Delay Characterization of the Inverter

An inevitable feature of an inverter is the delay introduced by it, especially in a digital circuit. This delay however, is very small for each independent inverter module and hence would require highly sophisticated apparatus for monitoring. A workaround is to use a ring oscillator and model the delay indirectly, as performed in this part of the experiment.

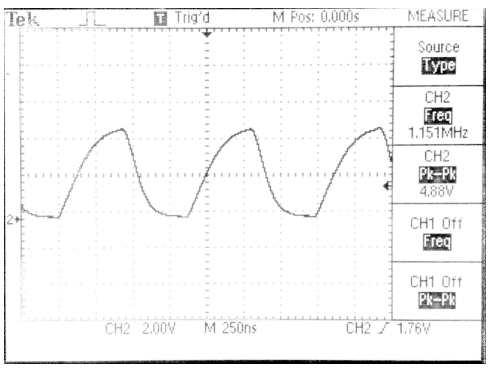
For this part, a 17-stage ring oscillator was used. We rely on the fact that the delay of an inverter can be modelled as

$$d_{abs} = k_0 + k_1 C_{load}$$

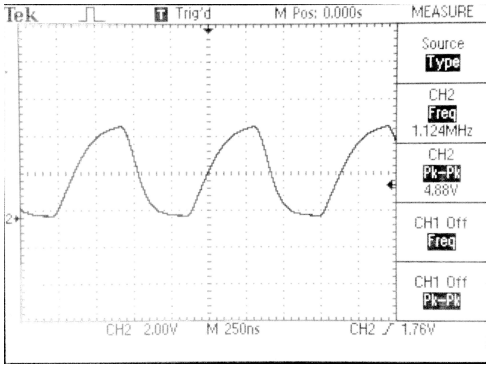
where C_{load} is the load capacitance being driven, which can be controlled by varying the number of load nodes. The basic equations guiding this scenario, in a simplified format are as follows.

$$d_{abs} = k_0 + \tau_{inv} \frac{C_{load}}{C_{in}}$$

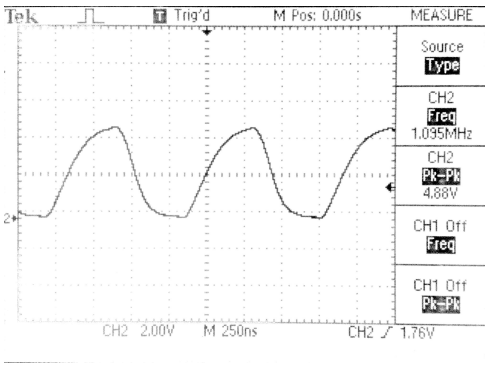
$$d_{inv} = p_{inv} + \frac{C_{load}}{C_{in}}$$



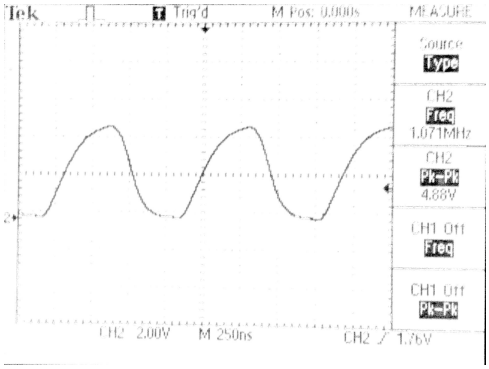
Load = 2



Load = 3



Load = 4



Load = 5

Table 4: Snapshots of the output waveform at different loads ($V_{DD} = 5V$)

Number of Load Nodes	Frequency (MHz)
2	1.151
3	1.124
4	1.095
5	1.071

Table 5: Variation of the frequency of oscillation with load *($V_{DD} = 5V$)*

Clearly, an increase in the load results in a lowering of the frequency and hence an increase in the period of oscillation. The relation is better shown as a plot.

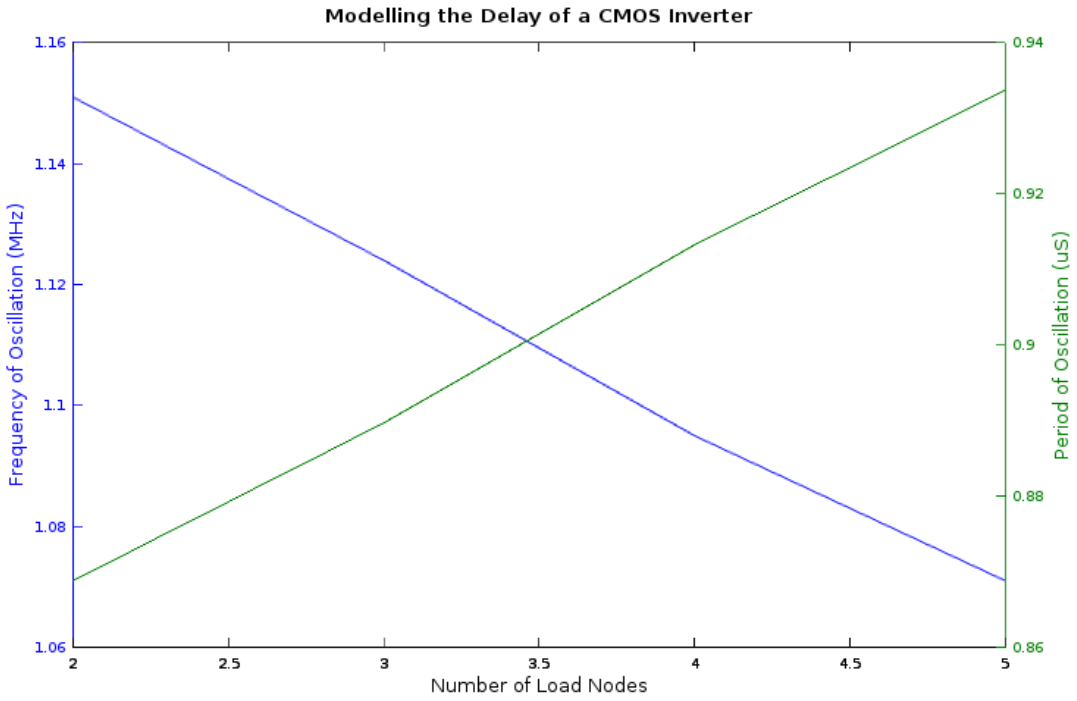


Figure 6

We have period of oscillation given by

$$\tau \times (34p_{inv} + (32 + (2 \times (1 + AdditionalLoadOutput)))$$

measured in seconds, given the rise and fall times are equal. We thus have

$$Slope = 2\tau = 0.022\mu s$$
$$Intercept = 34(\tau(p_{inv} + 1)) = 0.827$$

From above, we have

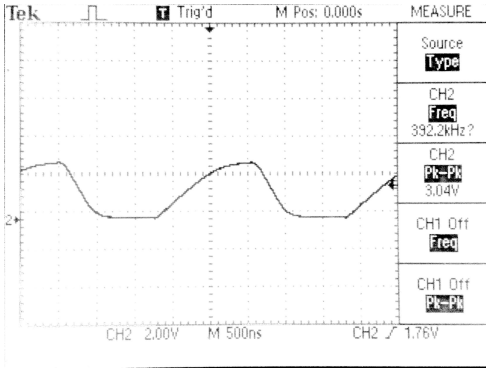
$$\tau = 0.011\mu s$$
$$p_{inv} = 1.21$$

2.4 Delay Variation with Supply Voltage

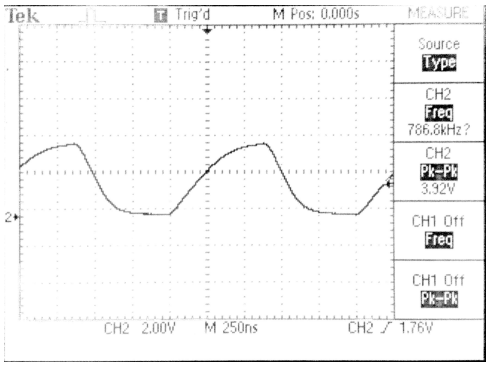
An essential feature of the CMOS inverter is that we can assume the analog device to be digital, and operational on digital H/L voltages. The definition of this high/low, however, does affect the characteristics and in this part, I have presented the variation of the delay with change in V_{DD}.
From theory,

$$Period \propto \frac{V_{DD}}{(V_{DD} - V_t)^2}$$

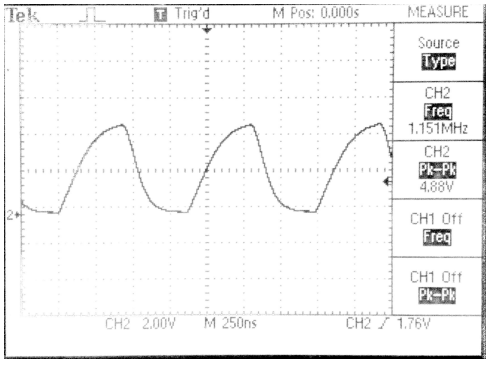
In this exercise, I will demonstrate the same relation, from experimental observations.



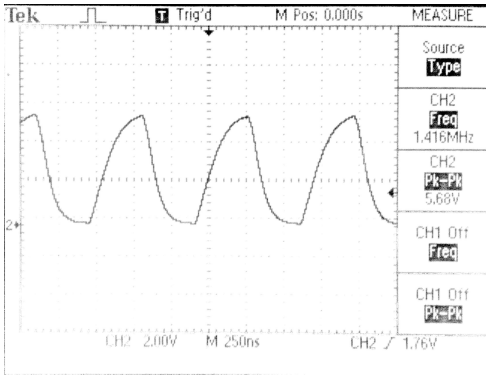
$V_{DD} = 3$



$V_{DD} = 4$



$V_{DD} = 5$



$V_{DD} = 6$

Table 6: Snapshots of the output waveform at different supply voltages *(Load = 2)*

Supply Voltage (V_{DD})	**Frequency (MHz)**
3	0.3922
4	0.7868
5	1.151
6	1.416

Table 7: Variation of the frequency of oscillation with V_{DD}. *(Load = 2)*

The reduction of the frequency with the increase in supply voltage is evident from the above snapshots, as suggested by the relation. This can be better represented as below. From the proportionality relation above, we expect the period of oscillation to go down inversely with the supply voltage. Figure 7 is in agreement with the formula, and hence the dependence can be verified.

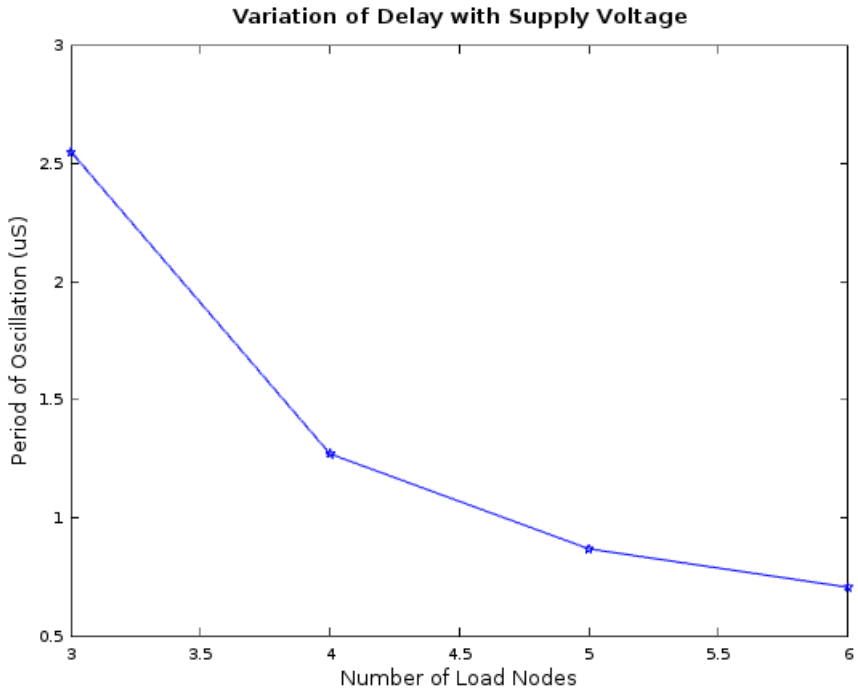


Figure 7

2.5 Current drawn by the Ring Oscillator

Whenever an inverter output *switches* from low to high, current is drawn from the power supply. The current drawn is approximately a triangular pulse whose width is essentially the delay of the gate. The current drawn by the ring oscillator is essentially the sum of the currents drawn by the individual inverters. [2]

Measured Values: $\langle I \rangle = -4.33mV$ $I_{P-P} = 22.4mV$

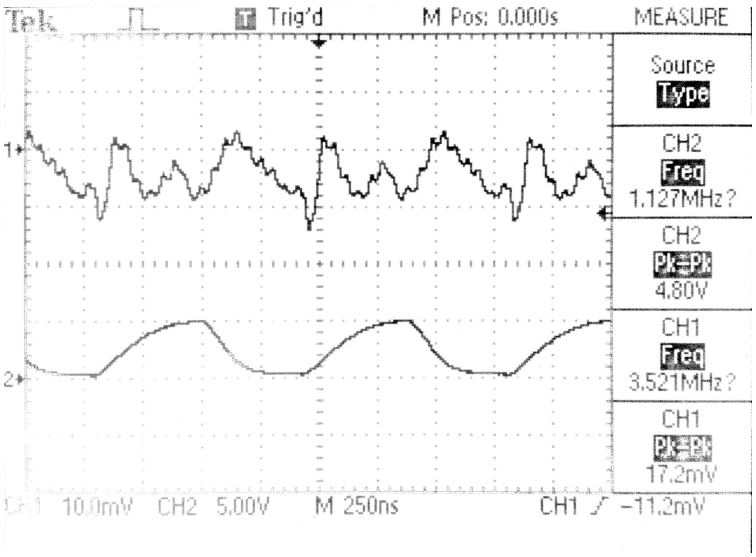


Figure 8: Snapshot of the DSO, measuring the switching current alongside V_{out}

[2]Note that, however, the switching events do not all happen at once. The signals do add, though.