

Using Quartus II and UrJTAG for Krypton

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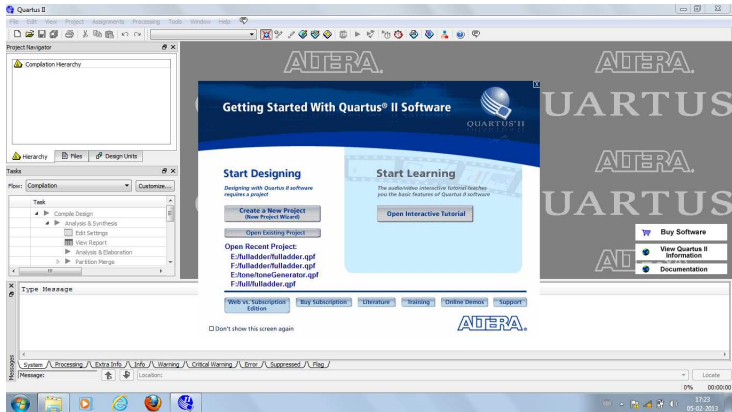
Department of Electrical Engineering
IIT Bombay
February 5, 2013

The usual process to implement a design on a programmable logic device (PLD) is as follows.

- Writing the VHDL/Verilog description of the required design logic.
- **Analysis and Elaboration**- This process checks for syntax and logical errors (analysis) and translates the HDL description into an equivalent logic circuit (elaboration).
- **Place and Route (P & R)**- In this process, the input/output lines of the required logic design is mapped to the pins of the PLD for physical implementation e.g. for a 2-input AND gate, 3 pins of the PLD are required (2 inputs and 1 output).
- Generating the programming file and transferring it to the PLD.

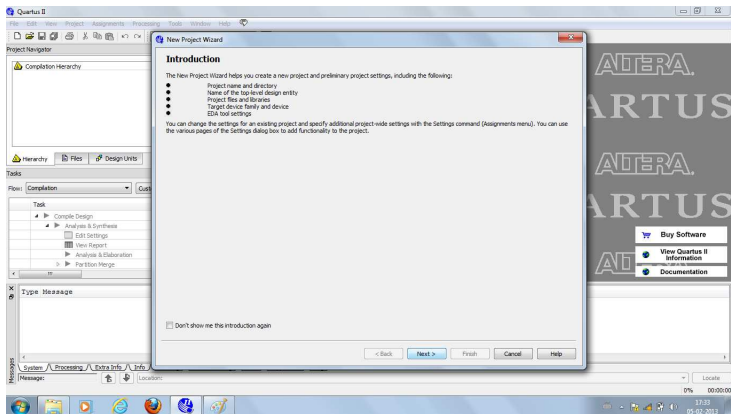
Using Quartus II

Quartus II is the Integrated Development Environment (IDE) provided by Altera Corp. to develop a digital circuit design using HDL to implement on a CPLD/FPGA. First, ensure that you have Quartus II (v11.0 or later) installed on your PC. Now, open Quartus II, and click on Create a New Project.



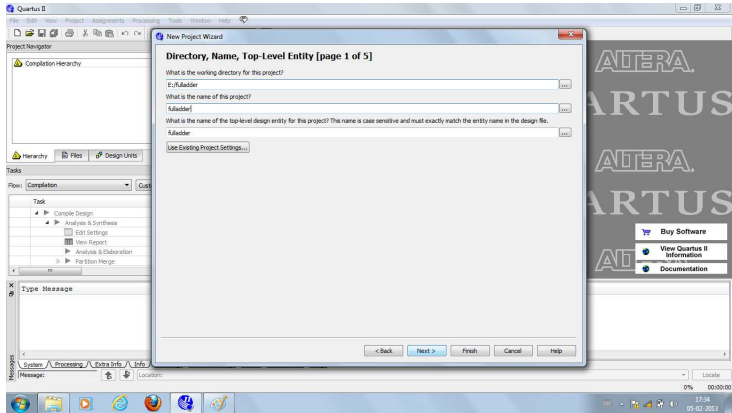
Using Quartus II- New Project

In the introductory page, click Next.



Using Quartus II- Project Directory and Top-level Module

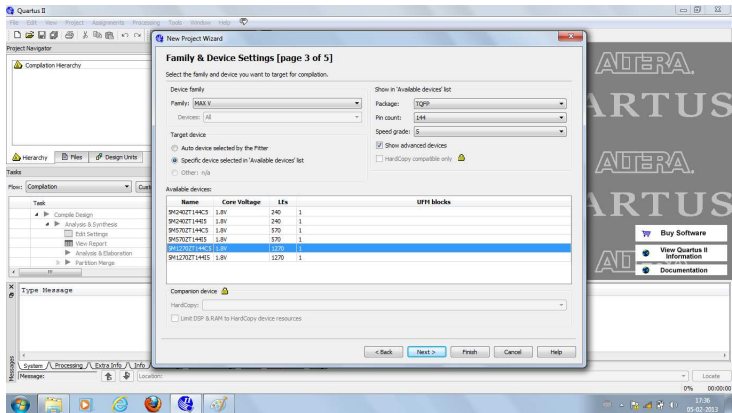
In Page 1, specify a working directory for your project. It is a good practice to open a new folder for every new project.



Note that it is helpful to keep the project name same as the top level module- by default, upon giving a project name (2nd field), the module gets the same name (3rd field).

Using Quartus II

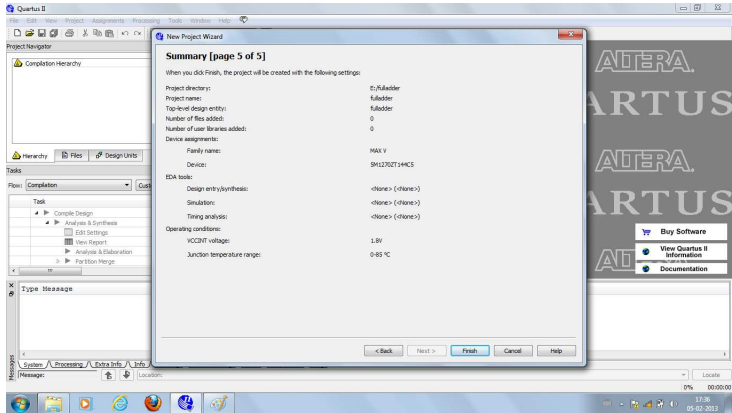
Page 2 may be skipped. In Page 3, select the target CPLD. Use the 4 drop-down lists in this window (device family- **MAX V**, package- **TQFP**, pin count- **144**, speed grade- **5**).



The final device to be selected from the device list is **5M1270ZT144C5**.

Using Quartus II

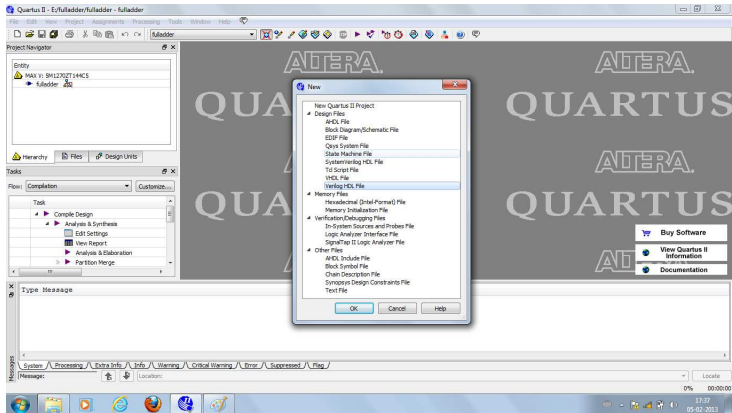
Page 4 may be skipped. Page 5 shows you a project summary- the project name, top level module, selected device etc. If there are mistakes, you can go back and change them.



If you're satisfied, click **Finish**.

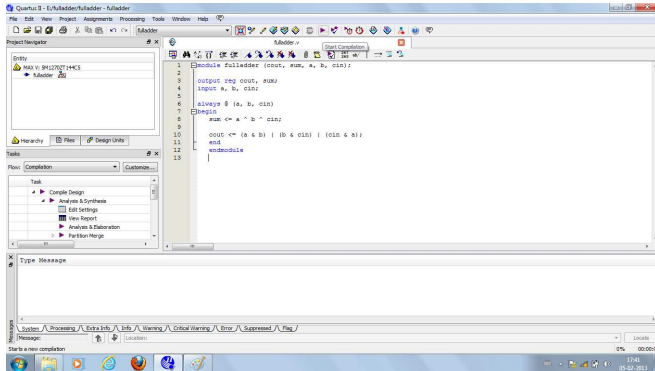
Using Quartus II

Now go to **File** → **New**. Select the kind of HDL code you wish to write—in this case, Verilog HDL.



Using Quartus II

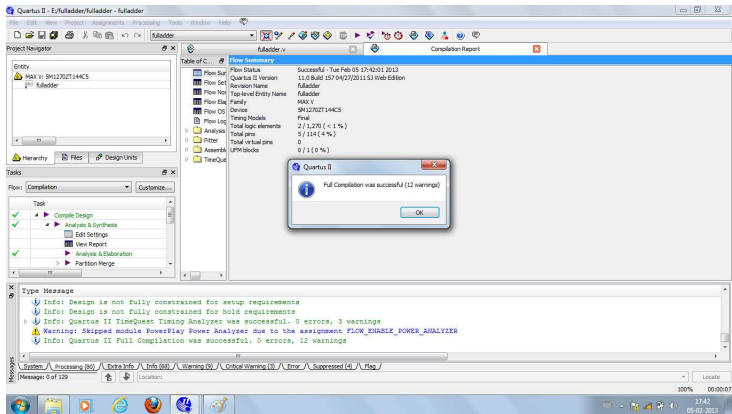
A blank text window opens up. Write your Verilog HDL description. This example shows a full adder- with three inputs and two outputs. Observe that the module name and the project name are same, i.e. fulladder.



Once done, save the file with a .v extension and click on Start Compilation. Shortcut- Ctrl+L or else go to Processing → Start Compilation.

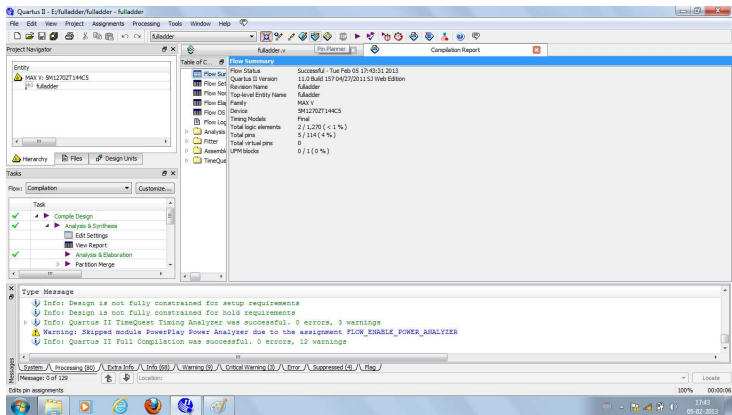
Using Quartus II

The compilation report will show errors, if any. Go back to the Verilog file and edit it in case of any errors. Warnings may be ignored as of now 😊



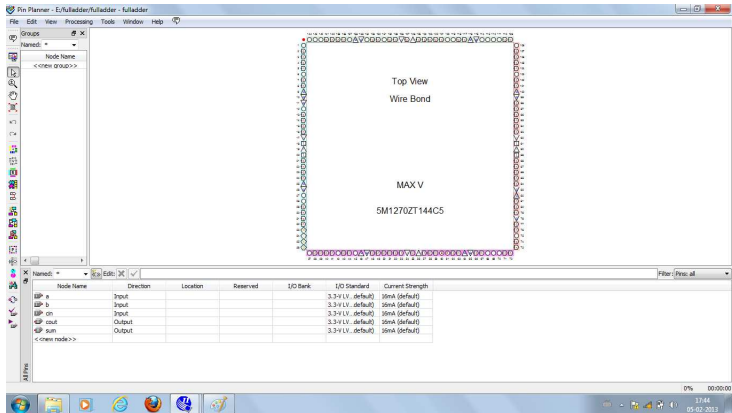
Using Quartus II

Now, click on Pin Planner. Or else, go to Assignments → Pin Planner.



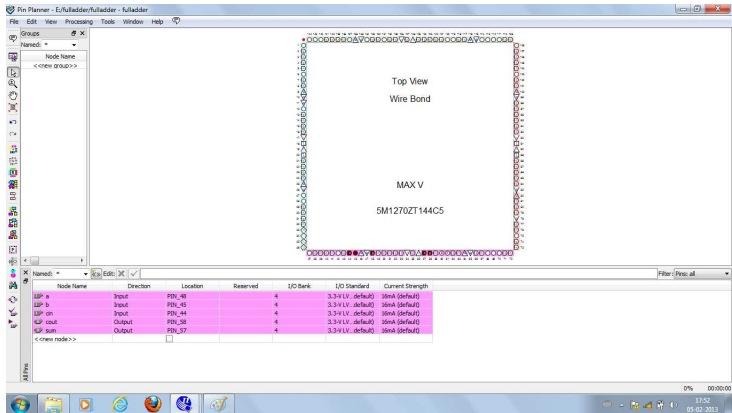
Using Quartus II

A new window opens up, showing a top view of the target CPLD and below it, the input/output lines in the design.



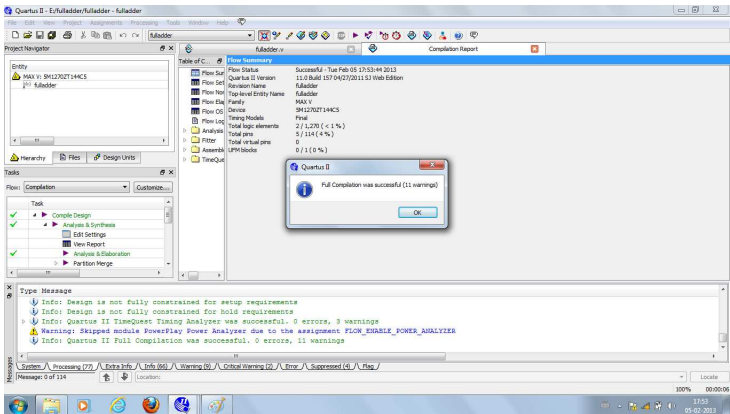
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Refer the Krypton user manual provided, to map the inputs to the on-board switches; and outputs to the on-board LEDs. Provide the pin numbers in the Location column. The completed Pin Planner is as shown.



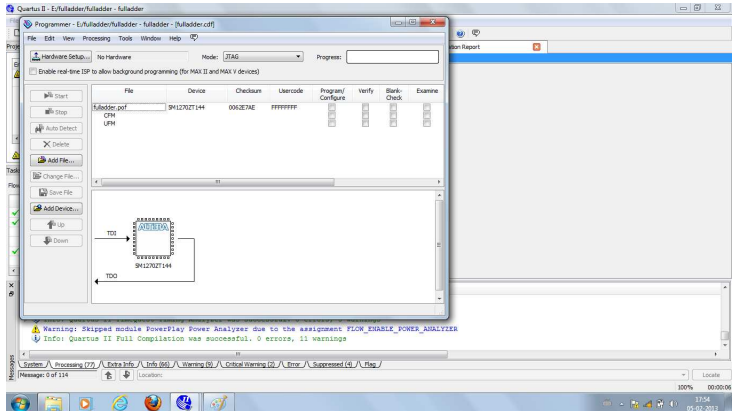
Using Quartus II

Once the pin assignments are done, recompile the project (again, Start Compilation).



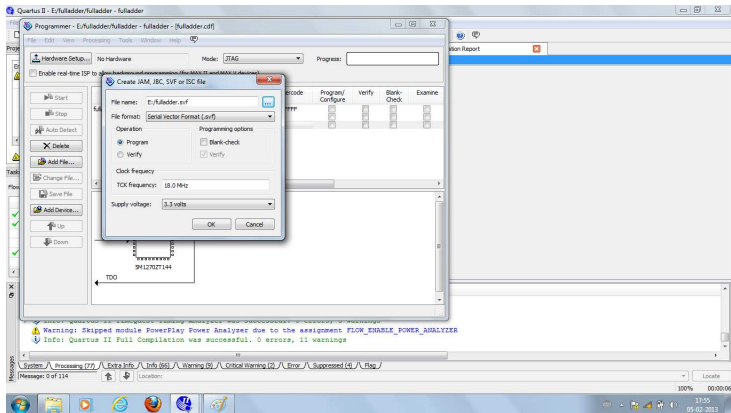
Using Quartus II

Now, go to Tools → Programmer. A new programmer window opens up, and you should be able to see your project output file `fulladder.pof` in this window. If not, you're in trouble and will need to remake the entire project again 😞!!



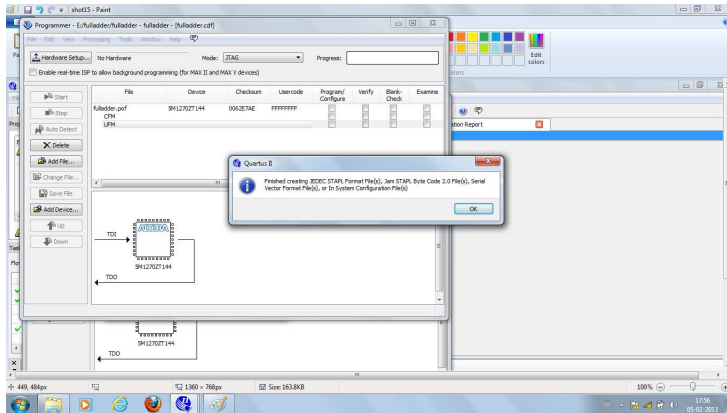
Using Quartus II

In the Programmer window, go to File → Create JAM, JBC, SVF or ISC file. In the new window, select the output file format as Serial Vector Format (SVF). Preferably, save the SVF file directly in a drive (C:, D: etc.). There is no need to change other parameters like TCK frequency, Supply voltage etc.



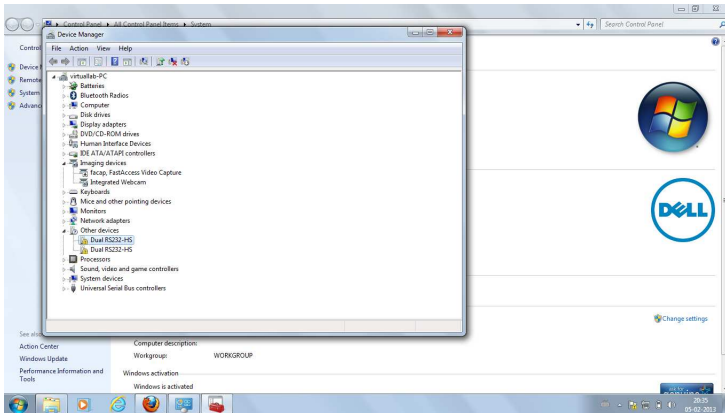
Using Quartus II

Click on OK. The SVF file is now created, and saved in the folder specified in the above step. And ***drumbeats*** you're done!! You are now ready to transfer the SVF file to the CPLD.



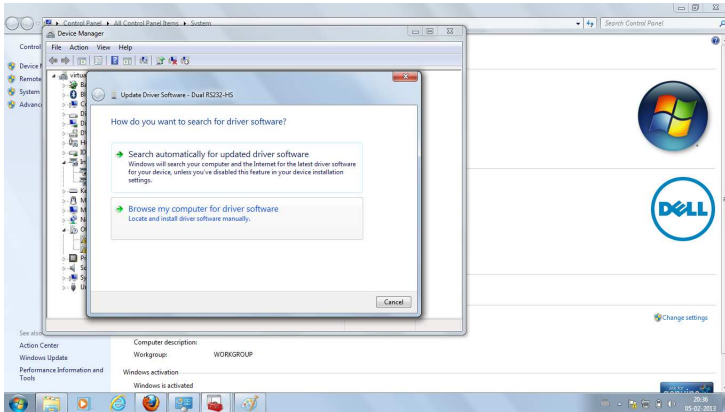
Getting Krypton Working with your PC

Plug in the Krypton board on a USB port in your PC. In Windows 7 and later, the drivers will NOT be auto-installed. Make sure you have downloaded the `krypton_files` folder containing the CMD20812 drivers and UrJTAG folder. Now, open Device Manager. The 2 uninstalled devices will be shown as Dual RS232-HS.



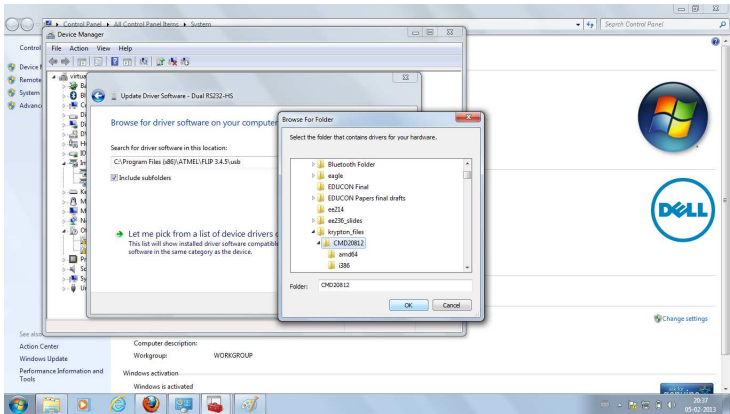
Getting Krypton Working with your PC

Right click on one of the devices Dual RS232-HS and click on 'Update Driver'. Select Browse my computer for driver software.



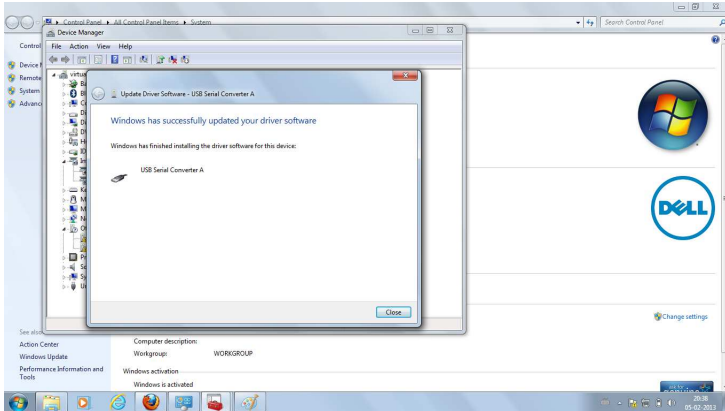
Getting Krypton Working with your PC

Now, browse to the downloaded `krypton_files` folder and select the `CMD20812` driver folder and proceed.



Getting Krypton Working with your PC

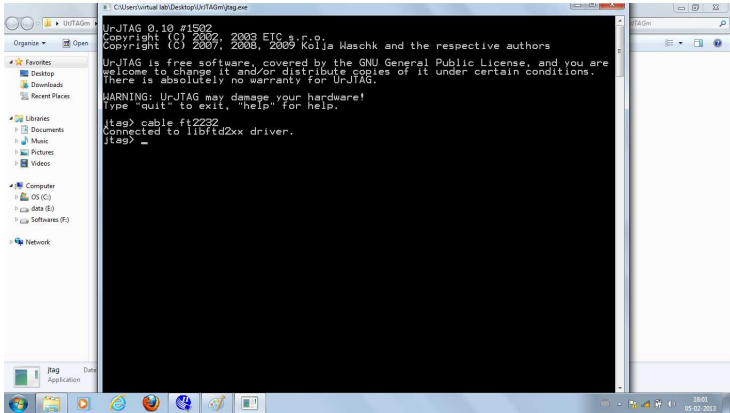
The driver for Krypton will now be installed and you should see a message like this.



And for the Dual RS232-HS, just repeat the process! You are now ready to use Krypton.

Using UrJTAG

Open the UrJTAG folder in your PC, and double click on the `jtag.exe` inside. A command window with a `jtag>` prompt opens up. Type the command `cable ft2232` and hit enter.



```
UrJTAG 0.10 #1502
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Copyright (C) 2007, 2008, 2009 Kolja Waschk and the respective authors

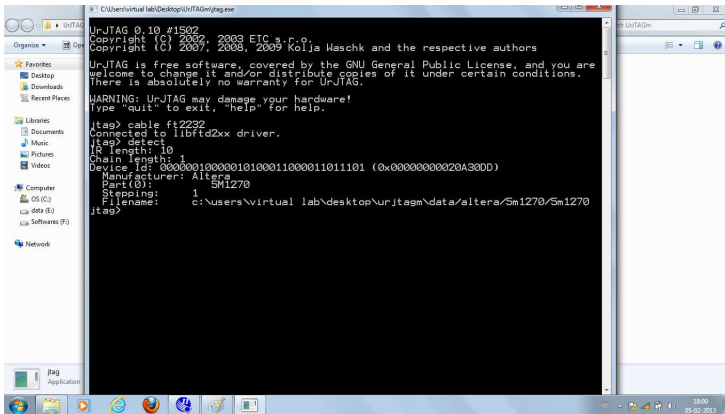
UrJTAG is free software, covered by the GNU General Public License, and you are
welcome to change it and/or distribute copies of it under certain conditions.
There is absolutely no warranty for UrJTAG.

WARNING: UrJTAG may damage your hardware!
Type "quit" to exit, "help" for help.

jtag> cable ft2232
Connected to libftd2xx driver.
jtag> _
```

Using UrJTAG

Now type the command detect, and hit enter. The target CPLD details will be shown.



```
UrJTAG 0.10 #1502
Copyright (C) 2002, 2003 ETC a.r.o.
Copyright (C) 2007, 2008, 2009 Kolja Waschk and the respective authors

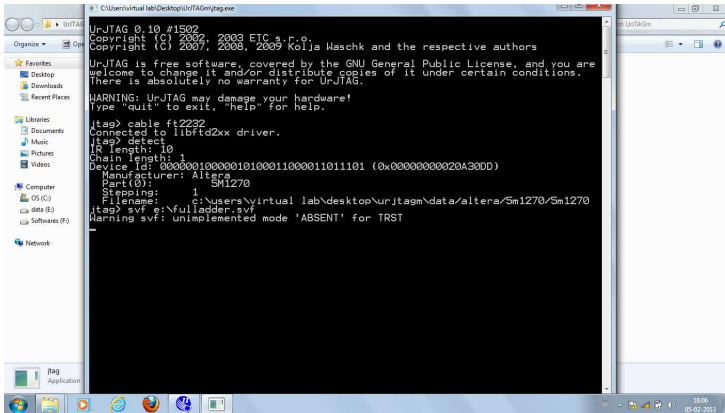
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welcome to change it and/or distribute copies of it under certain conditions.
There is absolutely no warranty for UrJTAG.

WARNING: UrJTAG may damage your hardware!
Type "quit" to exit, "help" for help.

jtag> cable ft2232
Connected to libftd2xx driver.
jtag> detect
IR length: 10
Chain length: 1
Device id: 00000010000010100011000011011101 (0x0000000020A300D)
Manufacturer: Altera
Part(0): SM1270
Stepping: 1
Filename: c:\users\virtual lab\desktop\urjtagm\data\altera\Sm1270\Sm1270
jtag>
```

Using UrJTAG

Finally, give the command to transfer the SVF file from your PC to the CPLD. The command is `svf` followed by the pathname to the file. When you hit enter, the `jtag>` prompt will disappear for about 50 seconds (while the CPLD is being programmed). Once the prompt comes back, you should be able to test your design on the board. Voila!



The screenshot shows the UrJTAG application window. The title bar reads "C:\Users\virtual lab\Desktop\UrJTAGm\jtag.exe". The main window contains a text area with the following text:

```
UrJTAG 0.10 #1502
Copyright (C) 2002, 2003 ETC s.r.o.
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UrJTAG is free software, covered by the GNU General Public License, and you are
welcome to change it and/or distribute copies of it under certain conditions.
There is absolutely no warranty for UrJTAG.

WARNING: UrJTAG may damage your hardware!
Type "quit" to exit, "help" for help.

jtag> cable ft232
Connected to libftd2xx driver.
jtag> detect
IR length: 10
Chain length: 1
Device id: 00000010000010100011000011011101 (0x0000000020A30DD)
Manufacturer: Altera
Part(0): 1 SM1270
Stepping:
Filename: c:\users\virtual lab\Desktop\urjtagm\data\altera\sm1270\sm1270
jtag> svf e:\fulladder.svf
Warning svf: unimplemented mode 'ABSENT' for TRST
```

The left sidebar of the application shows a file explorer view with "Favorites" (Desktop, Downloads, Recent Places), "Libraries" (Documents, Music, Pictures, Videos), "Computer" (OS (C:), data (E:), Softwares (F:)), and "Network". The taskbar at the bottom shows the Windows Start button, several application icons, and the system clock displaying 18:06 on 05-02-2013.

Keep in mind that...

- the Page 2 in Quartus II is for including pre-existing Verilog files as part of your design. If you wish to include, feel free to do so! And Page 4 is to include any simulator (such as ModelSIM) if you wish to simulate your design before implementing.
- the driver installation needs to be done the first time you connect Krypton to your PC. However, exceptions have been known to occur in different Windows versions and distributions!
- the driver installation process will vary slightly for different versions of Windows. You are expected to have good working computer knowledge to know the difference!
- the cable `ft2232` and `detect` commands must be executed every time (a) you open a new UrJTAG command window and (b) you connect Krypton to your PC and power it on.
- the supply voltage on Krypton is $V_{DD} = 3.3V$. You should handle external input voltages to the board safely.

- **Quartus II**- Just google it and download the free web edition from Altera's website. Keep in mind that you need to have about 5-6GB of free space in your PC. Or use the DVD given by WEL Lab.
- **UrJTAG and CMD20812**- Download the `krypton_files` folder from the link/DVD given by WEL Lab **ONLY!**
- **User Manual**- Make sure you read this document in order to know the pin mapping and board usage details which will help you in further experiments.

Happy Learning by Doing!!