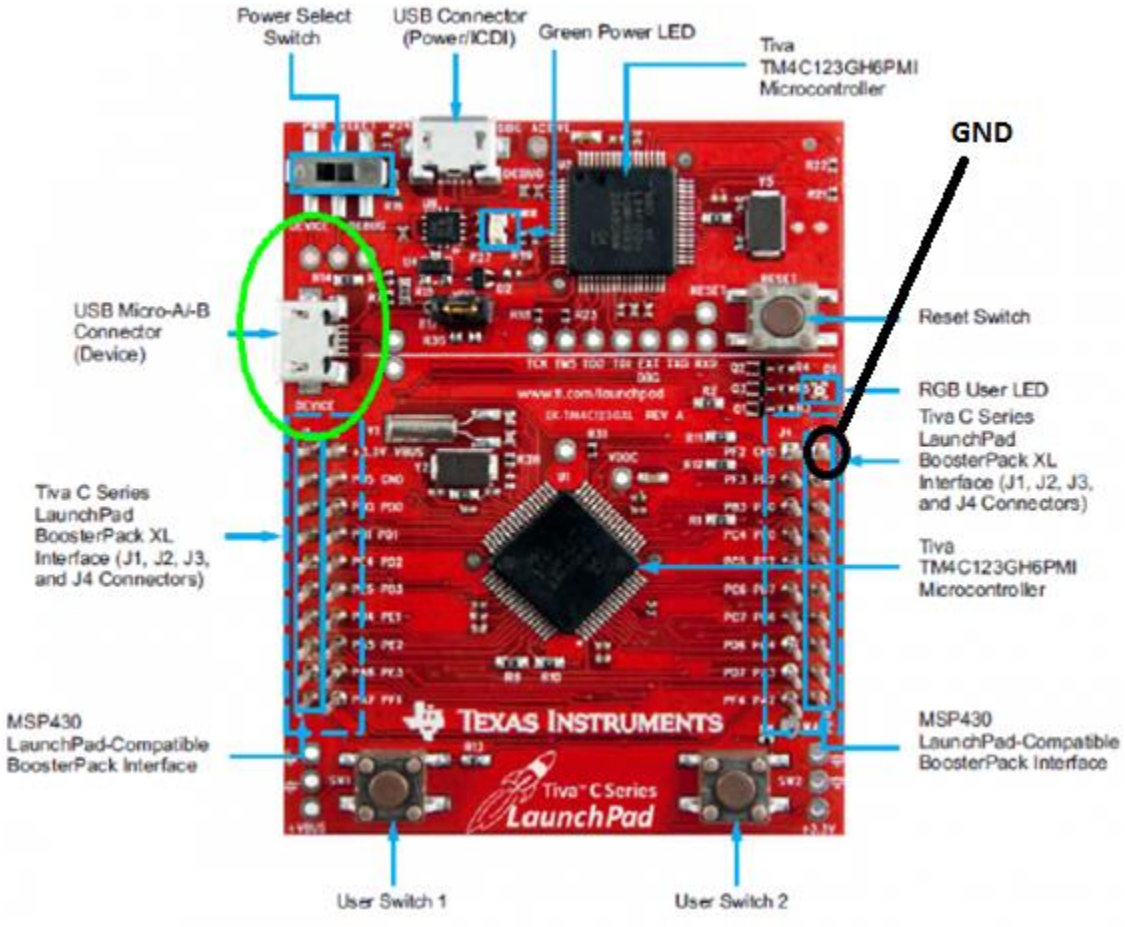
Probable Mistakes Committed while doing Scan-Chain based Testing

- Scan chain and DUT (Design under Test) are to be wrapped inside a top level entity called Top_Level. Make sure that this wrapping is done correctly.
- Tiva-C board has pins on both sides of its board in a two column structure. The names of the pins are written on its inner side as shown below. Make sure that you are connecting to the correct ground terminal (as shown below in a black circle) and not pin PF2.



- When you are doing pin-planning in Quartus by clicking on 'Start I/O O/P analysis', Quartus compiles the code. Make sure you do Full Compilation once again and then only generate the svf file.
- Scan chain testing sometimes will show you some failures and some successes. When this happens, crosscheck whether you are getting a 'success' for non-zero outputs because if there is some issue (in hardware connections or svf that you generated) then default output will be zero. So, in this case, those successes can be misleading!
- Some students programmed scan-chain code on the Krypton board without including the design (DUT) itself. Don't make this stupid mistake.