# EE214: Assignment for January 19-20, 2017

January 16, 2017

Instructions to download and install **ghdl** are given in Chapter 5 of the laboratory manual. The **ghdl** simulator is installed in the WEL lab computers, as well as in the PC lab.

## 1 Use ghdl to simulate the TwoBitAdder using the generic testbench

On the moodle webpage, we have uploaded a generic test-bench which can be used to verify the two-bit adder which was discussed in the lecture last week.

Using ghdl, simulate the generic test-bench instantiating the two-bit adder. Show the waveforms in the TwoBitAdder instance from 0 ns to 100 ns.

## 2 Use ghdl to simulate the TwoBitAdder using the generic testbench

Implement a two-bit subtractor in a manner similar to the two-bit adder. The inputs to the subtractor are bits x1,x0 (representing the integer $x$) and bits y1,y0 (representing the integer $y$). The outputs of the subtractor are bits b1,b0 (representing the integer $b$). We have $b = (a - b) \bmod 2$.

First derive formulas for b1,b0 in terms of x1,x0,y1,y0. Describe the TwoBitSubtractor in VHDL. Customize the generic test-bench and use it to verify your design with the following trace:

```
x1x0y1y0  b1b0
```

```
0000        00
0001        11
0010        10
0011        01
0100        01
0101        00
0110        11
0111        10
1000        10
1001        01
1010        00
1011        11
1100        11
1101        10
1110        01
1111        00
```

# 3 Submission

Together with your report, submit the VHDL files of the TwoBitSubtractor, the customized generic testbench (with the DUT entity), the waveforms from your simulation, and the output file generated by your simulation.