 

# 2024

*Time : 3 hours*

*Full Marks : 70*

*Candidates are required to give their answers in their own words as far as practicable.*

*The figures in the margin indicate full marks.*

*Answer from **all** the Parts as directed.*

## Part – A

## (Objective Type Questions)

## (Compulsory)

1. Choose the correct answer of the following : 1×5 = 5

(a) Demultiplexer is also known as :

(i) MUX

(ii) DEMUX

(iii) D / A converter

(iv) None of these

(b) ISA stands for :

(i) Industry Standard Architecturastion

(ii) Industry Standard Architecture

(iii) Industry Standard Architect

(iv) None of these

(c) Which is Bidirectional ?

(i) Data Bus

(ii) Address Bus

(iii) Control Bus

(iv) None of these

(d) How many state of Flags ?

(i) 2

(ii) 3

(iii) 4

(iv) 5

(e) How many pair of Register in Computer org ?

(i) 3

(ii) 4

(iii) 2

(iv) None of these



2. Fill in the blanks with appropriate answer : 1×5 = 5

(a) In 8086 Microprocessor, Address Bus is _____.

(b) MBR stands for _____.

(c) GPR stands for _____.

(d) PIC stands for _____.

(e) Multiplexer denoted as _____.

## Part – B

## (Short-answer Type Questions)

3. Answer any **four** questions of the following : 5×4 = 20

(a) Explain the Demultiplexer.

(b) What is Instruction cycle ?

(c) Explain the timing and control in CSA.

(d) What is Interrupt ?

(e) Explain the System Bus.

(f) Explain any **two** of the following :

(i) Shift Register

(ii) Cache Memory

(iii) DX and SX up

(iv) Parallel port

## Part – C

## (Long-answer Type Questions)

4. Answer any **four** questions of the following : 10×4 = 40

(a) What is Register Organisation ? Explain the type of Register in Registration Organisation.

(b) What is Mapping ? Explain the types of Mapping.

(c) Differentiate between Encoder and Decoder with diagram.

(d) Differentiate between 80386 DX and 80386 SX Microprocessor.

(e) Explain the Real mode and Protected mode.

(f) Explain the Bus interconnection design of the basic computer.

(g) Explain the following :

(i) Instruction set

(ii) Associative memory

(iii) Ports

(iv) Logic microoperation