

BQ2404x 1A, Single-Input, Single Cell Li-Ion and Li-Pol Battery Charger With Auto Start

1 Features

- Charging
 - 1% Charge voltage accuracy
 - 10% Charge current accuracy
 - Pin selectable USB 100 mA and 500 mA maximum input current limit
 - Programmable termination and precharge threshold, BQ24040 and BQ24045
 - High voltage (4.35 V) chemistry support with BQ24045
- Protection
 - 30V Input rating; with 6.6 V or 7.1 V input overvoltage protection
 - Input voltage dynamic power management
 - 125°C thermal regulation; 150°C thermal shutdown protection
 - OUT Short-circuit protection and ISET short detection
 - Operation over JEITA range via battery NTC -1/2 fast-charge-current at Cold, 4.06V at Hot, BQ24040 and BQ24045
 - Fixed 10 hour safety timer, BQ24040 and BQ24045

System

- Automatic termination and timer disable mode (TTDM) for absent battery pack with thermistor, BQ24040 and BQ24045
- Status indication charging and done
- Available in small 2 × 2 mm² DFN-10 package
- Integrated auto start function for production line testing, BQ24041
- Functional Safety-Capable (BQ24040)
 - Documentation available to aid functional safety system design
- Safety-Related Certifications:
 - IEC 62368-1 CB Certification (BQ24040, BQ24045)

2 Applications

- TWS Headsets and headphones
- Smartwatches and wristbands
- Wireless speakers
- Mobile POS
- Portable medical devices

3 Description

The BQ2404x series of devices are highly integrated Li-Ion and Li-Pol linear chargers devices targeted at space-limited portable applications. The devices operate from either a USB port or AC adapter. The high input voltage range with input overvoltage protection supports low-cost unregulated adapters.

The BQ2404x has a single power output that charges the battery. A system load can be placed in parallel with the battery as long as the average system load does not keep the battery from charging fully during the 10 hour safety timer.

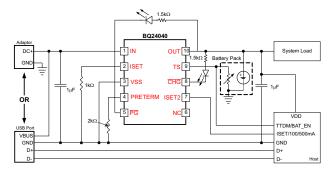
The battery is charged in three phases: conditioning, constant current and constant voltage. In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if an internal temperature threshold is exceeded.

The charger power stage and charge current sense functions are fully integrated. The charger function has high accuracy current and voltage regulation loops, charge status display, and charge termination. The pre-charge current and termination current threshold are programmed through an external resistor on the BQ24040 and BQ24045. The fast charge current value is also programmable through an external resistor.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
BQ24040		
BQ24041	WSON (10)	2.00 mm x 2.00 mm
BQ24045		

For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic



Table of Contents

1 Features1	8.4 Device Functional Modes17
2 Applications1	9 Application and Implementation22
3 Description1	9.1 Application Information22
4 Revision History2	9.2 Typical Applications22
5 Device Comparison4	10 Power Supply Recommendations29
6 Pin Configuration and Functions4	11 Layout30
7 Specifications6	11.1 Layout Guidelines30
7.1 Absolute Maximum Ratings6	11.2 Layout Example30
7.2 ESD Ratings	11.3 Thermal Considerations31
7.3 Recommended Operating Conditions6	12 Device and Documentation Support32
7.4 Thermal Information7	12.1 Device Support32
7.5 Electrical Characteristics7	12.2 Documentation Support32
7.6 Timing Requirements10	12.3 Receiving Notification of Documentation Updates32
7.7 Typical Operational Characteristics (Protection	12.4 Support Resources32
Circuits Waveforms)11	12.5 Trademarks32
8 Detailed Description12	12.6 Electrostatic Discharge Caution32
8.1 Overview	12.7 Glossary32
8.2 Functional Block Diagram13	13 Mechanical, Packaging, and Orderable
8.3 Feature Description14	Information32
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (June 2020) to Revision H (February 2	2021) Page
Added BQ24040, BQ24045 to IEC 62368-1 CB Certification Feature	ture1
Changed I _{BD-SINK} minimum from 7 mA to 6 mA	7
Changed I _{IH} maximum from 8 μA to 9.5 μA	7
Changes from Revision F (March 2015) to Revision G (June 202	20) Page
Added Functional Safety-Capable Feature	1
Added IEC 62368-1 Feature	
Changed Applications	
Deleted Disconnect after Detection from Simplified Schematic	1
Changed thermal pad description	4
Added I _{OUT(SC)} test condition	7
Changed Figure 7-5	
Changed the Section 8.3.4 section	
Added (BQ24040) to Figure 8-4 and Figure 8-5	18
Deleted Disconnect after Detection from Figure 9-1	
Added link to BQ24040 Application Report	23
Deleted Disconnect after Detection from Figure 9-20	27
Moved Section 11.3 to Layout section	
Changes from Revision E (February 2014) to Revision F (March	2015) Page
Changed the Device Information table header information, and re-	· · · · · · · · · · · · · · · · · · ·

device number1 Changed the Handling Ratings table To: Section 7.2 and updated the guidelines......6



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•	Added the package family to the column heading in the Section 7.4	
_		
	hanges from Revision D (March 2013) to Revision E (February 2014) Added Handling Ratings table, Feature Description section, Device Functional Modes section, App	Page
	and Implementation section, Power Supply Recommendations section, Layout section, Device and	ication
	Documentation Support section, and Mechanical, Packaging, and Orderable Information section	1
•	Changed the Dissipation Rating table to the Section 7.4	<mark>7</mark>
•	Changed V _{O_HT(REG)} in the Electrical Characteristics table to include new values BQ24045	<mark>7</mark>
•	Added the Timing Requirements table	
•	Deleted the last sentence in the first paragraph of the TS (BQ24040/5) section	19
•	Added the Section 9.2.1.3	24
C	hanges from Revision C (February 2013) to Revision D (March 2013)	Page
•	Changed Feature From: Fixed 10 Hour Safety Timer To: Fixed 10 Hour Safety Timer, BQ24040 and	
•	Changed the OUT terminal <i>DESCRIPTION</i>	
•	Changed R _{ISET} NOM value in the ROC table From: 49.9 kΩ To: 10.8 kΩ	<mark>6</mark>
•	Changed R _{ISET SHORT} test conditions From: R_{ISET} : $600\Omega \rightarrow 250\Omega$ To: R_{ISET} : $540\Omega \rightarrow 250\Omega$	<mark>7</mark>
•	Changed I _{OUT} $\stackrel{-}{\text{CL}}$ test conditions From: R _{ISET} : $600\Omega \rightarrow 250\Omega$ To: R _{ISET} : $540\Omega \rightarrow 250\Omega$	<mark>7</mark>
•	Deleted: Internally Set: BQ24041 from the TERMINATION section	<mark>7</mark>
•	Added BQ24040 and BQ24045 only to the BATTERY CHARGING TIMERS AND FAULT TIMERS s	ection10
•	Changed text in the ISET section From: "maximum current between 1.1A and 1.35A" To: "maximum between 1.05A and 1.4A"	current
	Changed the Timers section	
•	Deleted: I _{OUT TERM} = 54mA from the Typical Application Circuit: BQ24041, with ASI and ASO condi	
CI	hanges from Revision B (June 2012) to Revision C (February 2013)	Page
•	Added device BQ24045	
•	Added additional K _{ISET} information to the Electrical Characteristics table	
•	Added graph - Load Regulation	
•	Added graph - Line Regulation	
C	hanges from Revision A (September 2009) to Revision B (June 2012)	Page
•	Changed all occurrences of Li-Ion To: Li-Ion and Li-Pol	1
C	hanges from Revision * (August 2009) to Revision A (September 2009)	Page
•	Changed the status of the devices From: Product Preview To: Production Data	1



5 Device Comparison

PART NO.	V _{O(REG)}	V _{OVP}	PreTerm	ASI/ASO	TS/BAT_EN	PG	PACKAGE
BQ24040	4.20 V	6.6 V	Yes	No	TS (JEITA)	Yes	10-pin 2 × 2mm ² DFN
BQ24041	4.20 V	7.1 V	No	Yes	BAT_EN Terminaton Disabled	Yes	10-pin 2 × 2mm ² DFN
BQ24045	4.35V	6.6V	Yes	No	TS (JEITA)	Yes	10-pin 2 × 2mm ² DFN

6 Pin Configuration and Functions

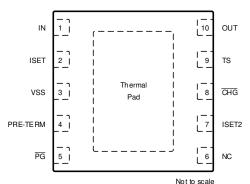


Figure 6-1. BQ24040 and BQ24045 DSQ Package 10-Pin WSON Top View

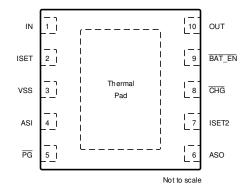


Figure 6-2. BQ24041 DSQ Package 10-Pin WSON Top View

Table 6-1. Pin Functions

	PIN				
NAME	NAME BQ24040 BQ24041		I/O	DESCRIPTION	
IN	1	1	ı	Input power, connected to external DC supply (AC adapter or USB port). Expected range of bypass capacitors 1μF to 10μF, connect from IN to V _{SS} .	
OUT	10	10	0	Battery Connection. System Load may be connected. Expected range of bypass capacitors 1μF to 10μF.	
PRE-TERM	4	-	ı	Programs the Current Termination Threshold (5 to 50% of lout which is set by ISET) and Sets the Pre-Charge Current to twice the Termination Current Level. Expected range of programming resistor is 1k to 10kΩ (2k: Ipgm/10 for term; Ipgm/5 for precharge)	
ISET	2	2	ı	Programs the Fast-charge current setting. External resistor from ISET to VSS defines fast charge current value. Range is $10.8k$ ($50mA$) to 540Ω ($1000mA$).	
ISET2	7	7	ı	Programming the Input/Output Current Limit for the USB or Adaptor source: BQ24040/5 => High = 500mAmax, Low = ISET, FLOAT = 100mAmax. BQ24041 => High = 410mAmax, Low = ISET, FLOAT = 100mAmax.	
TS	9(1)	-	I	Temperature sense terminal connected to BQ24040/5 -10k at 25°C NTC thermistor, in the battery pack. Floating T terminal or pulling High puts part in TTDM "Charger" Mode and disable TS monitoring, Timers and Termination. Pulling terminal Low disables the IC. If NTC sensing is not needed, connect this terminal to VSS through an external $10~\text{k}\Omega$ resistor. A $250\text{k}\Omega$ from TS to ground will prevent IC entering TTDM mode when battery with thermistor is removed.	
BAT_EN	-	9	ı	Charge Enable Input (active low)	
VSS	3	3	-	Ground terminal	
CHG	8	8	0	Low (FET on) indicates charging and Open Drain (FET off) indicates no Charging or Charge complete.	
PG	5	5	0	Low (FET on) indicates the input voltage is above UVLO and the OUT (battery) voltage.	

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Table 6-1. Pin Functions (continued)

	PIN				
NAME	BQ24040 BQ24045	BQ24041	I/O	DESCRIPTION	
ASI	-	4	ı	Auto start External input. Internal 200kΩ pull-down.	
ASO	-	6	0	Auto Start Logic Output	
NC	6	-	NA	Do not make a connection to this terminal (for internal use) – Do not route through this terminal	
Thermal Pad and Package	Pad 2x2mm²	Pad 2x2mm ²	ı	Connect exposed thermal pad to VSS terminal of the device and main ground plane. The thermal pad must be connected to the same potential as the VSS terminal on the printed circuit board. Do not use the thermal pad as th primary ground input for the device. VSS terminal must be connected to ground at all times.	

(1) Spins have different terminal definitions



7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Input voltage	IN (with respect to VSS)	-0.3	30	V	
	Input voltage	OUT (with respect to VSS)	-0.3	7	V
		PRE-TERM, ISET, ISET2, TS, CHG, PG, ASI, ASO (with respect to VSS)	-0.3	7	V
	Input current	IN		1.25	Α
	Output current (continuous)	OUT		1.25	Α
	Output sink current	CHG		15	mA
TJ	Junction temperature		-40	150	°C
T _{stg}	Storage temperature		-65	150	°C

⁽¹⁾ Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

7.2 ESD Ratings

			VALUE	UNIT
		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±3000	
V _(ESD)	Electrostatic discharge ⁽³⁾	Charged-device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±1500	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
- (3) The test was performed on IC terminals that may potentially be exposed to the customer at the product level. The BQ2404x IC requires a minimum of the listed capacitance, external to the IC, to pass the ESD test. The D+ D- lines require clamp diodes such as CM1213A-02SR from CMD to protect the IC for this testing.

7.3 Recommended Operating Conditions

see (1)

		MIN	NOM	UNIT
V _{IN}	IN voltage range	3.5	28	V
	IN operating voltage range, Restricted by V _{DPM} and V _{OVP}	4.45	6.45	V
I _{IN}	Input current, IN terminal		1	Α
I _{OUT}	Current, OUT terminal		1	Α
TJ	Junction temperature	0	125	°C
R _{PRE-TERM}	Programs precharge and termination current thresholds	1	10	kΩ
R _{ISET}	Fast-charge current programming resistor	0.540	10.8	kΩ
R _{TS}	10k NTC thermistor range without entering BAT_EN or TTDM	1.66	258	kΩ

(1) Operation with V_{IN} less than 4.5V or in drop-out may result in reduced performance.



7.4 Thermal Information

		BQ2404x	
	THERMAL METRIC(1)	DSQ (WSON)	UNIT
		10 PINS	_
R _{0JA}	Junction-to-ambient thermal resistance	63.5	°C/W
R _{0JC(top)}	Junction-to-case (top) thermal resistance	79.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.9	°C/W
ΨЈТ	Junction-to-top characterization parameter	7.8	°C/W
ΨЈВ	Junction-to-board characterization parameter	34.3	°C/W
R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance	7.5	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

Over junction temperature range $0^{\circ}\text{C} \le T_{\text{J}} \le 125^{\circ}\text{C}$ and recommended supply voltage (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
UVLO	Undervoltage lock-out Exit	V_{IN} : 0V \rightarrow 4V Update based on sim/char	3.15	3.3	3.45	V
V _{HYS_UVLO}	Hysteresis on V _{UVLO_RISE} falling	V_{IN} : $4V\rightarrow 0V$, $V_{UVLO_FALL} = V_{UVLO_RISE} - V_{HYS-UVLO}$	175	227	280	mV
V _{IN-DT}	Input power good detection threshold is V _{OUT} + V _{IN-DT}	(Input power good if $V_{IN} > V_{OUT} + V_{IN-DT}$); $V_{OUT} = 3.6V$, V_{IN} : $3.5V \rightarrow 4V$	30	80	145	mV
V _{HYS-INDT}	Hysteresis on V _{IN-DT} falling	V_{OUT} = 3.6V, V_{IN} : 4V \rightarrow 3.5V		31		mV
·	land the second land and a second land through and	V _{IN} : 5V → 12V (BQ24040, BQ24045)	6.5	6.65	6.8	V
V _{OVP}	Input over-voltage protection threshold	V _{IN} : 5V → 12V (BQ24041)	6.9	7.1	7.3	V
V _{HYS-OVP}	Hysteresis on OVP	V_{IN} : 11V \rightarrow 5V		95		mV
V	USB/Adaptor low input voltage protection. N-DPM Restricts lout at V _{IN-DPM}	Feature active in USB mode; Limit Input Source Current to 50mA; V_{OUT} = 3.5V; R_{ISET} = 825 Ω	4.34	4.4	4.46	V
V _{IN-DPM}		Feature active in Adaptor mode; Limit Input Source Current to 50mA; V _{OUT} = 3.5V; R _{ISET} = 825	4.24	4.3	4.46	V
	USB input I-Limit 100mA	ISET2 = Float; R_{ISET} = 825Ω	85	92	100	
I _{IN-USB-CL}	USB input I-Limit 500mA, BQ24040, BQ24045	ISET2 = High; R_{ISET} = 825 Ω	430	462	500	mA
	USB input I-Limit 380mA, BQ24041	ISET2 = High; R_{ISET} = 825 Ω	350	386	420	
ISET SHORT O	CIRCUIT TEST					
R _{ISET_SHORT}	Highest Resistor value considered a fault (short). Monitored for lout>90mA	$R_{\text{ISET}}\!\!: 540\Omega \to 250\Omega,$ lout latches off. Cycle power to Reset.	280		500	Ω
I _{OUT_CL}	Maximum OUT current limit Regulation (Clamp)	V_{IN} = 5V, V_{OUT} = 3.6V, V_{ISET2} = Low, R_{ISET} : 540 Ω \rightarrow 250 Ω , I_{OUT} latches off after $t_{\text{DGL-SHORT}}$	1.05		1.4	А
BATTERY SHO	ORT PROTECTION					
V _{OUT(SC)}	OUT terminal short-circuit detection threshold/ precharge threshold	V_{OUT} : 3V \rightarrow 0.5V, no deglitch	0.75	0.8	0.85	V
V _{OUT(SC-HYS)}	OUT terminal Short hysteresis	Recovery ≥ V _{OUT(SC)} + V _{OUT(SC-HYS)} ; Rising, no Deglitch		77		mV
I _{OUT(SC)}	Source current to OUT terminal during short-circuit detection	V _{OUT} < 0.8 V	10	15	20	mA
QUIESCENT C	URRENT					
I _{OUT(PDWN)}	DUT(PDWN) Battery current into OUT terminal V _{IN} = 0V				1	
I _{OUT(DONE)}	OUT terminal current, charging terminated	V _{IN} = 6V, V _{OUT} > V _{OUT(REG)}			6	μA
I _{IN(STDBY)}	Standby current into IN terminal	TS = LO, V _{IN} ≤ 6V			125	μA
I _{CC}	Active supply current, IN terminal	TS = open, V _{IN} = 6V, TTDM – no load on OUT terminal, V _{OUT} > V _{OUT(REG)} , IC enabled		0.8	1	mA



7.5 Electrical Characteristics (continued)

Over junction temperature range $0^{\circ}C \le T_{J} \le 125^{\circ}C$ and recommended supply voltage (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
BATTERY CHA	ARGER FAST-CHARGE					
V	Detter very letion velters	V_{IN} = 5.5V, I_{OUT} = 25mA, $(V_{TS-45^{\circ}C} \le V_{TS} \le V_{TS-0^{\circ}C}, BQ24040)$	4.16	4.2	4.23	V
V _{OUT(REG)}	Battery regulation voltage	$V_{IN} = 5.5V$, $I_{OUT} = 25mA$, $(V_{TS-45^{\circ}C} \le V_{TS} \le V_{TS-0^{\circ}C}$, BQ24045)	4.30	4.35	4.40	V
V _{O HT(REG)}	Battery hot regulation voltage	$V_{IN} = 5.5V$, $I_{OUT} = 25\text{mA}$, $(V_{TS.45^{\circ}C} \le V_{TS} \le V_{TS.0^{\circ}C}$, BQ24040)	4.02	4.06	4.1	V
*O_HI(REG)	Suiter, net regulation reliage	$V_{IN} = 5.5V$, $I_{OUT} = 25mA$, $(V_{TS.45^{\circ}C} \le V_{TS} \le V_{TS.0^{\circ}C}$, BQ24045)	4.16	4.2	4.23	•
I _{OUT(RANGE)}	Programmed Output "fast charge" current range	$V_{OUT(REG)}$ > V_{OUT} > V_{LOWV} ; V_{IN} = 5V, ISET2 = LO, R_{ISET} = 540 to 10.8k Ω	10		1000	mA
V _{DO(IN-OUT)}	Drop-Out, VIN – VOUT	Adjust VIN down until I_{OUT} = 0.5A, V_{OUT} = 4.15V, R_{ISET} = 540 , ISET2 = Lo (adaptor mode); $T_J \le 100^{\circ}C$		325	500	mV
I _{OUT}	Output "fast charge" formula	$V_{OUT(REG)} > V_{OUT} > V_{LOWV}$; $V_{IN} = 5V$, ISET2 = Lo		K _{ISET} /R _{ISET}		Α
		$R_{ISET} = K_{ISET} / I_{OUT}$; 50 < I_{OUT} < 1000 mA	510	540	570	
K _{ISET}	Fast charge current factor	$R_{ISET} = K_{ISET} / I_{OUT}$; 25 < I_{OUT} < 50 mA	480	527	600	ΑΩ
		R _{ISET} = K _{ISET} /I _{OUT} ; 10 < I _{OUT} < 25 mA	350	520	680	
		R _{ISET} = K _{ISET} /I _{OUT} ; 50 < I _{OUT} < 1000 mA	510	560	585	
K _{ISET}	Fast charge current factor (BQ24045)	R _{ISET} = K _{ISET} /I _{OUT} ; 25 < I _{OUT} < 50 mA	480	557	596	ΑΩ
		R _{ISET} = K _{ISET} /I _{OUT} ; 10 < I _{OUT} < 25 mA	350	555	680	
PRECHARGE	- SET BY PRETERM terminal: BQ24040 / BQ24	1045; Internally Set: BQ24041				
V _{LOWV}	Pre-charge to fast-charge transition threshold		2.4	2.5	2.6	V
I _{PRE-TERM}	See the Termination Section					
%PRECHG	Pre-charge current, default setting	V _{OUT} < V _{LOWV} ; R _{ISET} = 1080Ω; BQ24040: R _{PRE-TERM} = High Z ; BQ24041: Internally Fixed	18	20	22	%I _{OUT-CC}
TREGIG	Pre-charge current formula	$R_{PRE-TERM} = K_{PRE-CHG} (\Omega/\%) \times \%_{PRE-CHG} (\%)$	R _P	%		
		$\begin{split} &V_{OUT} < V_{LOWV}, V_{IN} = 5V, R_{PRE-TERM} = 2k \text{ to } 10k\Omega; R_{ISET} = \\ &1080\Omega , R_{PRE-TERM} = K_{PRE-CHG} \times \%l_{FAST-CHG}, where \\ &\%l_{FAST-CHG} \text{ is } 20 \text{ to } 100\% \end{split}$	90	100	110	Ω/%
K _{PRE-CHG}	% Pre-charge Factor	$\begin{aligned} &V_{OUT} < V_{LOWV}, V_{IN} = 5V, R_{PRE-TERM} = 1k \text{ to } 2k\Omega; R_{ISET} = \\ &1080\Omega, R_{PRE-TERM} = V_{PRE-CHG} \times \%I_{FAST-CHG}, \text{where} \\ &\%I_{FAST-CHG} \text{ is } 10\% \text{ to } 20\% \end{aligned}$	84	100	117	Ω/%
TERMINATION	I - SET BY PRE-TERM terminal: BQ24040 / BQ	24045				
%TERM	Termination Threshold Current, default setting	V _{OUT} > V _{RCH} ; R _{ISET} = 1k; BQ24040 / BQ24045: R _{PRE-TERM} = High Z	9	10	11	%I _{OUT-CC}
% I ERIVI	Termination Current Threshold Formula, BQ24040 / BQ24045	$R_{PRE-TERM} = K_{TERM} (\Omega/\%) \times \%TERM (\%)$	F	R _{PRE-TERM} / K _{TERM}		
K _{TERM}	% Term Factor	$\begin{split} &V_{OUT} > V_{RCH}, V_{IN} = 5V, R_{PRE\text{-}TERM} = 2k \text{ to } 10k\Omega \text{ ; } R_{ISET} = \\ &750\Omega K_{TERM} \times \%I_{FAST\text{-}CHG}, \text{where } \%I_{FAST\text{-}CHG} \text{ is } 10 \text{ to } 50\% \end{split}$	182	200	216	Ω/%
· · IERM	, 10 doc.	$V_{OUT} > V_{RCH}$, V_{IN} = 5V, $R_{PRE-TERM}$ = 1k to 2k Ω ; R_{ISET} = 750 Ω K _{TERM} × %lset, where %lset is 5 to 10%	174	199	224	22,70
I _{PRE-TERM}	Current for programming the term. and prechg with resistor. I _{Term-Start} is the initial PRE- TERM curent.	$R_{PRE-TERM} = 2k$, $V_{OUT} = 4.15V$	71	75	81	μА
%TERM	Termination current formula			R _{TERM} / K _{TERM} %		
I _{Term-Start}	Elevated PRE-TERM current for, t _{Term-Start} , during start of charge to prevent recharge of full battery,		80	85	92	μA
RECHARGE O	OR REFRESH - BQ24040 / BQ24045					
.,	Recharge detection threshold – Normal Temp	V_{IN} = 5V, V_{TS} = 0.5V, V_{OUT} : 4.25V \rightarrow V_{RCH}	V _{O(REG)} -0.120	V _{O(REG)} -0.095	V _{O(REG)} — 0.070	V
V _{RCH}	Recharge detection threshold – Hot Temp	V_{IN} = 5V, V_{TS} = 0.2V, V_{OUT} : 4.15V \rightarrow V_{RCH}	V _{O_HT(REG)} -0.130	V _{O_HT(REG)} -0.105	V _{O_HT(REG)} -0.080	V
BATTERY DET	FECT ROUTINE - BQ24040 / BQ24045 (NOTE: I	n Hot mode V _{O(REG)} becomes V _{O_HT(REG)})				
V _{REG-BD}	VOUT Reduced regulation during battery detect	V _{IN} = 5V, V _{TS} = 0.5V, Battery Absent	V _{O(REG)} -0.450	V _{O(REG)} -0.400	V _{O(REG)} -350	V
I _{BD-SINK}	Sink current during V _{REG-BD}	•	6		10	mA
V _{BD-HI}	High battery detection threshold	V _{IN} = 5V, V _{TS} = 0.5V, Battery Absent	V _{O(REG)} -0.150	V _{O(REG)} -0.100	V _{O(REG)} -0.050	V
V _{BD-LO}	Low battery detection threshold	V _{IN} = 5V, V _{TS} = 0.5V, Battery Absent	V _{REG-BD}	V _{REG-BD} +0.1	V _{REG-BD}	V

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7.5 Electrical Characteristics (continued)

Over junction temperature range $0^{\circ}C \le T_{J} \le 125^{\circ}C$ and recommended supply voltage (unless otherwise noted)

· , · · · · · ·	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
BATTERY-PAC	K NTC MONITOR; TS Terminal: BQ24040 / BC	1 224045: 10k NTC				
I _{NTC-10k}	NTC bias current	V _{TS} = 0.3V	48	50	52	μA
I _{NTC-DIS-10k}	10k NTC bias current when Charging is disabled.	V _{TS} = 0V	27	30	34	μA
I _{NTC-FLDBK-10k}	INTC is reduced prior to entering TTDM to keep cold thermistor from entering TTDM	V _{TS} : Set to 1.525V	4	5	6.5	μА
V _{TTDM(TS)}	Termination and timer disable mode Threshold – Enter	V _{TS} : 0.5V → 1.7V; Timer Held in Reset	1550	1600	1650	mV
V _{HYS-TTDM(TS)}	Hysteresis exiting TTDM	V _{TS} : 1.7V → 0.5V; Timer Enabled		100		mV
V _{CLAMP(TS)}	TS maximum voltage clamp	V _{TS} = Open (Float)	1800	1950	2000	mV
V _{TS_I-FLDBK}	TS voltage where INTC is reduce to keep thermistor from entering TTDM	INTC adjustment (90 to 10%; 45 to 6.6uS) takes place near this spec threshold. $V_{TS} \colon 1.425V \to 1.525V$		1475		mV
C _{TS}	Optional Capacitance – ESD			0.22		μF
V _{TS-0°C}	Low temperature CHG Pending	Low Temp Charging to Pending; V_{TS} : 1V \rightarrow 1.5V	1205	1230	1255	mV
V _{HYS-0°C}	Hysteresis at 0°C	Charge pending to low temp charging; V_{TS} : 1.5V \rightarrow 1V		86		mV
V _{TS-10°C}	Low temperature, half charge	Normal charging to low temp charging; V_{TS} : 0.5V \rightarrow 1V	765	790	815	mV
V _{HYS-10°C}	Hysteresis at 10°C	Low temp charging to normal CHG; V_{TS} : 1V \rightarrow 0.5V		35		mV
V _{TS-45°C}	High temperature at 4.1V	Normal charging to high temp CHG; V_{TS} : 0.5V \rightarrow 0.2V	263	278	293	mV
V _{HYS-45°C}	Hysteresis at 45°C	High temp charging to normal CHG; V_{TS} : $0.2V \rightarrow 0.5V$		10.7		mV
V _{TS-60°C}	High temperature Disable	High temp charge to pending; V_{TS} : 0.2V \rightarrow 0.1V	170	178	186	mV
V _{HYS-60°C}	Hysteresis at 60°C	Charge pending to high temp CHG; V_{TS} : 0.1V \rightarrow 0.2V		11.5		mV
V _{TS-EN-10k}	Charge Enable Threshold, (10k NTC)	V _{TS} : 0V → 0.175V	80	88	96	mV
V _{TS-DIS_HYS-10k}	HYS below $V_{\text{TS-EN-10k}}$ to Disable, (10k NTC)	V_{TS} : $0.125V \rightarrow 0V$		12		mV
THERMAL REG	GULATION					
$T_{J(REG)}$	Temperature regulation limit			125		°C
$T_{J(OFF)}$	Thermal shutdown temperature			155		°C
$T_{J(OFF\text{-HYS})}$	Thermal shutdown hysteresis			20		°C
BAT_EN, BQ24	1041					
I _{BAT_EN}	Current Sourced out of terminal	V _{BAT_EN} < 1.4 V	2.3	5	9	μΑ
V_{IL}	Logic LOW enables charger		0		0.4	V
V _{IH}	Logic HIGH disables charger		1.1		6	V
V _{CLAMP}	Floating Clamp Voltage	Floating BAT_EN terminal	1.4	1.6	1.8	V
LOGIC LIVELS	ON ISET2					
V _{IL}	Logic LOW input voltage	Sink 8 μA			0.4	V
V _{IH}	Logic HIGH input voltage	Source 8 µA	1.4			V
I _{IL}	Sink current required for LO	V _{ISET2} = 0.4V	2		9	μA
I _{IH}	Source current required for HI	V _{ISET2} = 1.4V	1.1		9.5	μA
V _{FLT}	ISET2 Float Voltage		575	900	1225	mV
	ASI AND ASO TERMINALS, BQ24041	1	1			
V _{ASIL}	Has 200k Internal Pull-down				0.4	V
V _{ASIH}			1.3			V
V _{ASOL}	Auto Start Output Sinks 1mA				0.4	V
V _{ASOH}	Auto Start Input Sources 1mA		V _{OUT} - 0.4			V
	ON CHG AND PG	1	301 3			-
V _{OL}	Output LOW voltage	I _{SINK} = 5 mA			0.4	V
	Leakage current into IC	V CHG = 5V, V PG = 5V			1	μA
I _{LEAK}	25a.ago ourroin into 10	CHG OV, V PG OV			'	



7.6 Timing Requirements

			MIN	NOM	MAX	UNIT
INPUT						
t _{DGL(PG_PWR)}	Deglitch time on exiting sleep.	Time measured from $V_{IN}\!\!:\!0V\to 5V$ 1µs rise-time to \overline{PG} = low, V_{OUT} = 3.6V	45			μs
t _{DGL(PG_NO-} PWR)	Deglitch time on $V_{\mbox{\scriptsize HYS-INDT}}$ power down. Same as entering sleep.	Time measured from V _{IN} : 5V \rightarrow 3.2V 1µs fall-time to \overline{PG} = OC, V _{OUT} = 3.6V	29			ms
t _{DGL(OVP-SET)}	Input over-voltage blanking time	V_{IN} : 5V \rightarrow 12V		113		μs
t _{DGL(OVP-REC)}	Deglitch time exiting OVP	Time measured from $V_{IN}\!\!: 12V \to 5V$ 1µs fall-time to \overline{PG} = LO		30		μs
ISET SHORT	CIRCUIT TEST					
t _{DGL_SHORT}	Deglitch time transition from ISET short to I_{OUT} disable	Clear fault by disconnecting IN or cycling (high / low) TS/ BAT_EN		1		ms
PRECHARGE	- SET BY PRETERM PIN: BQ24040 / BQ24	045; Internally Set: BQ24041				
t _{DGL1(LOWV)}	Deglitch time on pre-charge to fast-charge transition			70		μs
t _{DGL2(LOWV)}	Deglitch time on fast-charge to pre-charge transition			32		ms
TERMINATIO	N – SET BY PRE-TERM PIN: BQ24040 / BQ2	24045				
t _{DGL(TERM)}	Deglitch time, termination detected			29		ms
t _{Term-Start}	Elevated termination threshold initially active for $t_{\text{Term-Start}}$			1.25		min
RECHARGE (OR REFRESH – BQ24040 / BQ24045					
t _{DGL1(RCH)}	Deglitch time, recharge threshold detected	$ \begin{aligned} V_{\text{IN}} &= 5\text{V, V}_{\text{TS}} = 0.5\text{V, V}_{\text{OUT}}\text{: }4.25\text{V} \rightarrow 3.5\text{V in 1}\mu\text{s;} \\ t_{\text{DGL(RCH)}} \text{ is time to ISET ramp} \end{aligned} $		29		ms
t _{DGL2(RCH)}	Deglitch time, recharge threshold detected in OUT-Detect Mode	$V_{\rm IN}$ = 5V, $V_{\rm TS}$ = 0.5V, $V_{\rm OUT}$ = 3.5V inserted; $t_{\rm DGL(RCH)}$ is time to ISET ramp		3.6		ms
BATTERY DE	TECT ROUTINE - BQ24040 / BQ24045 (NO	TE: In Hot mode V _{O(REG)} becomes V _{O_HT(REG)})				
t _{DGL(HI/LOW}	Regulation time at V _{REG} or V _{REG-BD}			25		ms
BATTERY CH	ARGING TIMERS AND FAULT TIMERS: BQ	24040 and BQ24045 only			•	
t _{PRECHG}	Pre-charge safety timer value	Restarts when entering Pre-charge; Always enabled when in pre-charge.	1700	1940	2250	s
t _{MAXCH}	Charge safety timer value	Clears fault or resets at UVLO, TS/ BAT_EN disable, OUT Short, exiting LOWV and Refresh	34000	38800	45000	S
BATTERY-PA	CK NTC MONITOR; TS Terminal: BQ24040	/ BQ24045: 10k NTC				
t _{DGL(TTDM)}	Deglitch exit TTDM between states			57		ms
	Deglitch enter TTDM between states			8		μs
t _{DGL(TS_10C)}	Deglitch for TS thresholds: 10C.	Normal to Cold Operation; V_{TS} : 0.6V \rightarrow 1V		50		ms
		Cold to Normal Operation; V _{TS} : 1V → 0.6V		12		ms
t _{DGL(TS)}	Deglitch for TS thresholds: 0/45/60C.	Battery charging		30		ms

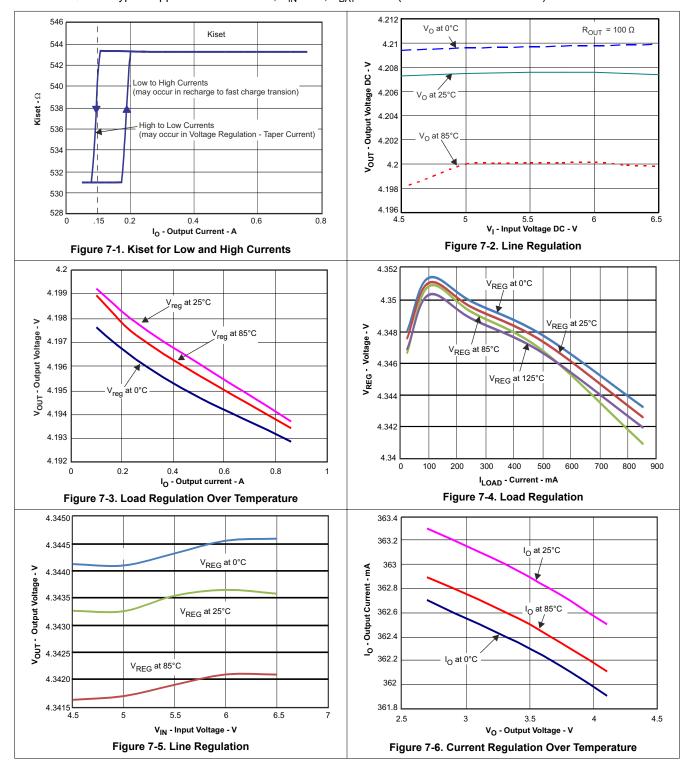
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7.7 Typical Operational Characteristics (Protection Circuits Waveforms)

SETUP: BQ24040 typical applications schematic; V_{IN} = 5V, V_{BAT} = 3.6V (unless otherwise indicated)



8 Detailed Description

8.1 Overview

The BQ2404x is a highly integrated family of 2×2 single cell Li-lon and Li-Pol chargers. The charger can be used to charge a battery, power a system or both. The charger has three phases of charging: Pre-charge to recover a fully discharged battery, fast-charge constant current to supply the buck charge safely and voltage regulation to safely reach full capacity. The charger is very flexible, allowing programming of the fast-charge current and Pre-charge/Termination Current (BQ24040/5 only). This charger is designed to work with a USB connection or Adaptor (DC out). The charger also checks to see if a battery is present.

The charger also comes with a full set of safety features: JEITA Temperature Standard (BQ24040/5 only), Over-Voltage Protection, DPM-IN, Safety Timers, and ISET short protection. All of these features and more are described in detail below.

The charger is designed for a single power path from the input to the output to charge a single cell Li-Ion or Li-Pol battery pack. Upon application of a 5VDC power source the ISET and OUT short checks are performed to assure a proper charge cycle.

If the battery voltage is below the LOWV threshold, the battery is considered discharged and a preconditioning cycle begins. The amount of precharge current can be programmed using the PRE-TERM terminal which programs a percent of fast charge current (10 to 100%) as the precharge current. This feature is useful when the system load is connected across the battery "stealing" the battery current. The precharge current can be set higher to account for the system loading while allowing the battery to be properly conditioned. The PRE-TERM terminal is a dual function terminal which sets the precharge current level and the termination threshold level. The termination "current threshold" is always half of the precharge programmed current level.

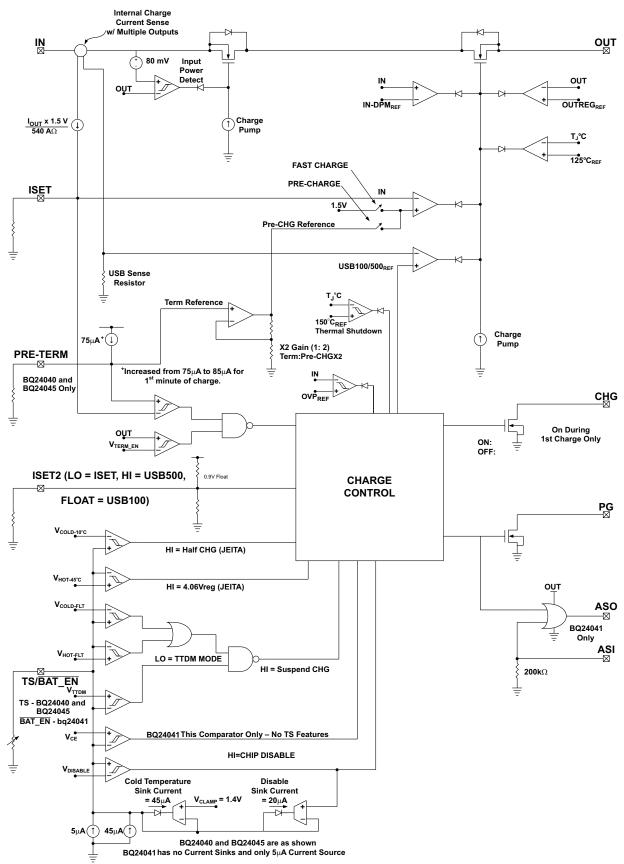
Once the battery voltage has charged to the VLOWV threshold, fast charge is initiated and the fast charge current is applied. The fast charge constant current is programmed using the ISET terminal. The constant current provides the bulk of the charge. Power dissipation in the IC is greatest in fast charge with a lower battery voltage. If the IC reaches 125°C the IC enters thermal regulation, slows the timer clock by half and reduce the charge current as needed to keep the temperature from rising any further. Figure 8-1 shows the charging profile with thermal regulation. Typically under normal operating conditions, the IC's junction temperature is less than 125°C and thermal regulation is not entered.

Once the cell has charged to the regulation voltage the voltage loop takes control and holds the battery at the regulation voltage until the current tapers to the termination threshold. The termination can be disabled if desired. The $\overline{\text{CHG}}$ terminal is low (LED on) during the first charge cycle only and turns off once the termination threshold is reached, regardless if termination, for charge current, is enabled or disabled.

Further details are mentioned in the Operating Modes section.



8.2 Functional Block Diagram



8.3 Feature Description

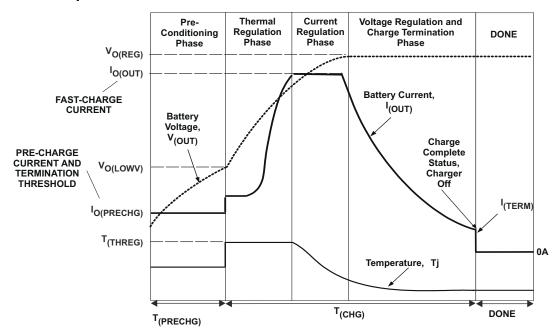


Figure 8-1. Charging Profile With Thermal Regulation

8.3.1 Power-Down or Undervoltage Lockout (UVLO)

The BQ2404x family is in power down mode if the IN terminal voltage is less than UVLO. The part is considered "dead" and all the terminals are high impedance. Once the IN voltage rises above the UVLO threshold the IC will enter Sleep Mode or Active mode depending on the OUT terminal (battery) voltage.

8.3.2 Power-up

The IC is alive after the IN voltage ramps above UVLO (see sleep mode), resets all logic and timers, and starts to perform many of the continuous monitoring routines. Typically the input voltage quickly rises through the UVLO and sleep states where the IC declares power good, starts the qualification charge at 100mA, sets the input current limit threshold base on the ISET2 terminal, starts the safety timer and enables the $\overline{\text{CHG}}$ terminal. See Figure 8-2.

8.3.3 Sleep Mode

If the IN terminal voltage is between than $V_{OUT}+V_{DT}$ and UVLO, the charge current is disabled, the safety timer counting stops (not reset) and the \overline{PG} and \overline{CHG} terminals are high impedance. As the input voltage rises and the charger exits sleep mode, the \overline{PG} terminal goes low, the safety timer continues to count, charge is enabled and the \overline{CHG} terminal returns to its previous state. See Figure 8-3.

8.3.4 New Charge Cycle

A new charge cycle is started when any of these events occur:

- A valid power source is applied;
- The chip is enabled/disabled using TS pin or BAT_EN;
- Exit of termination/Timer Disable Mode (TTDM);
- · Detection of batter insertion;
- OUT voltage drops below the VRCH threshold.

The CHG signal is active only during the first charge cycle. Exiting TTDM or the OUT voltage falling below VRCH will not activate the CHG signal if it is already in the open-drain (off) state.

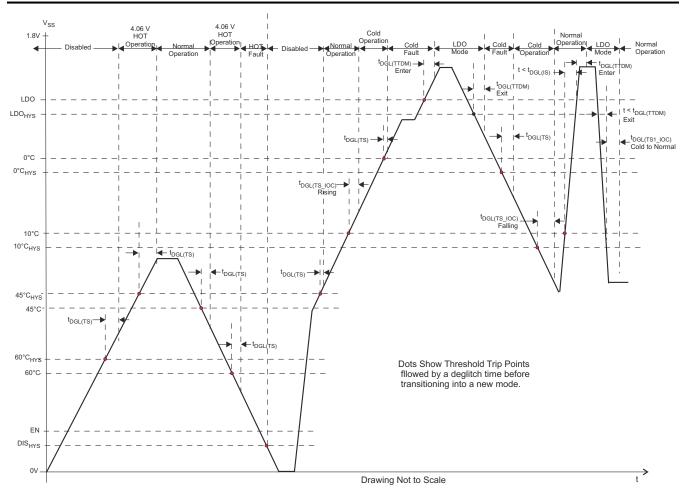


Figure 8-2. TS Battery Temperature Bias Threshold and Deglitch Timers



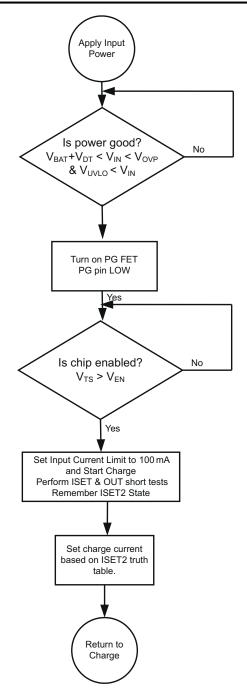


Figure 8-3. BQ2404x Power-Up Flow Diagram

8.3.5 Overvoltage-Protection (OVP) - Continuously Monitored

If the input source applies an overvoltage, the pass FET, if previously on, turns off after a deglitch, $t_{BLK(OVP)}$. The timer ends and the \overline{CHG} and \overline{PG} terminal goes to a high impedance state. Once the overvoltage returns to a normal voltage, the \overline{PG} terminal goes low, timer continues, charge continues and the \overline{CHG} terminal goes low after a 25ms deglitch. PG terminal is optional on some packages

8.3.6 Power Good Indication (PG)

After application of a 5V source, the input voltage rises above the UVLO and sleep thresholds ($V_{IN}>V_{BAT}+V_{DT}$), but is less than OVP ($V_{IN}<V_{OVP}$,), then the PG FET turns on and provides a low impedance path to ground. See Figure 9-6, Figure 9-19.

8.3.7 CHG Terminal Indication

The charge terminal has an internal open drain FET which is on (pulls down to V_{SS}) during the first charge only (independent of TTDM) and is turned off once the battery reaches voltage regulation and the charge current tapers to the termination threshold set by the PRE-TERM resistor. The BQ24041 does not terminate charge, however, the \overline{CHG} terminal will turn off once the battery current reaches 10% of the programmed charge current.

The charge terminal is high impedance in sleep mode and OVP (if \overline{PG} is high impedance) and return to its previous state once the condition is removed.

Cycling input power, pulling the TS terminal low and releasing or entering pre-charge mode causes the $\overline{\text{CHG}}$ terminal to go reset (go low if power is good and a discharged battery is attached) and is considered the start of a first charge.

8.4 Device Functional Modes

8.4.1 CHG and PG LED Pull-up Source

For host monitoring, a pullup resistor is used between the STATUS terminal and the V_{CC} of the host and for a visual indication a resistor in series with an LED is connected between the STATUS terminal and a power source. If the \overline{CHG} or \overline{PG} source is capable of exceeding 7V, a 6.2V Zener should be used to clamp the voltage. If the source is the OUT terminal, note that as the battery changes voltage, and the brightness of the LEDs vary.

CHARGING STATE

First charge after VIN applied

ON

Refresh charge

OVP

SLEEP

CHG FET/LED

ON

ON

Table 8-1.

Table 8-2.

ON for 1st Charge

TEMP FAULT

V _{IN} POWER GOOD STATE	PG FET/LED					
UVLO						
SLEEP mode	OFF					
OVP mode						
Normal input $(V_{OUT} + V_{DT} < V_{IN} < V_{OUP})$	ON					
PG is independent of chip disable						

8.4.2 Auto Start-up (BQ24041)

The auto start-up feature is an OR gate with two inputs; an internal power good signal (logic 1 when V_{IN} > V_{BAT} + V_{IN-DT}) and an external input from ASI terminal (internal 100k Ω pull-down). The ASO terminal outputs a signal that can be used as a system boot signal. The OR gate is powered by the OUT terminal and the OUT terminal must be powered by an external source (battery or P/S) or via the IN terminal for the ASO terminal to deliver a logic High. The ASI and/or the internal power good signal have to be logic high for the ASO to be logic high. The ASI/ASO, OUT and PG signals are used in production testing to test the system without a battery.

8.4.3 IN-DPM (V_{IN}-DPM or IN-DPM)

The IN-DPM feature is used to detect an input source voltage that is folding back (voltage dropping), reaching its current limit due to excessive load. When the input voltage drops to the $V_{\text{IN-DPM}}$ threshold the internal pass FET starts to reduce the current until there is no further drop in voltage at the input. This would prevent a source with voltage less than $V_{\text{IN-DPM}}$ to power the out terminal. This works well with current limited adaptors and USB ports as long as the nominal voltage is above 4.3V and 4.4V respectively. This is an added safety feature that helps protect the source from excessive loads.

8.4.4 OUT

The Charger's OUT terminal provides current to the battery and to the system, if present. This IC can be used to charge the battery plus power the system, charge just the battery or just power the system (TTDM) assuming the loads do not exceed the available current. The OUT terminal is a current limited source and is inherently protected against shorts. If the system load ever exceeds the output programmed current threshold, the output will be discharged unless there is sufficient capacitance or a charged battery present to supplement the excessive load.

8.4.5 ISET

An external resistor is used to Program the Output Current (50 to 1000mA) and can be used as a current monitor.

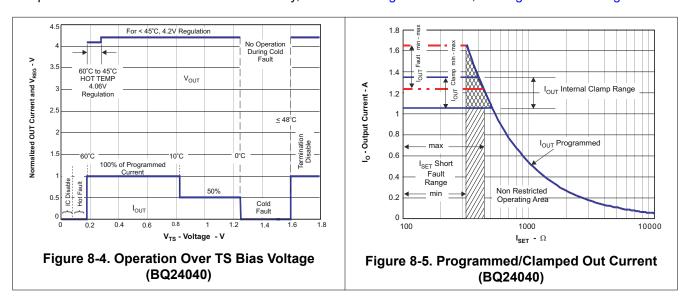
$$R_{ISET} = K_{ISET} / I_{OUT}$$
 (1)

where

- I_{OUT} is the desired fast charge current;
- K_{ISET} is a gain factor found in the electrical specification

For greater accuracy at lower currents, part of the sense FET is disabled to give better resolution. Figure 7-1 shows the transition from low current to higher current. Going from higher currents to low currents, there is hysteresis and the transition occurs around 0.15A.

The ISET resistor is short protected and will detect a resistance lower than *340Ω. The detection requires at least 80mA of output current. If a "short" is detected, then the IC will latch off and can only be reset by cycling the power. The OUT current is internally clamped to a maximum current between 1.05A and 1.4A and is independent of the ISET short detection circuitry, as shown in Figure 8-5. Also, see Figure 9-14 and Figure 9-15.



8.4.6 PRE_TERM - Pre-Charge and Termination Programmable Threshold, BQ24040/5

Pre-Term is used to program both the pre-charge current and the termination current threshold. The pre-charge current level is a factor of two higher than the termination current level. The termination can be set between 5 and 50% of the programmed output current level set by ISET. If left floating the termination and pre-charge are set internally at 10/20% respectively. The pre-charge-to-fast-charge, V_{lowy} threshold is set to 2.5V.

$$R_{PRE-TERM} = \% Term \times K_{TERM} = \% Pre-CHG \times K_{PRE-CHG}$$
 (2)

where

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- %Term is the percent of fast charge current where termination occurs;
- %Pre-CHG is the percent of fast charge current that is desired during precharge;
- K_{TERM} and K_{PRE-CHG} are gain factors found in the electrical specifications.

8.4.7 ISET2

ISET2 is a 3-state input and programs the Input Current Limit/Regulation Threshold. A low will program a regulated fast charge current via the ISET resistor and is the maximum allowed input/output current for any ISET2 setting, Float will program a 100mA Current limit and High will program a 500mA Current limit.

Below are two configurations for driving the 3-state ISET2 terminal:

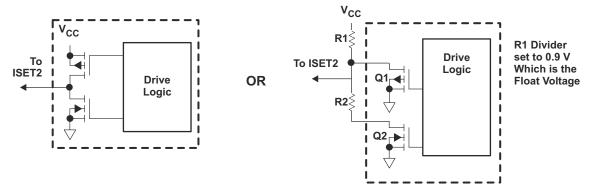


Figure 8-6. 3-State ISET2 Terminal Circuits

8.4.8 TS (BQ24040/5)

The TS function for the BQ24040/5 is designed to follow the new JEITA temperature standard for Li-lon and Li-Pol batteries. There are now four thresholds, 60°C, 45°C, 10°C, and 0°C. Normal operation occurs between 10°C and 45°C. If between 0°C and 10°C the charge current level is cut in half and if between 45°C and 60°C the regulation voltage is reduced to 4.1Vmax, see Figure 8-4.

The TS feature is implemented using an internal $50\mu A$ current source to bias the thermistor (designed for use with a 10k NTC β = 3370 (SEMITEC 103AT-2 or Mitsubishi TH05-3H103F) connected from the TS terminal to V_{SS} . If this feature is not needed, a fixed $10k\Omega$ can be placed between TS and V_{SS} to allow normal operation. This may be done if the host is monitoring the thermistor and then the host would determine when to pull the TS terminal low to disable charge.

The TS terminal has two additional features, when the TS terminal is pulled low or floated/driven high. A low disables charge (similar to a high on the BAT_EN feature) and a high puts the charger in TTDM.

Above 60°C or below 0°C the charge is disabled. Once the thermistor reaches \approx -10°C the TS current folds back to keep a cold thermistor (between -10°C and -50°C) from placing the IC in the TTDM mode. If the TS terminal is pulled low into disable mode, the current is reduce to \approx 30 μ A, see Figure 8-2. Since the I_{TS} curent is fixed along with the temperature thresholds, it is not possible to use thermistor values other than the 10k NTC (at 25°C).

8.4.9 Termination and Timer Disable Mode (TTDM) - TS Terminal High

The battery charger is in TTDM when the TS terminal goes high from removing the thermistor (removing battery pack/floating the TS terminal) or by pulling the TS terminal up to the TTDM threshold.

When entering TTDM, the 10 hour safety timer is held in reset and termination is disabled. A battery detect routine is run to see if the battery was removed or not. If the battery was removed then the \overline{CHG} terminal will go to its high impedance state if not already there. If a battery is detected the \overline{CHG} terminal does not change states until the current tapers to the termination threshold, where the \overline{CHG} terminal goes to its high impedance state if not already there (the regulated output will remain on).

The charging profile does not change (still has pre-charge, fast-charge constant current and constant voltage modes). This implies the battery is still charged safely and the current is allowed to taper to zero.

When coming out of TTDM, the battery detect routine is run and if a battery is detected, then a new charge cycle begins and the CHG LED turns on.

If TTDM is not desired upon removing the battery with the thermistor, one can add a 237k resistor between TS and V_{SS} to disable TTDM. This keeps the current source from driving the TS terminal into TTDM. This creates $\neq 0.1^{\circ}C$ error at hot and a $\neq 3^{\circ}C$ error at cold.

8.4.10 Timers, BQ24040 and BQ24045 only

The pre-charge timer is set to 30 minutes. The pre-charge current, can be programmed to off-set any system load, making sure that the 30 minutes is adequate. The BQ24041 does not have a safety timer.

The fast charge timer is fixed at 10 hours and can be increased real time by going into thermal regulation, IN-DPM or if in USB current limit. The timer clock slows by a factor of 2, resulting in a clock than counts half as fast when in these modes. If either the 30 minute or ten hour timer times out, the charging is terminated and the CHG terminal goes high impedance if not already in that state. The timer is reset by disabling the IC, cycling power or going into and out of TTDM.

8.4.11 Termination

Once the OUT terminal goes above VRCH, (reaches voltage regulation) and the current tapers down to the termination threshold, the $\overline{\text{CHG}}$ terminal goes high impedance and a battery detect route is run to determine if the battery was removed or the battery is full. If the battery is present, the charge current will terminate. If the battery was removed along with the thermistor, then the TS terminal is driven high and the charge enters TTDM. If the battery was removed and the TS terminal is held in the active region, then the battery detect routine will continue until a battery is inserted.

8.4.12 Battery Detect Routine

The battery detect routine should check for a missing battery while keeping the OUT terminal at a useable voltage. Whenever the battery is missing the CHG terminal should be high impedance.

The battery detect routine is run when entering and exiting TTDM to verify if battery is present, or run all the time if battery is missing and not in TTDM. On power-up, if battery voltage is greater than V_{RCH} threshold, a battery detect routine is run to determine if a battery is present.

The battery detect routine is disabled while the IC is in TTDM, or has a TS fault. See Figure 8-7 for the Battery Detect Flow Diagram.

8.4.13 Refresh Threshold

After termination, if the OUT terminal voltage drops to V_{RCH} (100mV below regulation) then a new charge is initiated, but the \overline{CHG} terminal remains at a high impedance (off).

8.4.14 Starting a Charge on a Full Battery

The termination threshold is raised by \$14%, for the first minute of a charge cycle so if a full battery is removed and reinserted or a new charge cycle is initiated, that the new charge terminates (less than 1 minute). Batteries that have relaxed many hours may take several minutes to taper to the termination threshold and terminate charge.



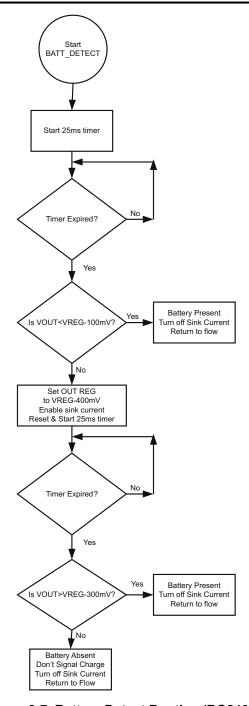


Figure 8-7. Battery Detect Routine (BQ24040)

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The BQ2404x series of devices are highly integrated Li-lon and Li-Pol linear chargers devices targeted at space-limited portable applications. The devices operate from either a USB port or AC adapter. The high input voltage range with input overvoltage protection supports low-cost unregulated adapters. These devices have a single power output that charges the battery. A system load can be placed in parallel with the battery as long as the average system load does not keep the battery from charging fully during the 10 hour safety timer.

9.2 Typical Applications

9.2.1 Typical Application: BQ24040 and BQ24045

I_{OUT FAST CHG} = 540mA; I_{OUT PRE CHG} = 108mA; I_{OUT TERM} = 54mA

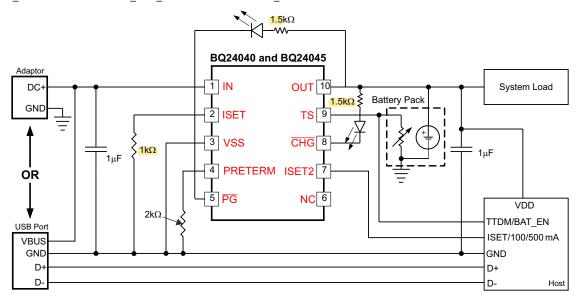


Figure 9-1. Typical Application Circuit: BQ24040 and BQ24045

9.2.1.1 Design Requirements

- Supply voltage = 5 V
- Fast charge current: I_{OUT-FC} = 540 mA; ISET-terminal 2
- Termination Current Threshold: %_{IOUT-FC} = 10% of Fast Charge or about 54mA
- Pre-Charge Current by default is twice the termination Current or about 108mA
- TS Battery Temperature Sense = 10k NTC (103AT)

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Calculations

For additional information on calculations, refer to BQ24040 Application Report.

9.2.1.2.1.1 Program the Fast Charge Current, ISET:

$$R_{ISET} = [K_{(ISET)} / I_{(OUT)}]$$
(3)

From Section 7.5:

- K_(SET) = 540AΩ
- $R_{ISET} = [540A\Omega/0.54A] = 1.0 k\Omega$

Selecting the closest standard value, use a 1.0 kΩ resistor between ISET (terminal 16) and VSS.

9.2.1.2.1.2 Program the Termination Current Threshold, ITERM:

$$R_{PRE-TERM} = K_{(TERM)} \times \%_{IOUT-FC}$$
 (4)

$$R_{PRE-TERM} = 200\Omega/\% \times 10\% = 2k\Omega \tag{5}$$

Selecting the closest standard value, use a 2 $k\Omega$ resistor between ITERM (terminal 15) and VSS.

One can arrive at the same value by using 20% for a pre-charge value (factor of 2 difference).

$$R_{PRE-TERM} = K_{(PRE-CHG)} \times \%_{IOUT-FC}$$
(6)

$$R_{PRE-TERM} = 100\Omega/\% \times 20\% = 2k\Omega \tag{7}$$

9.2.1.2.1.3 TS Function (BQ24040)

Use a 10k NTC thermistor in the battery pack (103AT).

To Disable the temp sense function, use a fixed 10k resistor between the TS (terminal 1) and VSS.

9.2.1.2.1.4 CHG and PG

LED Status: connect a 1.5k resistor in series with a LED between the OUT terminal and the CHG terminal. Connect a 1.5k resistor in series with a LED between the OUT terminal and the and PG terminal.

Processor Monitoring: Connect a pull-up resistor between the processor's power rail and the CHG terminal. Connect a pull-up resistor between the processor's power rail and the PG terminal.

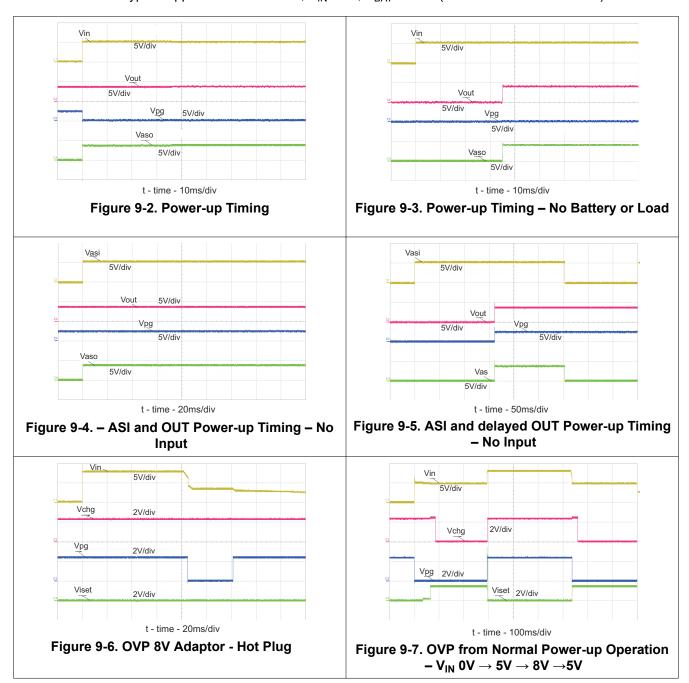
9.2.1.2.2 Selecting In and Out Terminal Capacitors

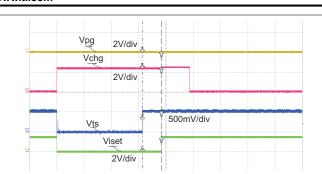
In most applications, all that is needed is a high-frequency decoupling capacitor (ceramic) on the power terminal, input and output terminals. Using the values shown on the application diagram, is recommended. After evaluation of these voltage signals with real system operational conditions, one can determine if capacitance values can be adjusted toward the minimum recommended values (DC load application) or higher values for fast high amplitude pulsed load applications. Note if designed for high input voltage sources (bad adaptors or wrong adaptors), the capacitor needs to be rated appropriately. Ceramic capacitors are tested to 2x their rated values so a 16V capacitor may be adequate for a 30V transient (verify tested rating with capacitor manufacturer).



9.2.1.3 Application Curves

SETUP: BQ24040 typical applications schematic; V_{IN} = 5V, V_{BAT} = 3.6V (unless otherwise indicated)





t - time - 50ms/div

 $10k\Omega$ resistor from TS to GND. $10k\Omega$ is shorted to disable the IC

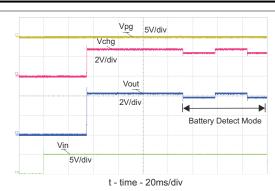


Figure 9-9. Hot Plug Source w/No Battery - Battery **Detection**

Figure 9-8. TS Enable and Disable

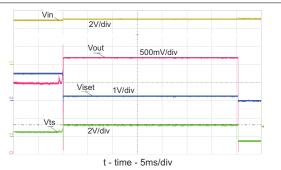


Figure 9-10. Battery Removal - GND Removed 1st, 42 Ω Load

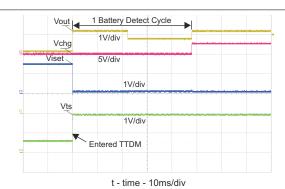
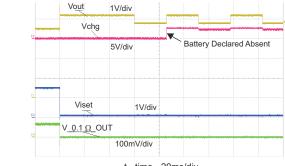
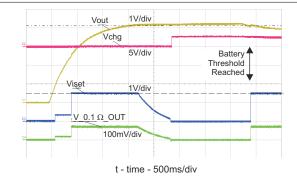


Figure 9-11. Battery Removal with OUT and TS Disconnect 1st, With 100 Ω Load



t - time - 20ms/div



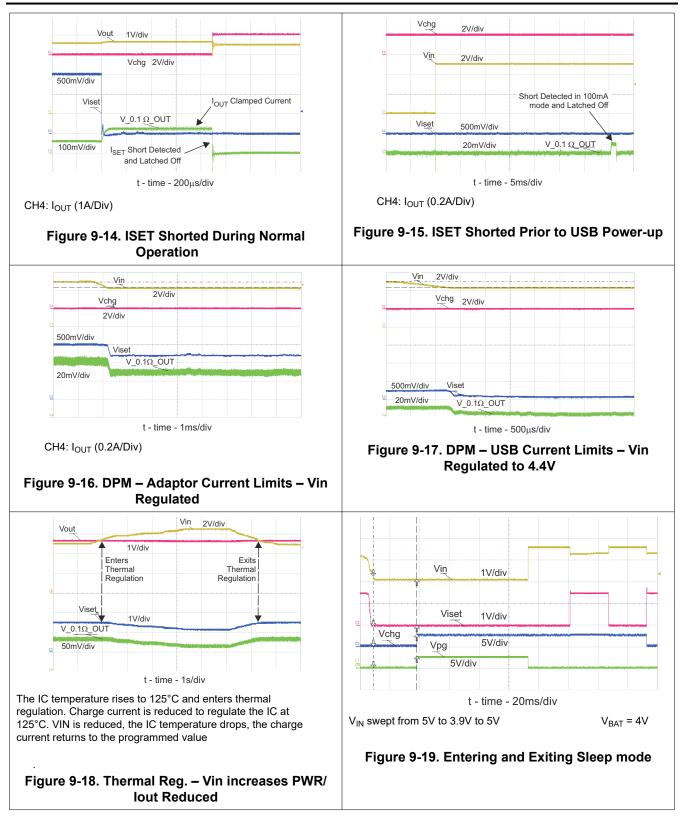


CH4: I_{OUT} (1A/Div)

Battery voltage swept from 0V to 4.25V to 3.9V.

Figure 9-13. Battery Charge Profile







9.2.2 Typical Application Circuit: BQ24041, with ASI and ASO

 $I_{OUT_FAST_CHG} = 540$ mA; $I_{OUT_PRE_CHG} = 108$ mA

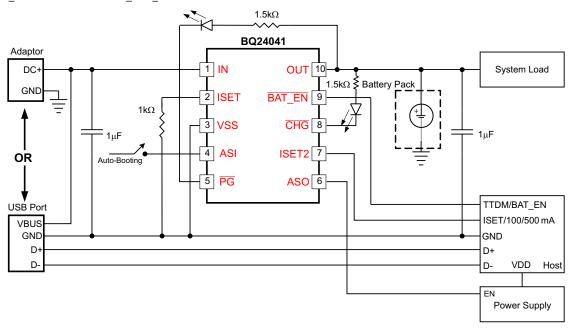


Figure 9-20. Typical Application Circuit: BQ24041, with ASI and ASO

9.2.2.1 Design Requirements

See Section 9.2.1 for design requirements.

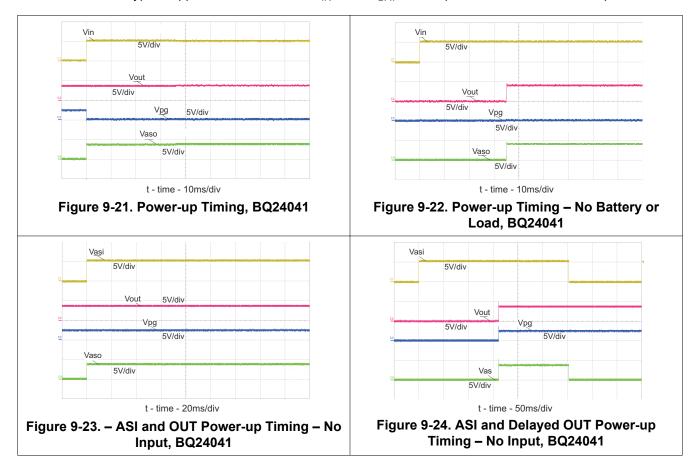
9.2.2.2 Detailed Design Procedure

See Section 9.2.1 for detailed design procedures.



9.2.2.3 Application Curves

SETUP: BQ24041 typical applications schematic; V_{IN} = 5V, V_{BAT} = 3.6V (unless otherwise indicated)





10 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 3.5 V and 28 V and current capability of at least the maximum designed charge current. This input supply should be well regulated. If located more than a few inches from the BQ24040x IN and GND terminals, a larger capacitor is recommended.

11 Layout

11.1 Layout Guidelines

To obtain optimal performance, the decoupling capacitor from IN to GND (thermal pad) and the output filter capacitors from OUT to GND (thermal pad) should be placed as close as possible to the BQ2405x, with short trace runs to both IN, OUT, and GND (thermal pad).

- All low-current GND connections should be kept separate from the high-current charge or discharge paths
 from the battery. Use a single-point ground technique incorporating both the small signal ground path and the
 power ground path.
- The high current charge paths into IN terminal and from the OUT terminal must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces
- The BQ2404x family is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB); this thermal pad is also the main ground connection for the device. Connect the thermal pad to the PCB ground connection. It is best to use multiple 10mil vias in the power pad of the IC and close enough to conduct the heat to the bottom ground plane. The bottom ground plane should avoid traces that "cut off" the thermal path. The thinner the PCB the less temperature rise. The EVM PCB has a thickness of 0.031 inches and uses 2 oz. (2.8mil thick) copper on top and bottom, and is a good example of optimal thermal performance.

11.2 Layout Example

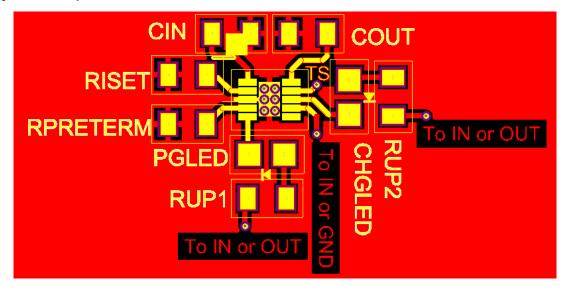


Figure 11-1. Board Layout

11.3 Thermal Considerations

The BQ2404x family is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB). The power pad should be directly connected to the VSS terminal. Full PCB design guidelines for this package are provided in the application note entitled: QFN/SON PCB Attachment Application Report. The most common measure of package thermal performance is thermal impedance ($R_{\theta JA}$) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for $R_{\theta JA}$ is:

$$R_{\theta JA} = (T_J - T) / P \tag{8}$$

where

- T_J = Chip junction temperature
- T = Ambient temperature
- P = Device power dissipation

Factors that can influence the measurement and calculation of $R_{\theta JA}$ include:

- 1. Whether or not the device is board mounted
- 2. Trace size, composition, thickness, and geometry
- 3. Orientation of the device (horizontal or vertical)
- 4. Volume of the ambient air surrounding the device under test and airflow
- 5. Whether other surfaces are in close proximity to the device being tested

Due to the charge profile of Li-Ion and Li-Pol batteries the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. Typically after fast charge begins the pack voltage increases to \$3.4V within the first 2 minutes. The thermal time constant of the assembly typically takes a few minutes to heat up so when doing maximum power dissipation calculations, 3.4V is a good minimum voltage to use. This is verified, with the system and a fully discharged battery, by plotting temperature on the bottom of the PCB under the IC (pad should have multiple vias), the charge current and the battery voltage as a function of time. The fast charge current will start to taper off if the part goes into thermal regulation.

The device power dissipation, P, is a function of the charge rate and the voltage drop across the internal PowerFET. It can be calculated from the following equation when a battery pack is being charged:

$$P = [V_{(IN)} - V_{(OUT)}] \times I_{(OUT)} + [V_{(OUT)} - V_{(BAT)}] \times I_{(BAT)}$$
(9)

The thermal loop feature reduces the charge current to limit excessive IC junction temperature. It is recommended that the design not run in thermal regulation for typical operating conditions (nominal input voltage and nominal ambient temperatures) and use the feature for non typical situations such as hot environments or higher than normal input source voltage. With that said, the IC will still perform as described, if the thermal loop is always active.

11.3.1 Leakage Current Effects on Battery Capacity

To determine how fast a leakage current on the battery will discharge the battery is an easy calculation. The time from full to discharge can be calculated by dividing the Amp-Hour Capacity of the battery by the leakage current. For a 0.75AHr battery and a $10\mu A$ leakage current (750 mAHr / 0.010 mA = 75000 hours), it would take 75k hours or 8.8 years to discharge. In reality the self discharge of the cell would be much faster so the $10\mu A$ leakage would be considered negligible.

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- BQ24040 Pin FMA Application Report
- BQ2404x FIT Rate Application Report
- BQ24040 Application Report
- QFN/SON PCB Attachment Application Report

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

Ti Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.





20-Jan-2021

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
BQ24040DSQR	ACTIVE	WSON	DSQ	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 125	NXE	Samples
BQ24040DSQT	ACTIVE	WSON	DSQ	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 125	NXE	Samples
BQ24041DSQR	ACTIVE	WSON	DSQ	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		NXF	Samples
BQ24041DSQT	ACTIVE	WSON	DSQ	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		NXF	Samples
BQ24045DSQR	ACTIVE	WSON	DSQ	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		SII	Samples
BQ24045DSQT	ACTIVE	WSON	DSQ	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		SII	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



PACKAGE OPTION ADDENDUM

20-Jan-2021

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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





Α0	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24040DSQR	WSON	DSQ	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ24040DSQT	WSON	DSQ	10	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ24041DSQR	WSON	DSQ	10	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
BQ24041DSQT	WSON	DSQ	10	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
BQ24045DSQR	WSON	DSQ	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ24045DSQT	WSON	DSQ	10	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

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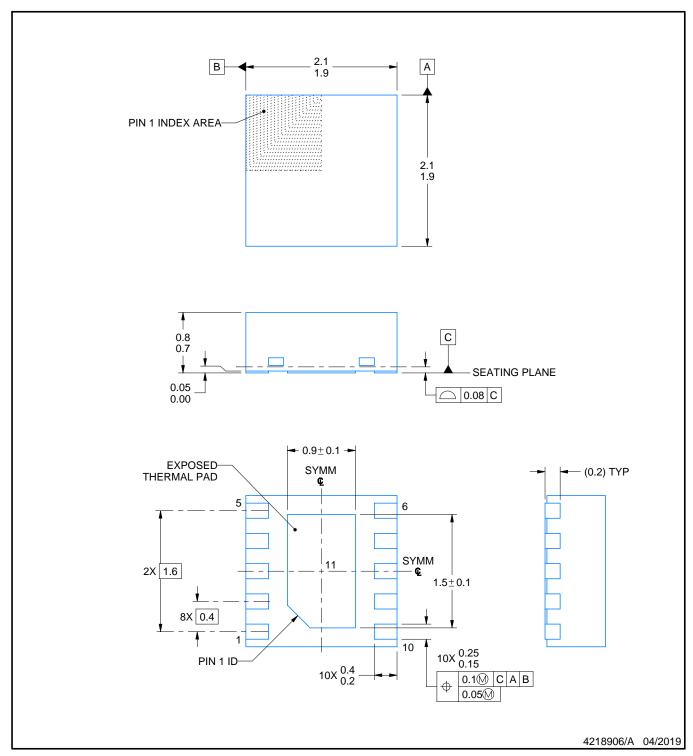


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24040DSQR	WSON	DSQ	10	3000	210.0	185.0	35.0
BQ24040DSQT	WSON	DSQ	10	250	210.0	185.0	35.0
BQ24041DSQR	WSON	DSQ	10	3000	213.0	191.0	35.0
BQ24041DSQT	WSON	DSQ	10	250	213.0	191.0	35.0
BQ24045DSQR	WSON	DSQ	10	3000	210.0	185.0	35.0
BQ24045DSQT	WSON	DSQ	10	250	210.0	185.0	35.0



PLASTIC SMALL OUTLINE - NO LEAD

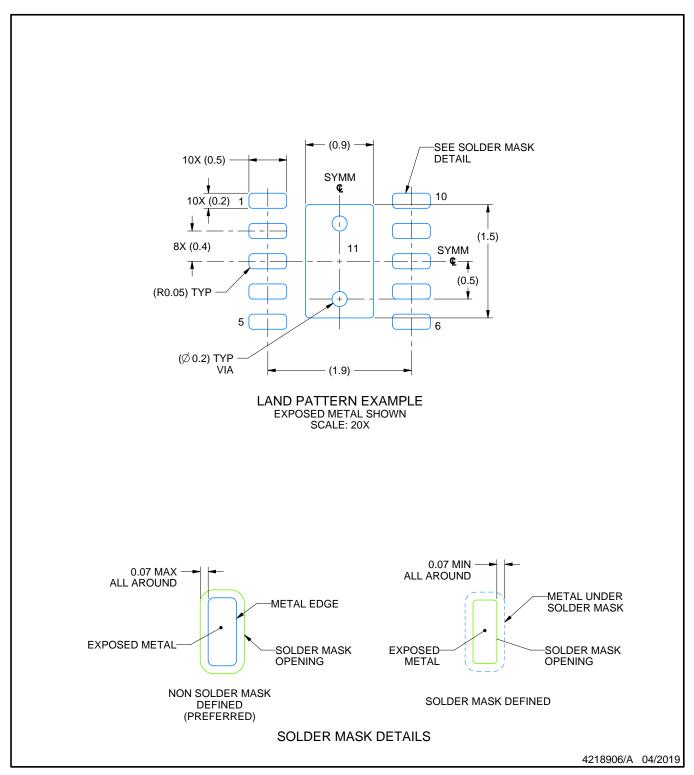


NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC SMALL OUTLINE - NO LEAD

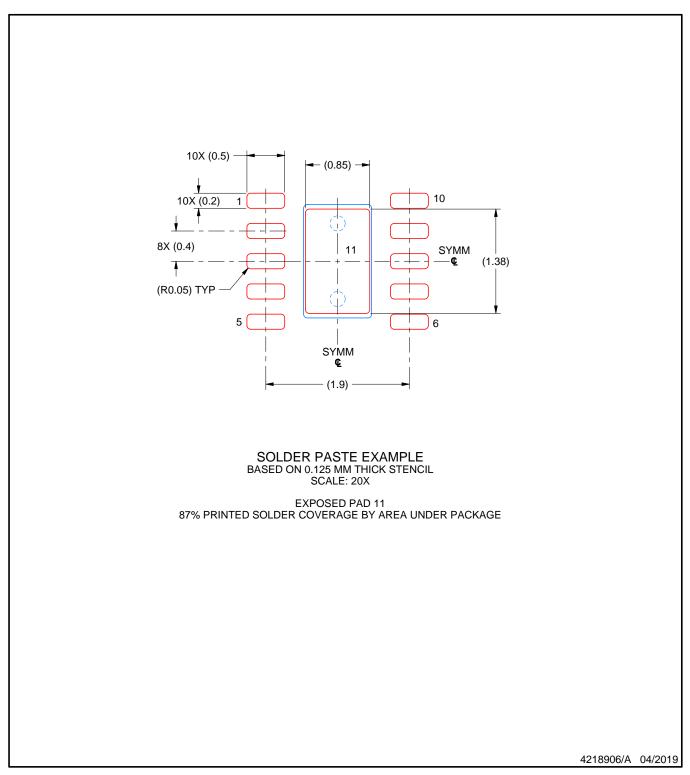


NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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