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School of Electrical Engineering
and Computer Science

Lab 2

3-Input Priority Encoder

Prepared for:

ELG 4137 - Principles & Application of VLSI Design

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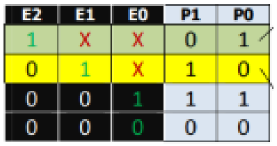
Prelab: K-map logical expression and verilog 1-bit comparator

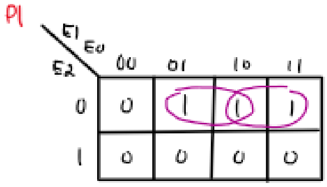
K-map and logical expression

-> 3-bit Priority encoder truth table.



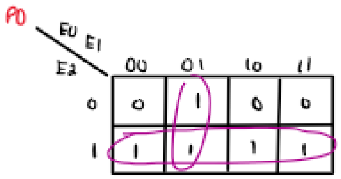
E2	E1	E0	P1	P0
1	X	X	0	1
0	1	X	1	0
0	0	1	1	1
0	0	0	0	0

-> K-map of truth table



P1

E1 E0 E2	00	01	10	11
0	0	1	1	1
1	0	0	0	0



P0

E0 E1 E2	00	01	10	11
0	0	1	0	0
1	1	1	1	1

-> Logical expressions from K-map

$P1 = E2'E0 + E2'E1 = E2'(E1 + E0)$

$P0 = E'E0 + E2$

Part II

-> 1-bit comparator truth table

A	B	A<B	A>B	A=B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

-> K-map from truth table

A<B

A B	0	1
0	0	1
1	0	0

A>B

A B	0	1
0	1	0
1	0	1

A=B

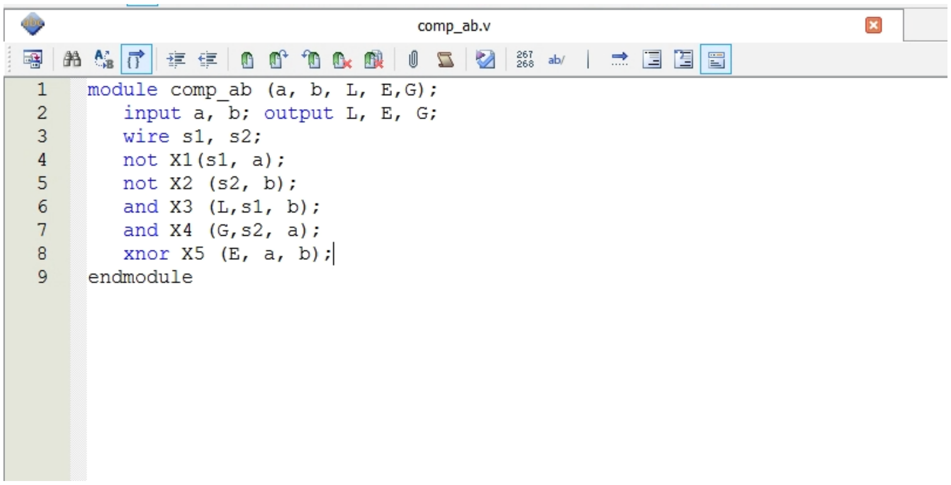
A B	0	1
0	0	0
1	1	0

$A<B = A'B$

$A>B = AB'$

$A=B = A'B' + AB$

1-Bit Comparator Verilog Code

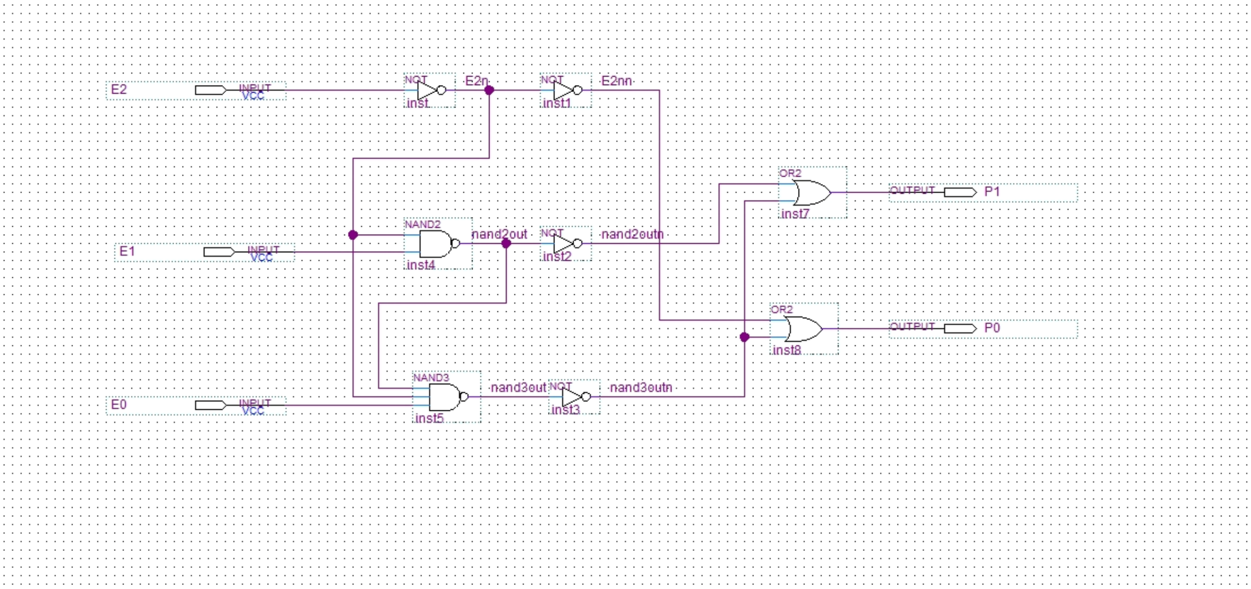


```
module comp_ab (a, b, L, E,G);
   input a, b; output L, E, G;
   wire s1, s2;
   not X1(s1, a);
   not X2 (s2, b);
   and X3 (L,s1, b);
   and X4 (G,s2, a);
   xnor X5 (E, a, b);
endmodule
```

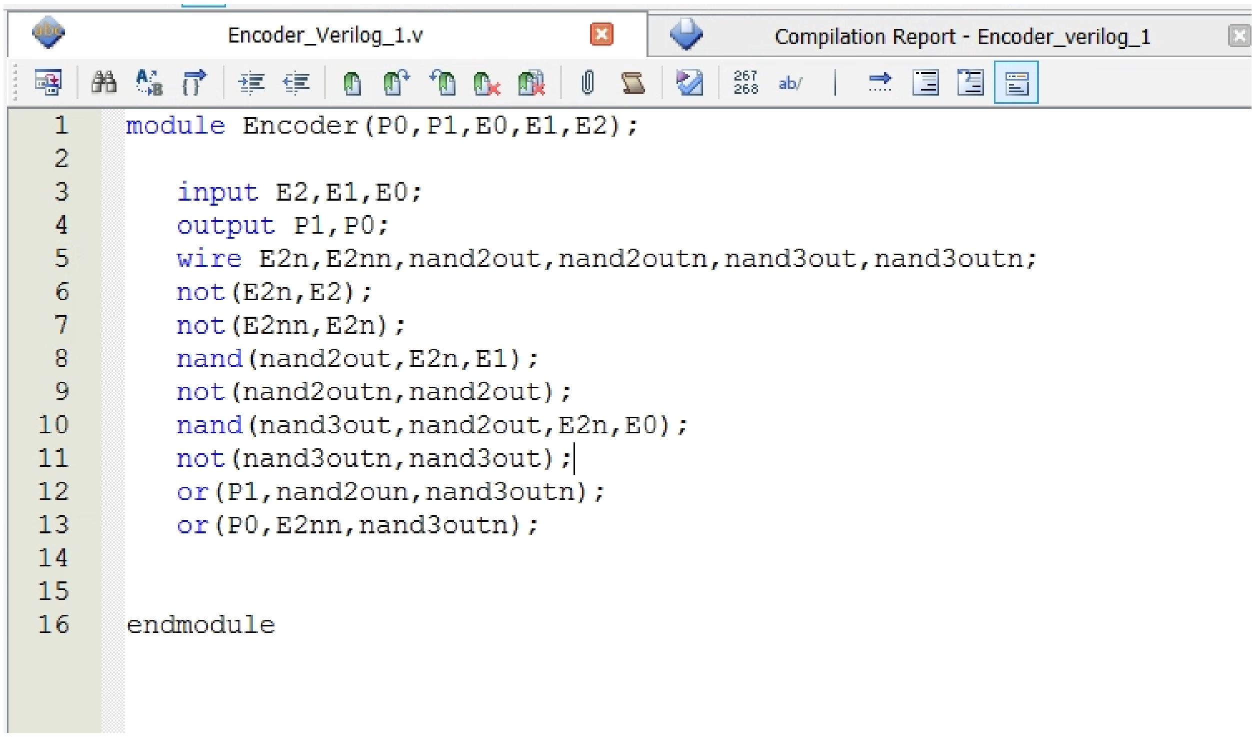
Part 1: Design of Priority Encoder

A priority encoder converts the 3-bit input into a binary (2-bit) representation. The output of the encoder takes the most significant active input and all other lower inputs are ignored.

3-Bit Priority Encoder Model

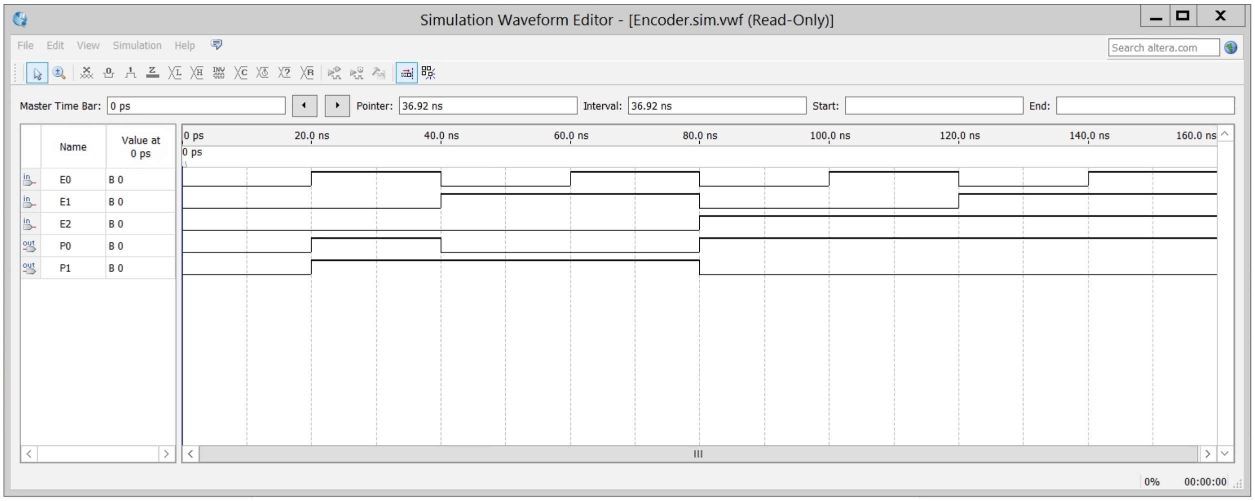


3-Bit Priority Encoder Verilog Program



```
module Encoder(P0,P1,E0,E1,E2);

   input E2,E1,E0;
   output P1,P0;
   wire E2n,E2nn,nand2out,nand2outn,nand3out,nand3outn;
   not(E2n,E2);
   not(E2nn,E2n);
   nand(nand2out,E2n,E1);
   not(nand2outn,nand2out);
   nand(nand3out,nand2out,E2n,E0);
   not(nand3outn,nand3out);
   or(P1,nand2oun,nand3outn);
   or(P0,E2nn,nand3outn);


endmodule
```

3-Bit Priority Encoder Waveform



Master Time Bar: 0 ps Pointer: 36.92 ns Interval: 36.92 ns Start: End:

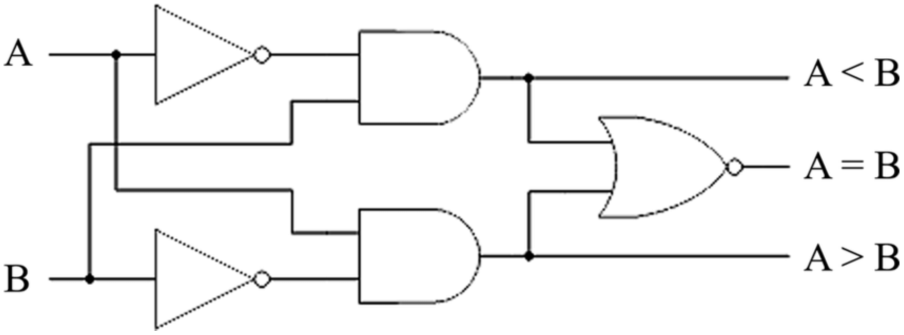
Name	Value at 0 ps
E0	B 0
E1	B 0
E2	B 0
P0	B 0
P1	B 0

After simulation of the 3-bit priority encoder all results were accurate with what was expected. Looking at the waveform above, depending on whether E2, E1 and E0 are high or low, P0 and P1 change accordingly. When E0 is high, P1P0 is equal to 11, when E1 is high P1P0 is equal to 10 and when E2 is high, P1P0 is 01.

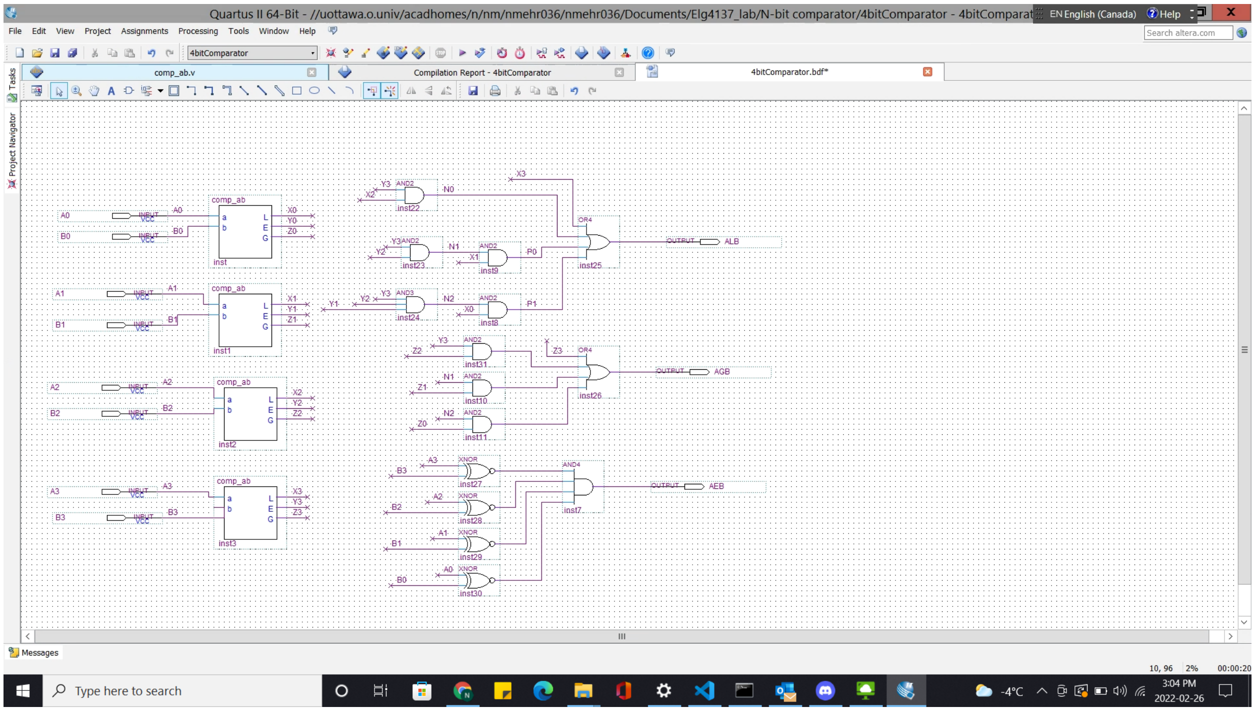
Part 2: Design of an N-bit Comparator

A N-bit comparator compares two N-bit numbers and evaluates whether the numbers are equal to one another or if one is larger than the other.

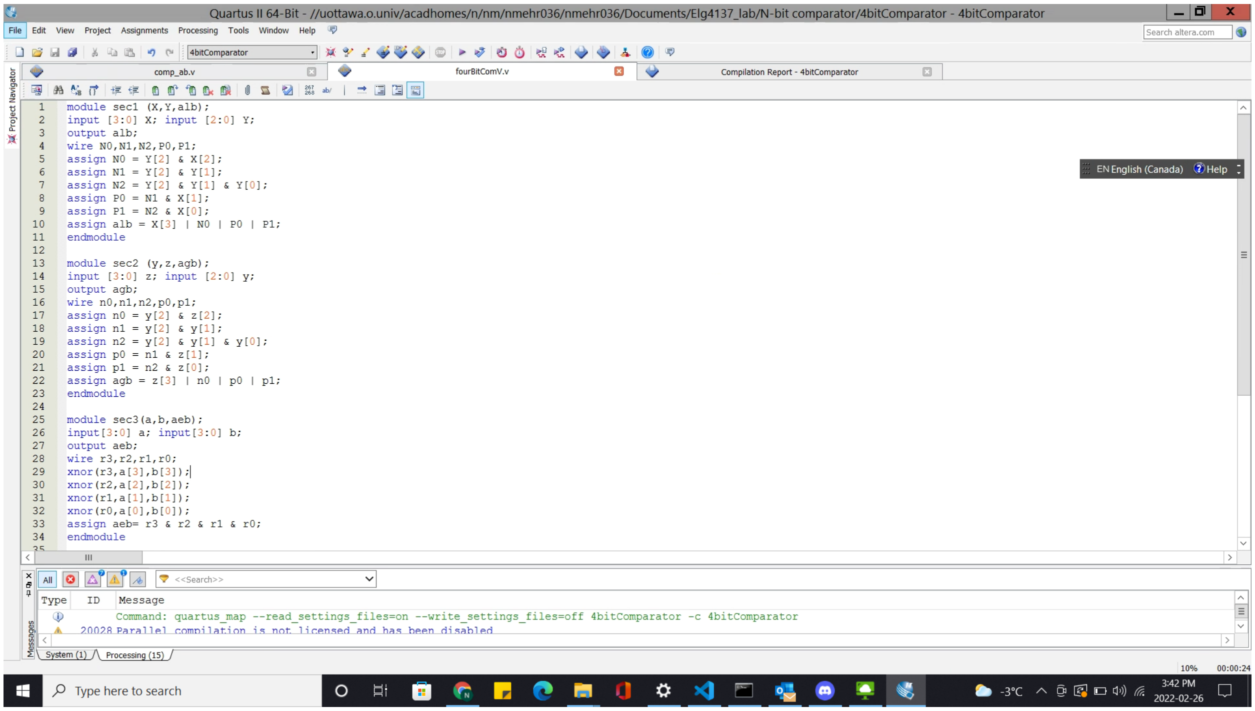
To develop a 4-bit comparator, a 1-bit comparator is designed first and then converted into a block representation. Combining four of these logic circuits to produce the 4-bit comparator.



4-bit Comparator Model

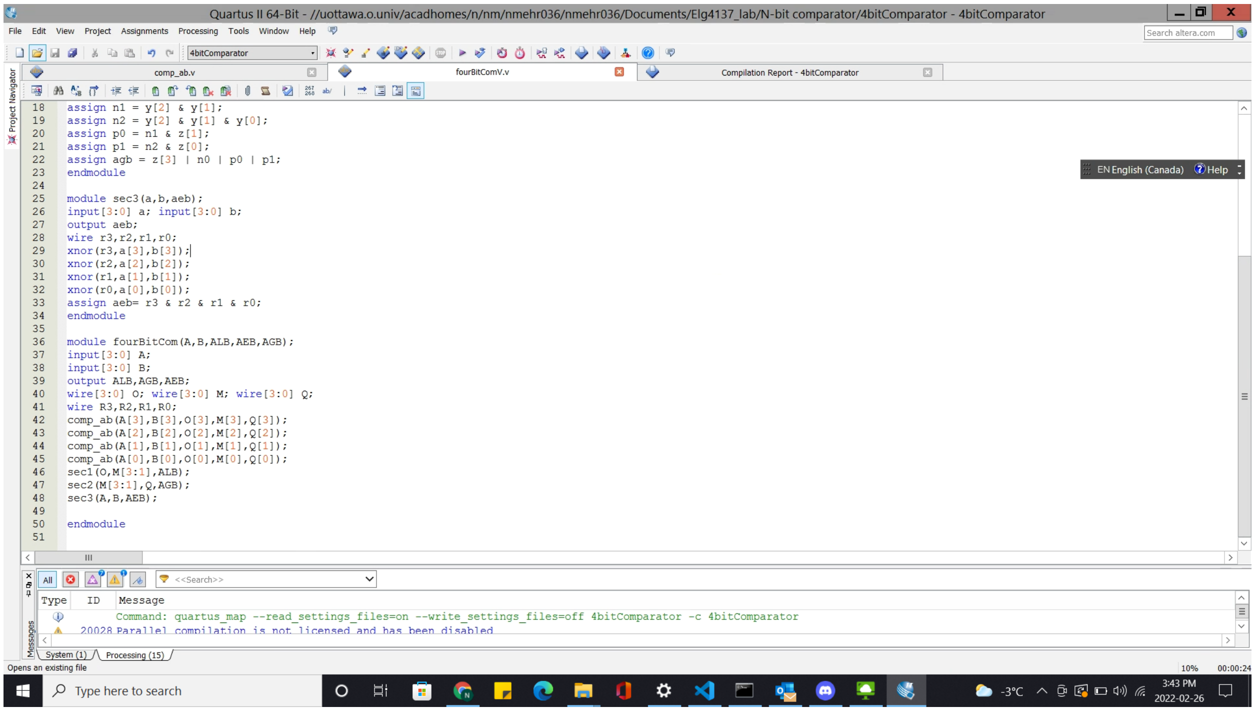


4-bit Comparator Verilog Program


Quartus II 64-Bit - //uottawa.o.univ/acadhomes/n/nm/nmehr036/nmehr036/Documents/Elg4137_lab/N-bit comparator/4bitComparator - 4bitComparator
File Edit View Project Assignments Processing Tools Window Help
4bitComparator
comp_ab.v
fourBitComV.v
Compilation Report - 4bitComparator
EN English (Canada) Help
All
<<Search>>
System (1)
Processing (15)
10%
00:00:24
Type here to search
-3°C
3:42 PM
2022-02-26

```
module sec1 (X,Y,alb);
input [3:0] X; input [2:0] Y;
output alb;
wire N0,N1,N2,P0,P1;
assign N0 = Y[2] & X[2];
assign N1 = Y[2] & Y[1];
assign N2 = Y[2] & Y[1] & Y[0];
assign P0 = N1 & X[1];
assign P1 = N2 & X[0];
assign alb = X[3] | N0 | P0 | P1;
endmodule

module sec2 (y,z,agb);
input [3:0] z; input [2:0] y;
output agb;
wire n0,n1,n2,p0,p1;
assign n0 = y[2] & z[2];
assign n1 = y[2] & y[1];
assign n2 = y[2] & y[1] & y[0];
assign p0 = n1 & z[1];
assign p1 = n2 & z[0];
assign agb = z[3] | n0 | p0 | p1;
endmodule

module sec3(a,b,aeb);
input[3:0] a; input[3:0] b;
output aeb;
wire r3,r2,r1,r0;
xnor(r3,a[3],b[3]);
xnor(r2,a[2],b[2]);
xnor(r1,a[1],b[1]);
xnor(r0,a[0],b[0]);
assign aeb= r3 & r2 & r1 & r0;
endmodule
```

```
Type  ID    Message
            Command: quartus_map --read_settings_files=on --write_settings_files=off 4bitComparator -c 4bitComparator
      20028 Parallel compilation is not licensed and has been disabled
```

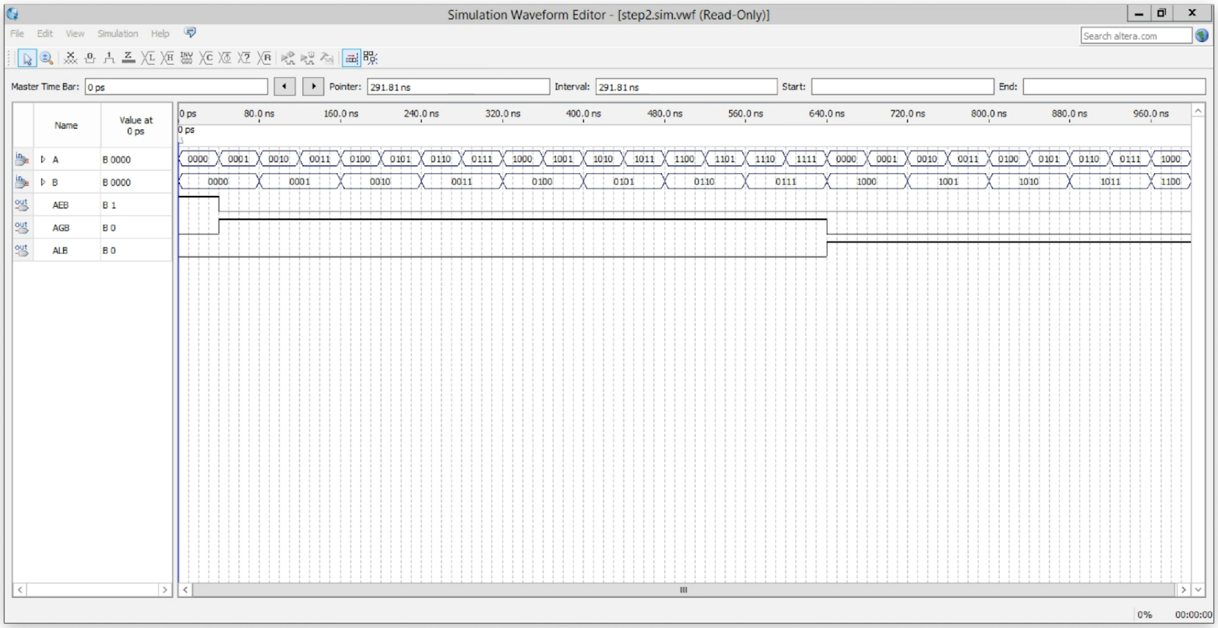

Quartus II 64-Bit - //uottawa.o.univ/acadhomes/n/nm/nmehr036/nmehr036/Documents/Elg4137_lab/N-bit comparator/4bitComparator - 4bitComparator
File Edit View Project Assignments Processing Tools Window Help
4bitComparator
comp_ab.v
fourBitComV.v
Compilation Report - 4bitComparator
EN English (Canada) Help
All
<<Search>>
System (1)
Processing (15)
Opens an existing file
10%
00:00:24
Type here to search
-3°C
3:43 PM
2022-02-26

```
assign n1 = y[2] & y[1];
assign n2 = y[2] & y[1] & y[0];
assign p0 = n1 & z[1];
assign p1 = n2 & z[0];
assign agb = z[3] | n0 | p0 | p1;
endmodule

module sec3(a,b,aeb);
input[3:0] a; input[3:0] b;
output aeb;
wire r3,r2,r1,r0;
xnor(r3,a[3],b[3]);
xnor(r2,a[2],b[2]);
xnor(r1,a[1],b[1]);
xnor(r0,a[0],b[0]);
assign aeb= r3 & r2 & r1 & r0;
endmodule
```

```

module fourBitCom(A,B,ALB,AEB,AGB);
input[3:0] A;
input[3:0] B;
output ALB,AGB,AEB;
wire[3:0] O; wire[3:0] M; wire[3:0] Q;
wire R3,R2,R1,R0;
comp_ab(A[3],B[3],O[3],M[3],Q[3]);
comp_ab(A[2],B[2],O[2],M[2],Q[2]);
comp_ab(A[1],B[1],O[1],M[1],Q[1]);
comp_ab(A[0],B[0],O[0],M[0],Q[0]);
sec1(O,M[3:1],ALB);
sec2(M[3:1],Q,AGB);
sec3(A,B,AEB);

endmodule

```

```
Type  ID    Message
            Command: quartus_map --read_settings_files=on --write_settings_files=off 4bitComparator -c 4bitComparator
      20028 Parallel compilation is not licensed and has been disabled
```

4-bit Comparator Waveform



Master Time Bar: 0 ps

Pointer: 291.81 ns

Interval: 291.81 ns

Start:

End:

Name	Value at 0 ps
A	B 0000
B	B 0000
AEB	B 1
AGB	B 0
ALB	B 0

After simulation of the 4-bit comparator all results were accurate with what was expected. Looking at the waveform diagram above it is clear when A is greater than B, AGB is active. When A is less than B, ALB is active and when A is equal to B, AEB is active.