University of Ottawa
School of Information Technology and Engineering

Laboratory Manual
For
Principles & Application of VLSI Design
ELG4132A

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Pre-requisite:

1. Go through the following link to learn about Quartus II:

   http://www.eecg.toronto.edu/~zvonko/AppendixB_quartus.pdf

2. Each group has to hand in a pre-lab report before the lab starts (one report for each group), which should include the followings:

   a. The K-map and logical expression according to the truth table for Part I.

   b. A Verilog program (compilation and simulation) of 1-bit comparator to be used in Part II.

3. In this lab, we will design two simple combinational circuits.

   a. Part I: **Design of a Priority Encoder**

Tips

A 3-bit **priority encoder** circuit basically converts the 3-bit input into a binary (2-bit) representation. Theoretically, if the input n^{th} bit is active, all lower inputs (n-1 … 0) are ignored. In this lab, we define the following priority index.

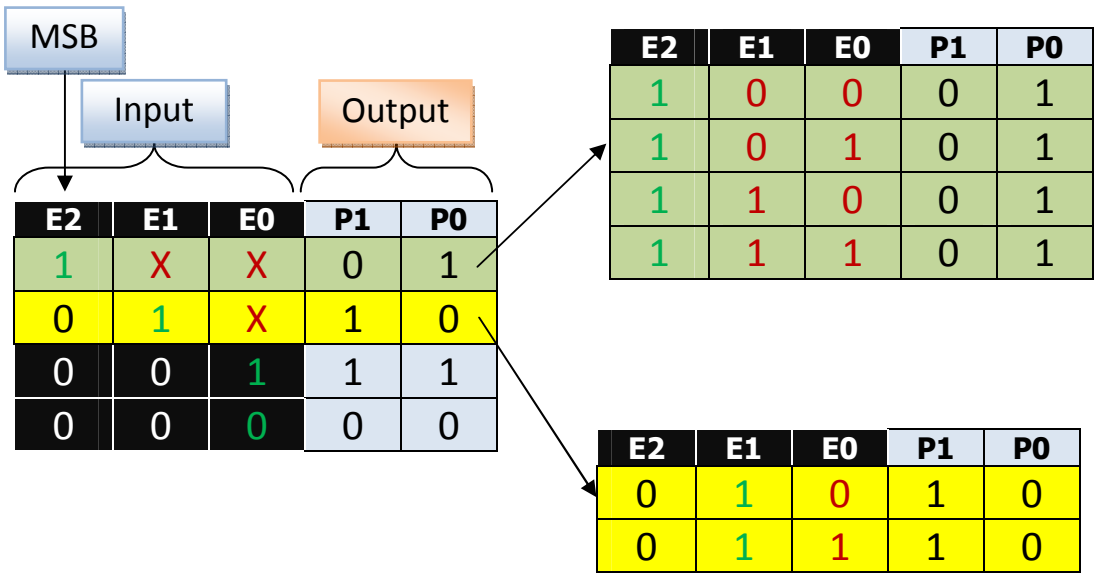

Fig. 1. (3:2) priority encoder

After simplifying the above K-map, a sample design yields the following figure

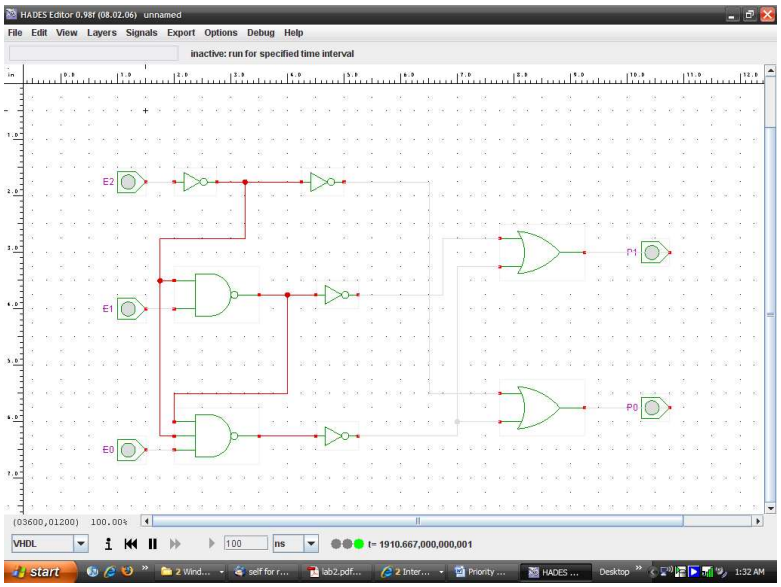

Fig. 2. Schematic diagram of the priority encoder shown in Figure 1.

Develop a Verilog behavior model for the above priority encoder. Simulate the model using Altera software.

Note: You might end up with different schematic diagrams that still produce the same output. Show your design steps in details.

b. Part II: **Design of an N-bit comparator**

An N-bit comparator compares two N-bit numbers A and B and indicates whether the numbers are equal or which of the numbers is greater. Hence there are two N-bit inputs to the comparator, A and B, and three one-bit outputs,

$$A < B,\ A = B,\ A > B.$$

Among several design approaches is to design a 1-bit comparator and then extend it to design an N-bit comparator.

Develop a Verilog behavior model for a 4-bit comparator using the 1-bit comparator you have designed earlier. Simulate the model using Altera software.

Tips

We will design a circuit with the following I/O characteristics

a) Inputs: two numbers, A and B, as bit-strings e.g. $A_{n-1}\ldots A_1 A_0$ and $B_{n-1}\ldots B_1 B_0$

b) Outputs: A < B, A = B, A > B.

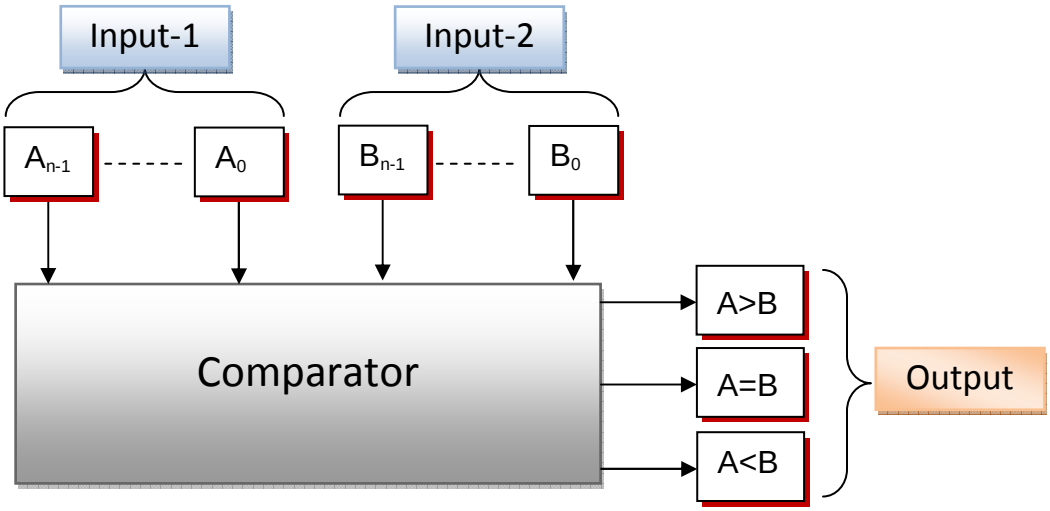

Fig. 3. N-bit comparator

1-bit comparator

The key to designing a comparator is to recognize that more significant bits override all less significant ones. For example,

$$10000_b > 01111_b$$

We start comparing the digits from the MSB and then the subsequent more significant bits.

We design a 1-bit comparator with the following four inputs:

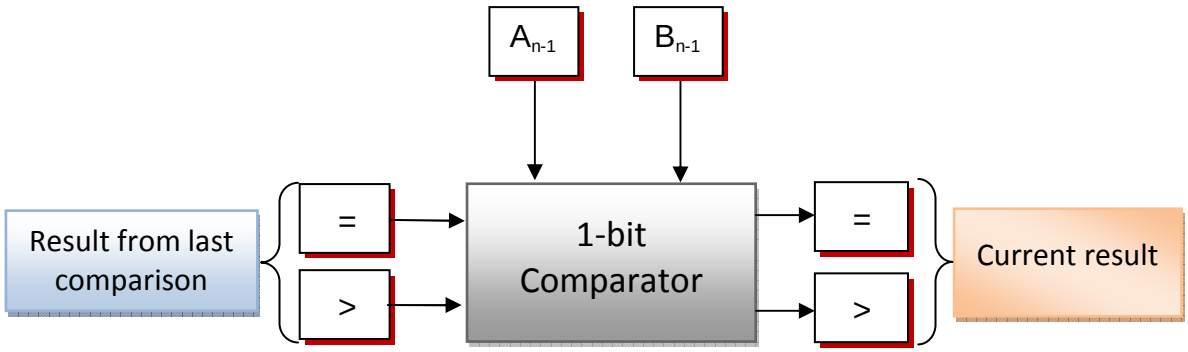

Fig. 4. 1-bit comparator

Then cascade them in serial fashion to form N-bit comparator by connecting the output of each block with the input of the next block. You may use inverters and 2 and 3-input AND, NAND, OR, NOR, exclusive-OR and exclusive-NOR gates.

4. This lab is a one-week lab. So you are supposed to finish the lab within the lab session. I also appreciate that you finish most of the work before the lab, and only demonstrate your work in the lab.