Analog Assignment 5

EE23BTECH11044 - Nimal Sreekumar

I. IC 555 Timer Design

A. Monostable Mode

Design an IC 555 timer in monostable mode for a variable pulse width ranging from 200 µs to 5 ms.

Time Period Equation:

$$T = RC\ln(3) \tag{1}$$

Using this equation to find R values for $C = 0.1\mu$F:

$$R = 1.8k\Omega \quad \textbf{for } 200\mu s$$

$$R = 45k\Omega \quad \textbf{for } 5ms$$

Circuit Diagram:

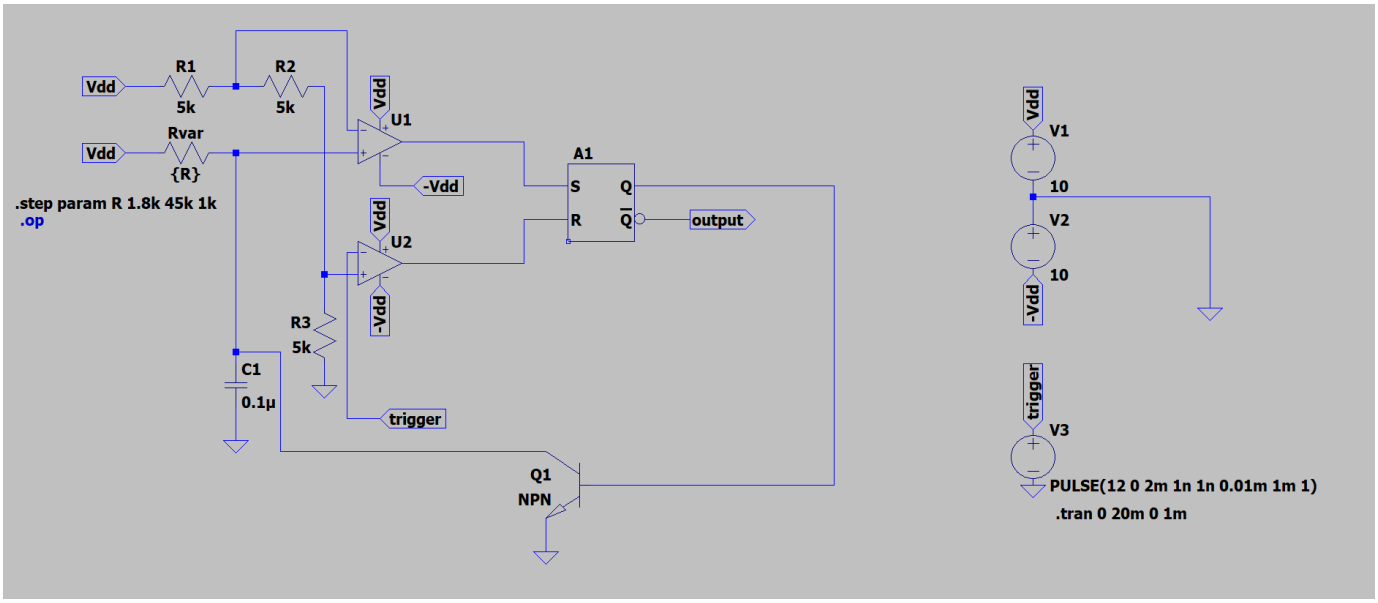

Fig. 0: Monostable Mode Circuit Diagram

Plot for Various Values of R:

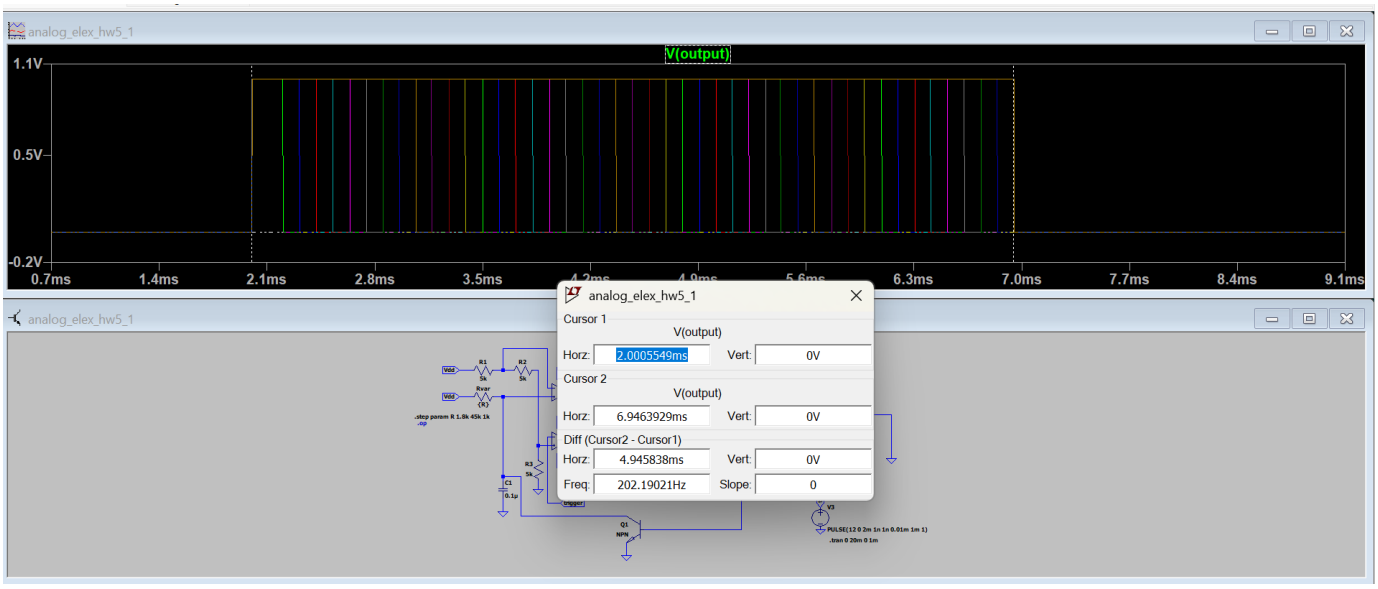

Fig. 0: Time Period Variation with Resistance

For $R = 1.8k\Omega$:

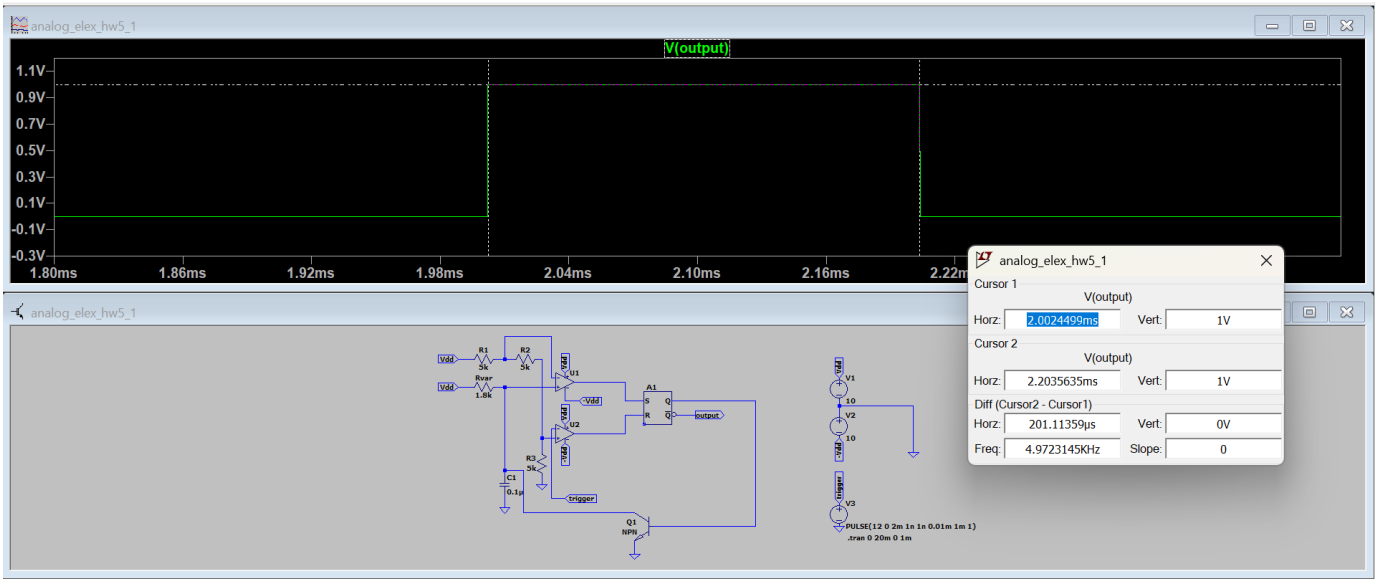

Fig. 0: Output Waveform for $R = 1.8k\Omega$

For $R = 45k\Omega$:

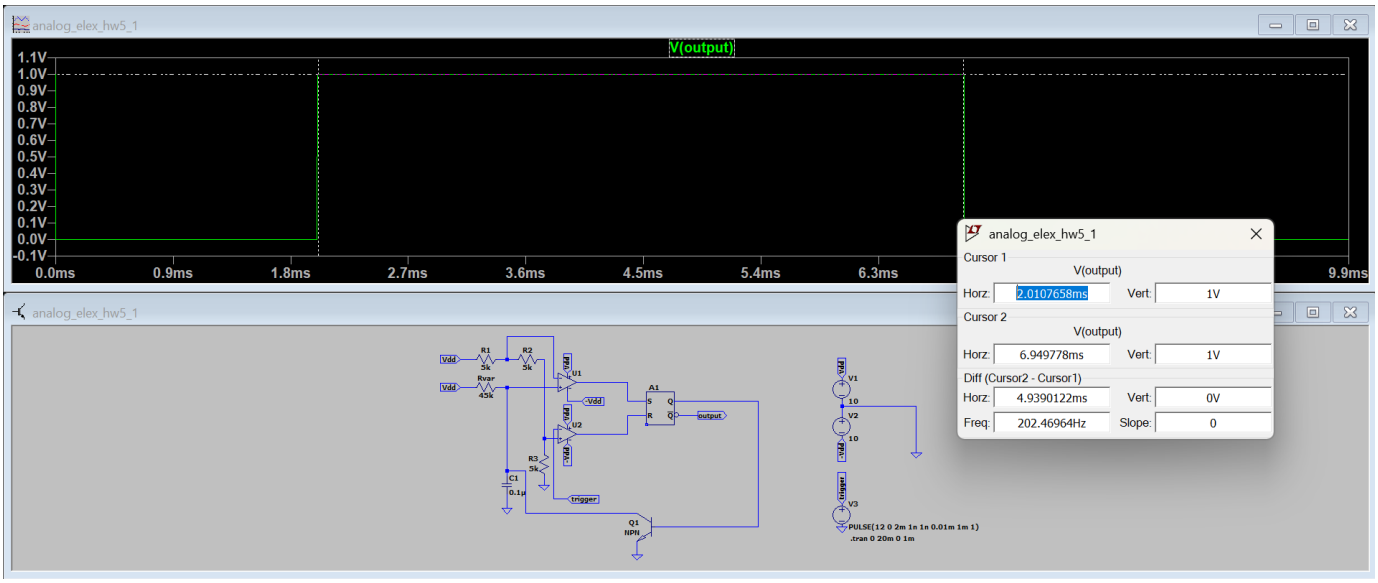

Fig. 0: Output Waveform for $R = 45k\Omega$

B. Astable Mode

Design an IC 555 timer in astable mode for a duty cycle of 75% with the fundamental frequency varying from 2 kHz to 20 kHz. Also, find the maximum achievable frequency.

Duty Cycle Relation:

$$\frac{T}{T_{on}} = 0.75 \tag{2}$$

For $T = 500\mu s$:

$$T_{on} = 375\mu s$$
$$T_{off} = 125\mu s$$

Using the formulas:

$$T_{on} = (R_1 + R_2)\ln(2)C \tag{3}$$
$$T_{off} = R_2 \ln(2)C \tag{4}$$

Taking $C = 0.1\mu$F, we find:

$$R_1 = 3.6k\Omega$$
$$R_2 = 1.8k\Omega$$

Circuit Diagram:

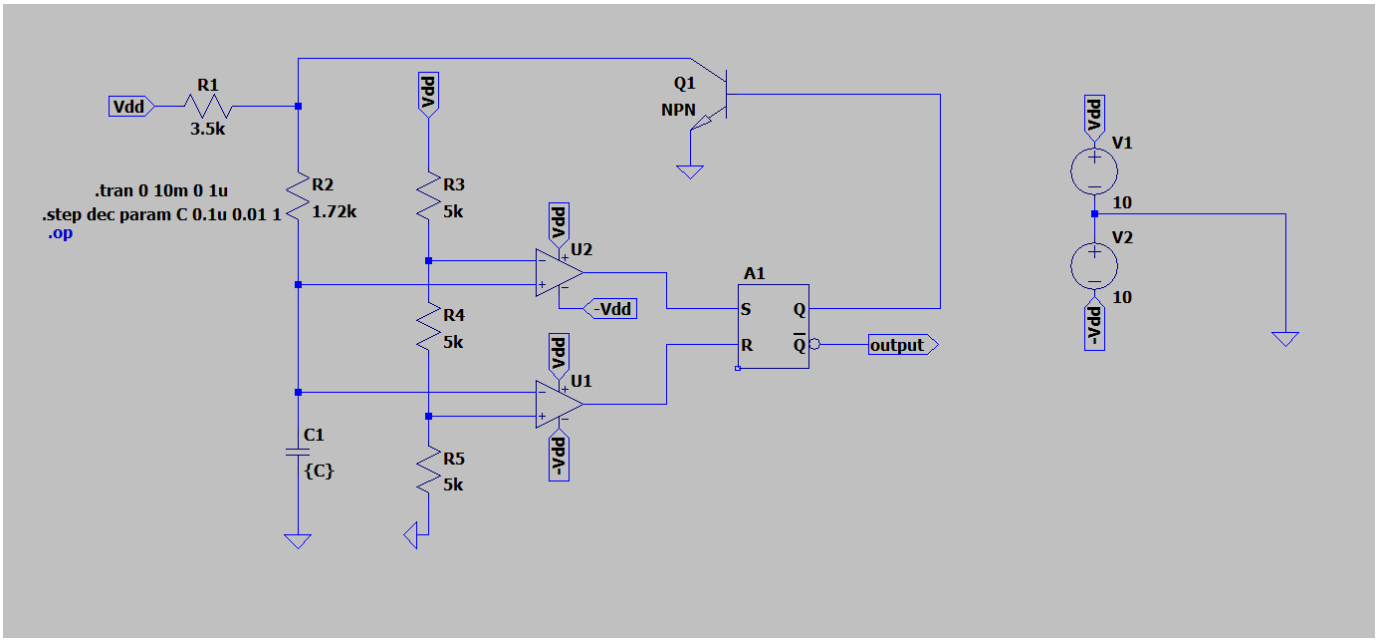

Fig. 0: Astable Mode Circuit Diagram

Frequency Variation Plot with Different C Values:

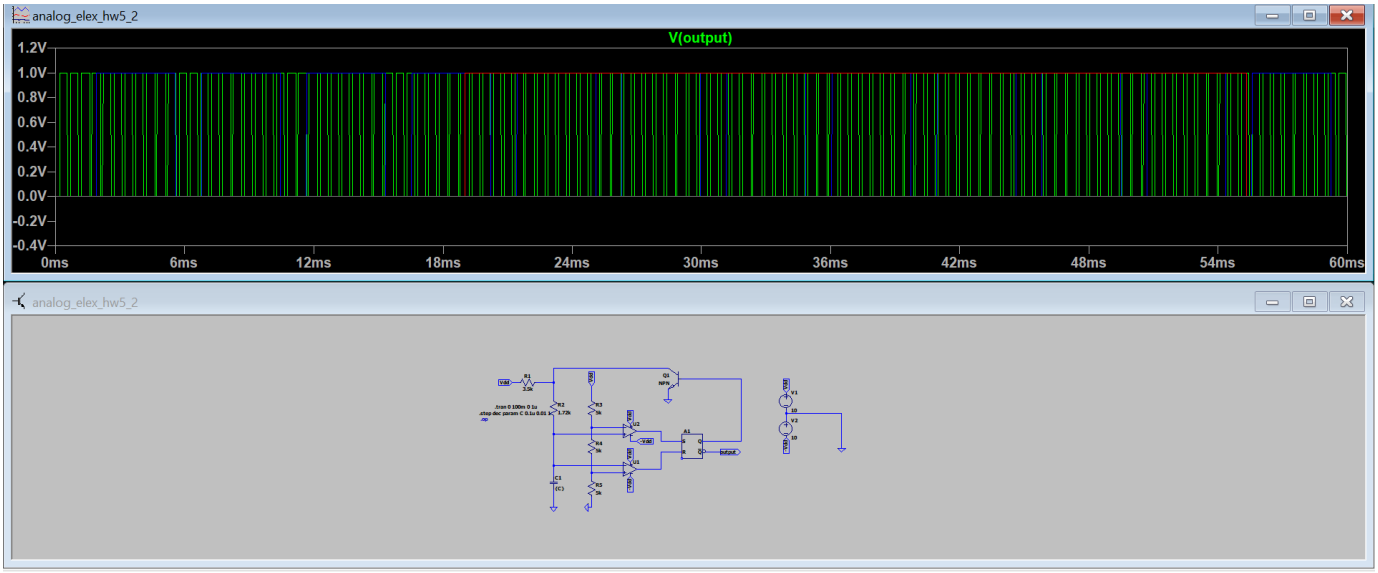

Fig. 0: Frequency Variation with Component Values

Output Waveform 1 with Time Interval 125us:

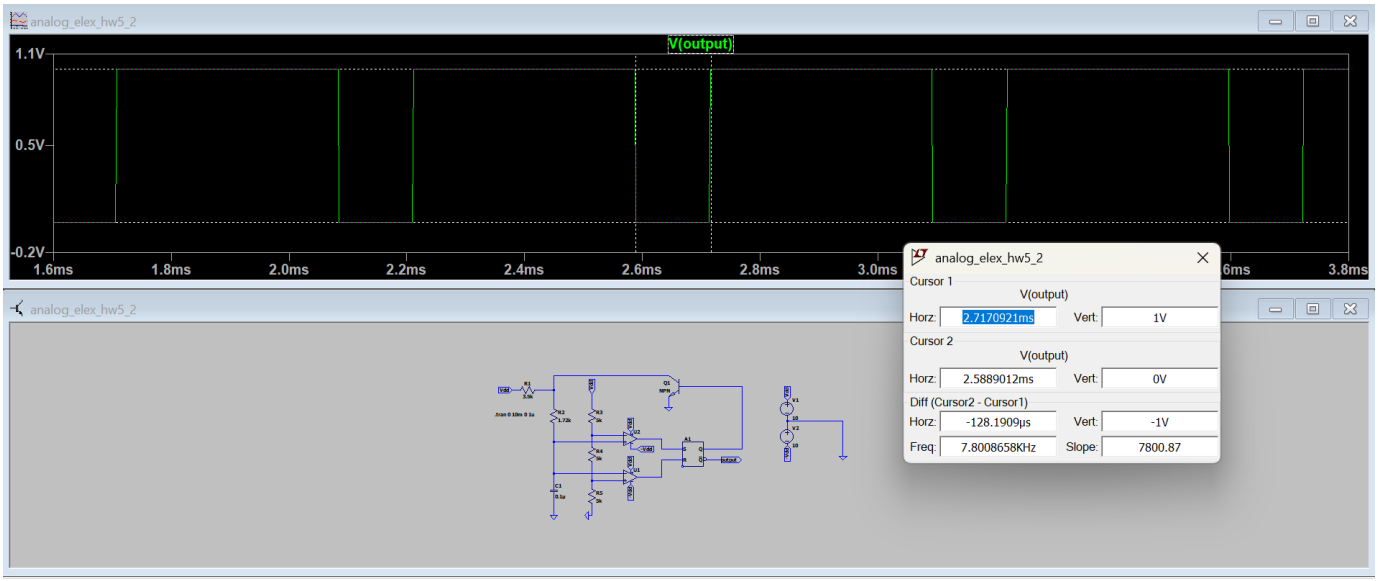

Fig. 0: Output Waveform for a Selected Frequency

Output Waveform 2 with Time Interval 375us:

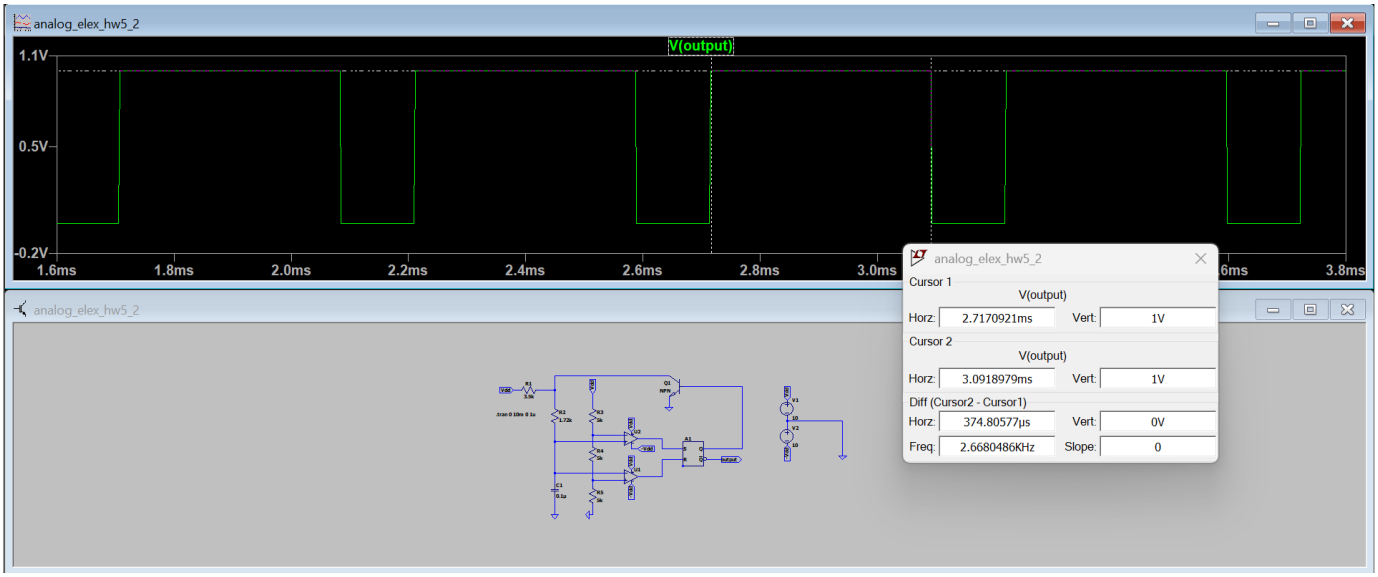

Fig. 0: Output Waveform for Another Selected Frequency

C. *Bistable Mode*

The bistable mode is similar to monostable mode but uses the reset pin to control the output state. The trigger pin is set at $t = 2$ms to start pulse generation. When the reset pin goes high, it resets the input to the S pin, making the output low.

Circuit diagram

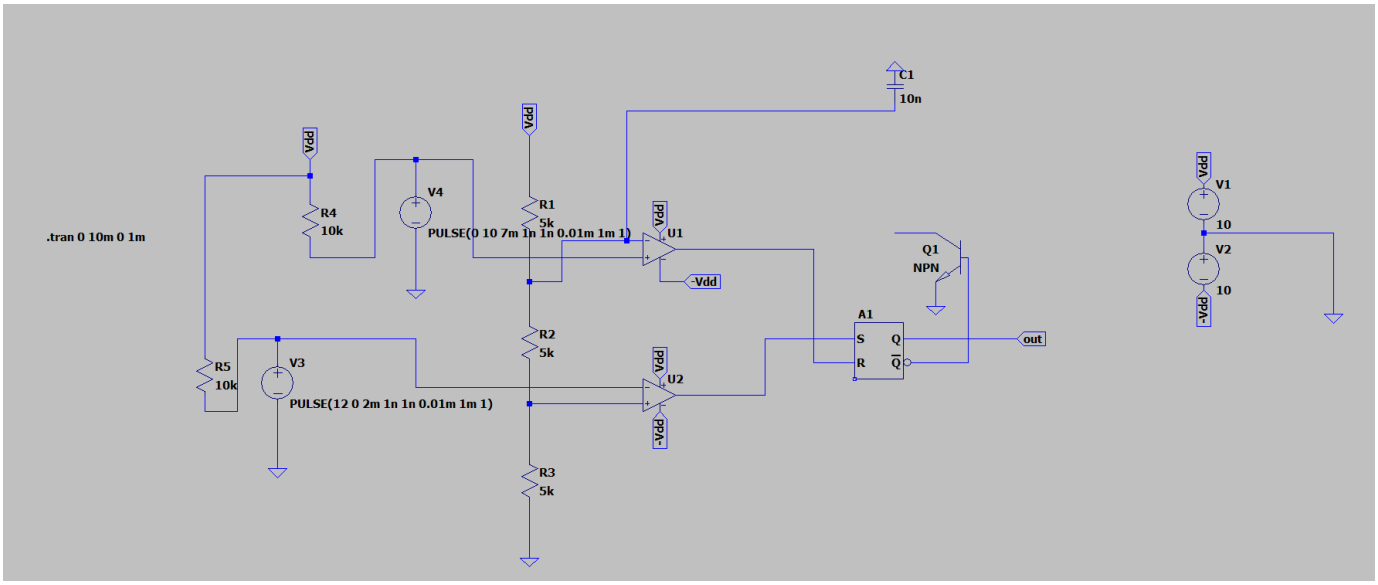

Fig. 0: Bistable Mode Output Waveform 1

Output Waveform:

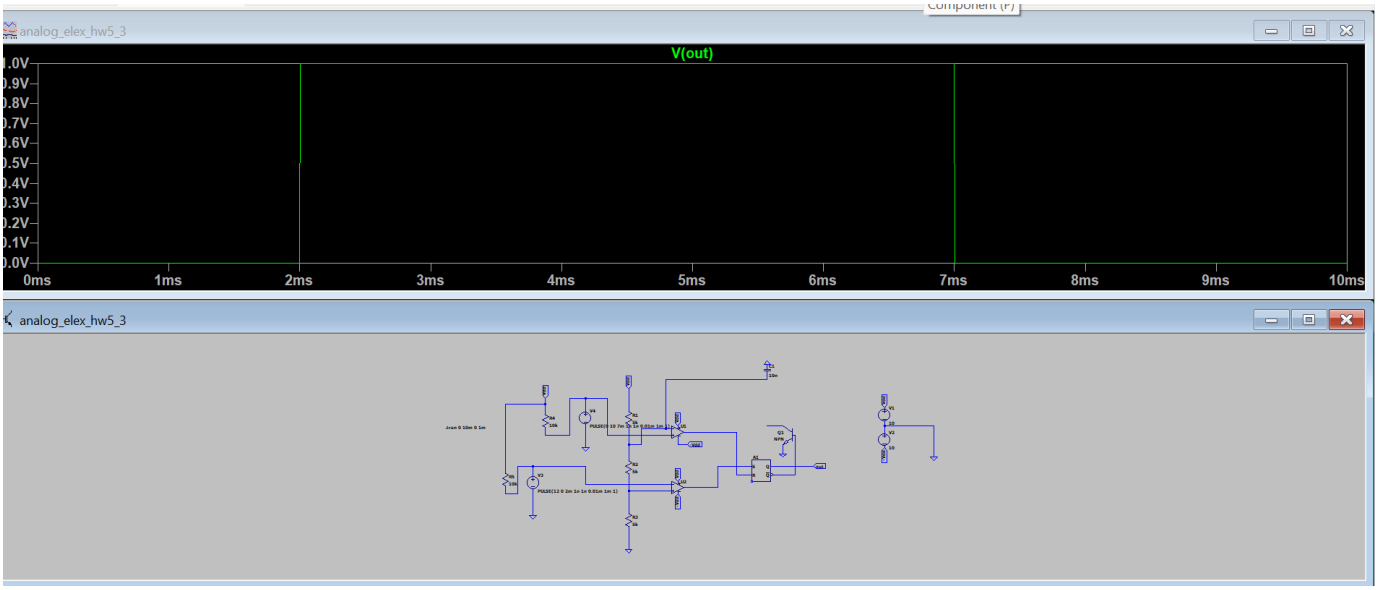

Fig. 0: Bistable Mode Output Waveform 2

II. LDO Design Using MOSFETs

A. *pMOS and nMOS Based LDOs*

Design a pMOS and nMOS MOSFET-based LDO with $V_{ref} = 3V$ and an output voltage range from 6V to 10V (variable). Determine the minimum V_{in} required for the entire range, given that the load current is 200µA and the transistor aspect ratio (W/L) is 10/1.

Voltage Divider Relation:

$$V_{out} = V_{ref}\left(\frac{R_1 + R_2}{R_2}\right) \tag{5}$$

Given $V_{ref} = 3V$:

$$\text{For } V_{out} = 6V, \quad R_1 = R_2$$
$$\text{For } V_{out} = 10V, \quad R_1 = 2.33R_2$$

Since $I_{DS} = 200A$:

$$V = IR_2 \tag{6}$$

Choosing $R_2 = 15k\Omega$, we determine that:

$$V_{in} \geq V_{GS,\text{max}} + V_{out} \geq 15V(\text{approx}) \tag{7}$$

Circuit Diagram:

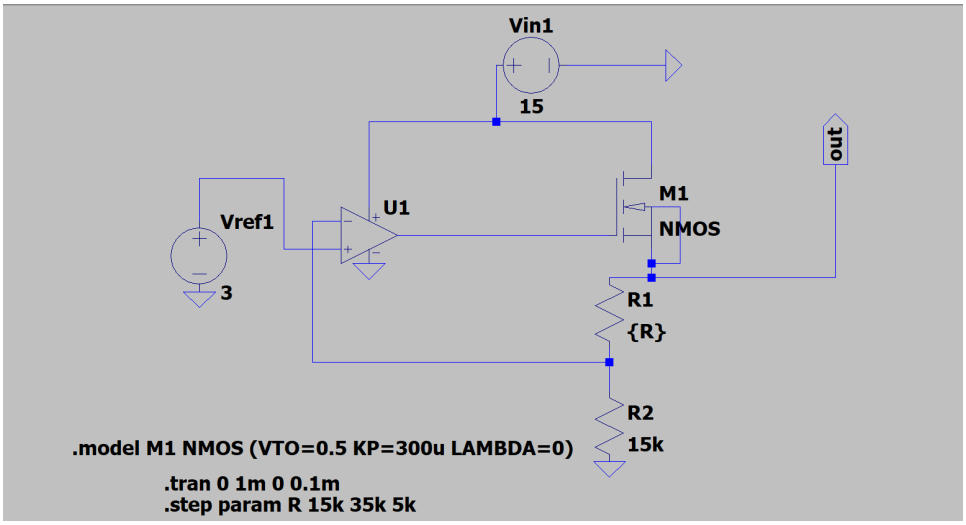

Fig. 0: LDO Circuit Diagram

Different Output Voltages for Various R Values:

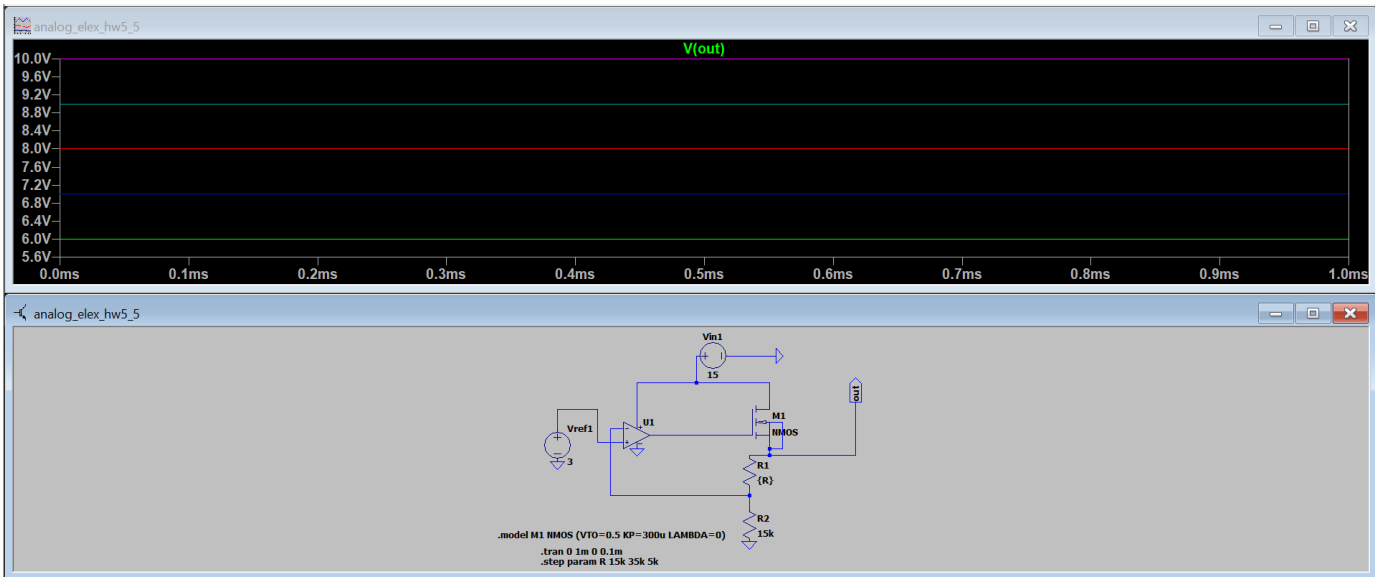

Fig. 0: Output Voltage Variations with Different R Values

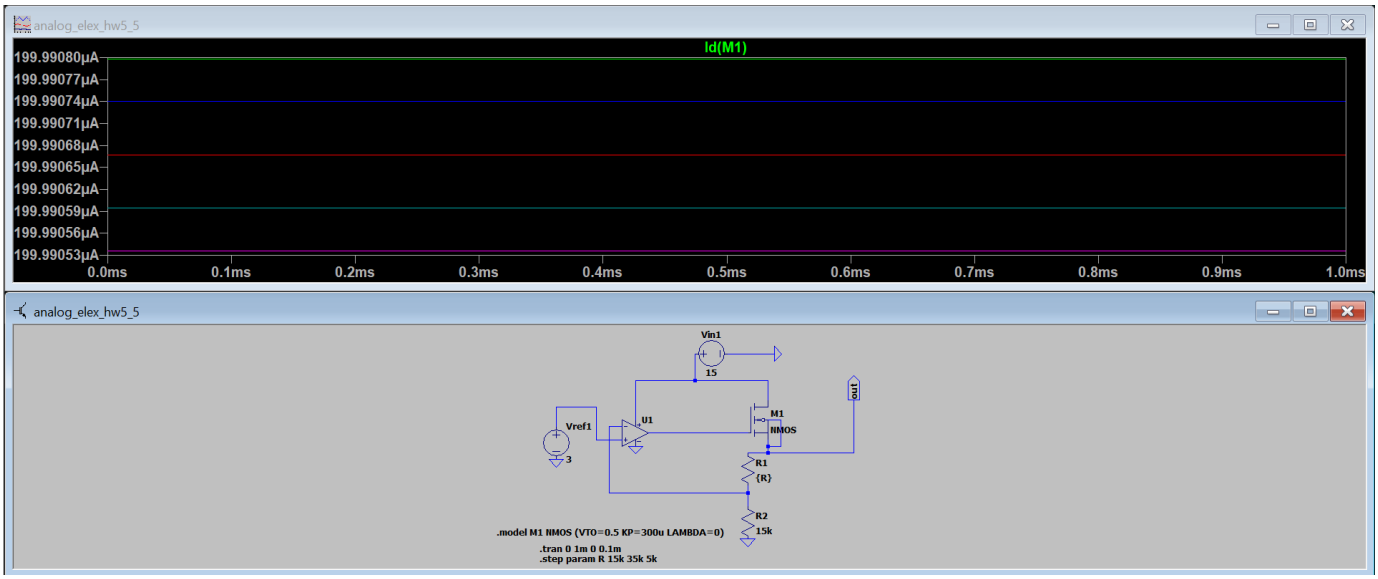

Fig. 0: I Variations with Different R Values