Analog Assignment 2

BY EE23BTECH11044 - Nimal Sreekumar

1) (a)Design (architecture and W/L ratio) a common source amplifier for a minimum small signal incremental gain of 25. Design the circuit for a maximize input and output swing for a given DC bias current of 100uA. Design the circuit with the proper biasing circuit.

ANSWER :

HOW THE CIRCUIT WAS MODELED:

In the question I_{DS} is 100 μA , β_n is 300 $\mu A/V^2$ and V_{Dsat} is 160 mV. Using these, we can now determine the $\frac{W}{L}$ ratio for nMOS, by

$$I_{DS} = \beta_n \times \frac{W}{L} \times V_{Dsat}$$

$$100\mu A = 300\mu A/V^2 \times \frac{W}{L} \times 160mV$$

$$\frac{W}{L} = 26$$

After substituting the values, we get the $\frac{W}{L}$ ratio to be 26. Now assume that L is $0.18\mu m$ (180nm technology); then W is $4.68\mu m$.

Next, we find a suitable gate voltage, V_{GS}. It is known that V_{Dsat} is 160 mV, then

$$V_{Dsat} = V_{GS} - V_{to}$$

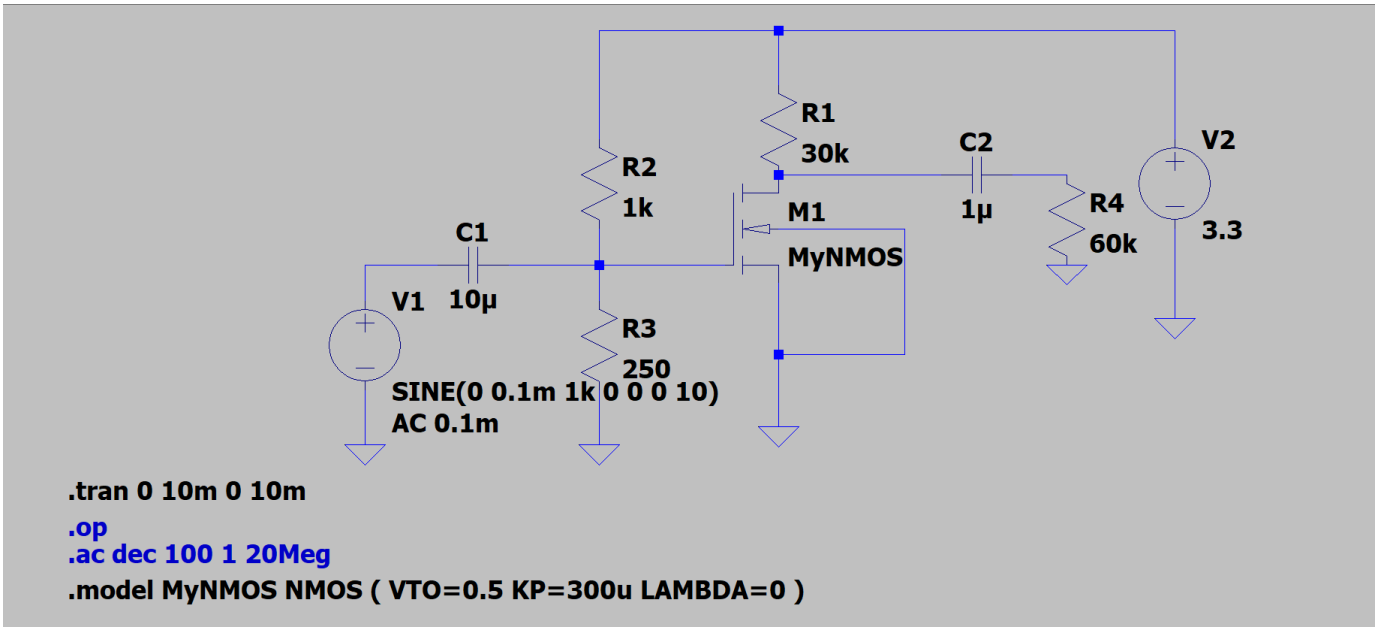
$$160mV = V_{GS} - 0.5V$$

From this we obtain the value of V_{GS} to be 660 mV.

We use a voltage divider circuit to make the gate voltage equal 660mV (I choose two resistors one of 1K and the other 250 Ω).

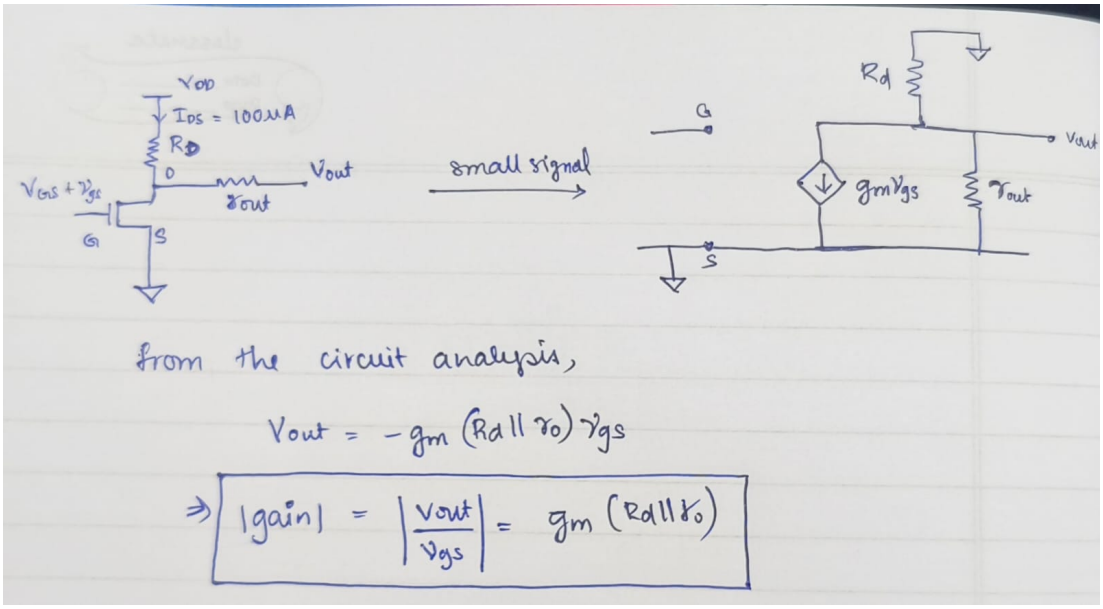
$$\frac{3.3 - V_{GS}}{R2} = \frac{V_{GS}}{R1}$$

$$\frac{R2}{R1} = 4$$



Now we have to provide the small signal Ac voltage that has to be amplified. An AC sinusoidal voltage source of 0.1mV of amplitude and a frequency of 1KHz is taken. A capacitor of 10μF has been used to filter the DC components from the small signal.

We have to get a gain of 25, we also know that from small signal modeling, the gain will be



$$|gain| = 25 = gm \times (R_D||r_{out})$$

where gm is,

$$gm = \beta \times \frac{W}{L} \times V_{Dsat}$$

$$gm = 300\mu A/V^2 \times 26 \times 160mV$$

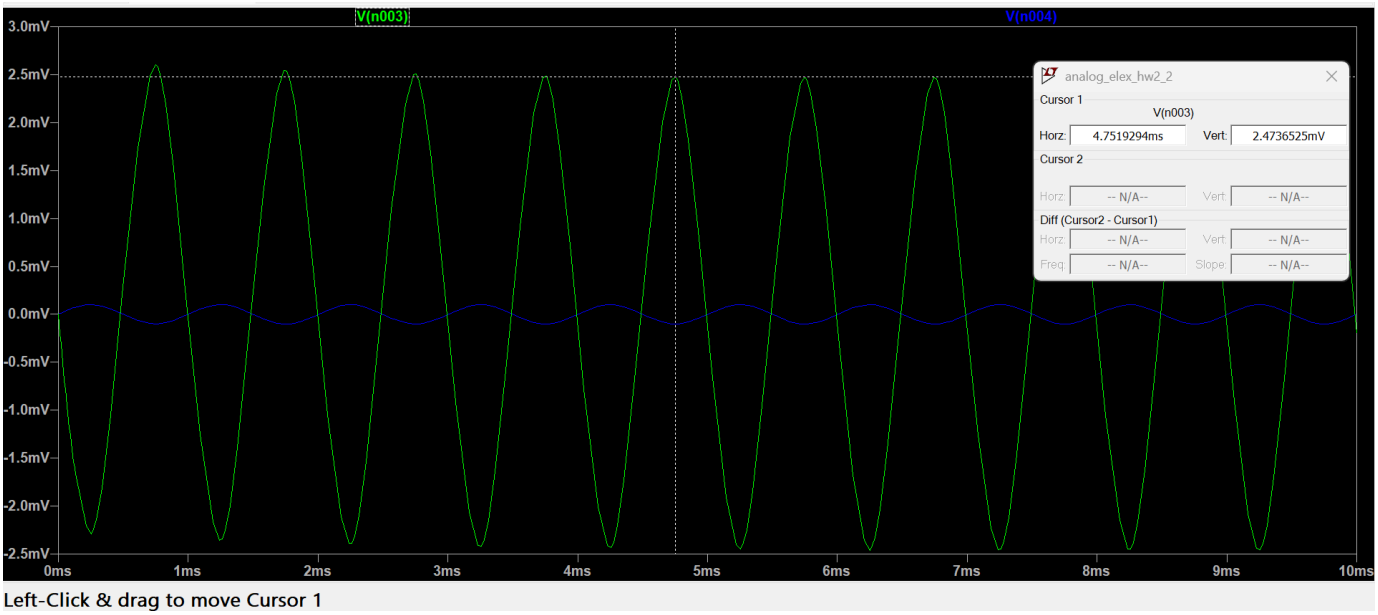
$$gm = 1248\mu A/V$$

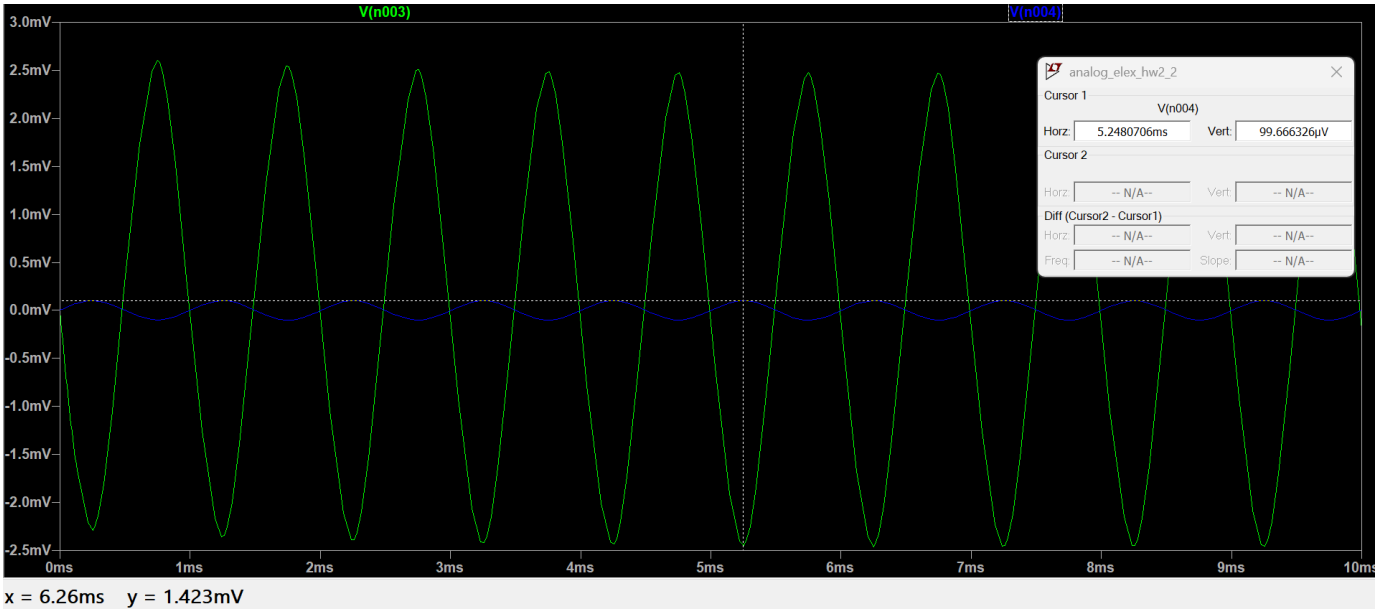
The next step is to just calculate a suitable $(R_D||r_{out})$. I took R_D as 30K, therefore, solving the gain equation, we get r_{out} to be 60K.

$$|gain| = gm \times (R_D||r_{out})$$

$$|gain| = 1248\mu \times 20K = 24.96$$

PLOTS REPRESENTING INPUT AND OUTPUT :





From the plots, it is clear that :

$$|gain| = \frac{Vout}{Vin} = \frac{2.47mV}{99.66\mu V} = 24.7$$

(b) Plot the frequency response of the amplifier and find its 3dB frequency (or BW) and Unity Gain Bandwidth (UGB).

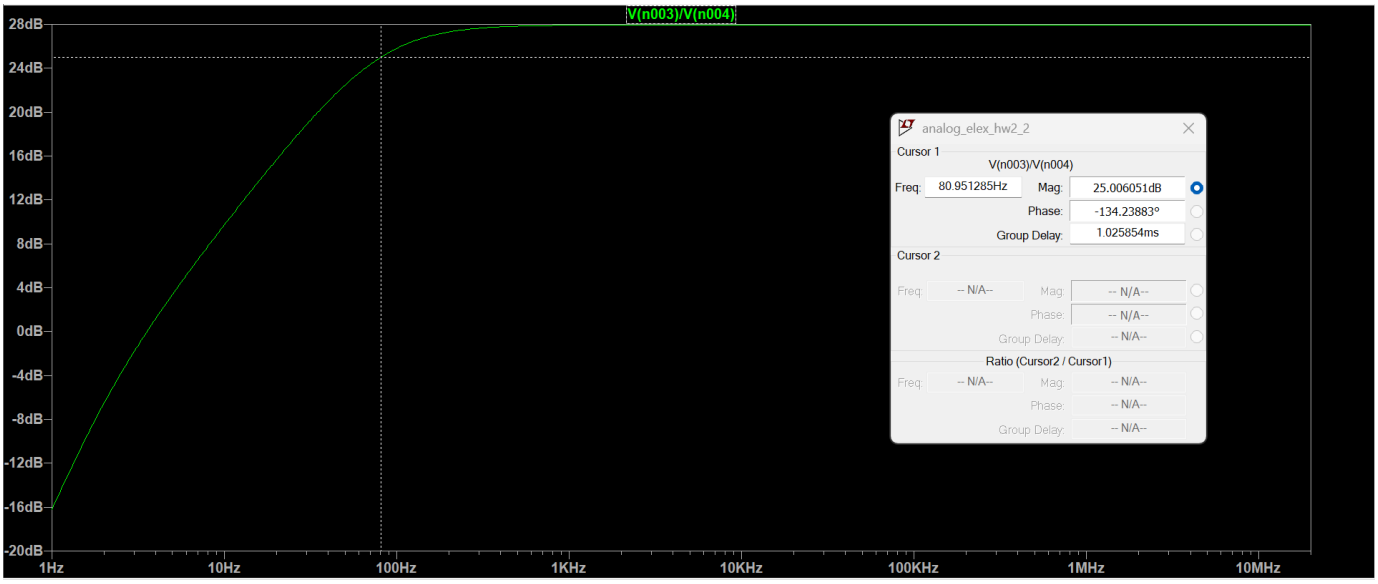
ANSWER : 3dB frequency is the frequency at which the voltage becomes $\frac{1}{\sqrt{2}}$ times the peak voltage. It is also called the cut-off frequency. From the plots

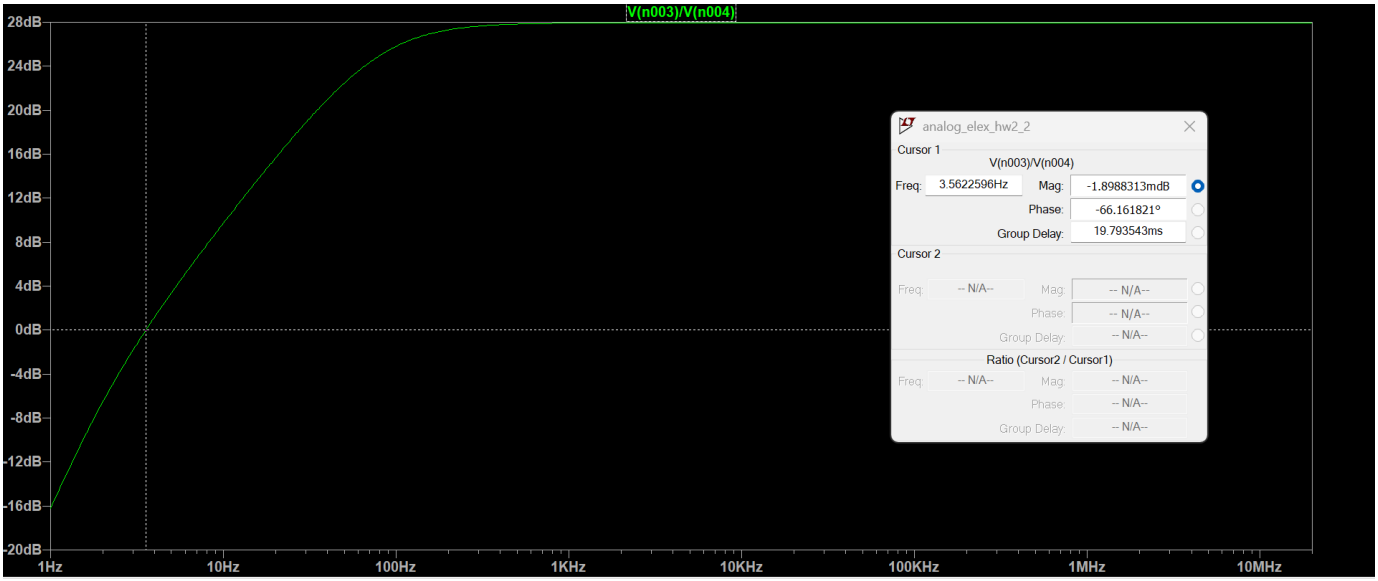
$$f_{cut-off} = 80.95Hz$$

$$B.W = \infty(\text{all values above 80.95Hz})$$

UGB is the frequency at which the gain of an amplifier becomes 1 (0 dB). Here it is :

$$UGB = 3.56Hz$$





(c) Apply a load capacitance of 1pF at the output and find its 3dB frequency (or BW) and Unity Gain Bandwidth (UGB).

ANSWER :

CIRCUIT AFTER CONNECTING LOAD CAPACITOR:

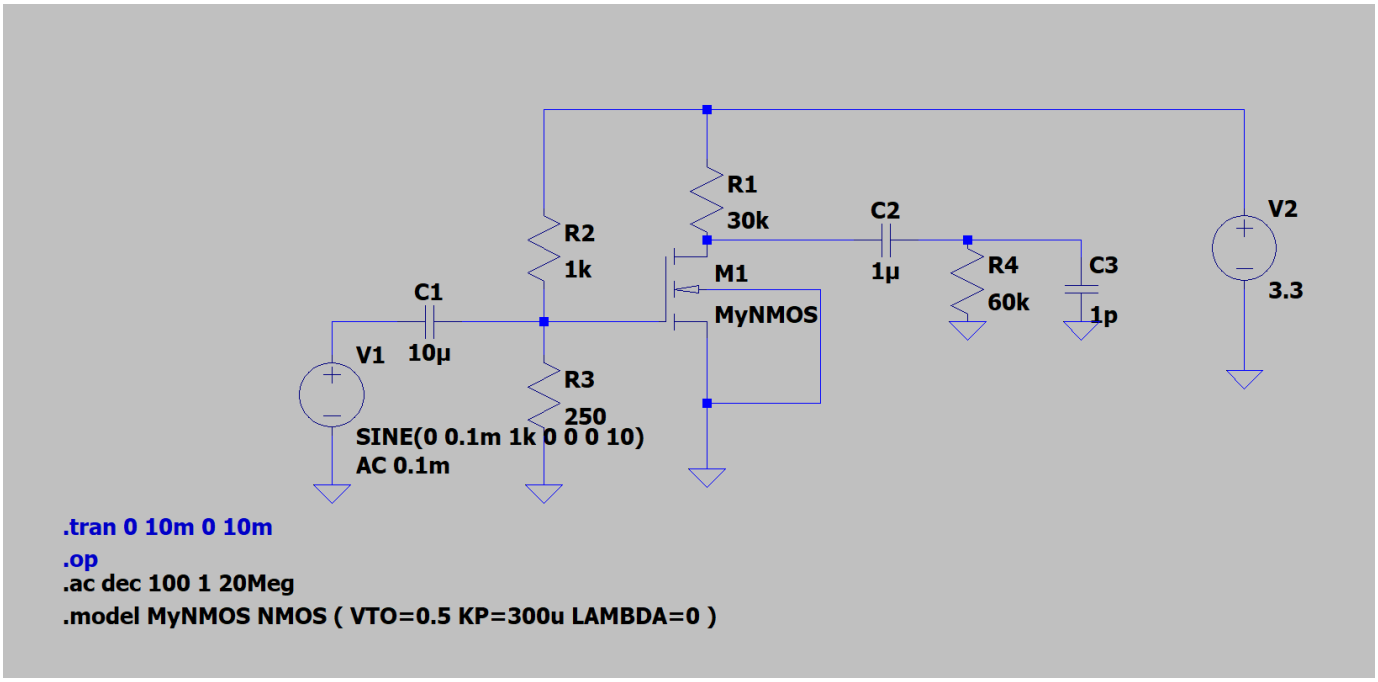
From the plots

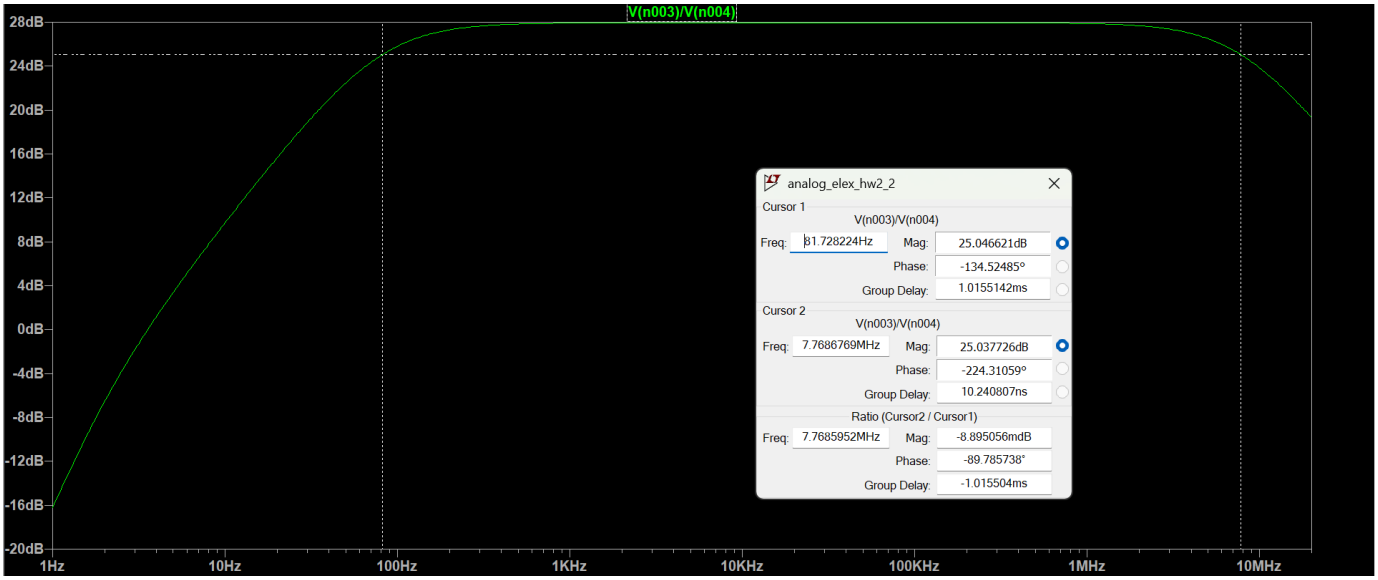
$$f_{cut-off} = 81.72Hz \ \ \& \ \ 7.77MHz$$

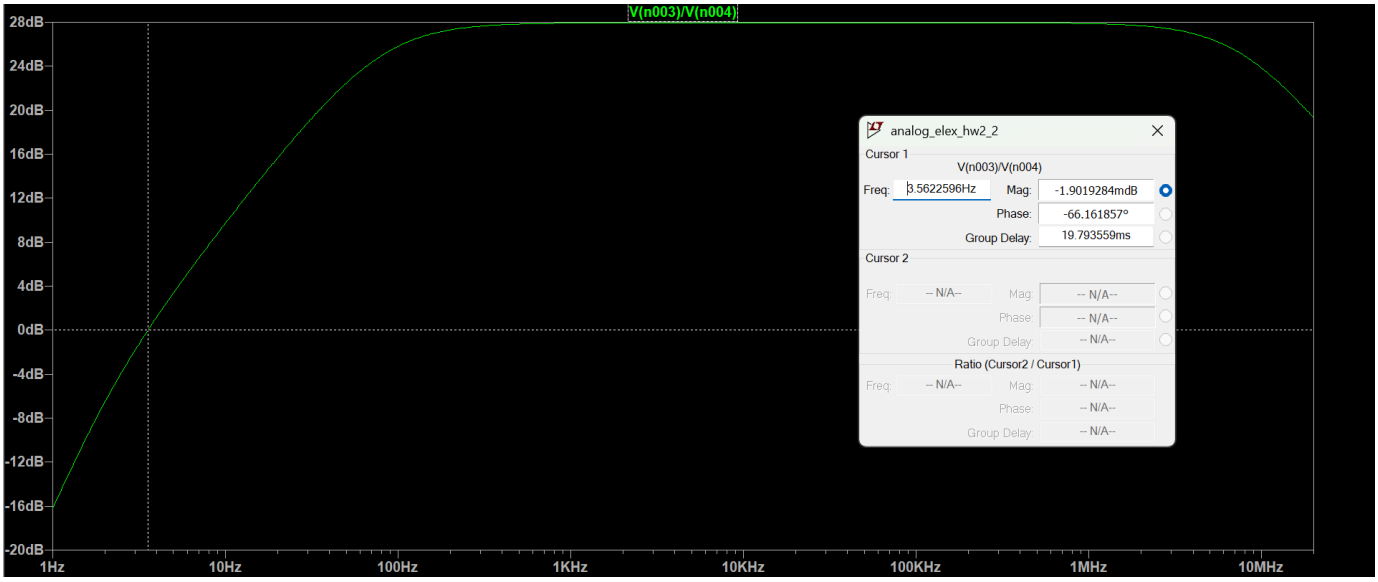
$$B.W = 7769918.28Hz (\text{all values between 81.72Hz and7.77MHz})$$

UGB is the frequency at which the gain of an amplifier becomes 1 (0 dB). Here it is :

$$UGB = 3.56Hz$$






V(n003)/V(n004)
28dB
24dB
20dB
16dB
12dB
8dB
4dB
0dB
-4dB
-8dB
-12dB
-16dB
-20dB
1Hz
10Hz
100Hz
1KHz
10KHz
100KHz
1MHz
10MHz
analog_elex_hw2_2
Cursor 1
V(n003)/V(n004)
Freq: 3.5622596Hz
Mag: -1.9019284mdB
Phase: -66.161857°
Group Delay: 19.793559ms
Cursor 2
Freq: -- N/A--
Mag: -- N/A--
Phase: -- N/A--
Group Delay: -- N/A--
Ratio (Cursor2 / Cursor1)
Freq: -- N/A--
Mag: -- N/A--
Phase: -- N/A--
Group Delay: -- N/A--