

# Software Implementation of (Post-Quantum) Public-Key Cryptography

Curve-Based

Patrick Longa  
Microsoft Research

SPACE 2020

Virtual Conference, December 2020

# Outline

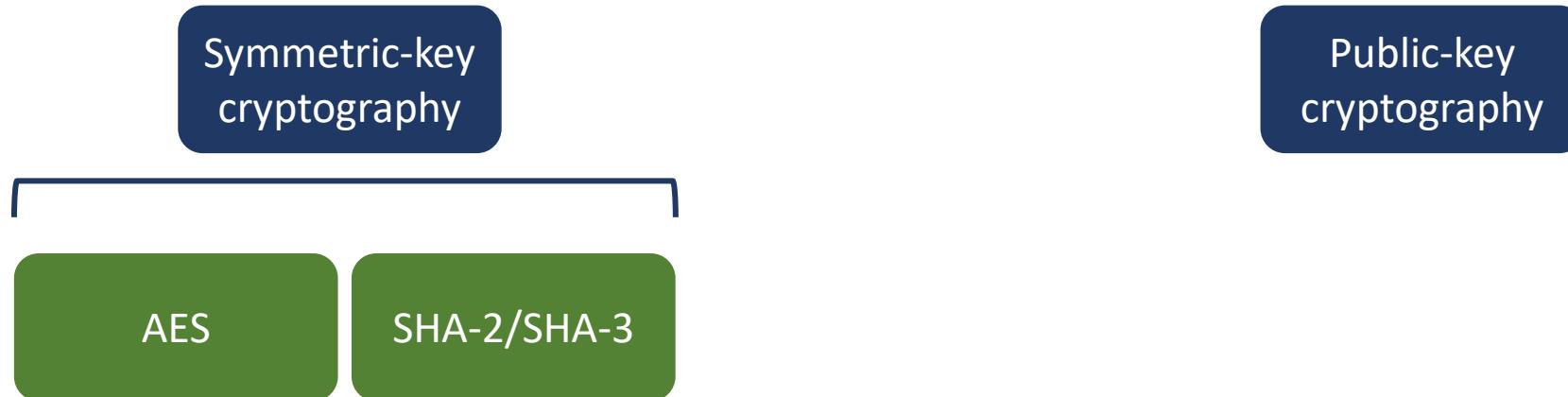
- Preliminaries: public-key cryptography
- (Post-quantum) public-key cryptography
  - Motivation: the quantum menace
- Implementation aspects of PKC
  - Preliminaries: CISC vs RISC, x64 ISA
  - Side-channel attacks: timing and cache attacks
  - Computer representation
  - Computer arithmetic (cases with ECC and SIKE)
  - Modular arithmetic
- The case of ECC
- The case of SIKE

# Cryptography in use today

Symmetric-key  
cryptography

Public-key  
cryptography

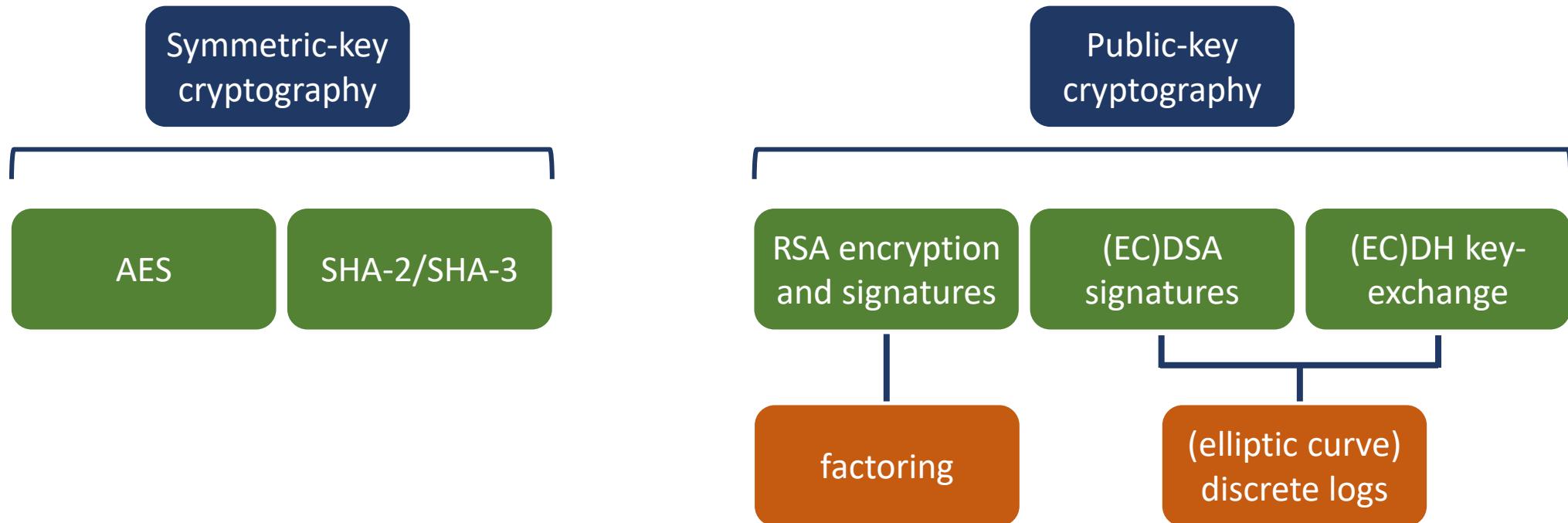
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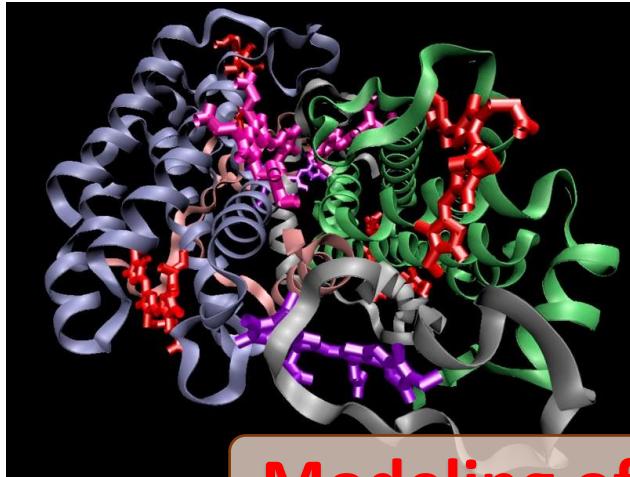
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Widely dominated by number theoretic cryptography.



# Motivation: the quantum menace

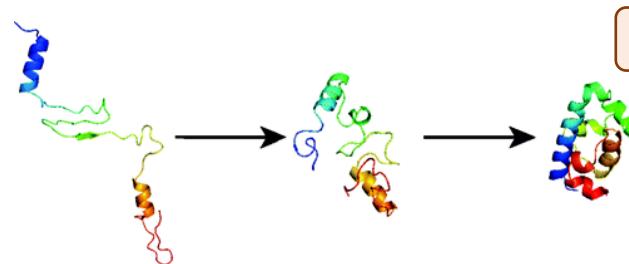
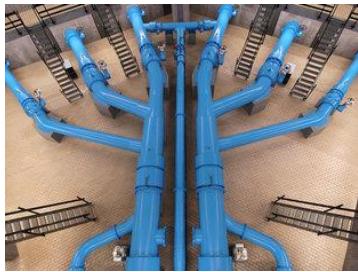
# Quantum computing



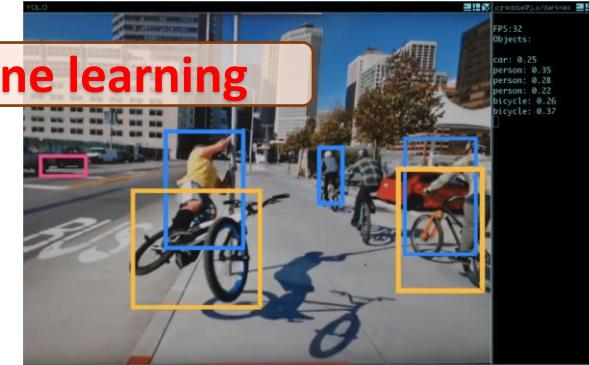
Modeling of nature



Computational optimization



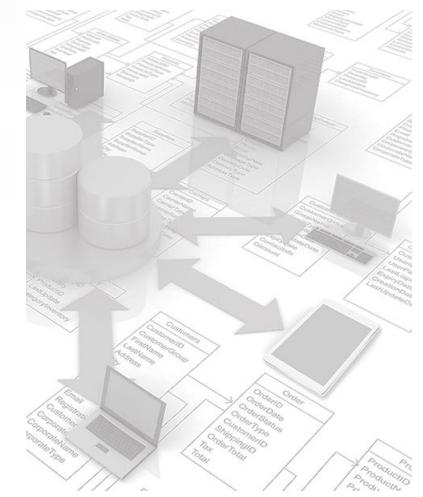
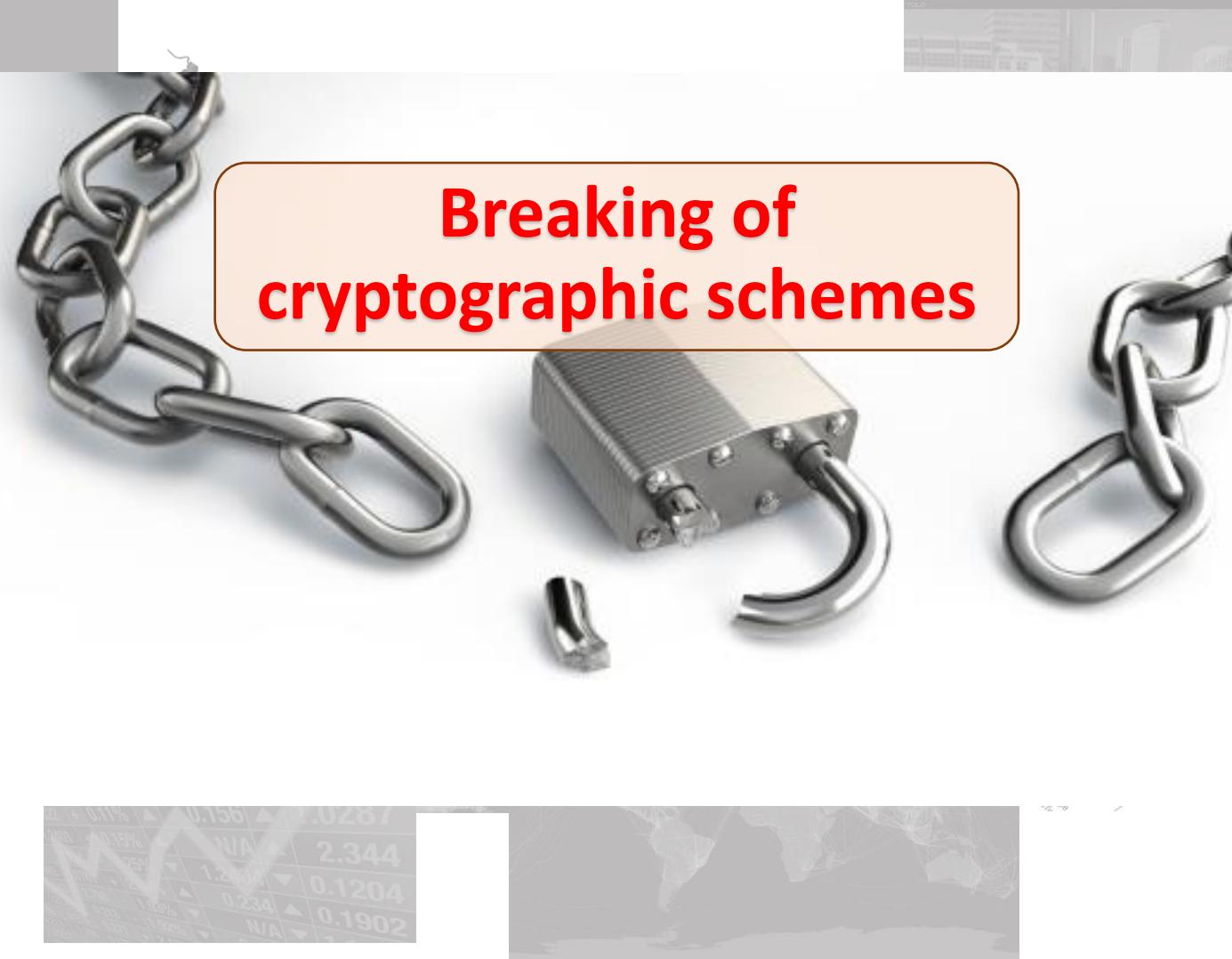
Machine learning



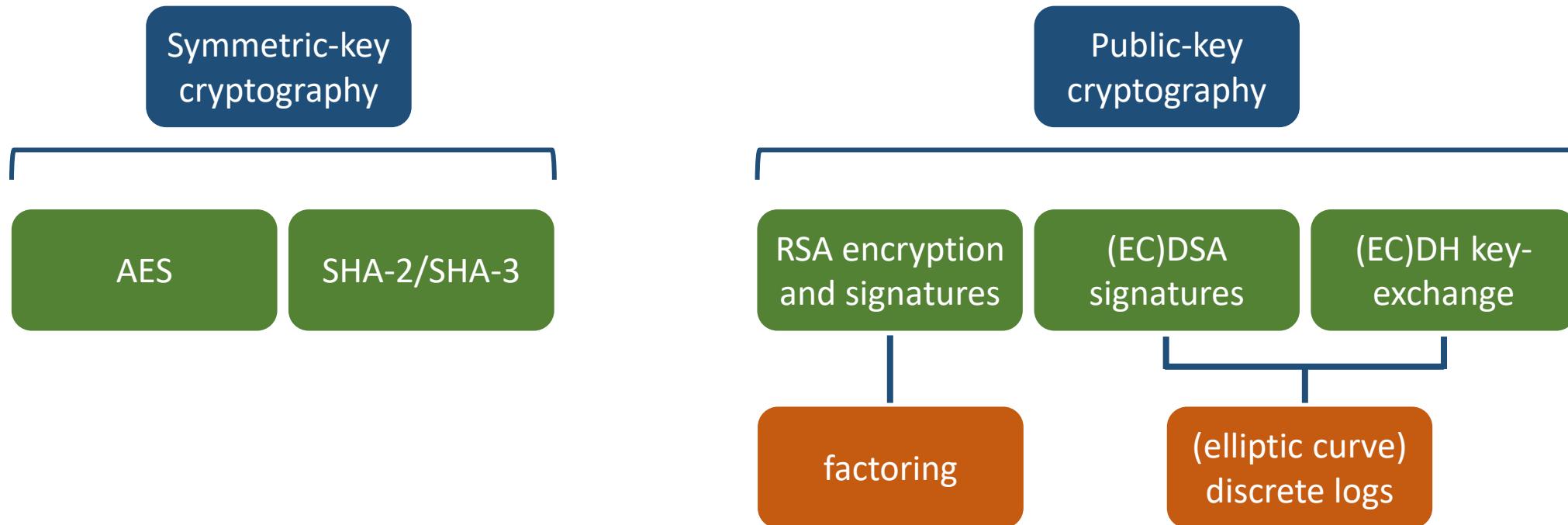
Database search



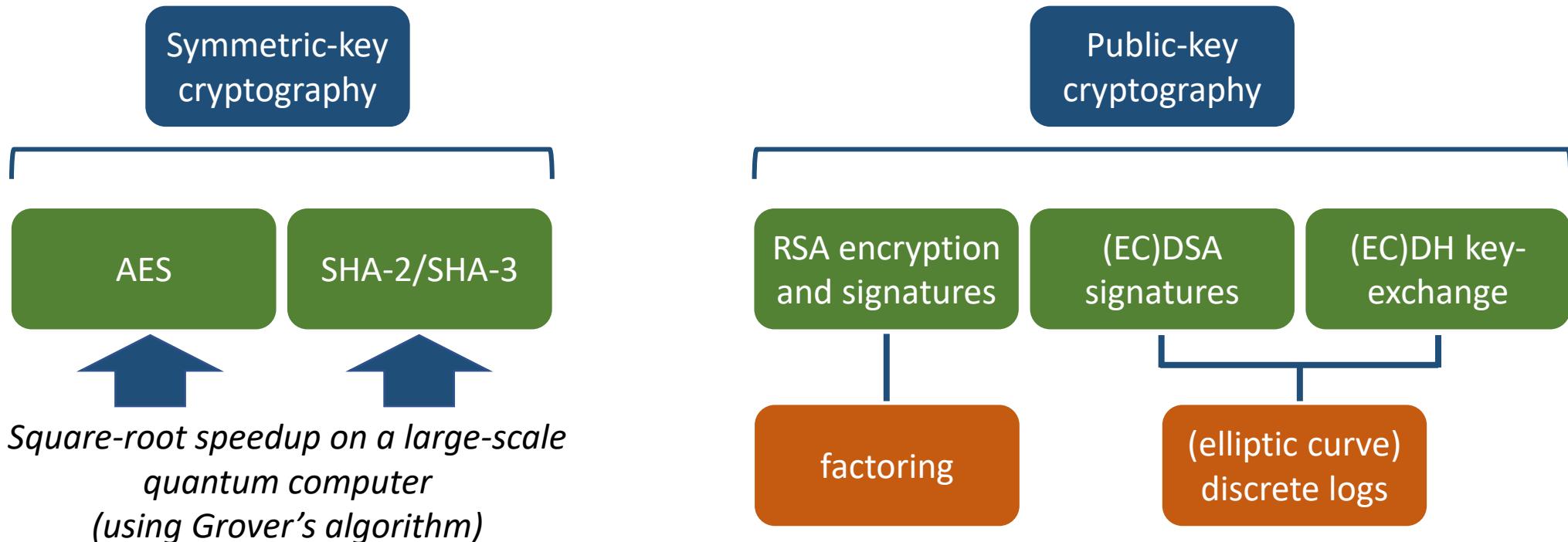
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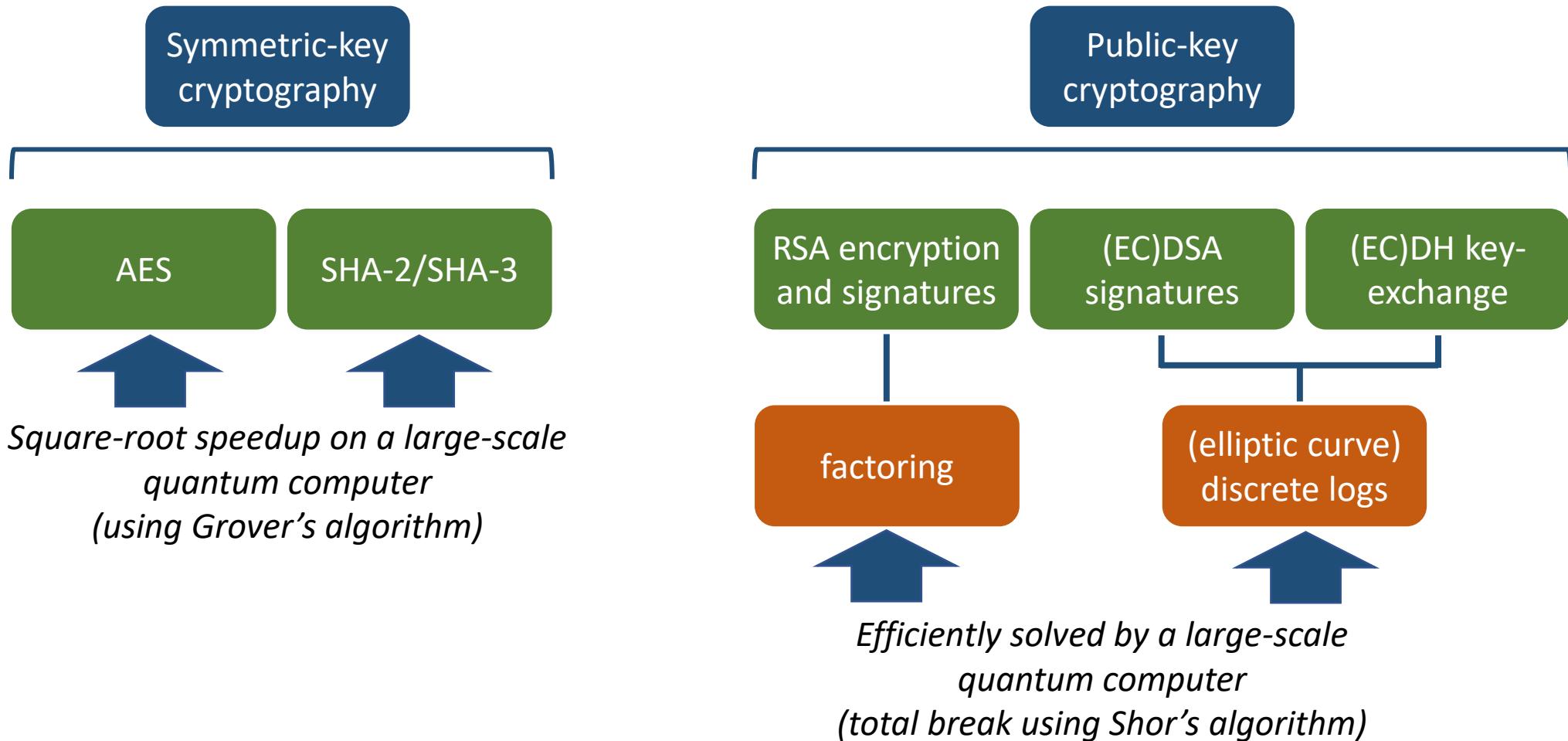
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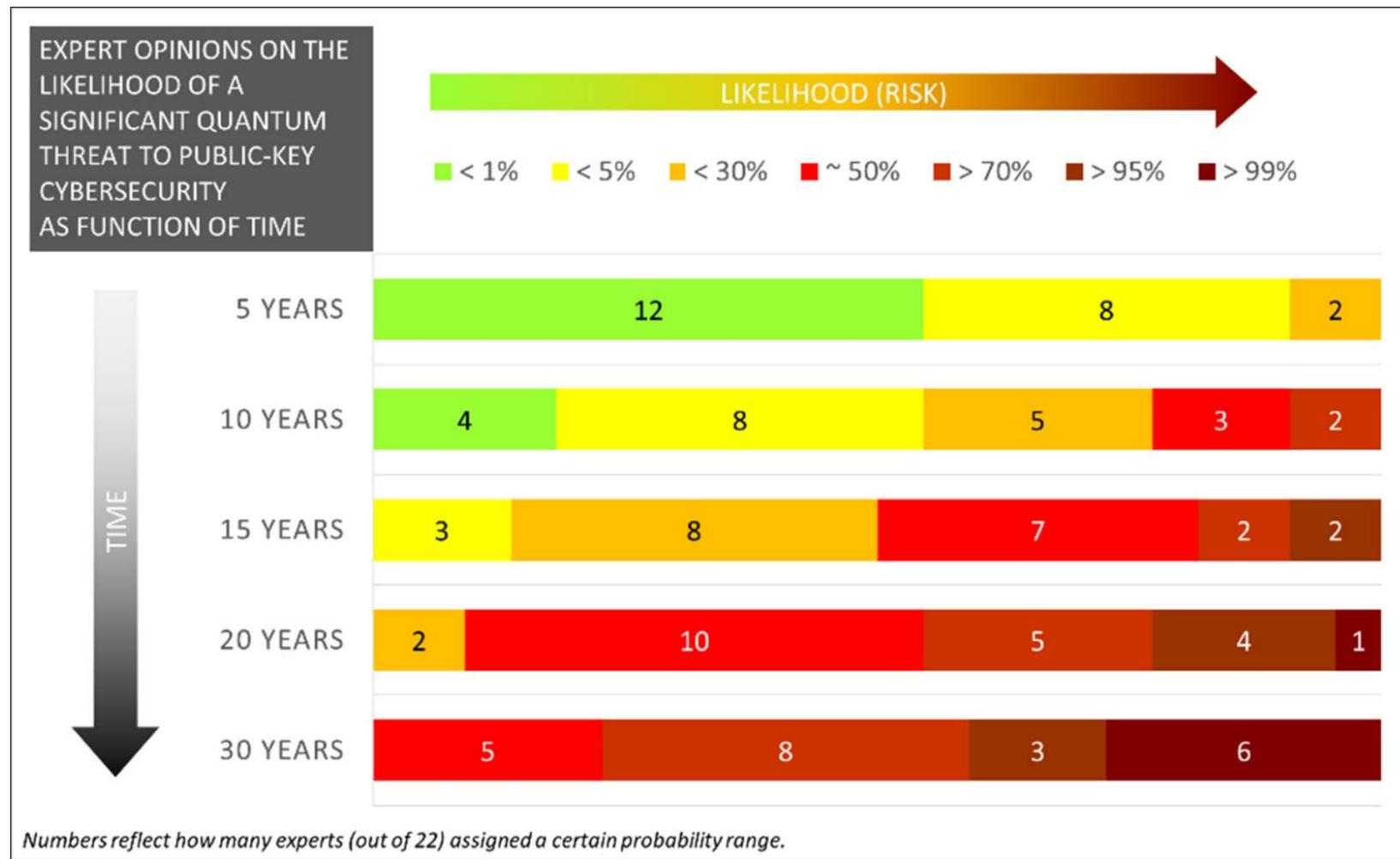
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## *When will a large-scale, fault-tolerant quantum computer be built?*

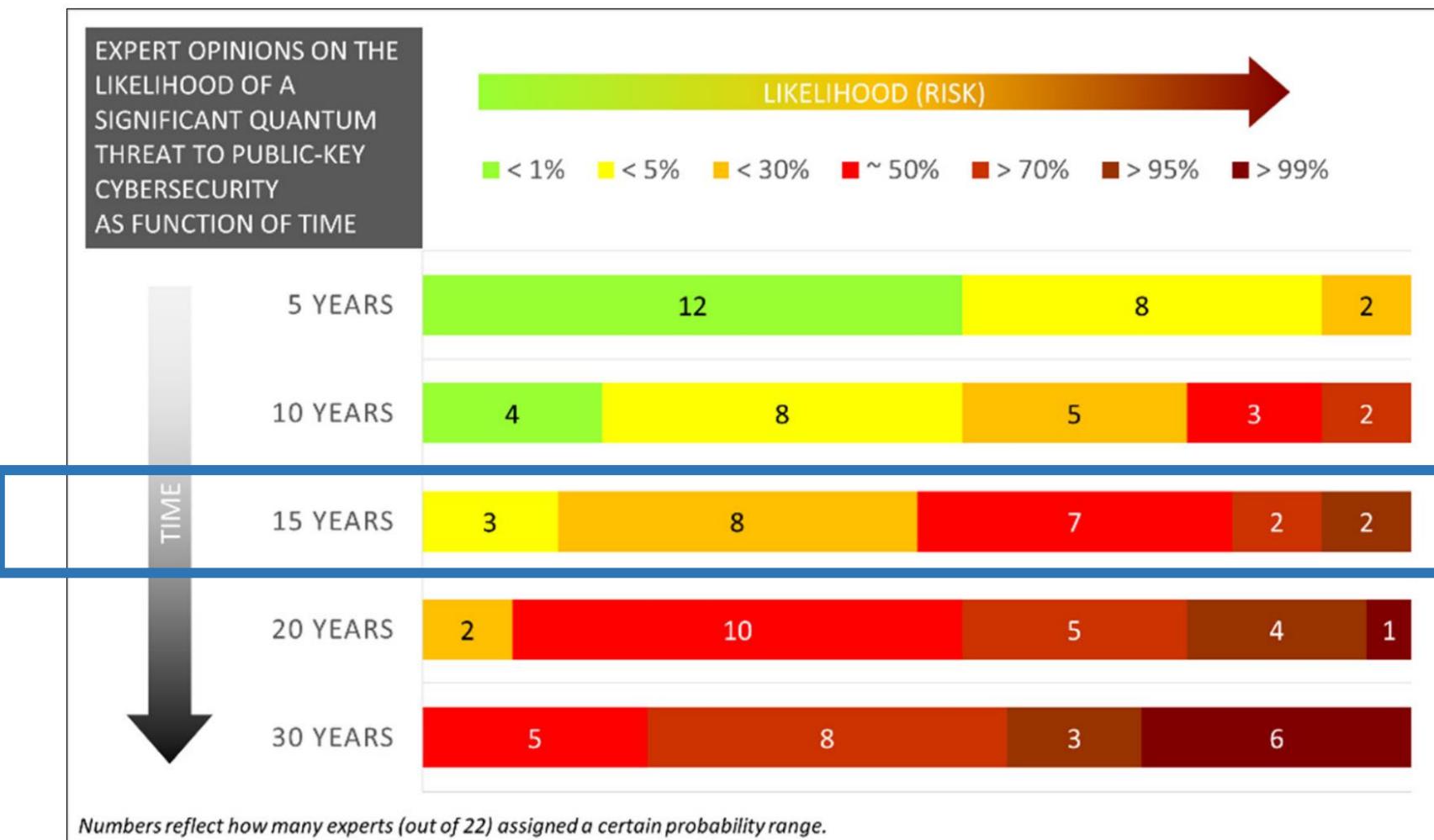


## *Expert opinions on the likelihood of the quantum threat to current public-key cryptosystems*



(\*) M. Mosca, M. Piani, “Quantum Threat Timeline”, Global Risk Institute (2019)

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A scalable, open approach to quantum computing

https://www.microsoft.com/en-us/quantum

https://www.theverge.com/2019/10/23/20928294/google-quantum-supremacy-sycamore-computer-chip

## Intel unveils its second-generation quantum computing control chip

Dean Takahashi @deantak December 3, 2020 12:00 PM Entrepreneur

Intel's Horse Ridge II quantum computing chip is hiding under all that refrigeration, packaging, and wiring. Image Credit: Intel

https://www.ibm.com/blogs/research/2020/09/ibm-quantum-roadmap/

IBM Research Blog Topics Labs About

Quantum Computing

## IBM's Roadmap For Scaling Quantum Technology

September 15, 2020 | Written by: Jay Gambetta

Categorized: Quantum Computing

Back in 1969, humans overcame unprecedented technological hurdles to make history: we put two of our own on the Moon and returned them safely. Today's computers are capable, but assuredly earthbound when it comes to accurately capturing the finest details of our universe. Building a device that truly captures the behavior of atoms—and can harness these behaviors to solve some of the most challenging problems of our time—might seem impossible if you limit your thinking to the computational world you know. But like the Moon landing, we have an ultimate objective to access a realm beyond what's possible on classical computers: we want to build a large-scale quantum computer. The future's quantum computer will pick up the slack where classical computers falter, controlling the behavior of atoms in order to run revolutionary applications across industries, generating world-changing materials or transforming the way we do business.

Today, we are releasing the roadmap that we think will take us from the noisy, small-scale devices of today to the million-plus qubit

https://venturebeat.com/2020/12/03/intel-unveils-its-second-generation-quantum-computing-control-chip/

## Google confirms 'quantum supremacy' breakthrough

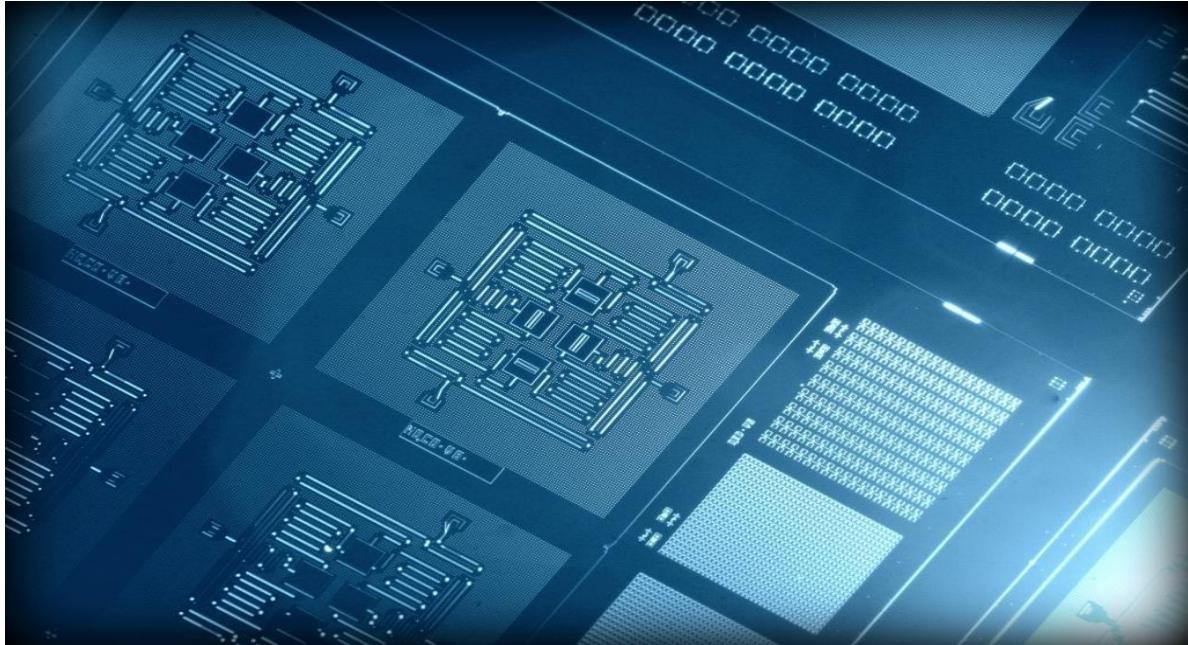
Its research paper is now available to read in its entirety

By Jon Porter | @JonPorter | Oct 23, 2019, 6:31am EDT

Google's Sycamore quantum processor, which was behind the breakthrough. | Credit: Google

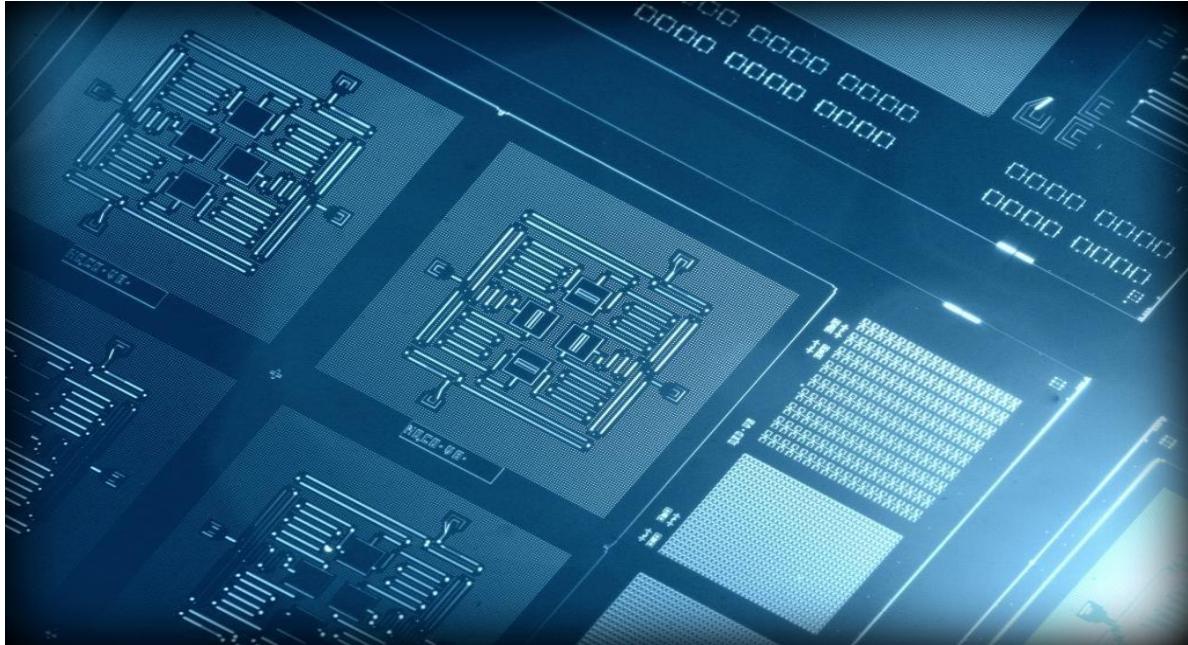
Google has officially announced that it's achieved quantum supremacy in a new article published in the scientific journal *Nature*. The announcement comes exactly one month after it initially leaked, when Google's paper was accidentally published early. Now, however, it's official, meaning the full details of the research are public, and the broader scientific community can fully scrutinize what Google says it's achieved.

# Cryptopocalypse and the NIST response



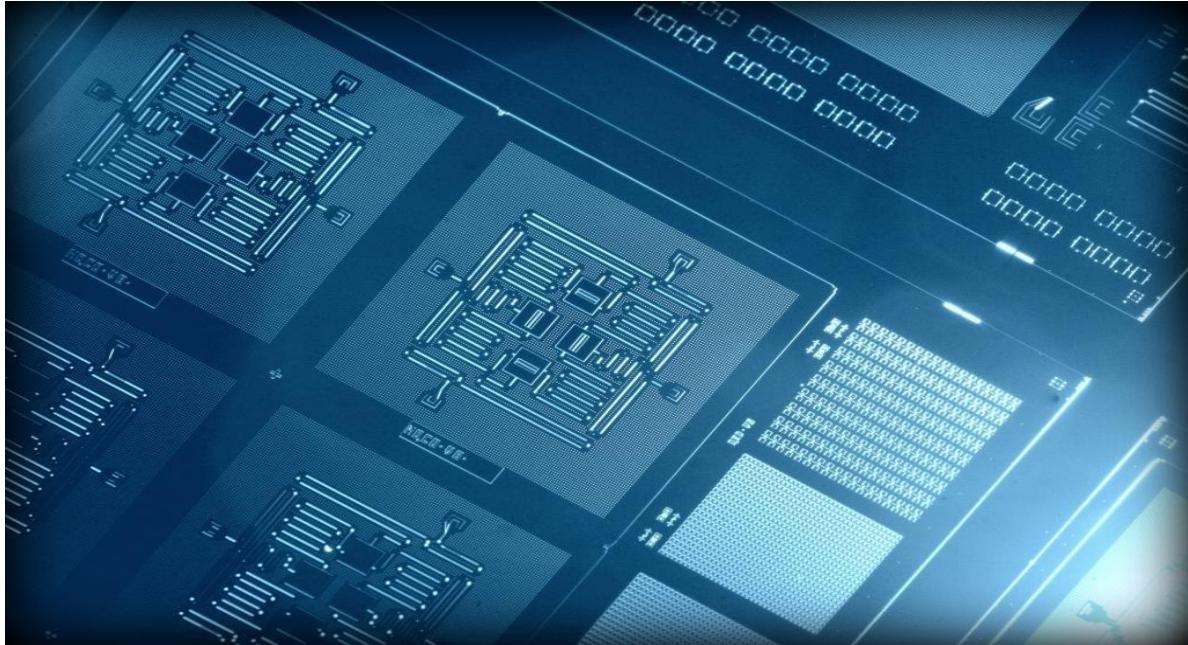
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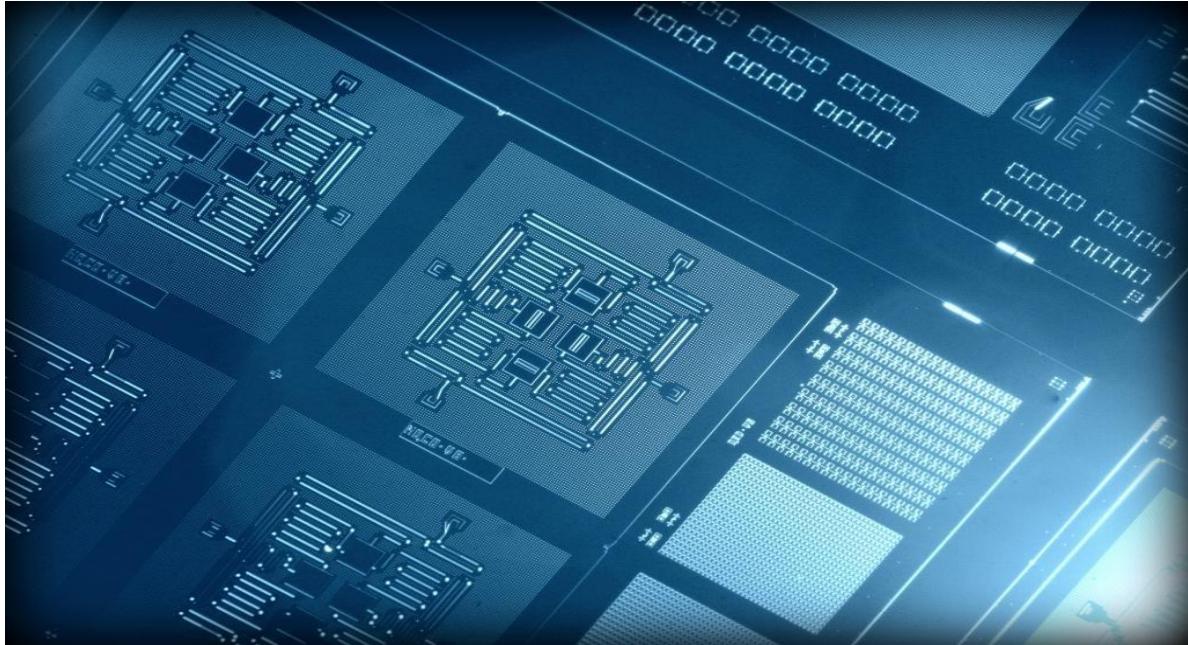
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*NIST: “The goal of this process is to select a number of acceptable candidate cryptosystems for standardization.” (This includes key encapsulation, encryption and digital signatures).*

# What do we need to protect *now*?

Assuming a *large-scale, fault tolerant* quantum computer will be developed in, say, 15 years:

- Attacker records encrypted data *today*...  
... uses quantum computer to access secret data *in 15 years* from now.

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Need quantum-resistant key agreement and encryption for long-term security

# Post-quantum (KEM) families

Code-based

Lattice-based

Isogeny-based

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Code-based

**Classic McEliece, BIKE, HQC**

Lattice-based

**NTRU, FrodoKEM (LWE), Kyber (M-LWE), Saber (M-LWR)**

Isogeny-based

**SIKE**

# Hybrid protocols

- Post-quantum crypto is still maturing
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- Post-quantum crypto is still maturing
  - Our confidence on its security and efficiency is growing rapidly but there is still a gap
- The current recommendation is to use a hybrid approach
  - Combine classical schemes (e.g., ECC) with post-quantum (e.g., SIKE)

Network Working Group  
Internet-Draft  
Intended status: Informational  
Expires: 18 April 2021

D. Stebila  
University of Waterloo  
S. Fluhrer  
Cisco Systems  
S. Gueron  
U. Haifa, Amazon Web Services  
15 October 2020

Hybrid key exchange in TLS 1.3  
draft-ietf-tls-hybrid-design-01

**Abstract**

Hybrid key exchange refers to using multiple key exchange algorithms simultaneously and combining the result with the goal of providing security even if all but one of the component algorithms is broken. It is motivated by transition to post-quantum cryptography. This document provides a construction for hybrid key exchange in the Transport Layer Security (TLS) protocol version 1.3.

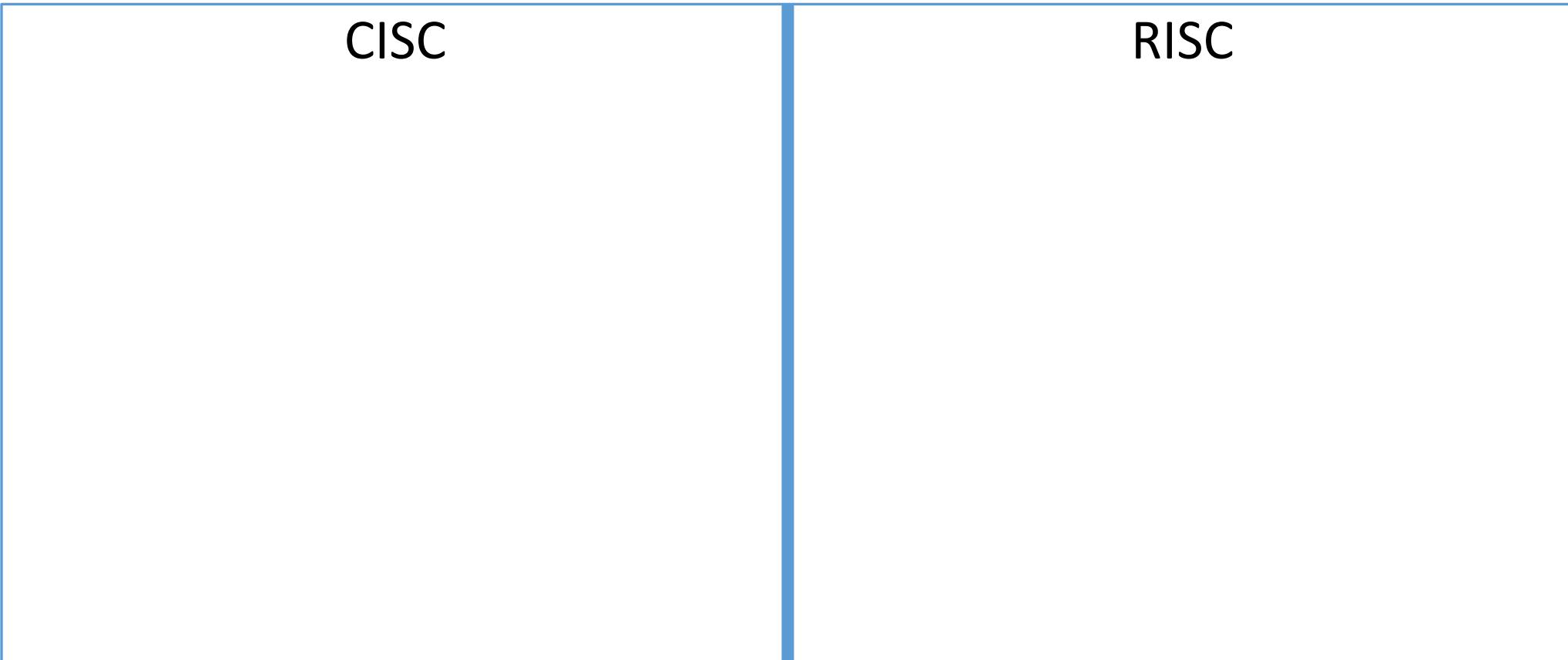
# PKC: implementation aspects

Preliminaries

# Computer architectures: CISC versus RISC

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*Before ...*



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## CISC

- Based on complex, multi-clock instructions that do multiple operations
- Memory instructions are incorporated in instructions
- Smaller code size
- Relies on more complex hardware
- Less compiler work to translate high-level language to assembly
- **Example:** x64 processors

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# Computer architectures: CISC versus RISC

*Today ...*

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  - Pipelining
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  - Out-of-order execution
- Software implementations can still take advantage of coarse-grained CISC/RISC differences, but **without losing track of specific architectural characteristics on a CPU-by-CPU basis**

# x64 Instruction Set Architecture

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- Sixteen 64-bit general purpose registers (`rax, rbx, rcx, rdx, rbp, rsp, rsi, rdi, r8-r15`)
- Arithmetic, logical, memory-to-register, and register-to-memory instructions operate over 64-bit integers
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- Fully backward compatible with 16- and 32-bit x86 code
- Some relevant instructions:

`add, adc, sub, sbb, shl, shr, shld, shrd, btr, bts, xor, and  
mov, push, pop`

`mul (128 ← 64 × 64)`

`mulx (128 ← 64 × 64), does not affect carry flag`

# PKC: implementation aspects

Side-channel attacks

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- (Depending on application) software implementations on small devices should also include protection against other attacks (e.g., power and EM attacks)
- We will mainly discuss about the **first line of defense** here

# Timing and cache attacks

There are *two* main sources of timing leakage in a computer program:

- Conditional statements (e.g., in if-then-else, do-while, etc.)
- Memory accesses through table lookups

Represent a risk if **execution conditions** or **table lookup indices** are secret-dependent.

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- Even when  $\text{instr}(\text{do\_this}) \equiv \text{instr}(\text{do\_that})$ , it can hold that  $\text{time}(\text{do\_this}) \neq \text{time}(\text{do\_that})$
- This timing difference is mainly due to the **branch predictor**

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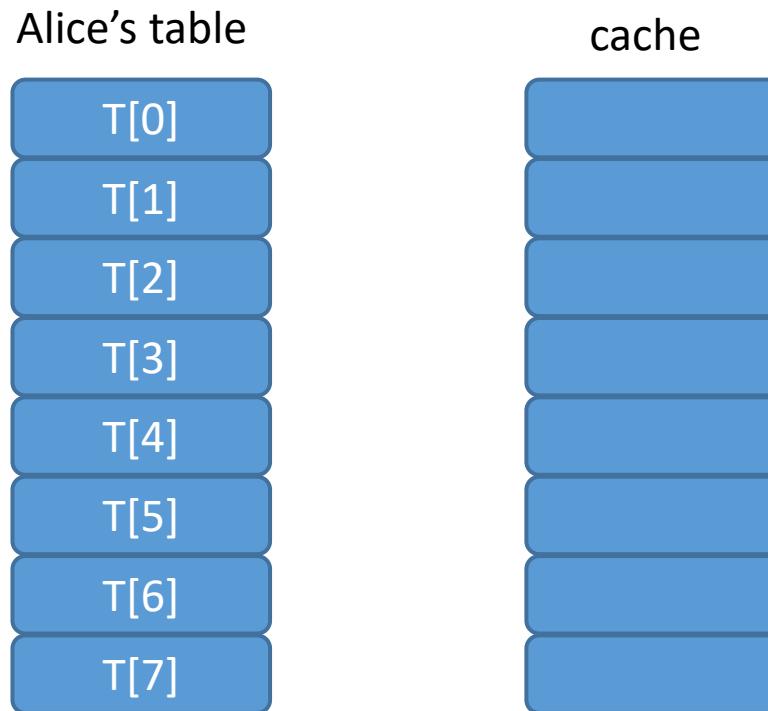
- In some cases, constant-time version can be *faster* than if-then-else version
  - Branch mispredictions can be expensive, especially in architectures with deep pipelines

# Timing and cache attacks

- Memory accesses through table lookups

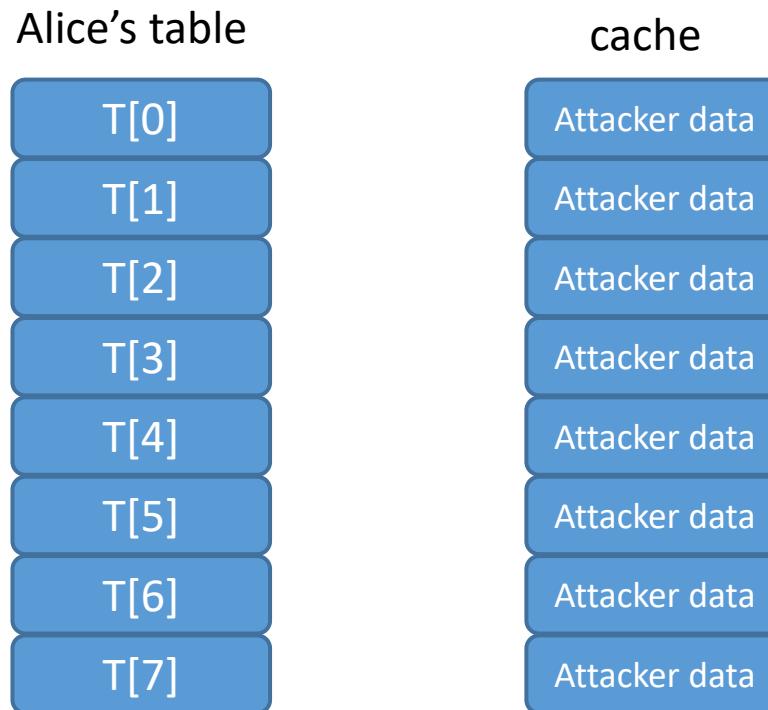
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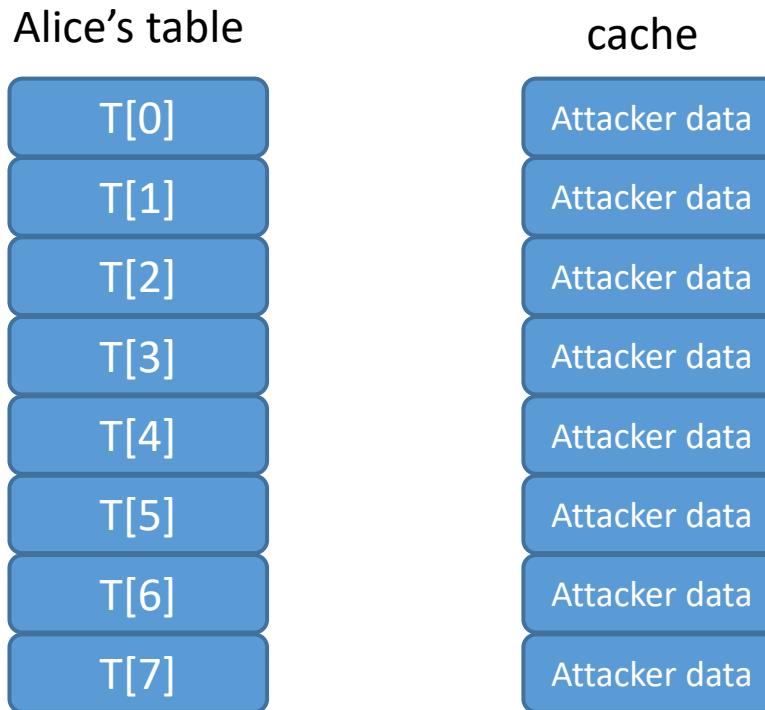
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# Timing and cache attacks

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- Alice needs first entry  $T[0]$ . She retrieves it



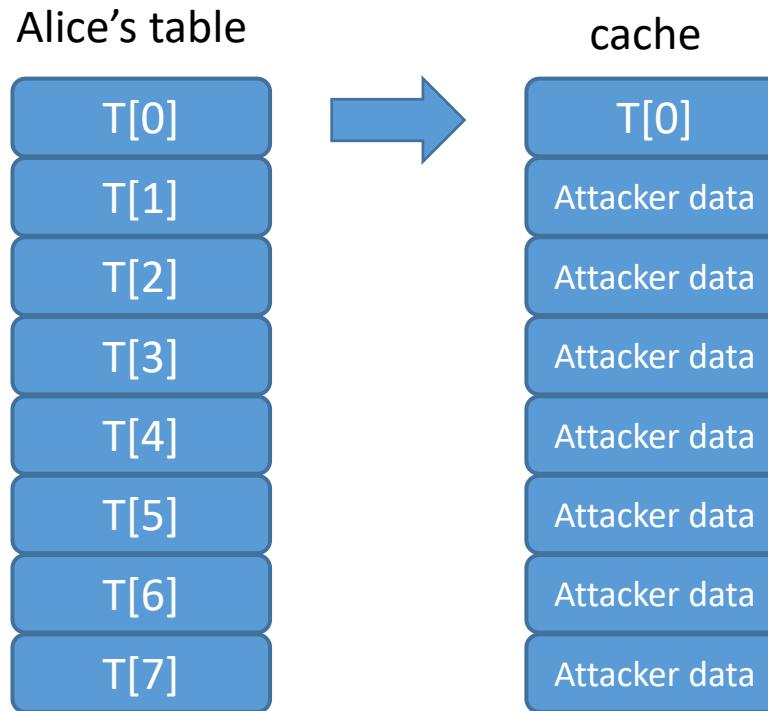
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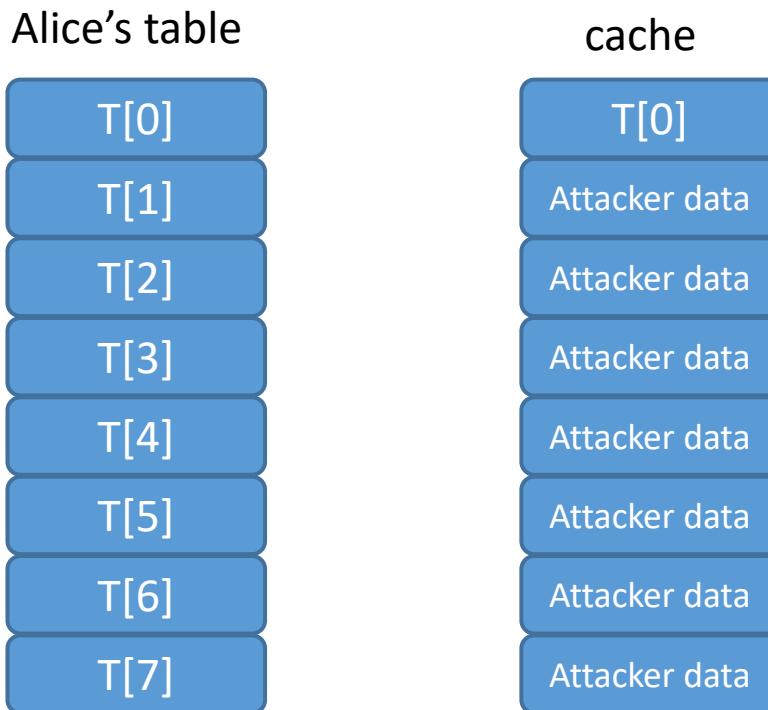
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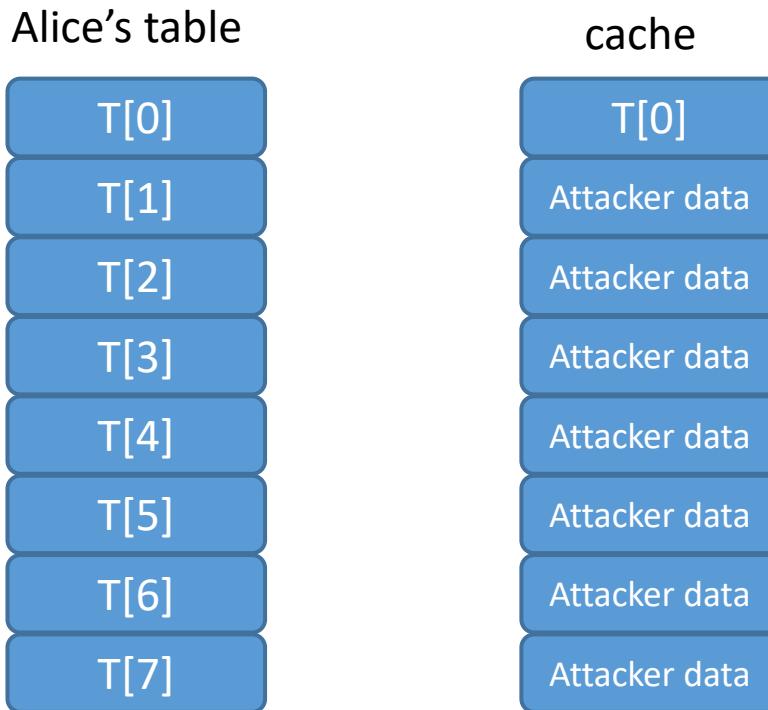
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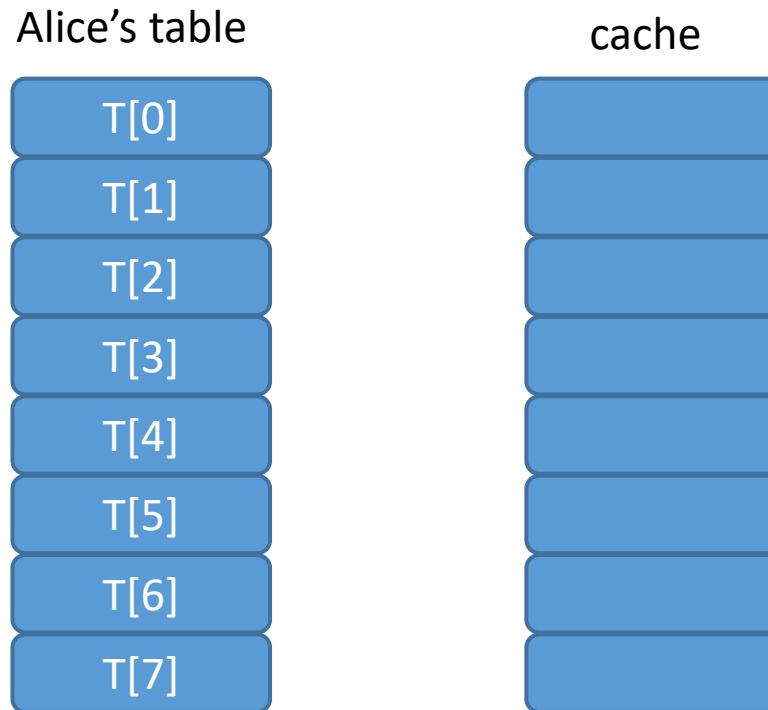
Reading first entry takes longer → learns that Alice retrieved  $T[0]$

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- **Countermeasure:** do linear pass over the full table and retrieve value through masking

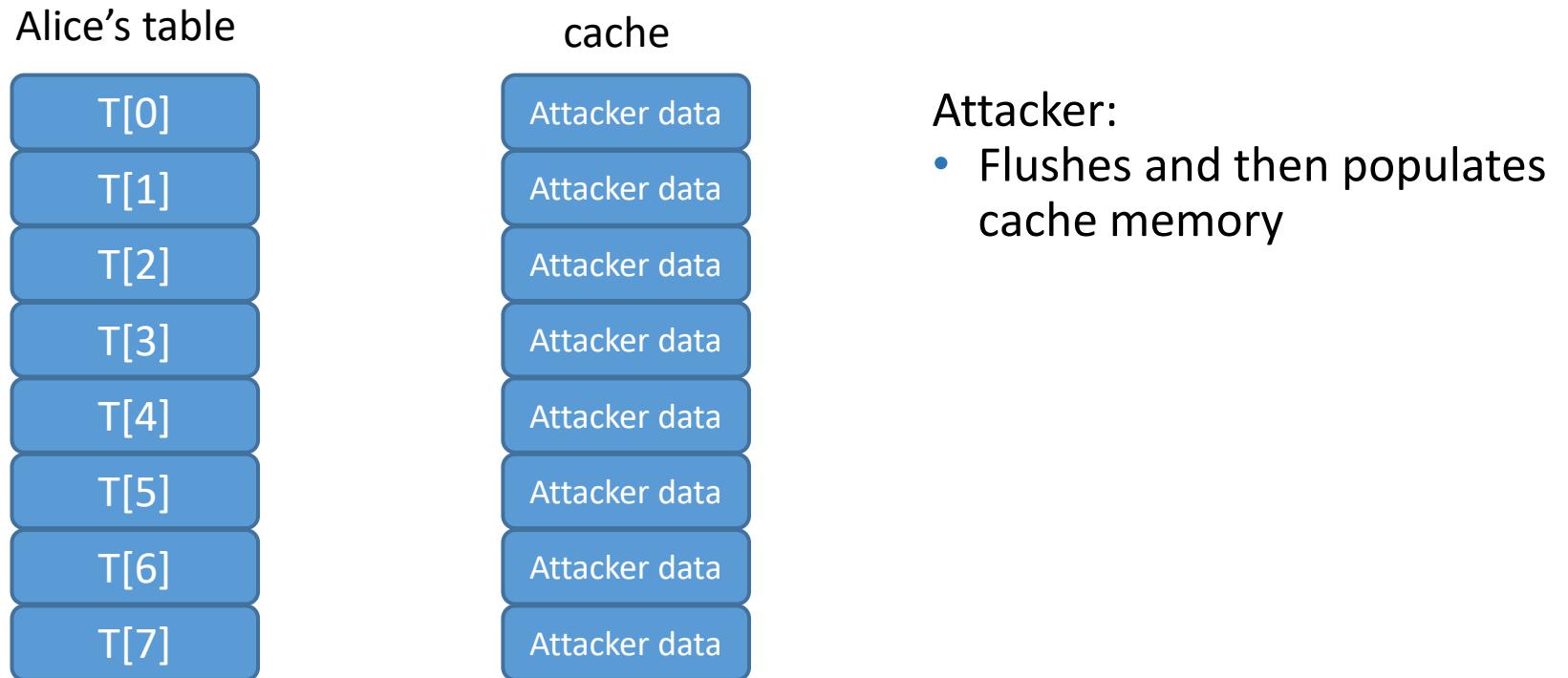
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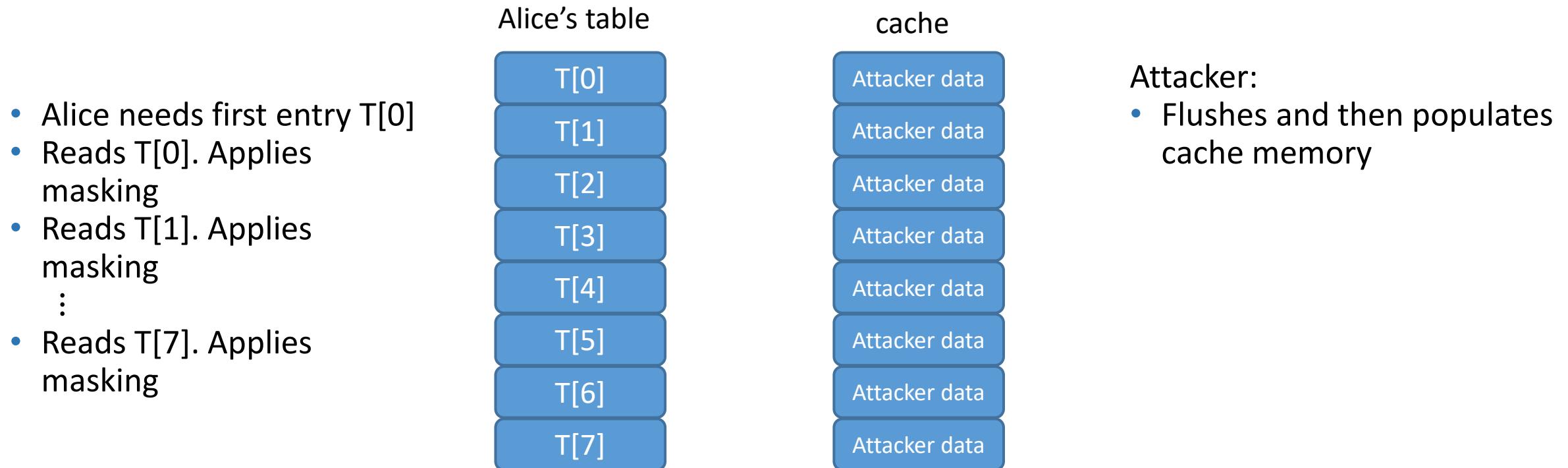
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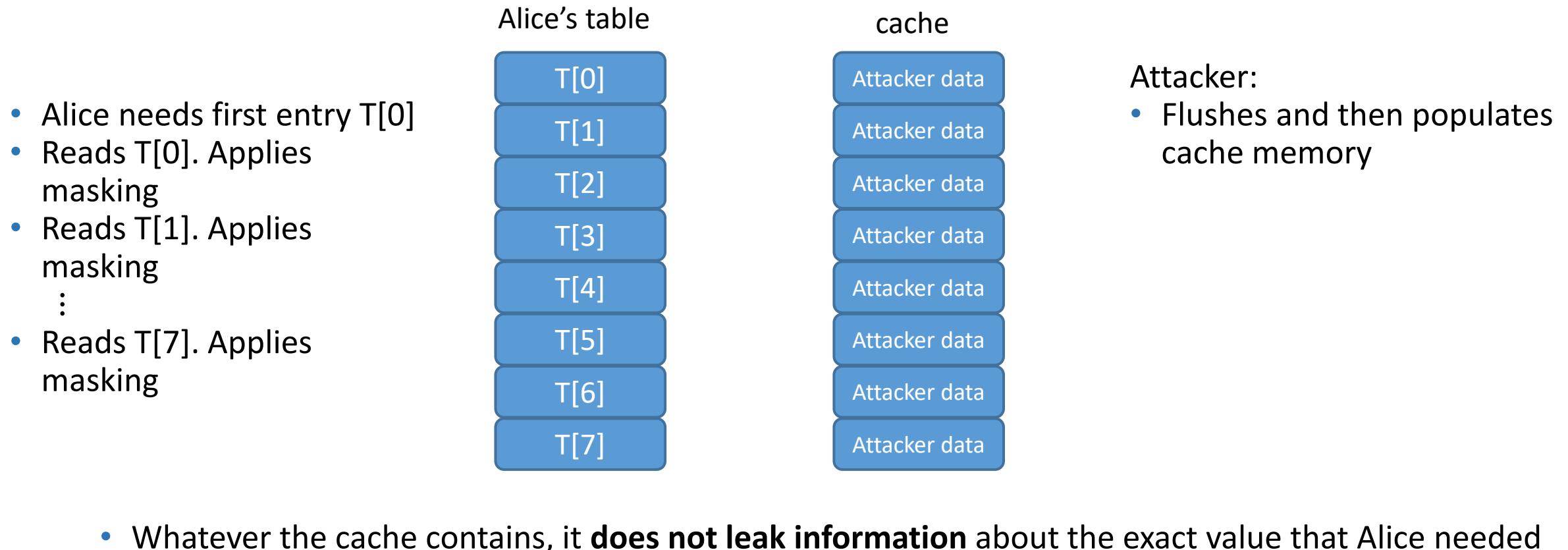
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# PKC: implementation aspects

Computer representation

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- A  $t$ -bit integer  $a$  is represented in radix  $2^r$  by

$$a = \sum_{i=0}^{s-1} a_i 2^{ir}$$

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- Let  $w$  be the computer wordsize (i.e., 8, 16, 32 or 64)
  - When  $r = w$ , we call it *full-radix* representation
  - When  $r < w$ , we call it *reduced-radix* representation

# Representation: full-radix vs. reduced-radix

**Full-radix:** e.g., view of  $t = 128$ -bit integer in radix  $2^{32}$



- $\#\text{limbs} = \lceil t/w \rceil$
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**Reduced-radix:**



- $\#\text{limbs} \geq \lceil (t + \delta)/w \rceil$ , for some  $\delta > 0$
- Extra room for accumulating intermediate values without word spilling
- Requires extra words if  $\lceil (t + \delta)/w \rceil > \lceil t/w \rceil$

# Representation: full-radix vs. reduced-radix

## Full-radix representation:

- Example: a 127-bit integer  $a$  is represented by  $(a_0, a_1, a_2, a_3)$  in radix  $2^{32}$
- More amenable for “generic” libraries
- Efficient when instructions with carries are efficient, multiplication is relatively expensive
- Example: non-vector implementations on 64-bit AMD, Intel Atom, Intel Quark, 32-bit ARM

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## Reduced-radix representation:

- Example: a 127-bit integer  $a$  is represented by  $(a_0, a_1, a_2, a_3, a_4)$  in radix  $2^{26}$
- More amenable for “special purpose” libraries
- Efficient when instructions with carries are relatively expensive, multiplication is efficient
- Example: vector implementations on 64-bit Intel desktop/server and 32-bit ARM,  
(in some cases) non-vector implementations on 64-bit Intel desktop/server
- Convenient when there is no direct access to instructions with carries (e.g., generic C)

# Representation: full-radix vs. reduced-radix

- Relative performance between Curve25519-based implementations:
  - **amd64-51** (reduced-radix  $2^{51}$ ) and **amd64-64** (full-radix  $2^{64}$ )
  - 255-bit finite field defined over  $p = 2^{255} - 19$

(\*) Source: SUPERCOP (2015)

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  - 255-bit finite field defined over  $p = 2^{255} - 19$
- Results in **BLACK** indicate amd64-51 is better, results in **RED** indicate amd64-64 is better

Intel Haswell (“wintermute”): **10%**

Intel Ivy Bridge (“hydra8”): **6%**

Intel Sandy Bridge (“hydra7”): **5%**

Intel Atom (“h8atom”): **-36%**

AMD Piledriver (“hydra9”): **-39%**

AMD Bulldozer (“hydra6”): **-38%**

AMD Bobcat (“h4e450”): **-47%**

(\*) Source: SUPERCOP (2015)

# PKC: implementation aspects

Computing arithmetic

# PKC: computational aspects

We will focus on two cases:

- **Classical side:** ECC
- **Post-quantum side:** SIKE

# PKC: computational aspects

Computation tree:

- **Underlying arithmetic level**
- **Primitive level**
- **Protocol level**

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- **Underlying arithmetic level:** e.g., modular arithmetic
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- **Protocol level:** e.g., key-exchange, signature, encryption scheme

# PKC: computational aspects

Computation tree: ECC

- **Field arithmetic**
- **Curve arithmetic**
- **Protocol level**

# PKC: computational aspects

Computation tree: ECC

- **Field arithmetic:** multiplication, squaring, addition, inversion over  $\mathbb{F}_p$  for  $p$  prime
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- **Curve arithmetic:** point addition/doubling, scalar multiplication
- **Protocol level:** ECDH key exchange, EC-based signatures (ECDSA, EdDSA)

# PKC: computational aspects

Computation tree: SIKE

- **Field arithmetic**
- **Curve and isogeny arithmetic**
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# PKC: computational aspects

Computation tree: SIKE

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Computation tree: SIKE

- **Field arithmetic:** multiplication, squaring, addition, inversion over  $\mathbb{F}_{p^2}$  for  $p$  prime
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- **Protocol level:** key exchange (SIDH), IND-CCA2-secure key encapsulation (SIKE)

# PKC: implementation aspects

Modular arithmetic

# Modular arithmetic

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  - Karatsuba method: asymptotic complexity  $O(n^{\log_2 3})$
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  - Karatsuba method: asymptotic complexity  $O(n^{\log_2 3})$
  - Toom-Cook multiplication: asymptotic complexity  $O(n^{\log_2 5})$
- **Karatsuba becomes attractive for a relatively large number of limbs:** in some cases, useful for high-security ECC (e.g., NIST P-521)

# Modular multiplication

- Many hybrid methods combining schoolbook/Comba/Karatsuba

# Modular multiplication

- Many hybrid methods combining schoolbook/Comba/Karatsuba
- Two generic flavours:
  - **Interleaved multiplication/reduction:** usually faster when standalone
  - **Non-interleaved multiplication/reduction:** usually faster when lazy reduction applies

# Modular reduction

- Two big categories for modular reduction:
  - General-form modulus** (RSA, ECC over general primes: e.g., Brainpool curves)
  - Special-form modulus** (high-performance ECC: e.g., NIST P-256, Curve25519, Four $\mathbb{Q}$ )
- Two main reduction methods: Barrett reduction and Montgomery reduction

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  - **Generalized pseudo-Mersenne primes** (a.k.a. Solinas primes)  
E.g., NIST P-256 prime  $p = 2^{256} - 2^{224} + 2^{192} + 2^{96} - 1$ ,  
Ed448-Goldilocks's prime  $p = 2^{448} - 2^{224} - 1$

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E.g., Curve25519's prime  $p = 2^{255} - 19$
  - **Mersenne primes**  
E.g., FourQ's prime  $p = 2^{127} - 1$ ,  
NIST P-521's prime  $p = 2^{521} - 1$

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E.g., Curve25519's prime  $p = 2^{255} - 19$
  - **Mersenne primes**  
E.g., FourQ's prime  $p = 2^{127} - 1$ ,  
NIST P-521's prime  $p = 2^{521} - 1$
- NIST prime choices targeted 32-bit platforms (popular at that time). Except for P-521, these primes are relatively expensive in constant-time and vectorized implementations

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- Inputs  $[a_0, a_1, a_2, a_3]$  and  $[b_0, b_1, b_2, b_3]$

- $t$  holds  $2 \times 64$  bits.
- $t_x$  hold 64 bits.
- $c$  is a carry or borrow bit.

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integer  
mult

$$[t_0, t] = a_0 \times b_0$$

$$[t_1, t] = a_0 \times b_1 + a_1 \times b_0 + t$$

$$[t_2, t] = a_0 \times b_2 + a_2 \times b_0 + a_1 \times b_1 + t$$

$$[t_3, t] = a_0 \times b_3 + a_3 \times b_0 + a_1 \times b_2 + a_2 \times b_1 + t$$

$$[t_4, t] = a_1 \times b_3 + a_3 \times b_1 + a_2 \times b_2 + t$$

$$[t_5, t] = a_2 \times b_3 + a_3 \times b_2 + t$$

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integer mult result  $\{t_0 - t_7\}$

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Reduction (using  $2^{256} \equiv 38$ )

- Set output in the range  $[0, 2^{256} - 38)$

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$$[t_6, t_7] = a_3 \times b_3 + t$$

integer mult result  $\{t_0 - t_7\}$

- Set output in the range  $[0, 2^{256} - 38)$

Reduction (using  $2^{256} \equiv 38$ )

$$[t_0, t] = t_0 + 38 \times t_4$$

$$[t_1, t] = t_1 + 38 \times t_5 + t$$

$$[t_2, t] = t_2 + 38 \times t_6 + t$$

$$[t_3, t] = t_3 + 38 \times t_7 + t$$

1st pass

- $t$  holds  $2 \times 64$  bits.
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# Modular reduction: special form primes

- Constant-time field multiplication with  $p = 2^{255} - 19$  (64-bit)
- Inputs  $[a_0, a_1, a_2, a_3]$  and  $[b_0, b_1, b_2, b_3]$

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- Set output in the range  $[0, 2^{256} - 38)$

Reduction (using  $2^{256} \equiv 38$ )

$$[t_0, t] = t_0 + 38 \times t_4$$

$$[t_1, t] = t_1 + 38 \times t_5 + t$$

$$[t_2, t] = t_2 + 38 \times t_6 + t$$

$$[t_3, t] = t_3 + 38 \times t_7 + t$$

$$[t_0, c] = t_0 + 38 \times (t + 1)$$

$$[t_1, c] = t_1 + c$$

$$[t_2, c] = t_2 + c$$

$$[t_3, c] = t_3 + c$$

1st pass

2nd pass  
Add extra 38

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# Modular reduction: special form primes

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$$[t_6, t_7] = a_3 \times b_3 + t$$

integer mult result  $\{t_0 - t_7\}$

- Set output in the range  $[0, 2^{256} - 38)$

Reduction (using  $2^{256} \equiv 38$ )

$$[t_0, t] = t_0 + 38 \times t_4$$

$$[t_1, t] = t_1 + 38 \times t_5 + t$$

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$$[t_3, t] = t_3 + 38 \times t_7 + t$$

$$[t_0, c] = t_0 + 38 \times (t + 1)$$

$$[t_1, c] = t_1 + c$$

$$[t_2, c] = t_2 + c$$

$$[t_3, c] = t_3 + c$$

$$[t_0, c] = t_0 - 38 \times c \text{ if } c = 1$$

$$[t_1, c] = t_1 - c$$

$$[t_2, c] = t_2 - c$$

$$[t_3, c] = t_3 - c$$

Output  $[t_0, t_1, t_2, t_3]$

1st pass

2nd pass  
Add extra 38

3rd pass with  
condition

- $t$  holds  $2 \times 64$  bits.
- $t_x$  hold 64 bits.
- $c$  is a carry or borrow bit.

# Modular reduction: special form primes

- Constant-time field multiplication with  $p = 2^{255} - 19$  (x64 assembly)

```

mov    rax,  [reg_p1]
mul    qword ptr [reg_p2]      // a0*b0
mov    r13,  rax               // t0
mov    r12,  rdx

mov    rbx,  [reg_p2+8]
mov    rax,  [reg_p1]
mul    rbx                      // a0*b1
add    r12,  rax
mov    r10,  rdx
adc    r10,  0

xor    r11,  r11
mov    rax,  [reg_p1+8]         // a1*b0
mul    qword ptr [reg_p2]
add    r12,  rax
mov    [reg_p3+8], r12         // t1
adc    r10,  rdx
adc    r11,  0

mov    rax,  [reg_p2]
mul    qword ptr [reg_p1+16]   // a2*b0
add    r10,  rax
adc    r11,  rdx

xor    rcx,  rcx
mov    rax,  [reg_p1+8]
mul    rbx                      // a1*b1
add    r10,  rax
adc    r11,  rdx
adc    rcx,  0

mov    rax,  [reg_p2+16]
mul    qword ptr [reg_p1]      // a0*b2
add    r10,  rax
mov    [reg_p3+16], r10         // t2
adc    r11,  rdx
adc    rcx,  0

```

```
xor r10, r10
mov rax, [reg_p2]
mul qword ptr [reg_p1+24] // a3*b0
add r11, rax
adc rcx, rdx
adc r10, 0

mov rax, [reg_p2+8]
mul qword ptr [reg_p1+16] // a2*b1
add r11, rax
adc rcx, rdx
adc r10, 0

mov rax, [reg_p2+16]
mul rbx // a1*b2
add r11, rax
adc rcx, rdx
adc r10, 0

mov rax, [reg_p2+24]
mul qword ptr [reg_p1] // a0*b3
add r11, rax
mov [reg_p3+24], r11 // t3
adc rcx, rdx
adc r10, 0

xor r11, r11
mov rax, [reg_p2+8]
mul qword ptr [reg_p1+24] // a3*b1
add rcx, rax
adc r10, rdx
adc r11, 0

mov rax, [reg_p2+16]
mul qword ptr [reg_p1+16] // a2*b2
add rcx, rax
adc r10, rdx
adc r11, 0
```

```

xor  rcx, rcx
mov  rax, constant_38
mul  r11
add  rax, r12
adc  rcx, 0
mov  r11, [reg_p3+16]
add  r11, rax          // r11 <- t2
adc  rcx, rdx

xor  r12, r12
mov  rax, constant_38
mul  r8
add  rax, rcx
adc  r12, 1
mov  r8, [reg_p3+24]
add  r8, rax          // r8 <- t3
adc  rdx, r12          // rdx <- t4 + 1

xor  r12, r12
mov  rax, constant_38
mul  rdx
add  r13, rax          // t0
adc  r10, 0              // t1
adc  r11, 0              // t2
adc  r8, 0               // t3

mov  rax, constant_38      // final correction
cmovc rax, r12
sub  r13, rax              // t0
mov [reg_p3], r13
sbb  r10, 0                // t1
mov [reg_p3+8], r10
sbb  r11, 0                // t2
mov [reg_p3+16], r11
sbb  r8, 0                 // t3
mov [reg_p3+24], r8

```

# Modular addition

- *Constant-time* field addition  $a + b \bmod p$ 
  - If  $r = a + b \geq p$  then  $r = r - p$ . Output  $r$
  - Eliminating **if-then-else statement** is usually straightforward

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  - Eliminating **if-then-else statement** is usually straightforward

**Example:** field addition with  $p = 2^{127} - 1$  (64-bit)

$$[t_0, c] = a_0 + b_0$$

$$t_1 = a_1 + b_1 + c$$

Write  $c = t_1 \gg 63$ ,  $t_1 = t_1 \& \text{mask\_63}$  (using  $2^{127} \equiv 1$ )

$$[t_0, c] = t_0 + c$$

$$t_1 = t_1 + c$$

**Output**  $[t_0, t_1]$

# Modular addition

- **Example:** *constant-time* field addition with  $p = 2^{127} - 1$  (x64 assembly)

```
mov    r8, [reg_p1]
mov    r9, [reg_p1+8]
add    r8, [reg_p2]
adc    r9, [reg_p2+8]

btr    r9, 63
adc    r8, 0
mov    [reg_p3], r8
adc    r9, 0
mov    [reg_p3+8], r9
```

# Modular addition

- **Example:** *constant-time* field addition with  $p = 2^{127} - 1$  (x64 assembly)

```
mov    r8, [reg_p1]
mov    r9, [reg_p1+8]
add    r8, [reg_p2]
adc    r9, [reg_p2+8]

btr    r9, 63
adc    r8, 0
mov    [reg_p3], r8
adc    r9, 0
mov    [reg_p3+8], r9
```

- **Example:** *constant-time* field subtraction with  $p = 2^{127} - 1$  (x64 assembly)

```
mov    r8, [reg_p1]
mov    r9, [reg_p1+8]
sub    r8, [reg_p2]
sbb    r9, [reg_p2+8]

btr    r9, 63
sbb    r8, 0
mov    [reg_p3], r8
sbb    r9, 0
mov    [reg_p3+8], r9
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After result of additions/subtractions in  $\mathbb{F}_{2^{127}-1}$ :

$$t_0 = t_0 + (t_2 \gg 41)$$

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- A reduced representation [43, 43, 41]-bit is obtained by running **two rounds** of the carry correction routine
- In some cases, it might be enough to run **one round** (after multiplications and squarings)

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- For our example, if there is access to `adc` then **full-radix is more efficient than reduced-radix** (e.g., when using assembly or intrinsics)

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- When using a high-level language, **reduced-radix can be simpler to implement in some cases**

# Modular arithmetic: case with reduced-radix

- **Example:** C implementation of field multiplication with  $p = 2^{127} - 1$  on Linux
- GNU GCC and clang support 128-bit datatypes (`int128_t`, `uint128_t`), not in ANSI C

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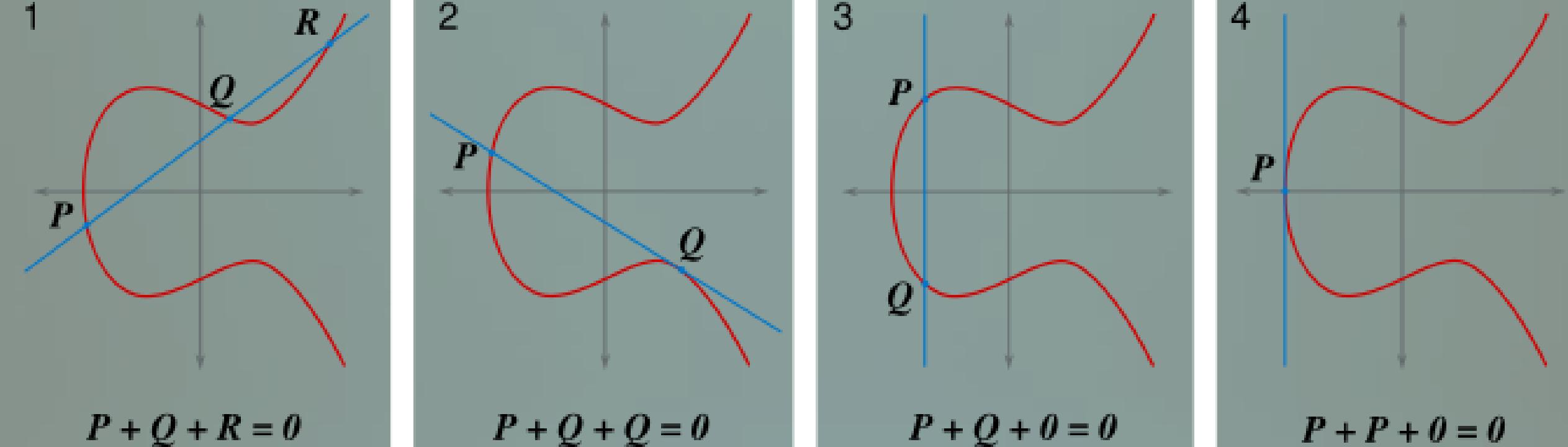
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```
void fpmul1271(const int64_t* a, const int64_t* b, int64_t* c)
{
    int128_t t[3];
    int64_t d1, d2;

    a0 = a[0]; a1 = a[1]; b0 = b[0]; b1 = b[1];

    d1 = a1 << 2;
    d2 = a2 << 2;
    t[0] = (int128_t)a0*b0 + (int128_t)d1*b2 + (int128_t)d2*b1;
    t[1] = (int128_t)a0*b1 + (int128_t)a1*b0 + (int128_t)d2*b2;
    t[2] = (int128_t)a0*b2 + (int128_t)a2*b0 + (int128_t)a1*b1;

    t[0] += (int64_t)(t[2] >> 41); c[2] = (int64_t)t[2] & mask_41;
    t[1] += (int64_t)(t[0] >> 43); c[0] = (int64_t)t[0] & mask_43;
    c[2] += (int64_t)(t[1] >> 43); c[1] = (int64_t)t[1] & mask_43;
    c[0] += (int64_t)(c[2] >> 41); c[2] &= mask_41;
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```



The case of ECC

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- Elliptic curve-based protocols require different variants of scalar multiplication:
  - **Variable-base scalar multiplication:**  $[k]P$  with variable point  $P$
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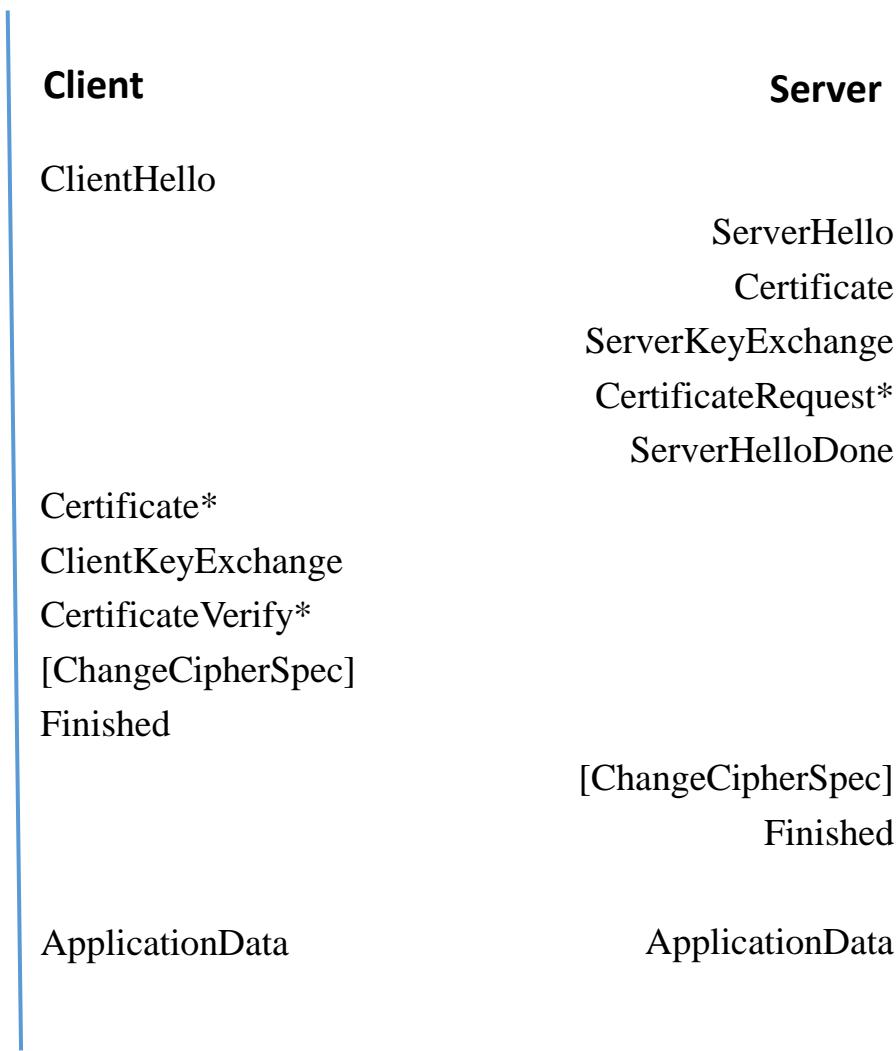
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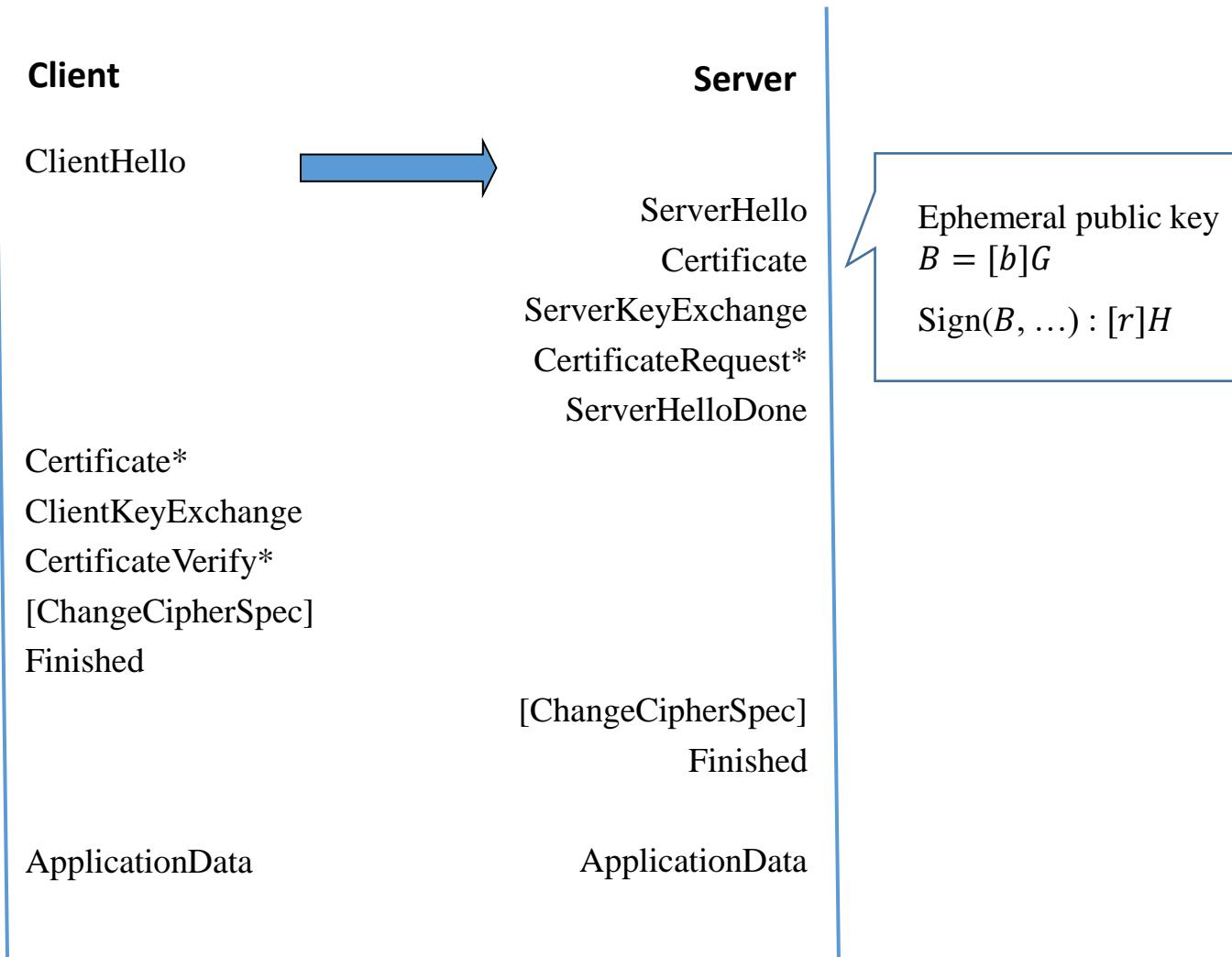
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- We will focus on **finite fields with large prime characteristic** ( $\mathbb{F}_p$  for  $p$  prime)

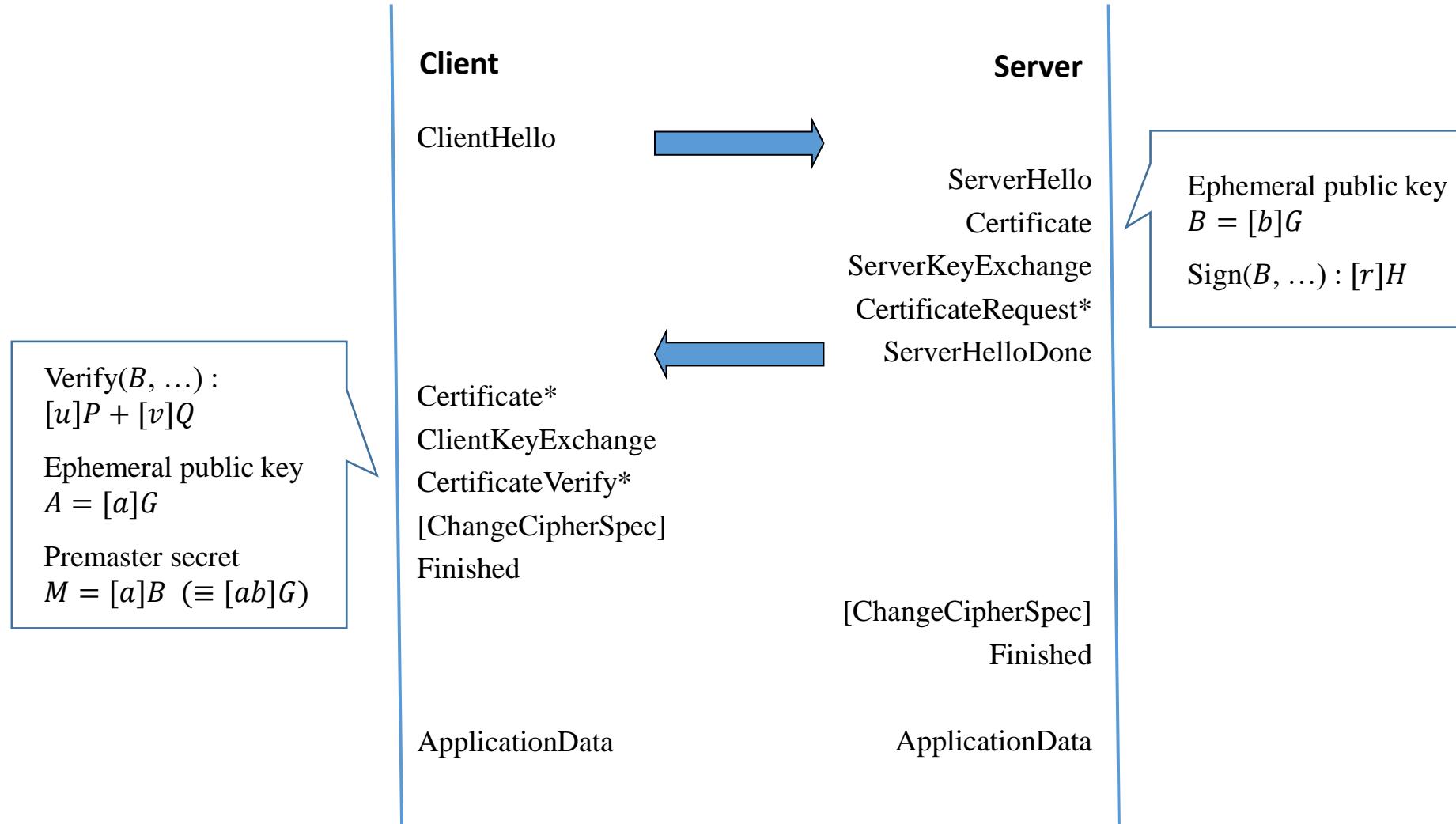
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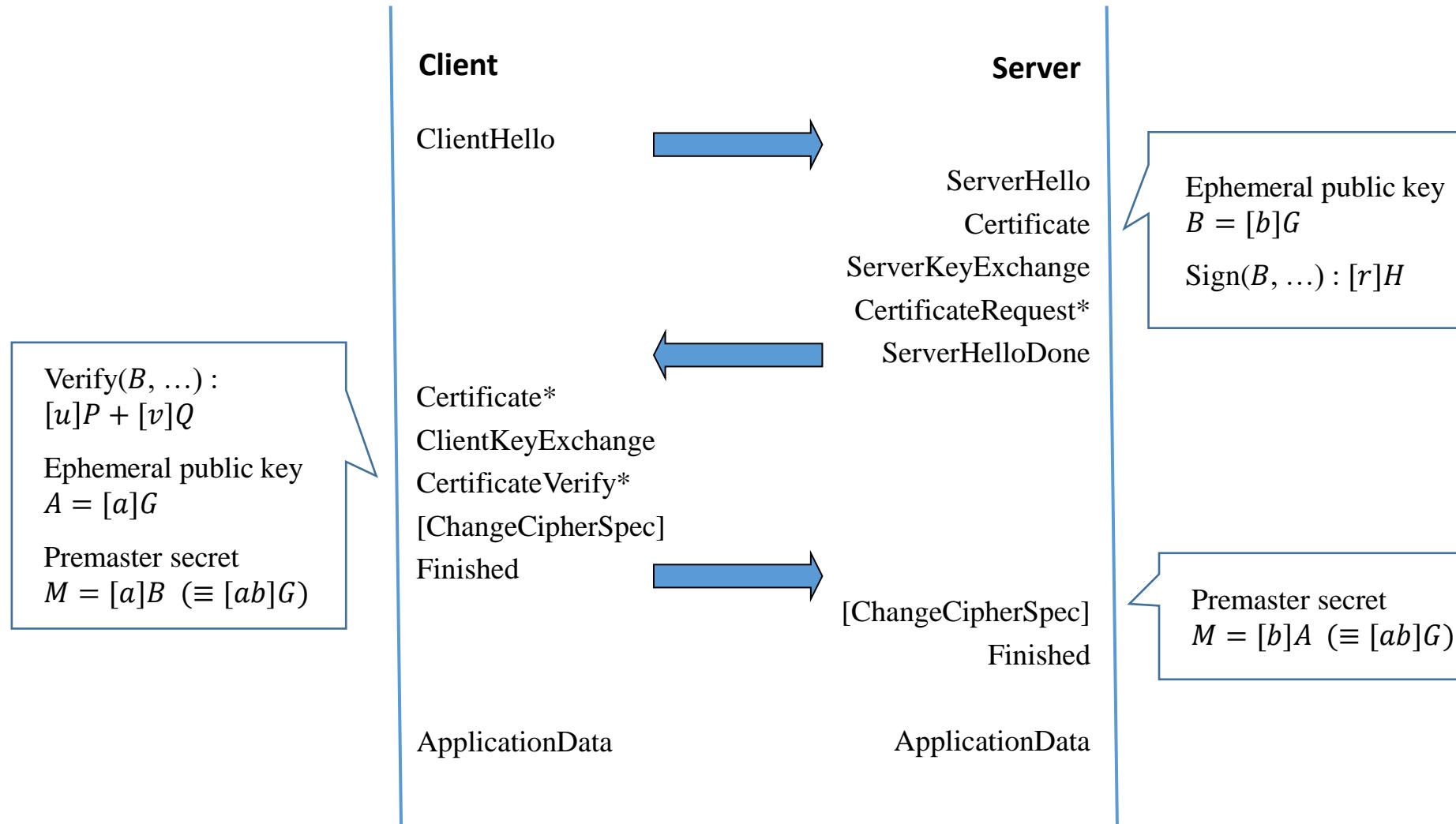
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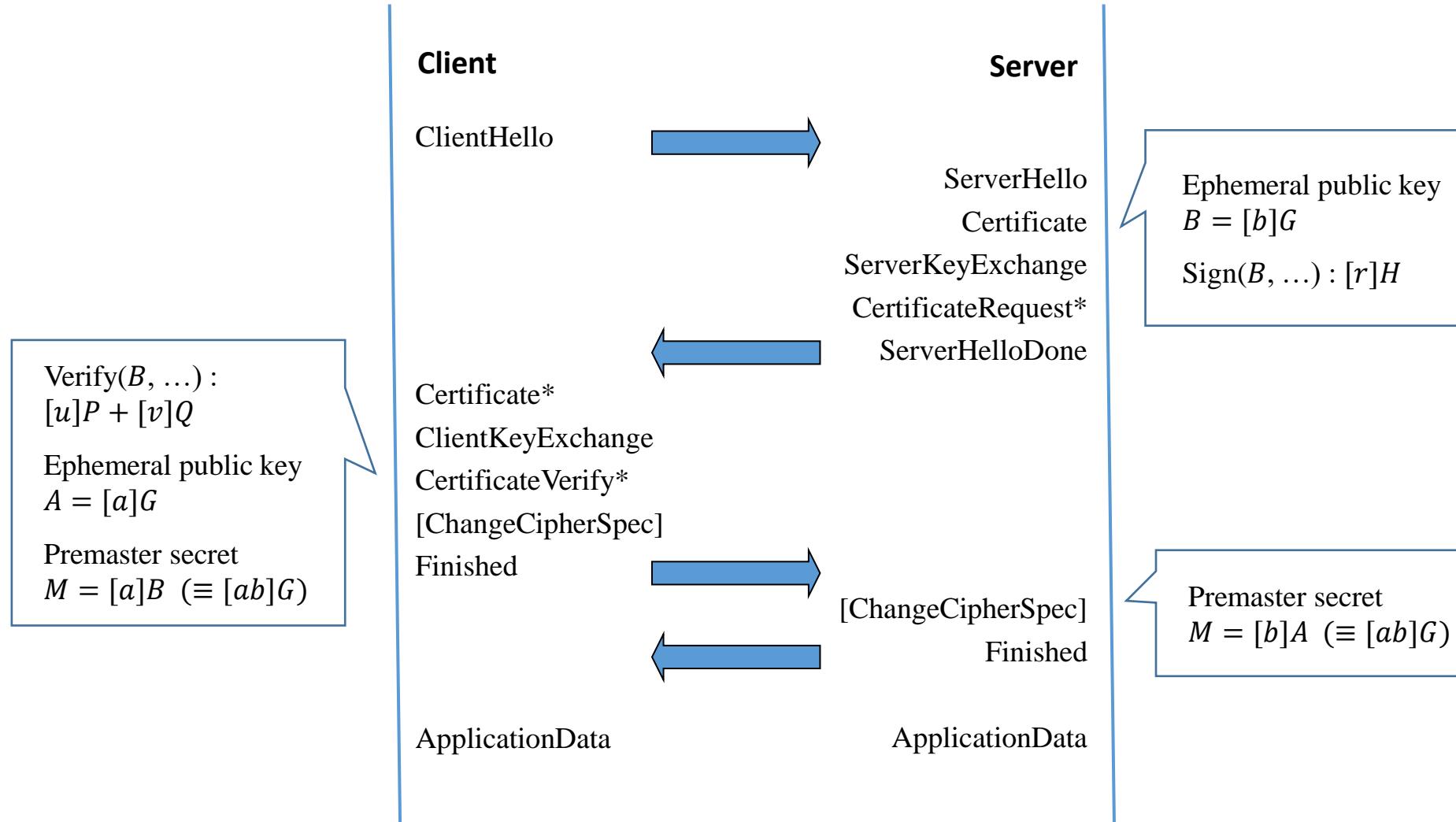
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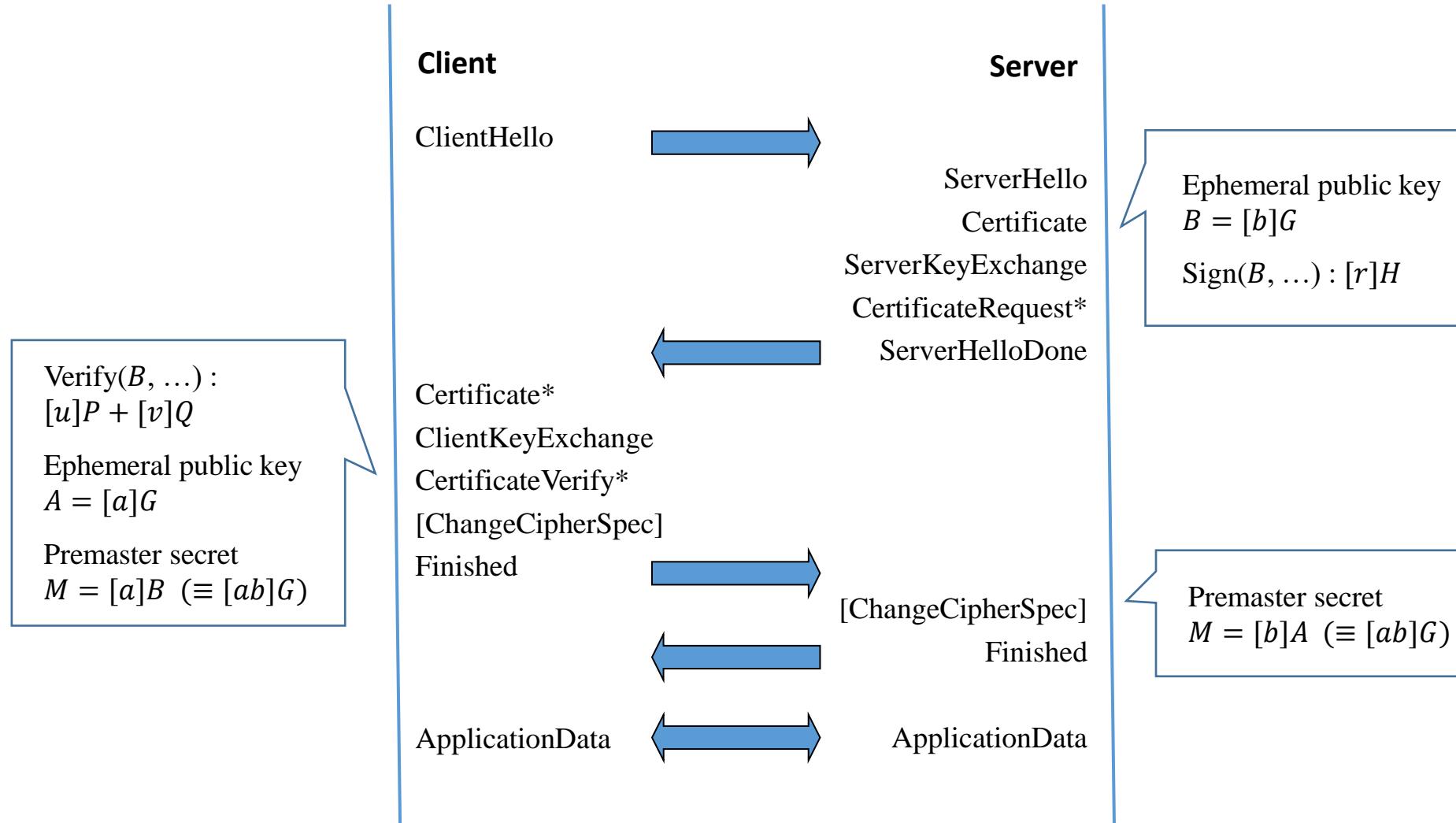
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$$E/\mathbb{F}_p: y^2 = x^3 + ax + b$$

where  $a, b \in \mathbb{F}_p$  and  $\Delta = -16(4a^3 + 27b^2) \neq 0$ .

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- Given points  $P$  and  $Q$ , any of the following cases can arise for  $R = P + Q$ :

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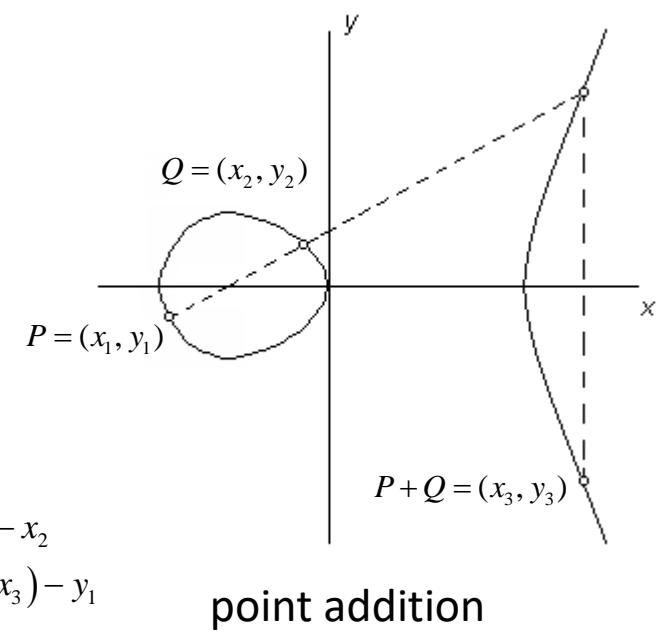
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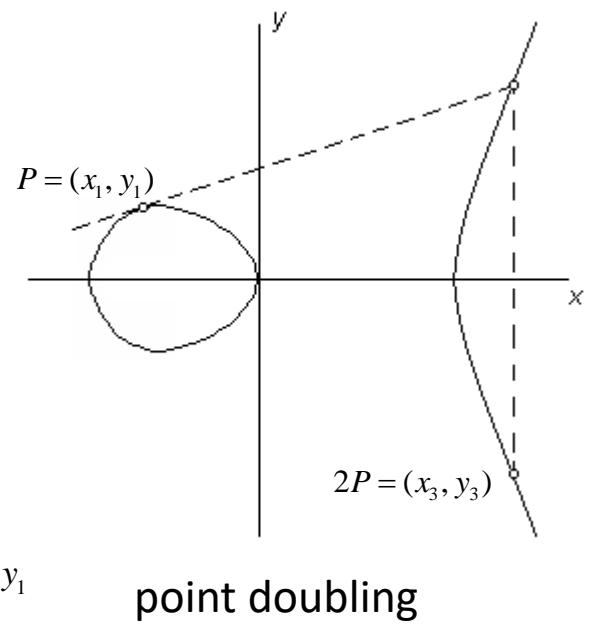
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# Elliptic curve forms

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- Prime order possible
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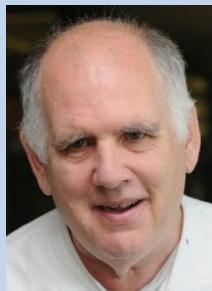


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## Montgomery curves

$$By^2 = x^3 + Ax^2 + x$$

- Subset of curves
- Not prime order
- Montgomery ladder



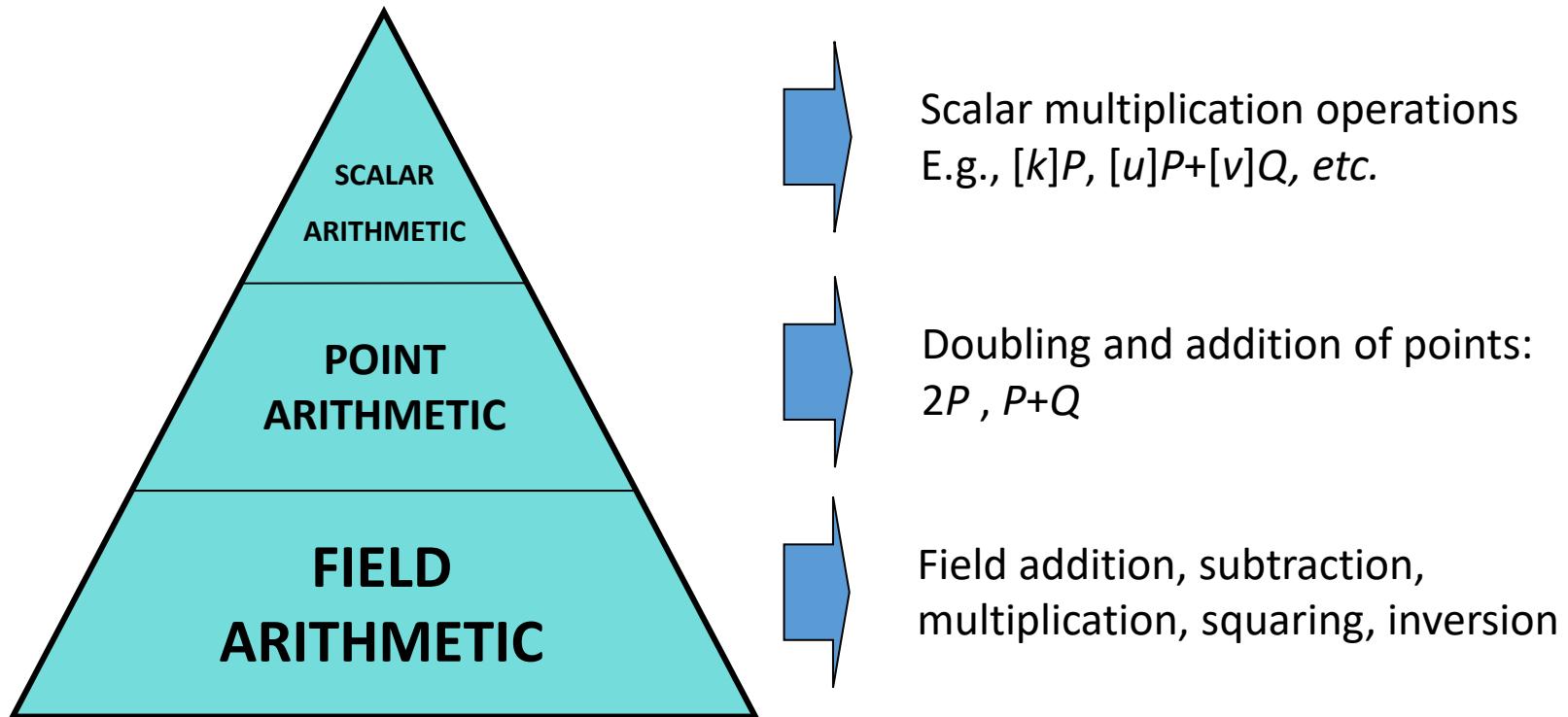
## (Twisted) Edwards curves

$$ax^2 + y^2 = 1 + dx^4y^4$$

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- Not prime order
- Fastest arithmetic
- Some have complete group law



# ECC arithmetic layers



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Unified addition:

- Simple and compact, but expensive

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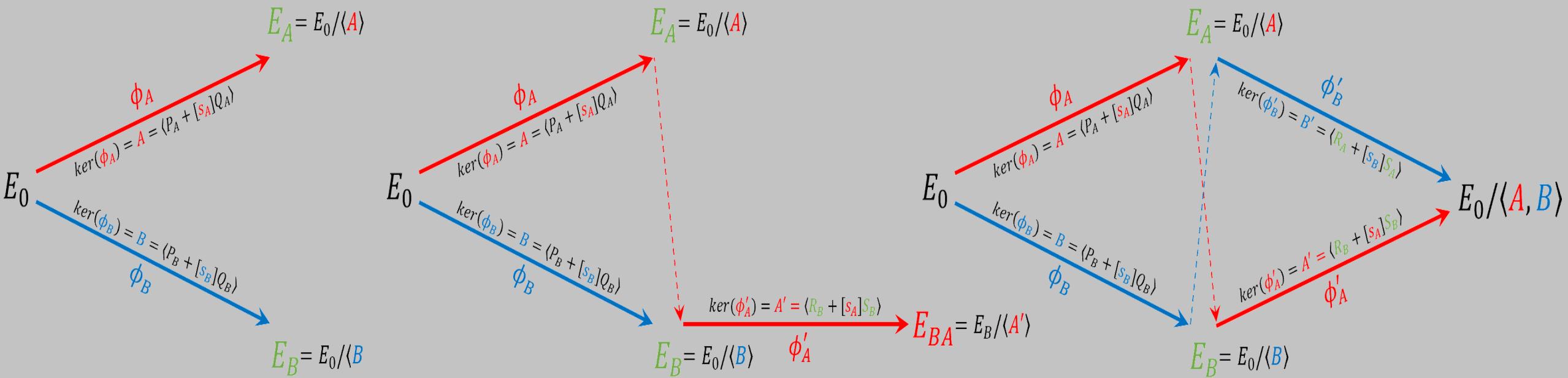
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Today, it runs in...

<b><math>46,000 \text{ cc}</math></b>	<b>Costello-Longa 2015 (FourQ)</b>
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# The case of SIKE

# Supersingular isogeny key exchange

## Supersingular isogeny Diffie-Hellman key exchange (SIDH)

- Proposed by Jao and De Feo in 2011.
- Compared to “predecessors” based on *ordinary isogenies*, SIDH has:
  - Much better performance
  - Exponential complexity of best classical and quantum attacks.

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## Supersingular isogeny key encapsulation (SIKE)

- Designed by Costello–De Feo–Jao–L–Naehrig–Renes in 2017.
- IND-CCA secure key encapsulation protocol based on SIDH.
- Submitted to the NIST PQC standardization process.

# Elliptic curves and isogenies

- Every elliptic curve over a field  $K$  with  $\text{char}(K) > 3$  can be defined in (short) Weierstrass form by

$$E: y^2 = x^3 + ax + b,$$

where  $a, b \in K$  and  $\Delta = -16(4a^3 + 27b^2) \neq 0$ .

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- For an extension field  $L$  of  $K$ , the set of  $L$ -rational points on  $E$

$$E(L) = \{(x, y) \in L \times L : y^2 - x^3 - ax - b = 0\} \cup \{\mathcal{O}\},$$

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- **Isomorphism classes** are determined by the  **$j$ -invariant**:  $j(E) = 1728 \cdot \frac{4a^3}{4a^3+27b^2}$

# Elliptic curves and isogenies

- Let  $E_1$  and  $E_2$  be elliptic curves defined over an extension field  $L$ .
- An isogeny is a (non-constant) rational map

$$\phi: E_1 \rightarrow E_2$$

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*Relevant properties:*

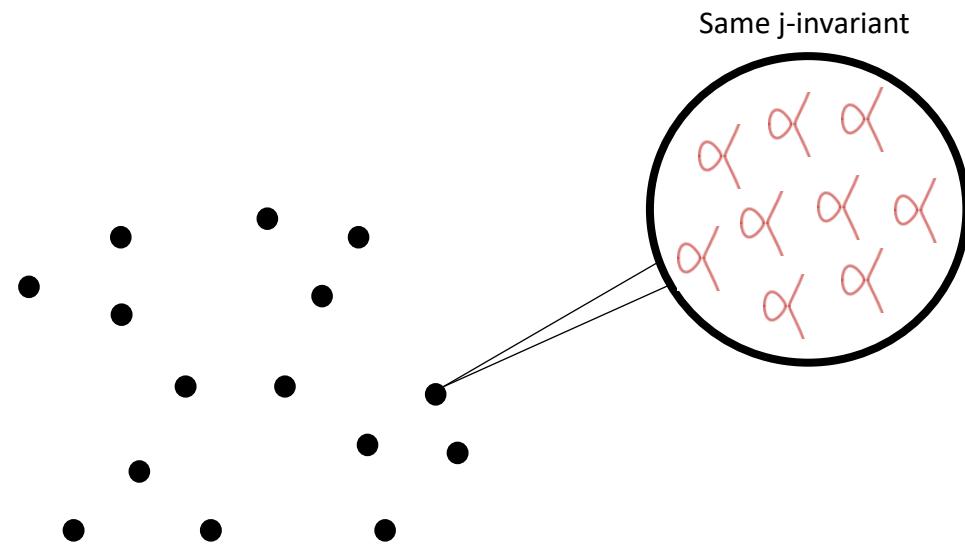
- Isogenies are group homomorphisms.
- For every finite subgroup  $\langle G \rangle \subseteq E_1$ , there is a unique curve  $E_2$  (up to isomorphism) and isogeny  $\phi: E_1 \rightarrow E_2$  with kernel  $\langle G \rangle$ . Write  $E_2 = \phi(E_1) = E_1/\langle G \rangle$ .
- (Separable) isogenies have  $\deg(\phi) = \# \ker(\phi)$ .

# Supersingular curves

- An elliptic curve  $E/L$  is supersingular if  $\#E(L) \equiv 1 \pmod{p}$ .
- All supersingular curves can be defined over  $\mathbb{F}_{p^2}$ .
- There are  $\sim \lfloor p/12 \rfloor$  **isomorphism classes** of supersingular curves.

# Supersingular isogeny graphs

- Vertices: the  $\sim \lfloor p/12 \rfloor$  isomorphism classes of supersingular curves over  $\mathbb{F}_{p^2}$ .

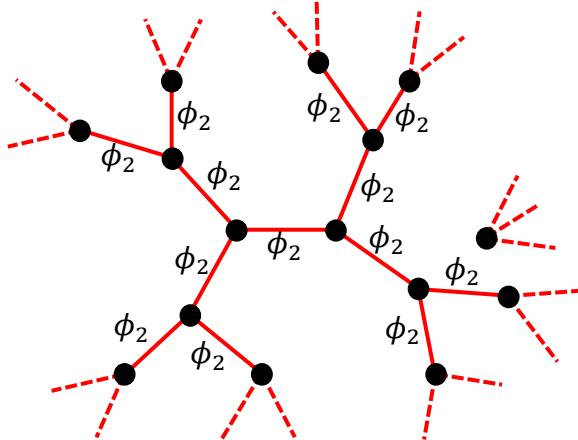


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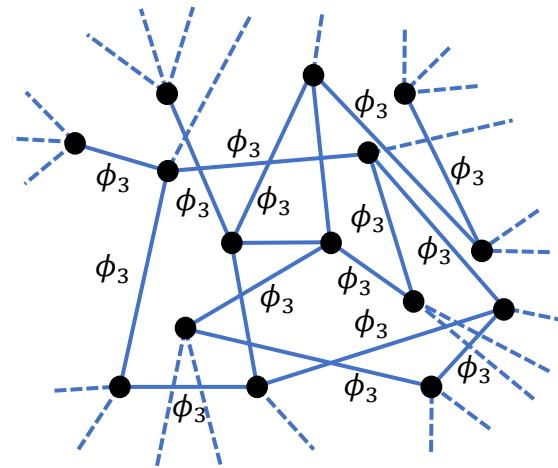
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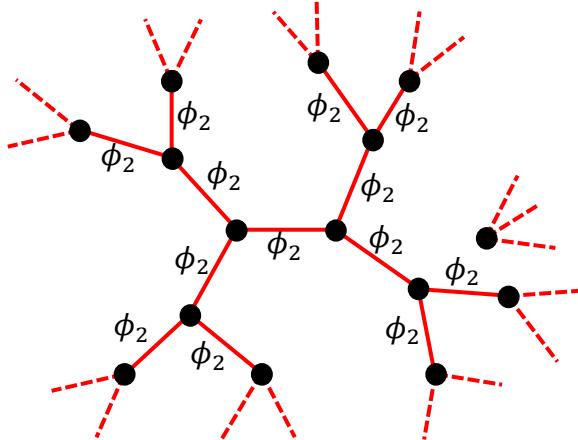


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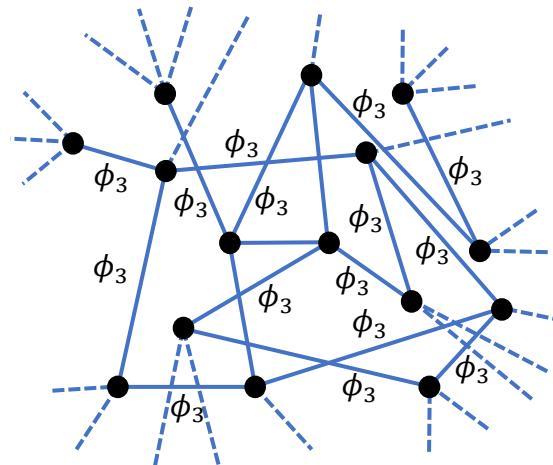
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For any prime  $\ell \nmid p$ , there exist  $(\ell + 1)$  isogenies of degree  $\ell$  originating from every supersingular curve.



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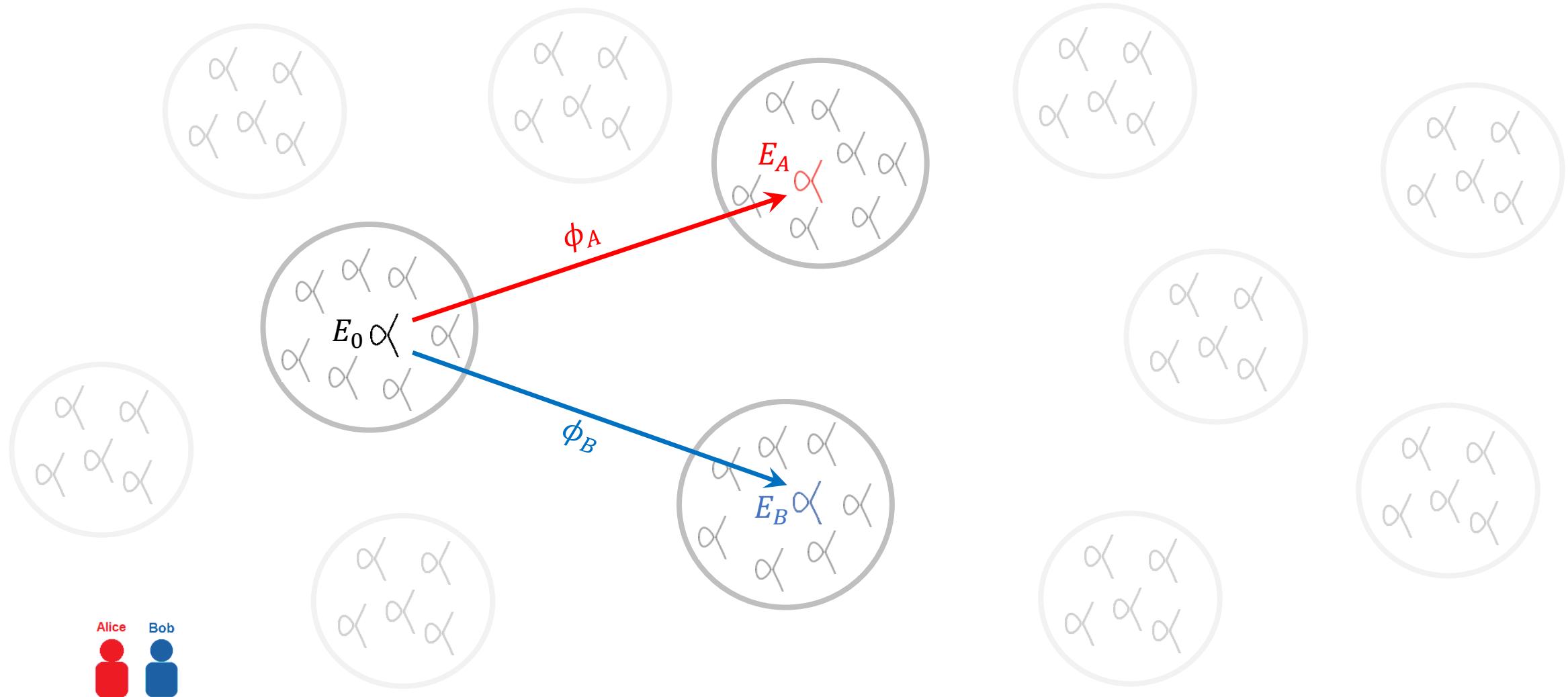
# SIDH in a nutshell



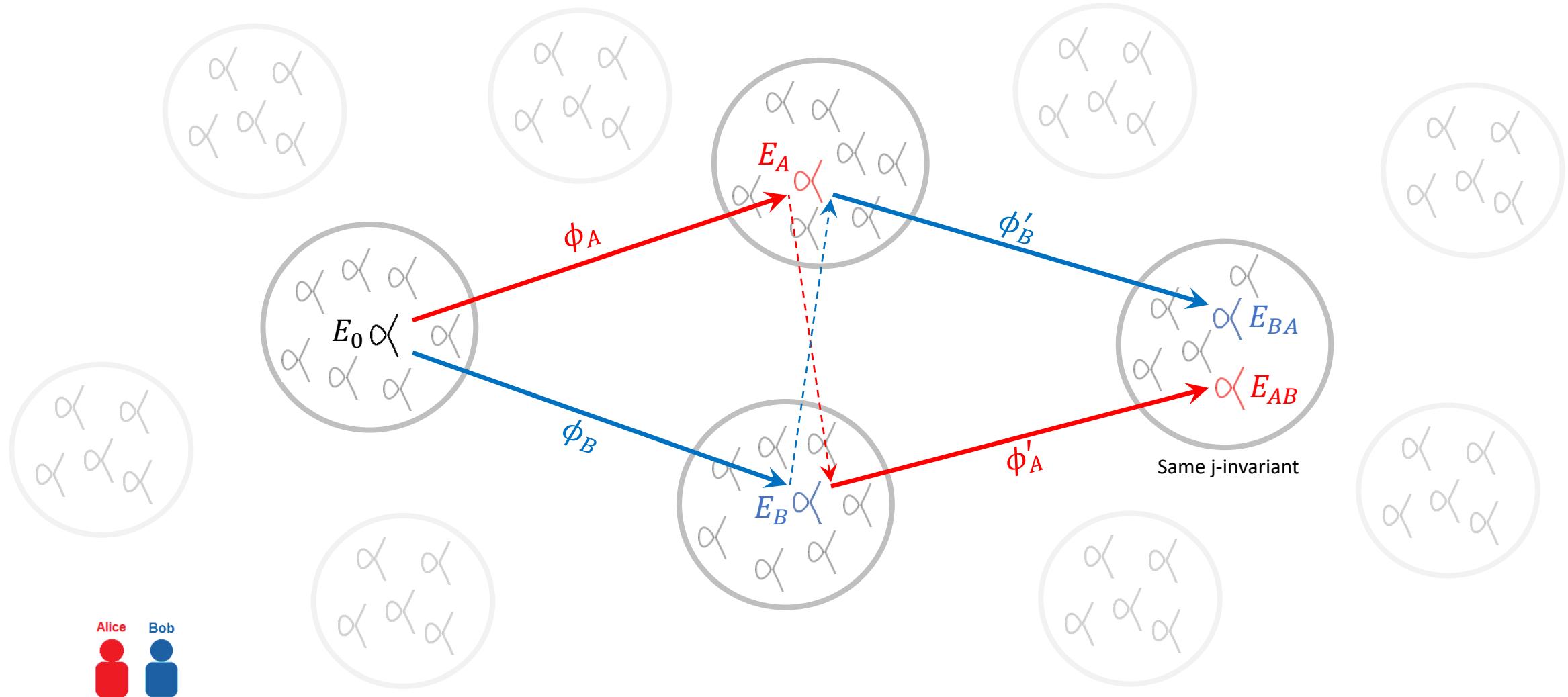
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# SIDH: setup

Set  $\ell \in \{2,3\}$ , supersingular curve  $E_0/\mathbb{F}_{p^2}$  with a prime  $p = f \cdot 2^{e_A} 3^{e_B} - 1$  such that  $2^{e_A} \approx 3^{e_B}$  and  $f$  small.

- Then:  $E[2^{e_A}], E[3^{e_B}] \subset E_0(\mathbb{F}_{p^2})$

Alice



works over  $E[2^{e_A}]$  using **2-isogenies** and linearly independent points  $P_A, Q_A$ .

Bob



works over  $E[3^{e_B}]$  using **3-isogenies** and linearly independent points  $P_B, Q_B$ .

# SIDH protocol

private Alice    private Bob  
public              params

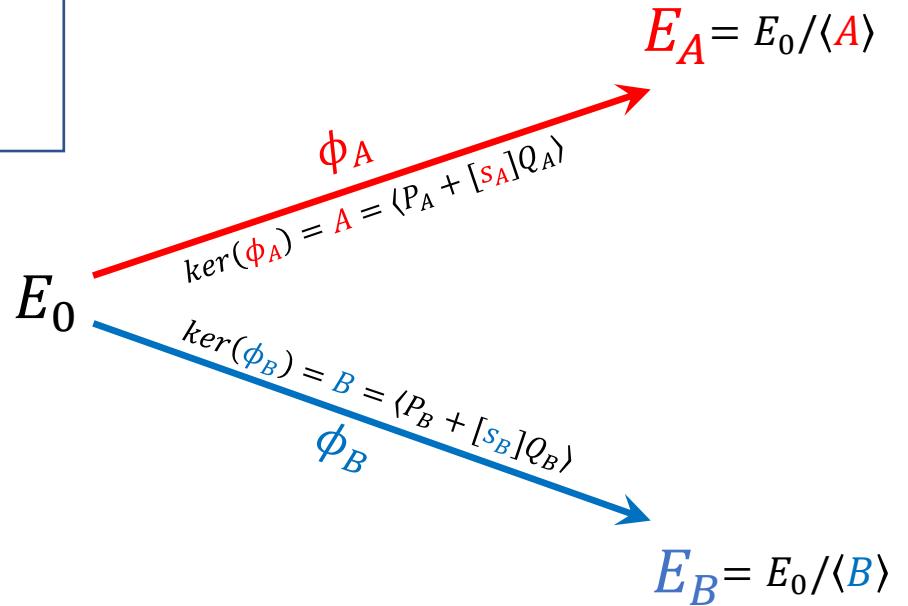
$E$ 's are isogenous curves  
 $P$ 's,  $Q$ 's,  $R$ 's,  $S$ 's are points

$$E_0 \xrightarrow{\phi_A} E_A = E_0 / \langle A \rangle$$

$\ker(\phi_A) = A = \langle P_A + [s_A]Q_A \rangle$

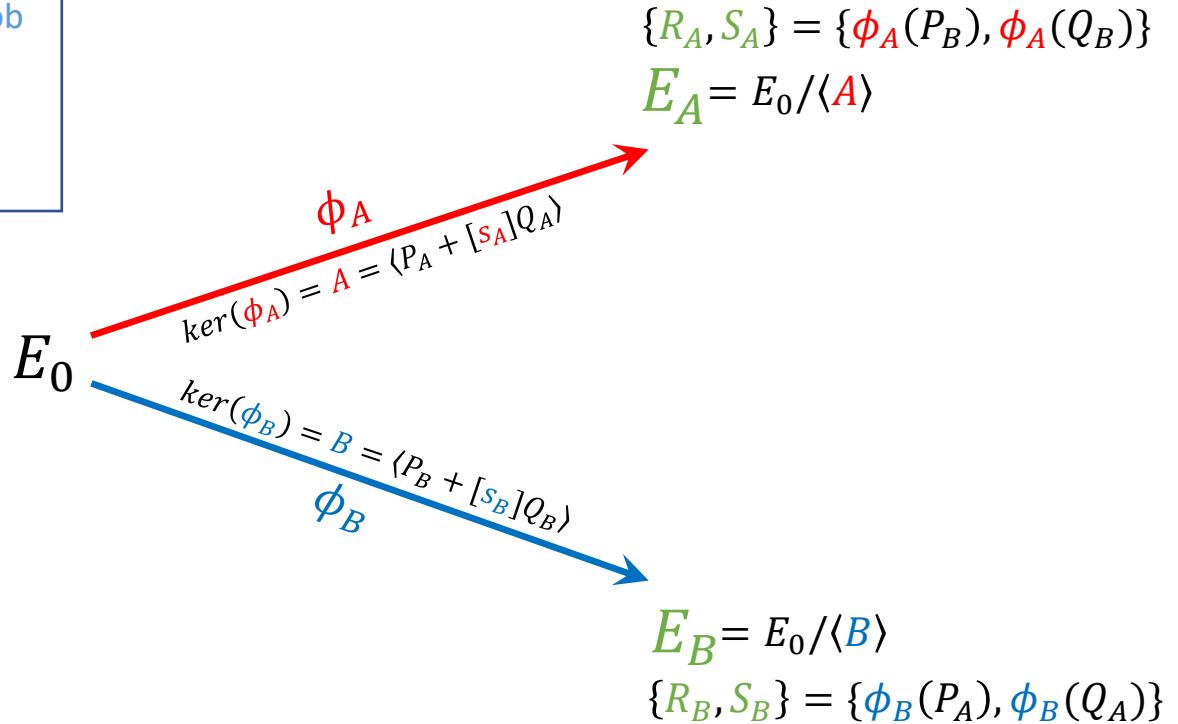
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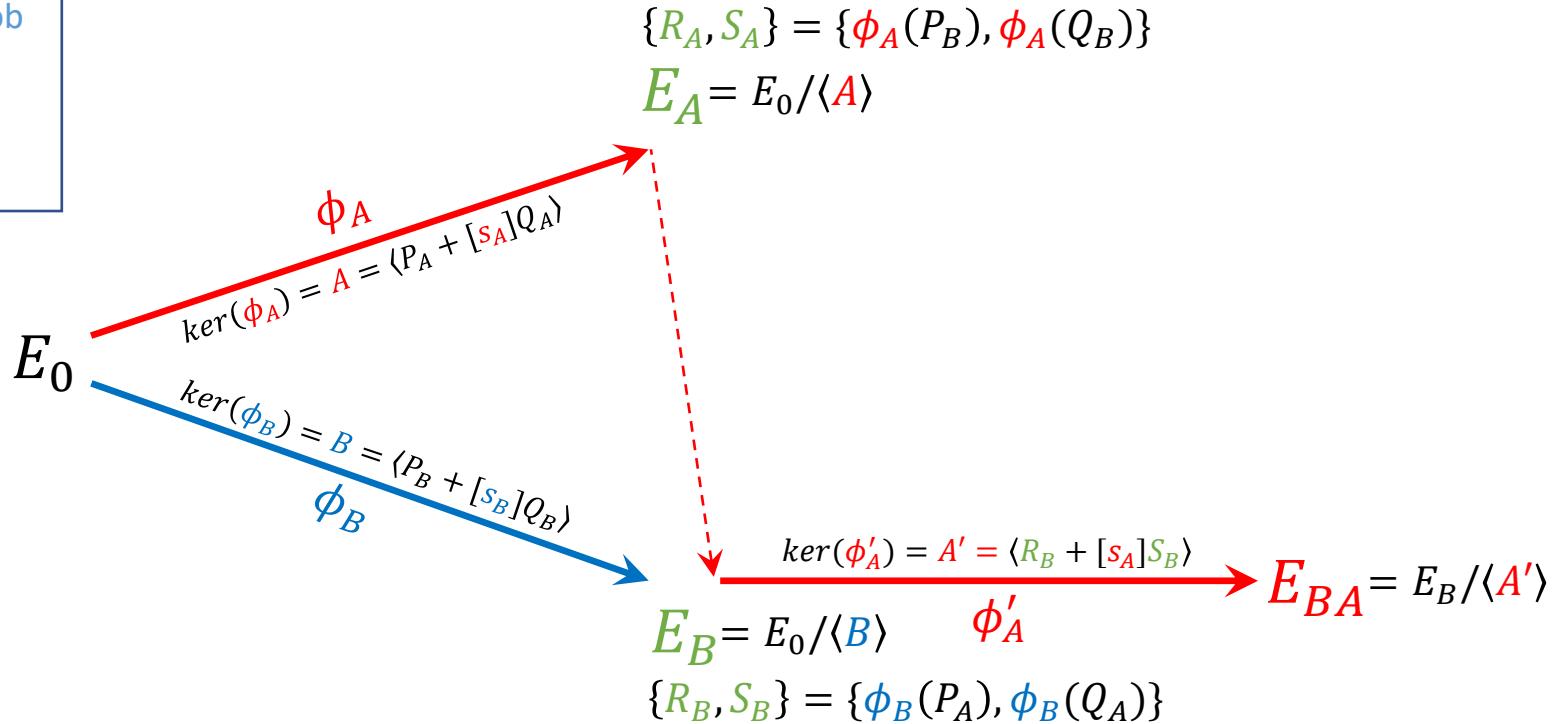
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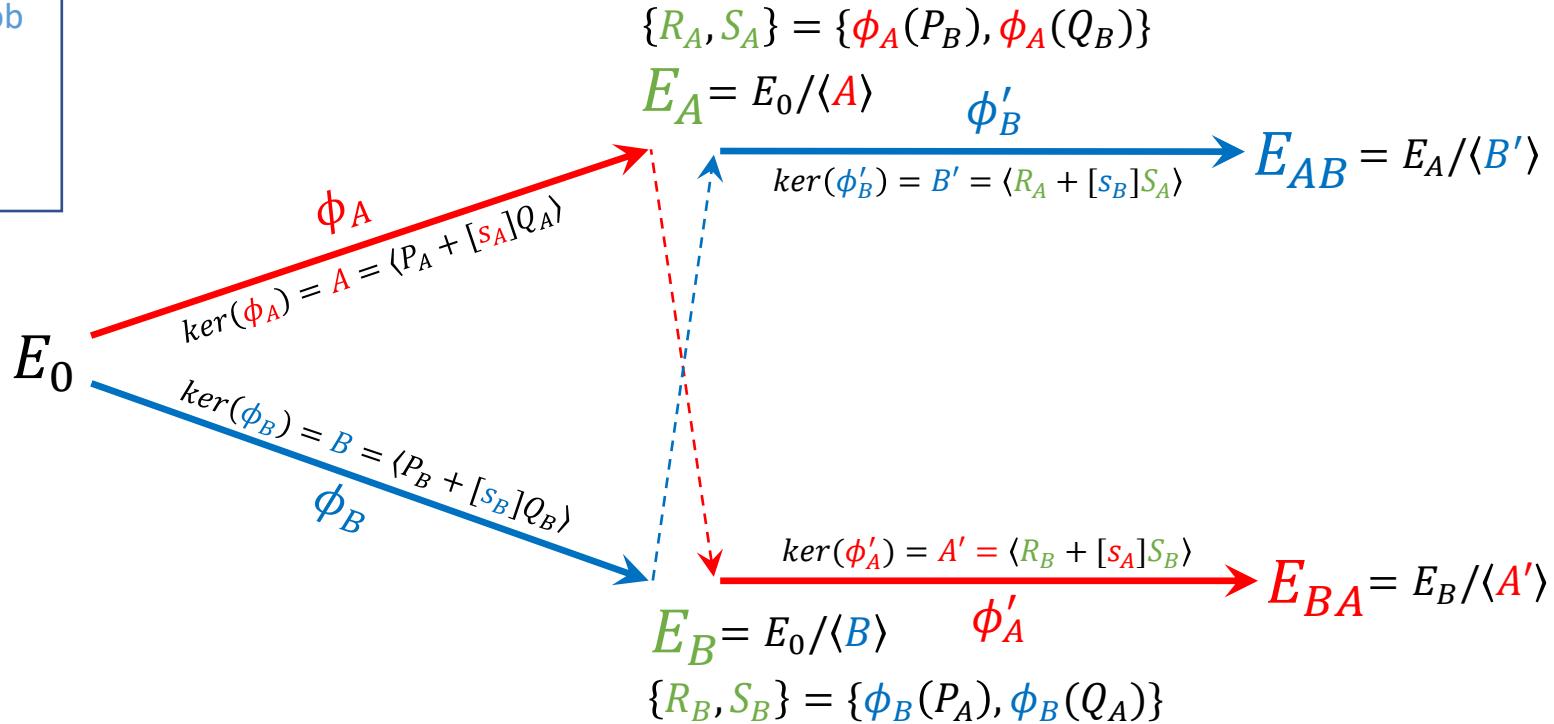
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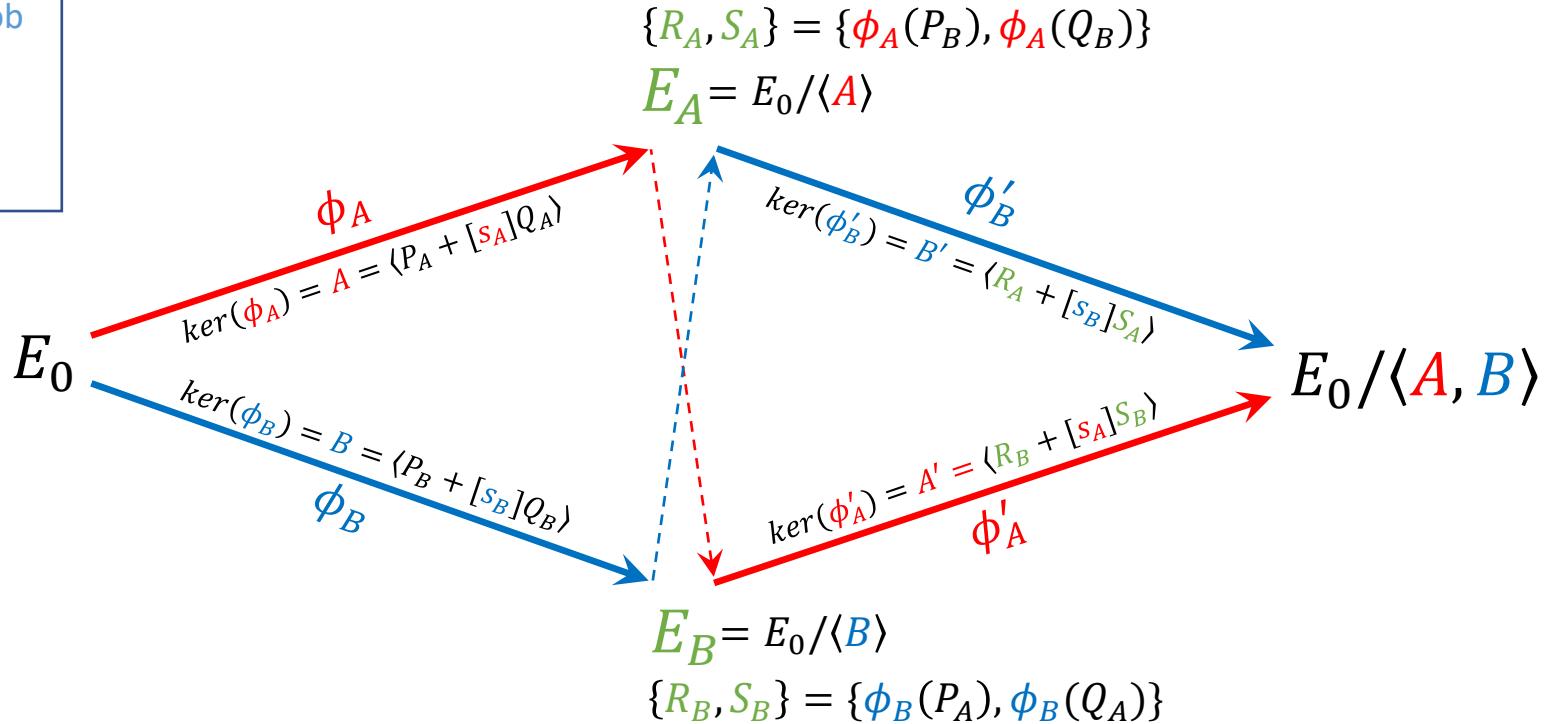
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$$E_{AB} = \phi'_B(\phi_A(E_0)) \cong E_0/\langle P_A + [s_A]Q_A, P_B + [s_B]Q_B \rangle \cong E_{BA} = \phi'_A(\phi_B(E_0))$$

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# SIDH protocol

## ***Drawback:***

- SIDH is not secure when keys are reused (Galbraith-Petit-Shani-Ti 2016)
  - Only recommended in **ephemeral mode**

# Supersingular isogeny key encapsulation (SIKE)

- IND-CCA secure key encapsulation: no problem reusing keys!
- Uses a variant of Hofheinz–Hövelmanns–Kiltz (HHK) transform:  
**IND-CPA PKE → IND-CCA KEM**
- HHK transform is secure in **both the classical and quantum ROM models**
- Offline key generation gives performance boost (no perf loss SIDH → SIKE)

# Supersingular isogeny key encapsulation (SIKE)

## KeyGen

---

1.  $s_B \in_R [0, 2^{\lfloor \log_2 3^{e_B} \rfloor})$
  2. Set  $\ker(\phi_B) = \langle P_B + [s_B]Q_B \rangle$
  3.  $\text{pk}_B = \{\phi_B(E_0), \phi_B(P_A), \phi_B(Q_A)\}$
  4.  $s \in_R \{0,1\}^n$
  5. **keypair:**  $\{\text{sk}_B = (s, s_B), \text{pk}_B\}$
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$F, G, H$  instantiated with cSHAKE256.

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1.  $j' = j(E_{BA}) = j(\phi'_B(\phi_A(E_0)))$
  2.  $m' = F(j') \oplus c[2]$
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  6. If  $\text{pk}'_A = c[1]$  then  
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$\text{pk}_B$

$c = (\text{pk}_A, F(j) \oplus m)$

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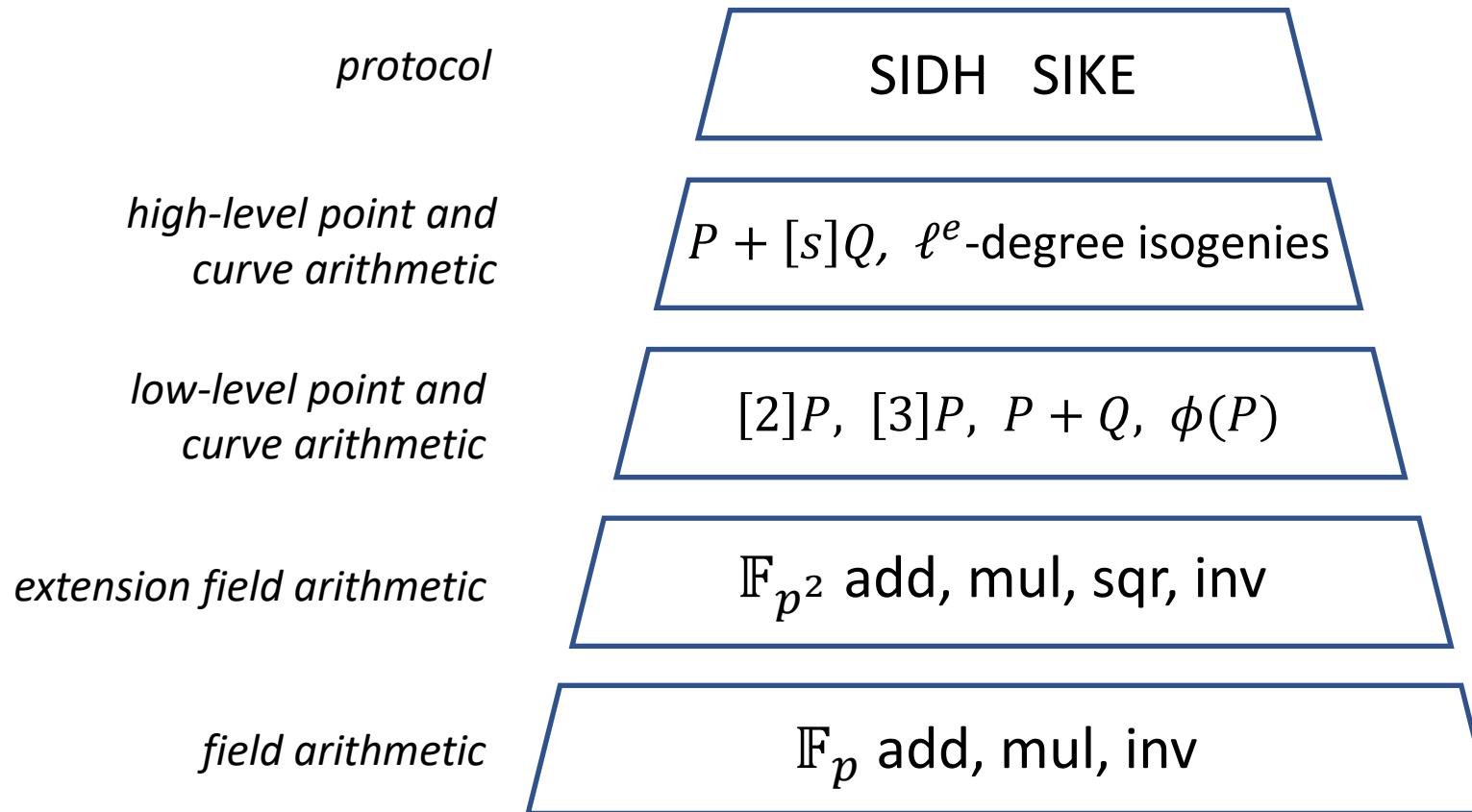
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# Computational aspects

# Computation layers



Computational aspects:  
High-level point and curve arithmetic

# High-level point and curve arithmetic

Two main internal computations:

- **Double-scalar multiplications** to construct kernels  $\langle P + [s]Q \rangle$
- **Smooth,  $\ell^e$ -degree isogeny** computations  $\phi: E_0 \rightarrow E'$

# Computing $P + [s]Q$

Three-point differential ladder (x-only, variable point)

- De Feo-Jao-Plût (2014), step cost = **1DBL + 2ADD**
- Faz-Hernández et al. (2018), step cost = **1DBL + 1ADD**

# Computing $P + [s]Q$

[Faz-Hernández–López–Ochoa-Jiménez–Rodríguez-Henríquez 2018]

$$s = (01100)_2$$

$$R_1 = P$$

$$R_0 = Q$$

$$R_2 = Q - P$$

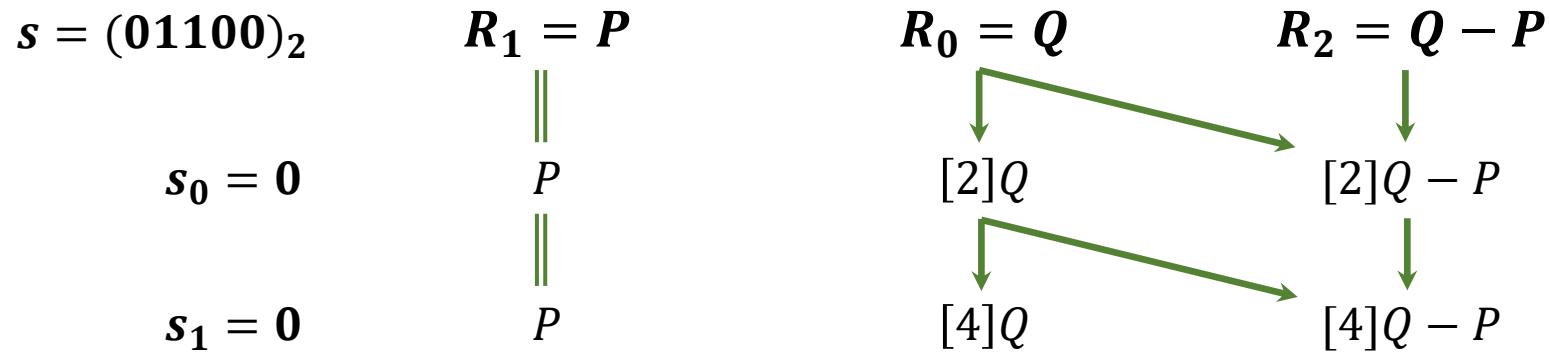
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$$\begin{array}{llll} s = (01100)_2 & R_1 = P & R_0 = Q & R_2 = Q - P \\ s_0 = 0 & \parallel P & \downarrow [2]Q & \downarrow [2]Q - P \end{array}$$

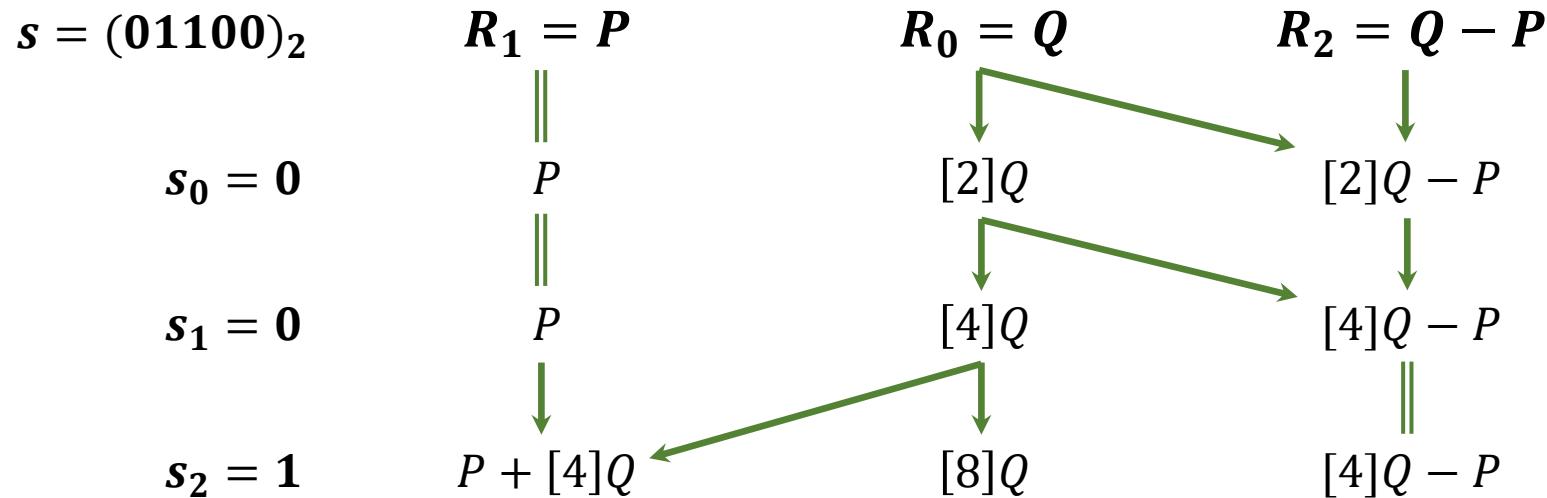
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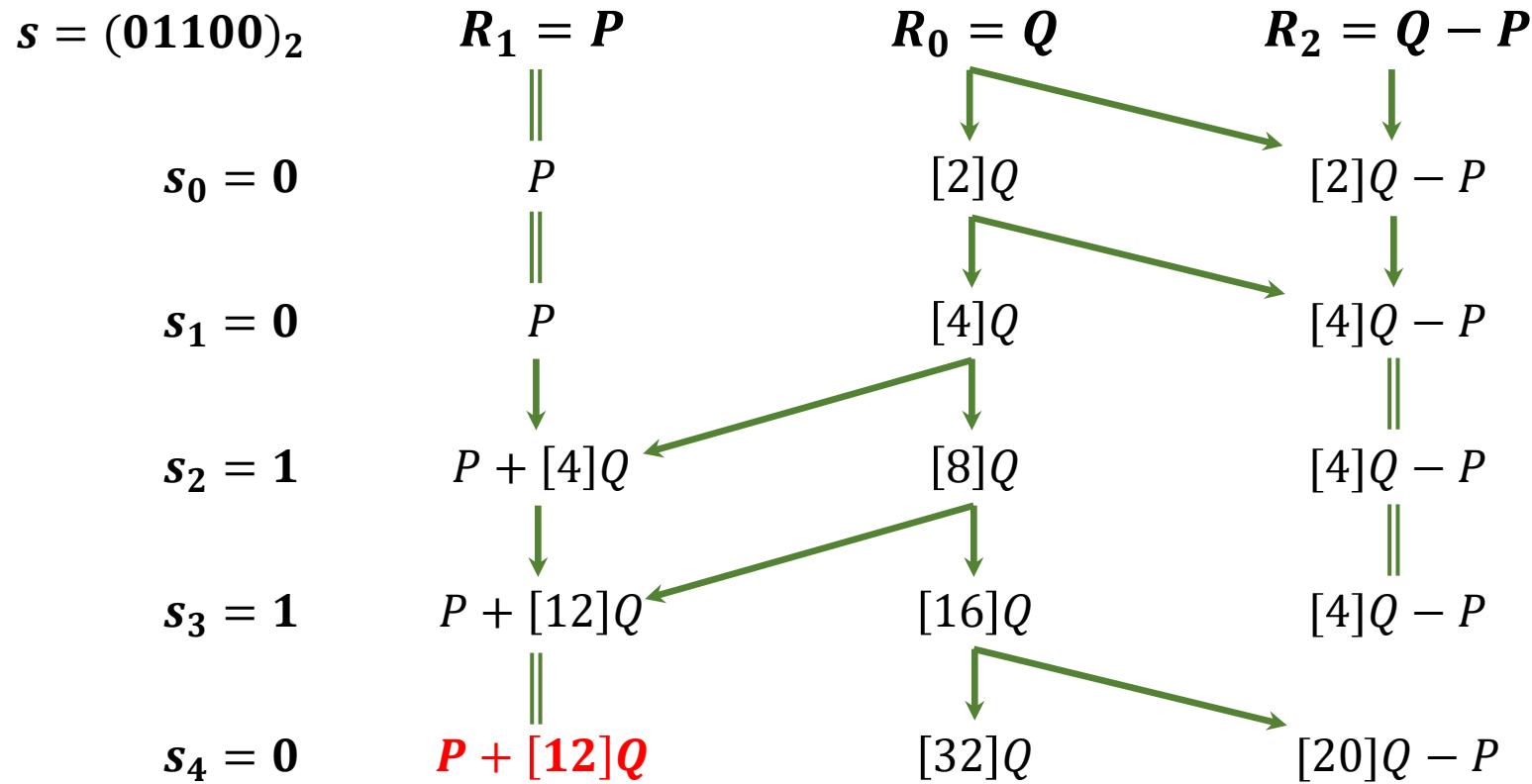
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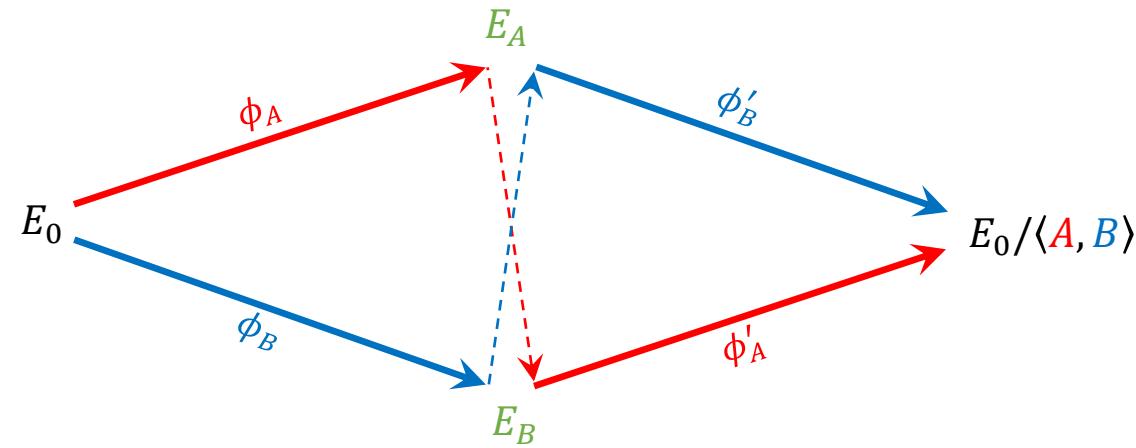
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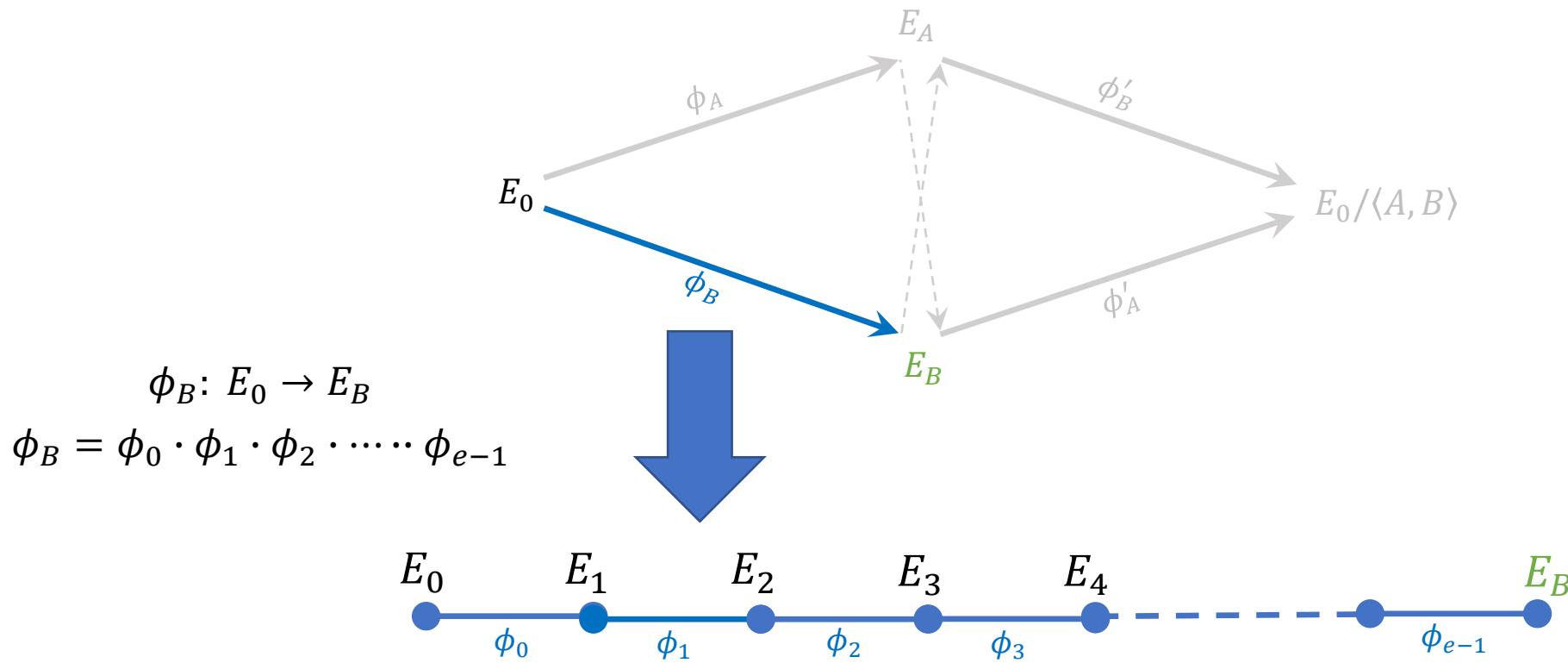
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- **Example:** Bob ( $\ell = 3$ ) computes  $E_B = \phi_B(E_0)$

Let base point  $P_0 \in E_0$ . Assume  $e = 4$

Compute  $3^4$ -degree isogeny:

$$\phi_B: E_0 \rightarrow E_4$$

$$\phi_B = \phi_0 \cdot \phi_1 \cdot \phi_2 \cdot \phi_3$$

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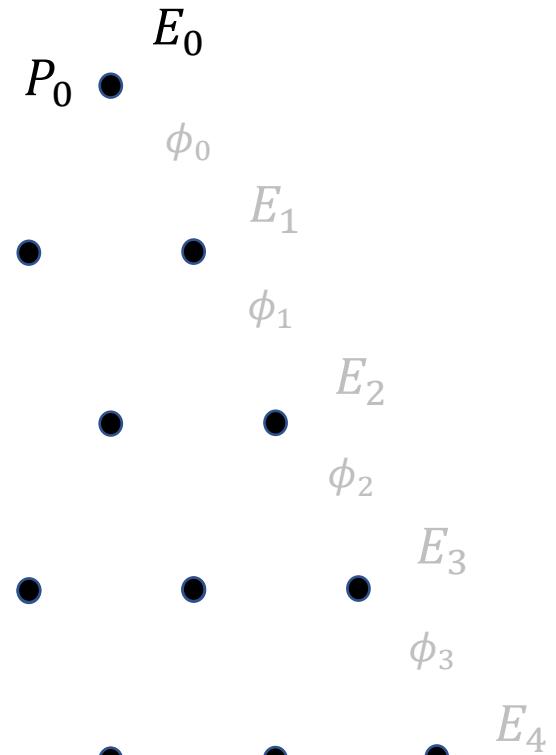
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$$E_4 = E_0 / \langle P_0 \rangle$$



- Iteratively compute:

$$E_{i+1} = E_i / \langle [\ell^{e-i-1}]P_i \rangle$$

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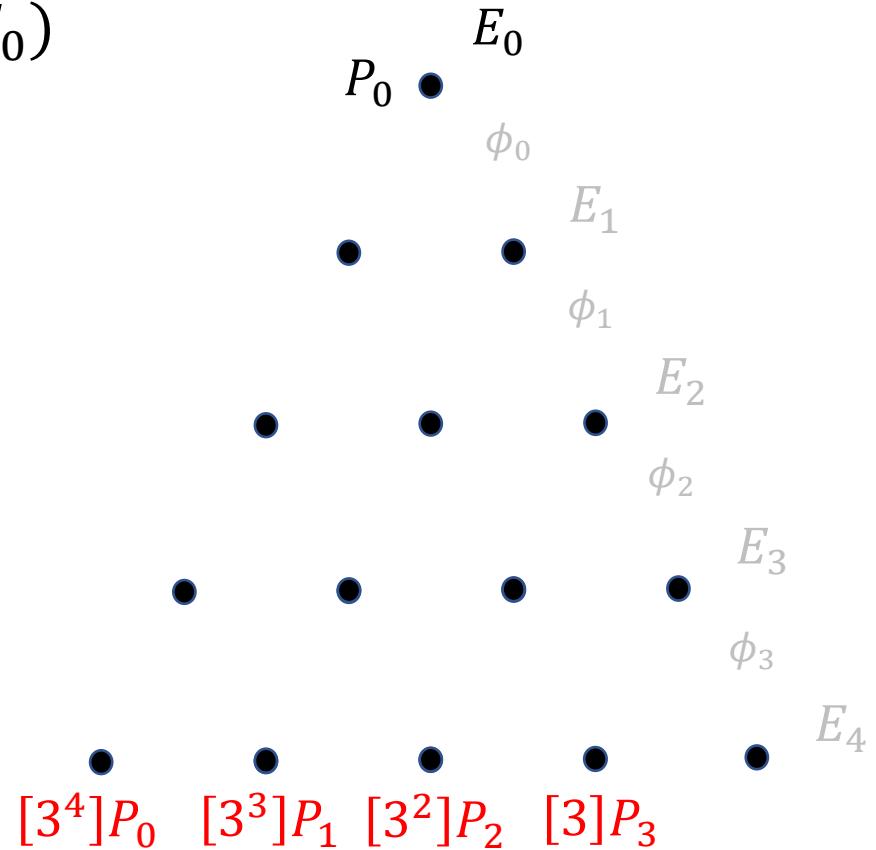
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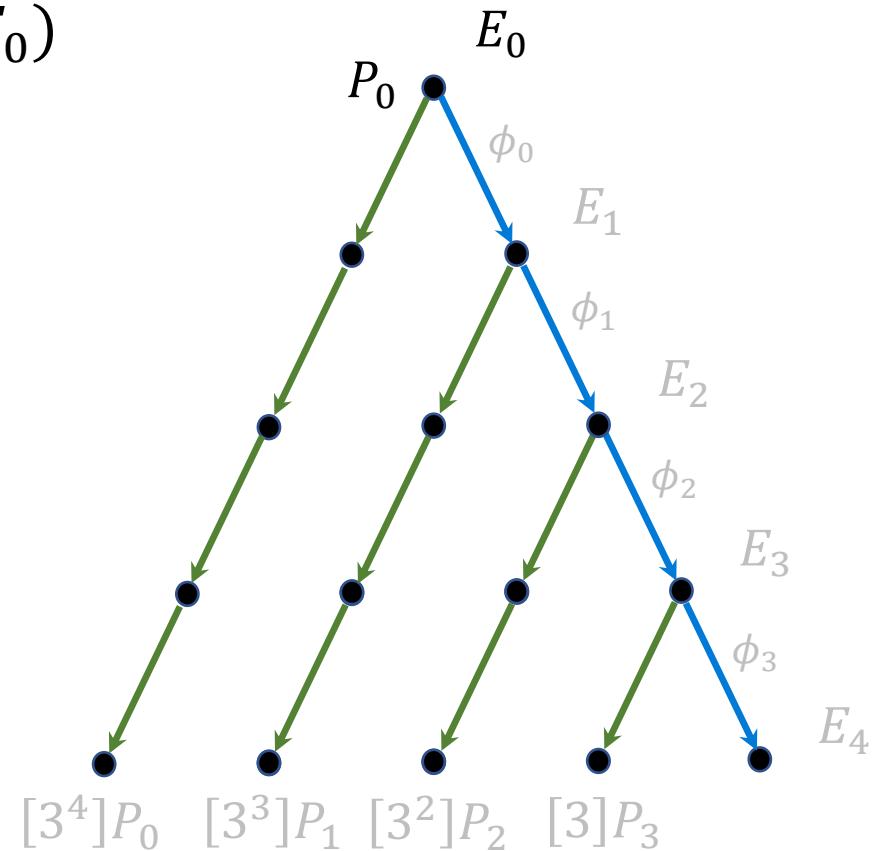
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$$E_4 = E_0 / \langle P_0 \rangle$$

- Iteratively compute:

$$E_{i+1} = E_i / \langle [\ell^{e-i-1}]P_i \rangle$$



(+) slope: point operations  
(-) slope: isogeny operations

# Computing $\ell^e$ -degree isogenies

- **Example:** Bob ( $\ell = 3$ ) computes  $E_B = \phi_B(E_0)$

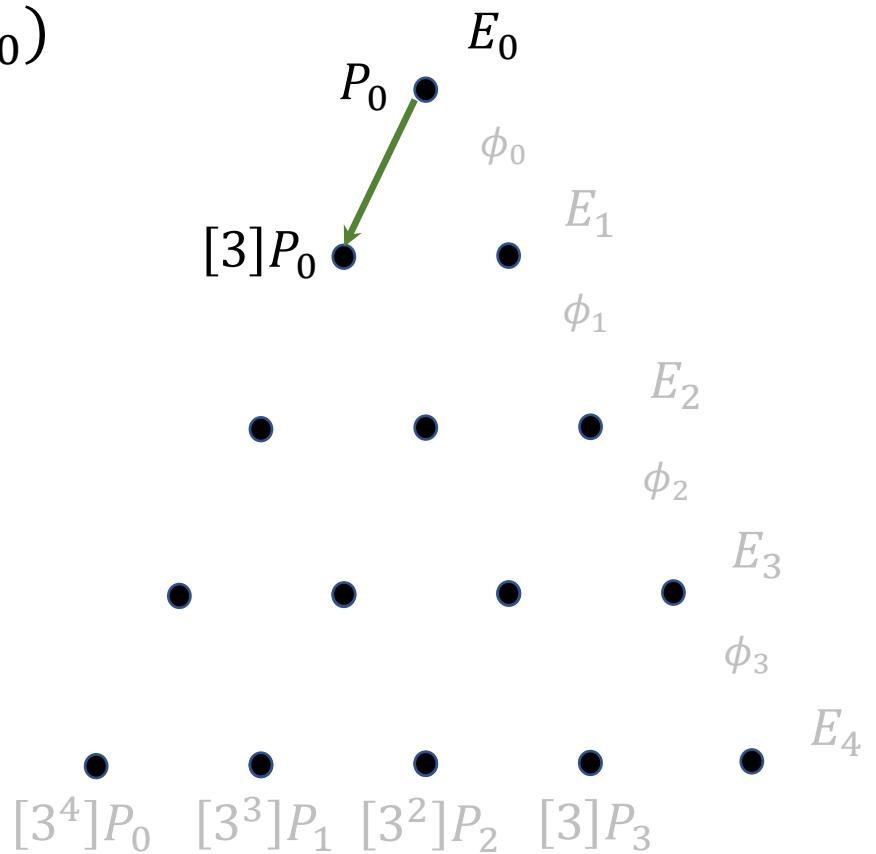
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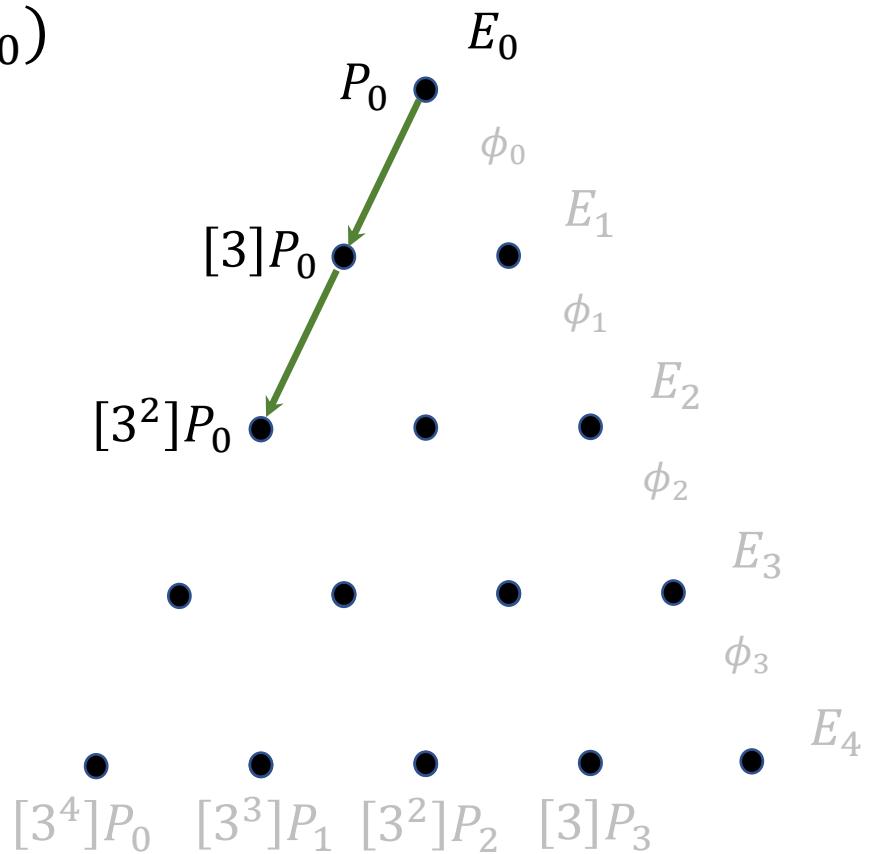
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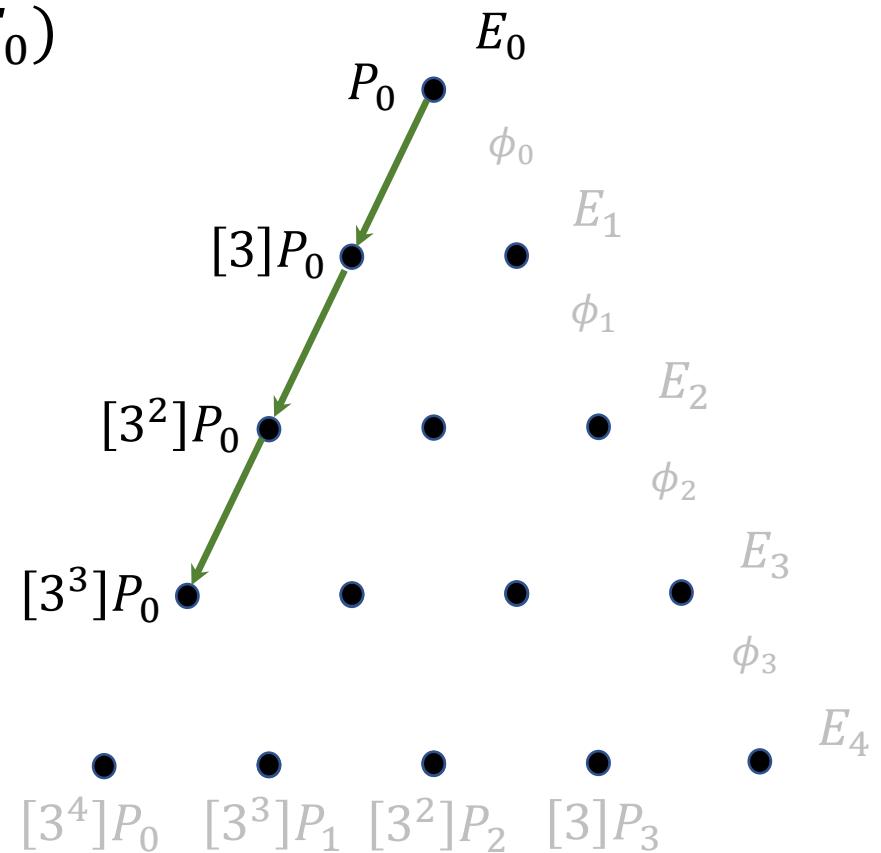
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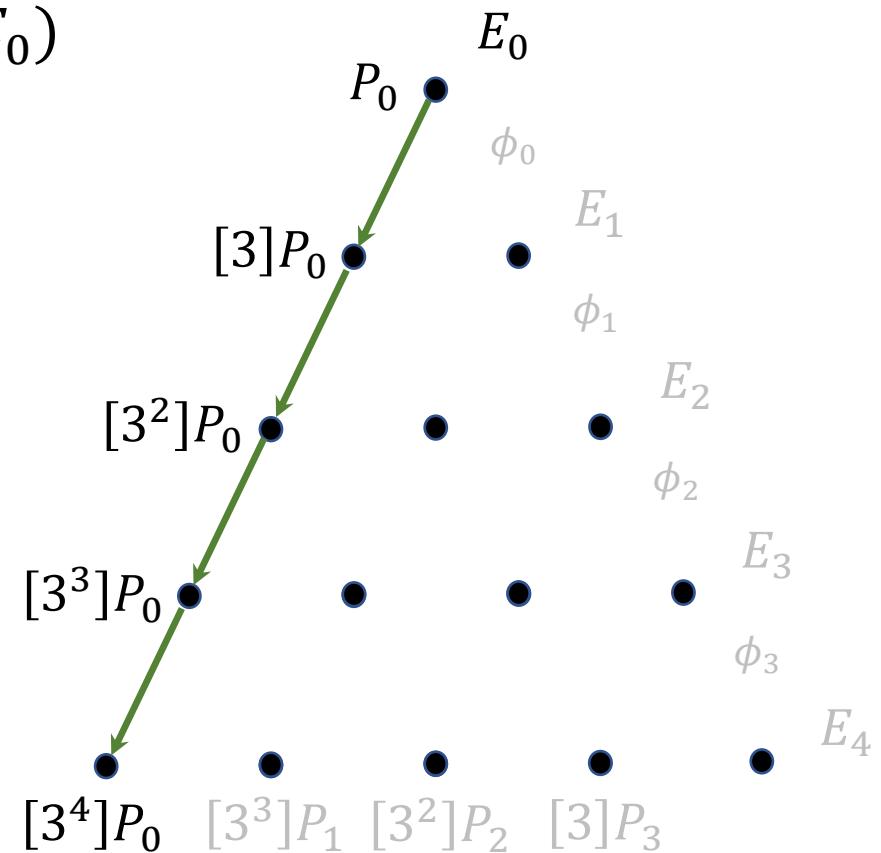
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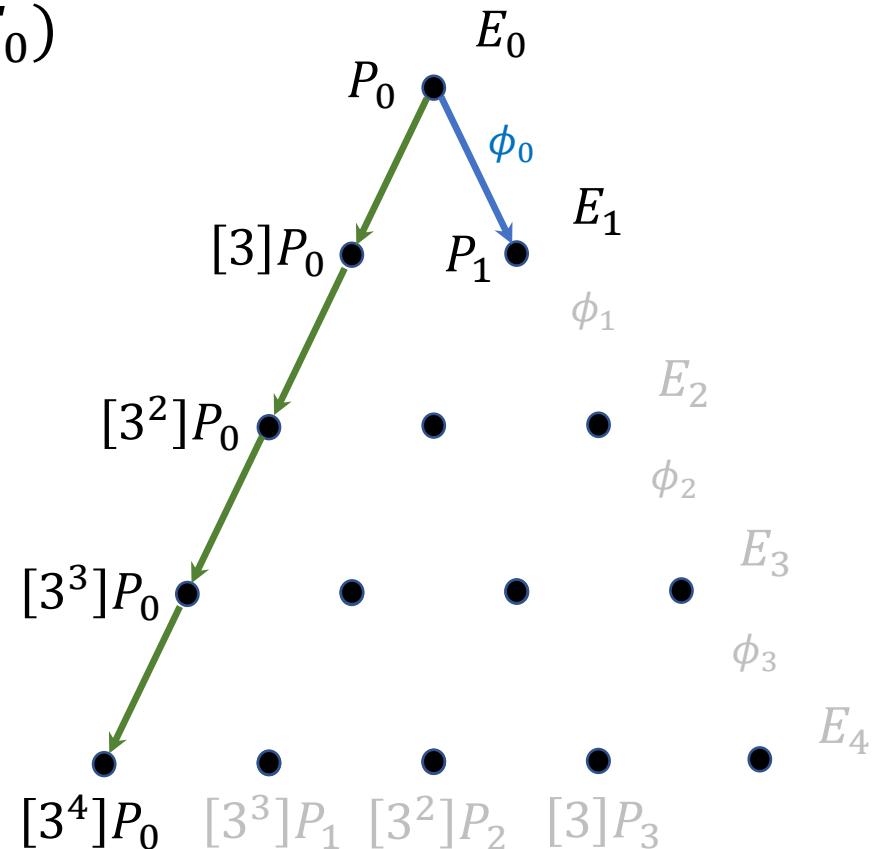
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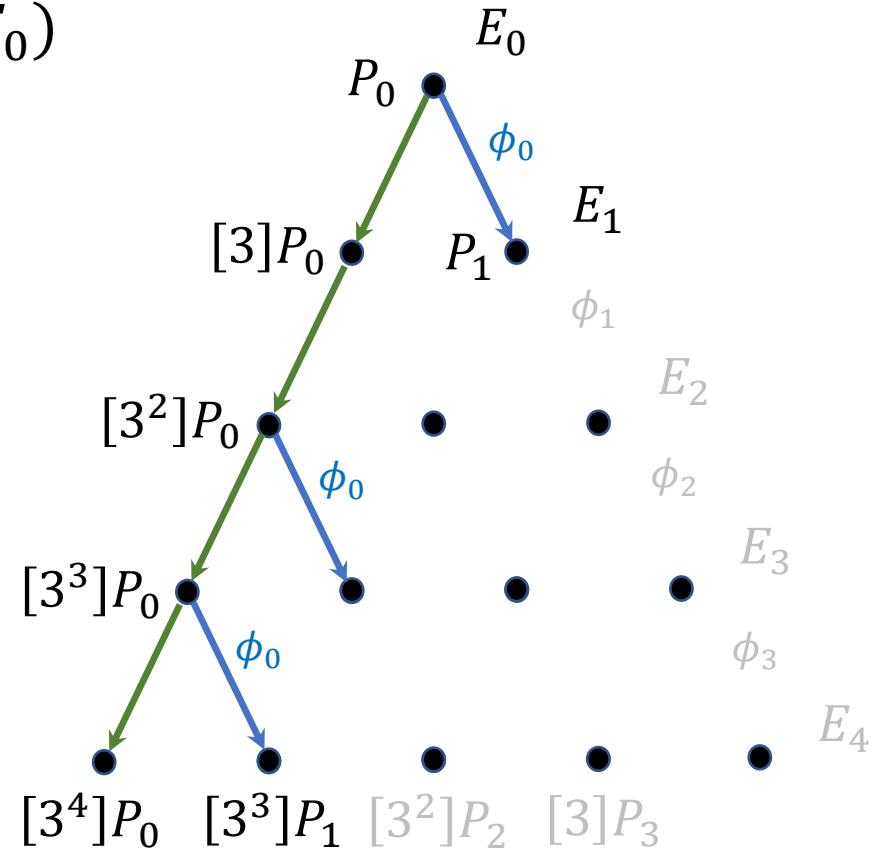
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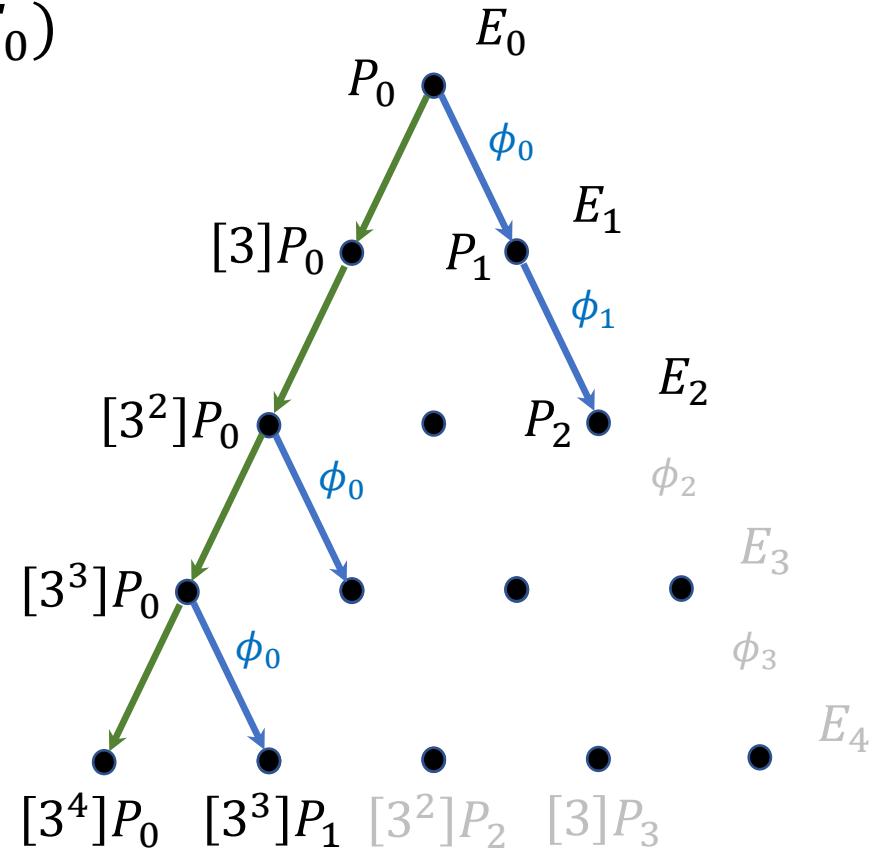
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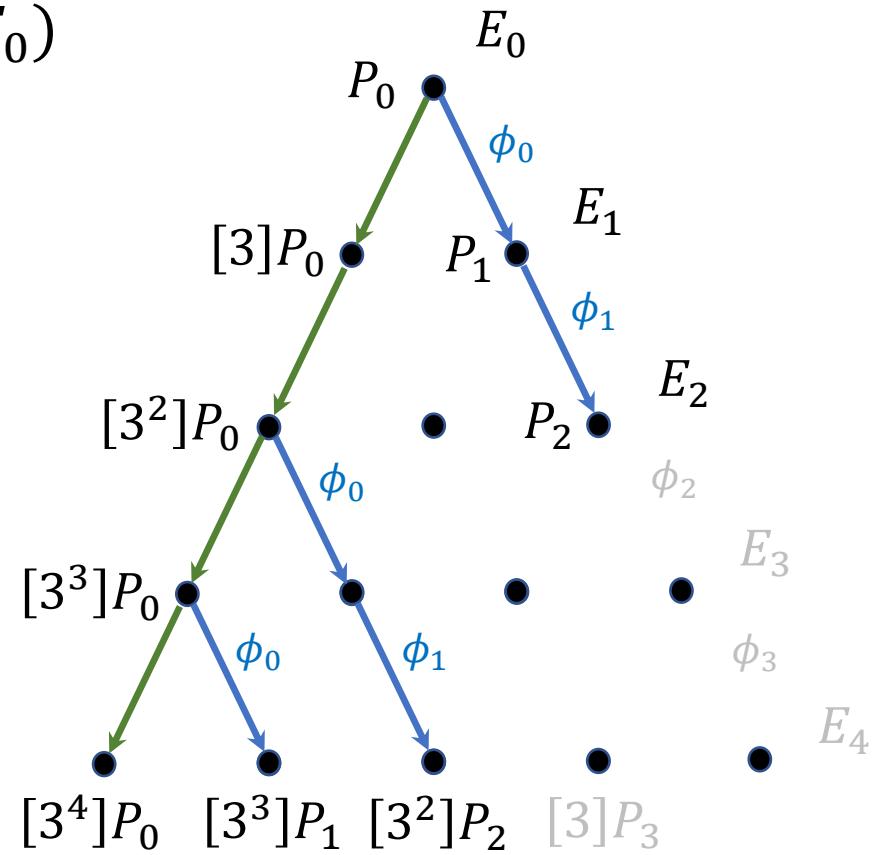
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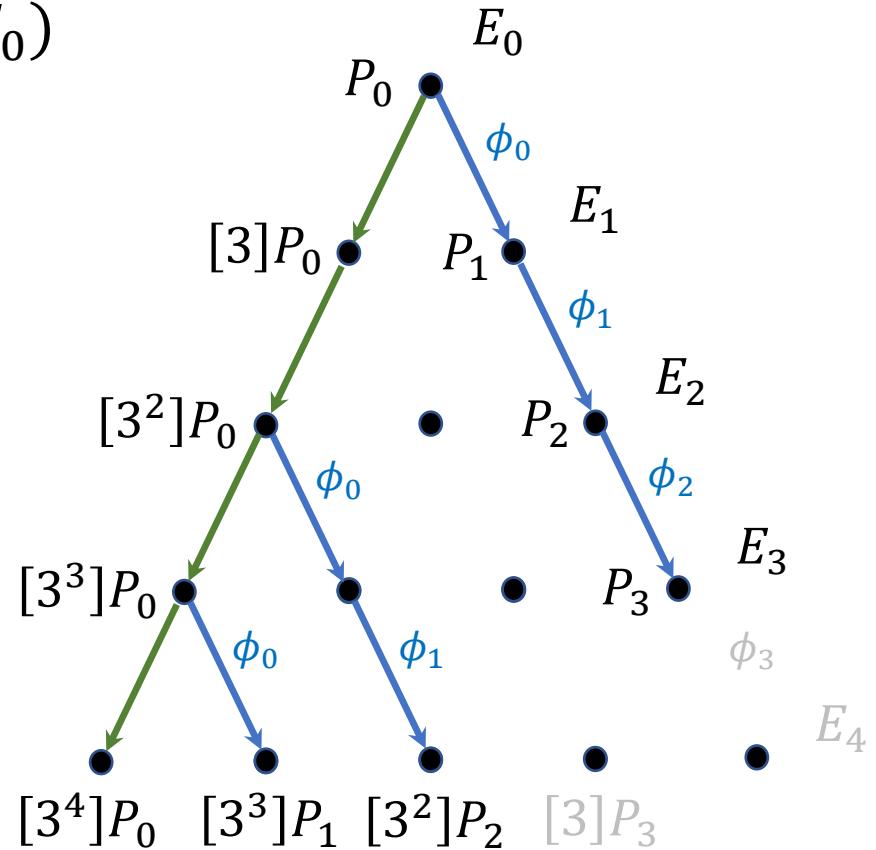
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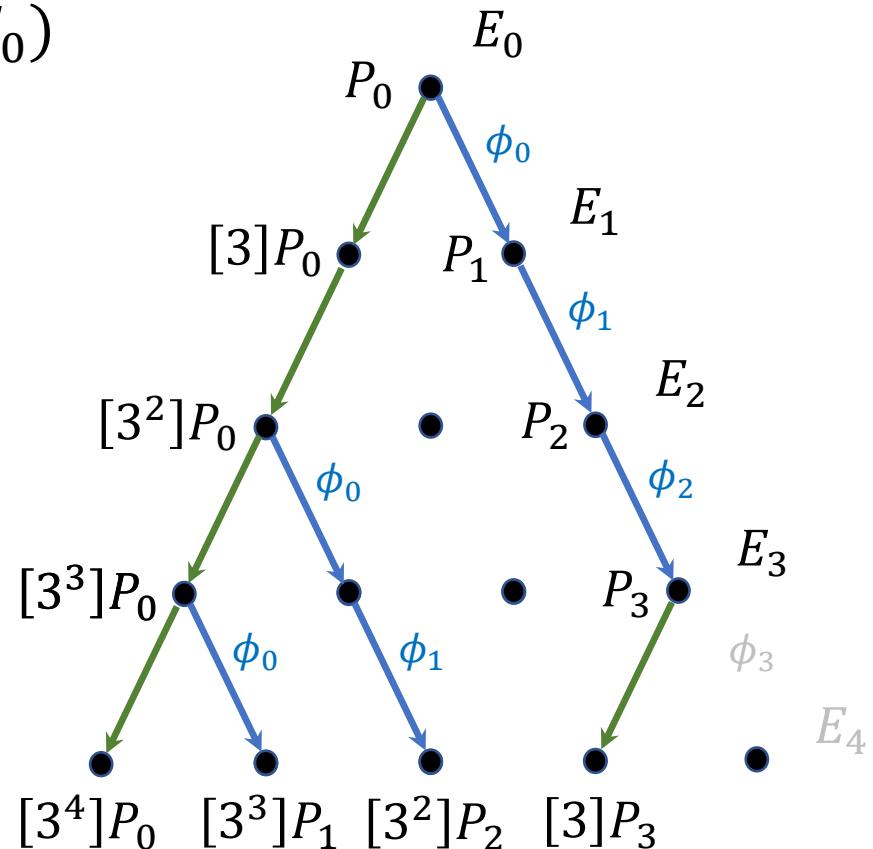
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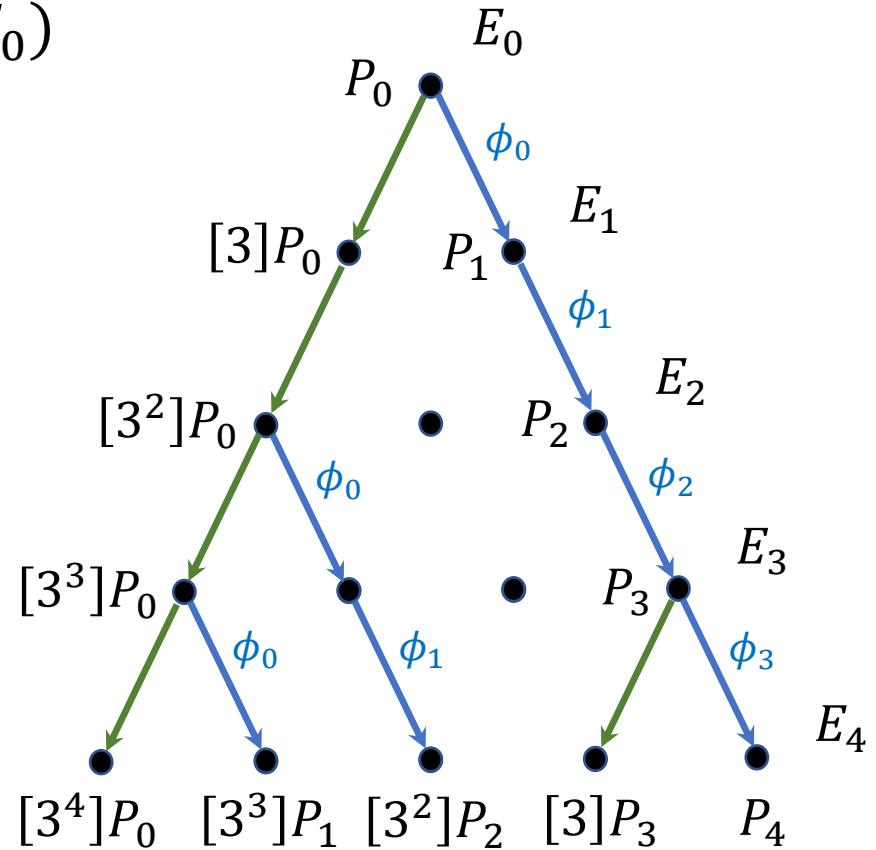
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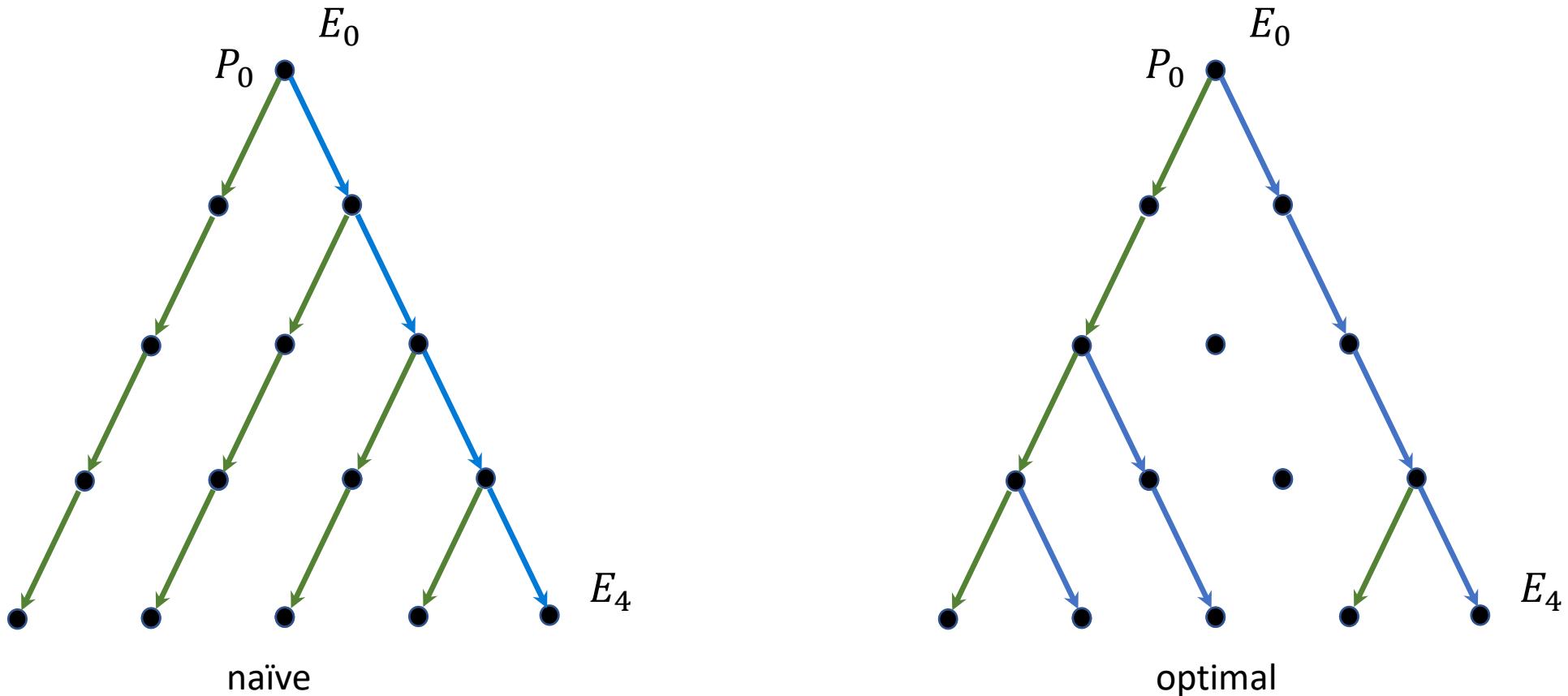
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$$E_4 = \phi_3(E_3)$$

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# Computing $\ell^e$ -degree isogenies



**Optimal strategy:** reduction from  $\mathcal{O}(e^2)$  operations to  $\mathcal{O}(e \log e)$

# Computational aspects: Field arithmetic

# Extension field arithmetic

**Constructing degree-2 extension field  $\mathbb{F}_{p^2}$  of a finite field  $\mathbb{F}_p$ :**

Fix  $\mathbb{F}_{p^2} = \mathbb{F}_p(\alpha)$ , with degree-2 irreducible polynomial  $f(x)$  in  $\mathbb{F}_p[x]$  s.t.  $f(\alpha) = 0$

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In our case: for a prime  $p \equiv 3 \pmod{4}$ , take  $\mathbb{F}_{p^2} = \mathbb{F}_p(i)$ , with  $i^2 + 1 = 0$

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Assume  $\mathbb{F}_{p^2} = \mathbb{F}_p(i)$ , with  $i^2 + 1 = 0$

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**cost:** 2  $\mathbb{F}_p$  mul + 2  $\mathbb{F}_p$  sqr + 1  $\mathbb{F}_p$  add + 1  $\mathbb{F}_p$  neg + 1  $\mathbb{F}_p$  inv

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- Separated (integer multiplication and reduction) approach is preferred in most software platforms
  - Enables lazy reduction at  $\mathbb{F}_{p^2}$  level

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- x64: limited number of registers, availability of carry-preserving instructions (e.g., `mulx`)
  - Can use one-level Karatsuba (top), two-level schoolbook (bottom)
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  - Can use two-level Karatsuba (top), one-level Comba (bottom)

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Also:  $p' \bmod 2^w \equiv 1$  for  $w = 32, 64$

# Security and parameters

# SIDH security

**Setting:** supersingular curves  $E_1/\mathbb{F}_{p^2}$  and  $E_2/\mathbb{F}_{p^2}$ , a large prime  $p$ , and isogeny  $\phi: E_1 \rightarrow E_2$  with fixed, smooth, public degree.

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For SIDH/SIKE: number of order- $\ell^{e/2}$  subgroups of  $E[\ell^e] = |S| \approx p^{1/4}$

Assume storage  $w \approx 2^{80}$

$$\mathcal{O}\left(\frac{|S|^{\frac{3}{2}}}{\sqrt{w}}\right)$$

# SIKE parameters (round 2 and 3)

- Eight parameter sets submitted to NIST:
  - SIKEp434, SIKEp503, SIKEp610, SIKEp751, and their corresponding compressed variants

Scheme (SIKEp + $\lceil \log_2 p \rceil$ )	$(e_A, e_B)$	Security level	Standard (bytes)		Compressed (bytes)	
			pk	ct	pk	ct
SIKEp434	(216,137)	AES-128 (level 1)	330	346	196	209
SIKEp503	(250,159)	SHA3-256 (level 2)	378	402	224	248
SIKEp610	(305,192)	AES-192 (level 3)	462	486	273	297
SIKEp751	(372,239)	AES-256 (level 5)	564	596	331	363

Starting curve  $E_0/\mathbb{F}_{p^2}$ :  $y^2 = x^3 + 6x^2 + x$ , where  $p = 2^{e_A}3^{e_B} - 1$ .

# Implementation results

# SIDH Library

- Current release: **version 3.3**  
<https://github.com/Microsoft/PQCrypto-SIDH>
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  - Portable C
  - High-performance 64-bit CPUs
    - With high-speed x64 assembly for the field arithmetic
    - With high-speed ARMv8-A assembly for the field arithmetic
- No secret branches, no secret memory accesses: protected against cache and timing attacks

# Performance on x64 (SIDH v3.3)

- Total time: Encapsulation + Decapsulation

Primitive	Standard		Compressed	
	Cycles ( $\times 10^6$ )	Time	Cycles ( $\times 10^6$ )	Time
SIKEp434	20.0	5.9 ms	26.2	7.7 ms
SIKEp503	27.9	8.2 ms	36.3	10.7 ms
SIKEp610	54.7	16.1 ms	66.9	19.7 ms
SIKEp751	84.6	24.9 ms	110.1	32.4 ms

(\*) Obtained on a 3.4GHz Intel Core i7-6700 (Skylake) processor.

# Performance on 64-bit ARM (SIDH v3.3)

Primitive	NIST sec level	Cycles ( $\times 10^6$ )	Time @1.992GHz
<b>Passively secure key-exchange</b>			
SIDHp434	1	60.8	30.5 ms
SIDHp503	2	88.4	44.4 ms
<b>IND-CCA secure KEMs</b>			
SIKEp434	1	59.4	29.8 ms
SIKEp503	2	82.7	41.5 ms

(\*) Obtained on a 1.992GHz ARM Cortex-A72 (ARMv8-A) processor.

# Performance on x64

Primitive	PQ security	Problem	Speed	Comm.
<b>Classical</b>				
RSA 3072	~0 bits	factoring	4.6 ms	0.8 KB
ECDH NIST P-256	~0 bits	EC dlog	1.4 ms	0.1 KB
<b>Passively secure key-exchange</b>				
SIDHp434	128 bits	isogenies	6.0 ms	0.6 KB
<b>IND-CCA secure KEMs</b>				
Kyber	100 bits	M-LWE	0.03 ms	0.7 KB
FrodoKEM	108 bits	LWE	1.1 ms	9.5 KB
SIKEp434	128 bits	isogenies	5.9–7.7 ms	0.2–0.3 KB

very fast    slow    very small    large

(\*) Obtained on 3.4GHz Intel Haswell (Kyber) or Skylake (FrodoKEM and SIKE).

# Recent research

**The Cost to Break SIKE: A Comparative Hardware-Based Analysis with AES and SHA-3, L-Wang-Szefer, 2020.** <https://eprint.iacr.org/2020/1457>

- Uses a budget-based cost model to estimate cryptanalysis cost of vOW versus brute forcing AES.

# Recent research

**The Cost to Break SIKE: A Comparative Hardware-Based Analysis with AES and SHA-3**, L-Wang-Szefer, 2020. <https://eprint.iacr.org/2020/1457>

- Uses a budget-based cost model to estimate cryptanalysis cost of vOW versus brute forcing AES.
- E.g., suggests SIKEp377 to match AES128 security (level 1).
  - ~1.4x faster than SIKEp434, ~13% smaller public keys

# SIKE in the NIST post-quantum “competition”

- SIKE website: <http://sike.org/>
- SIKE specification: <http://sike.org/files/SIDH-spec.pdf>
- SIDH Library: <https://github.com/Microsoft/PQCrypto-SIDH>
- Package (protocol specification and implementations) submitted to NIST:  
<https://csrc.nist.gov/CSRC/media/Projects/post-quantum-cryptography/documents/round-3/submissions/SIKE-Round3.zip>

# Software Implementation of (Post-Quantum) Public-Key Cryptography

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