Digital Systems : LAB4

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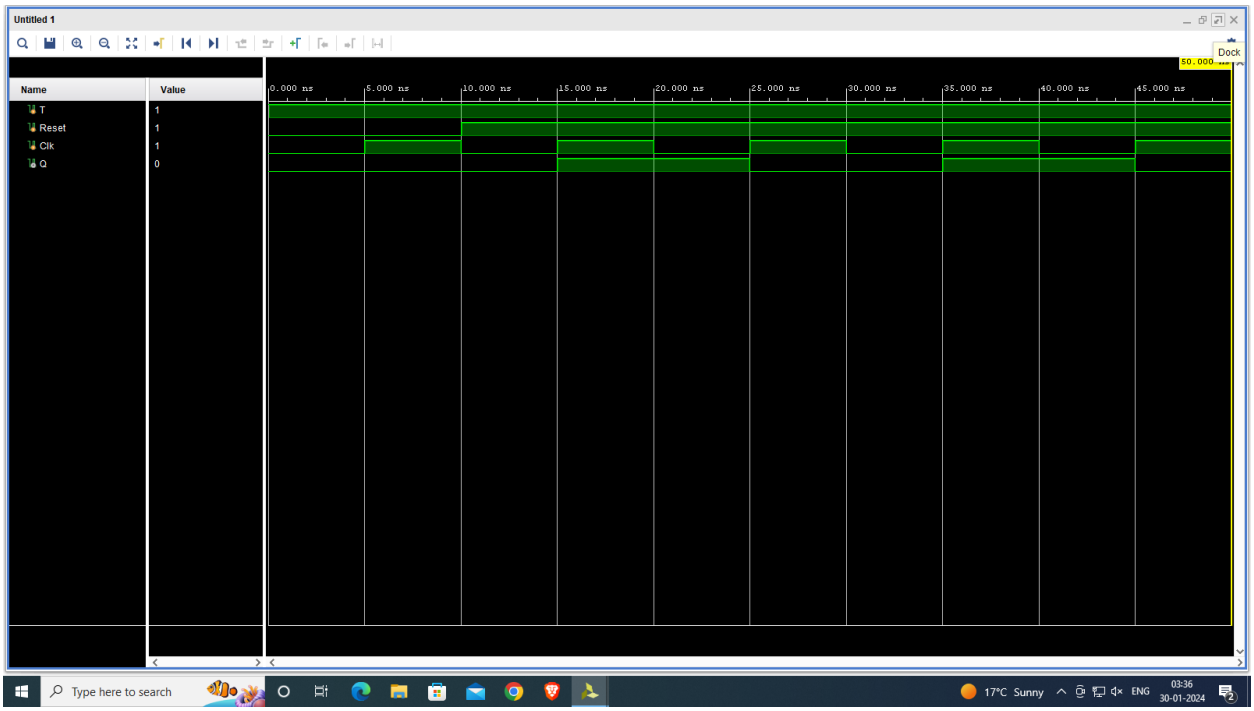
Toggle Flip Flop

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 30.01.2024 03:16:52
// Design Name:
// Module Name: Tff
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module Tff(
    input T,
    input Clk,
    input Reset,
    output reg Q
```

```
    );
    always @(posedge Clk, negedge Reset)
    begin
        begin
        if (!Reset)
            Q <= 0;
        else
            begin
            if ( T == 1)
                Q <= ~Q;
            else
                Q <= Q;
            end
        end
    end
endmodule
```

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 30.01.2024 03:29:37
// Design Name:
// Module Name: Tff_tb
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
```

```
//
//////////////////////////////////////////////////////////////////


module Tff_tb();
    reg T, Reset, Clk;
    wire Q;
    Tff uut(T, Clk, Reset, Q);
    initial
    begin
    Clk = 0;
        forever #5 Clk = ~Clk;
    end
    initial
    begin
    T = 1; Reset = 0;
    #10;

    T = 1; Reset = 1;
    #10;
    T = 1; Reset = 1;
    #10;
    T = 1; Reset = 1;
    #10;
    T = 1; Reset = 1;
    #10;
    $finish();
    end
endmodule
```



Asynchronous Counter

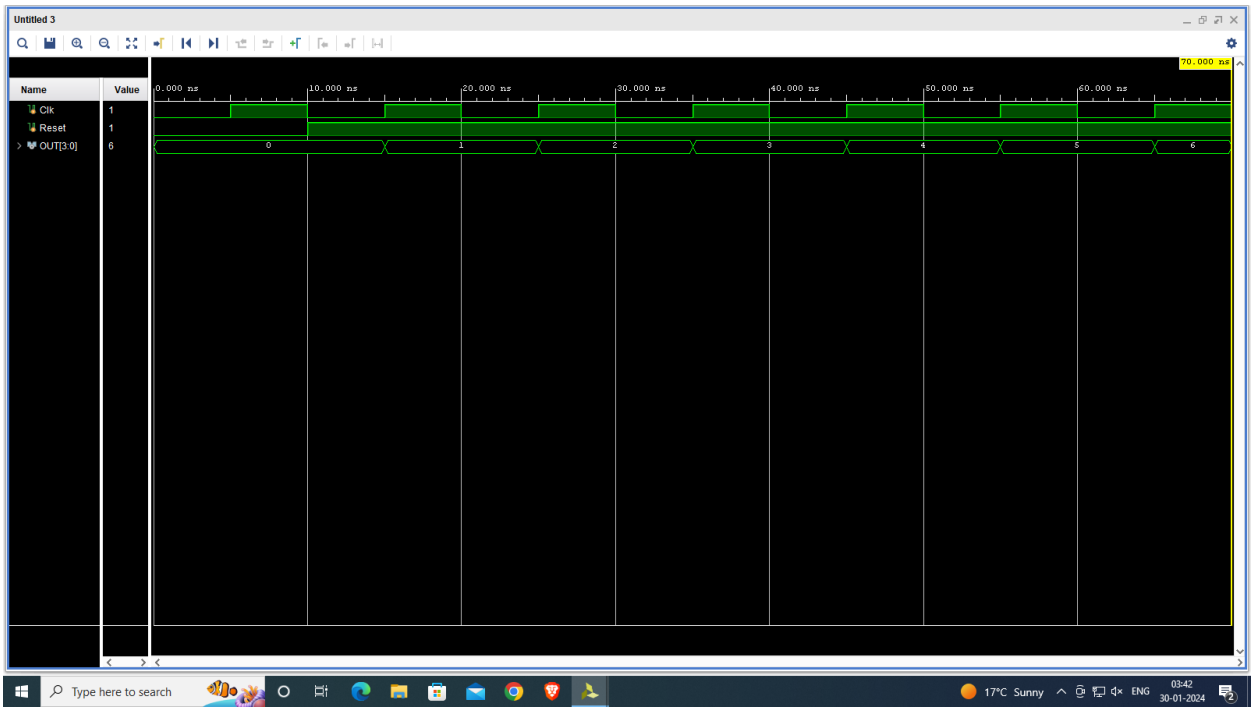
```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 30.01.2024 03:24:17
// Design Name:
// Module Name: Ascounter
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
```

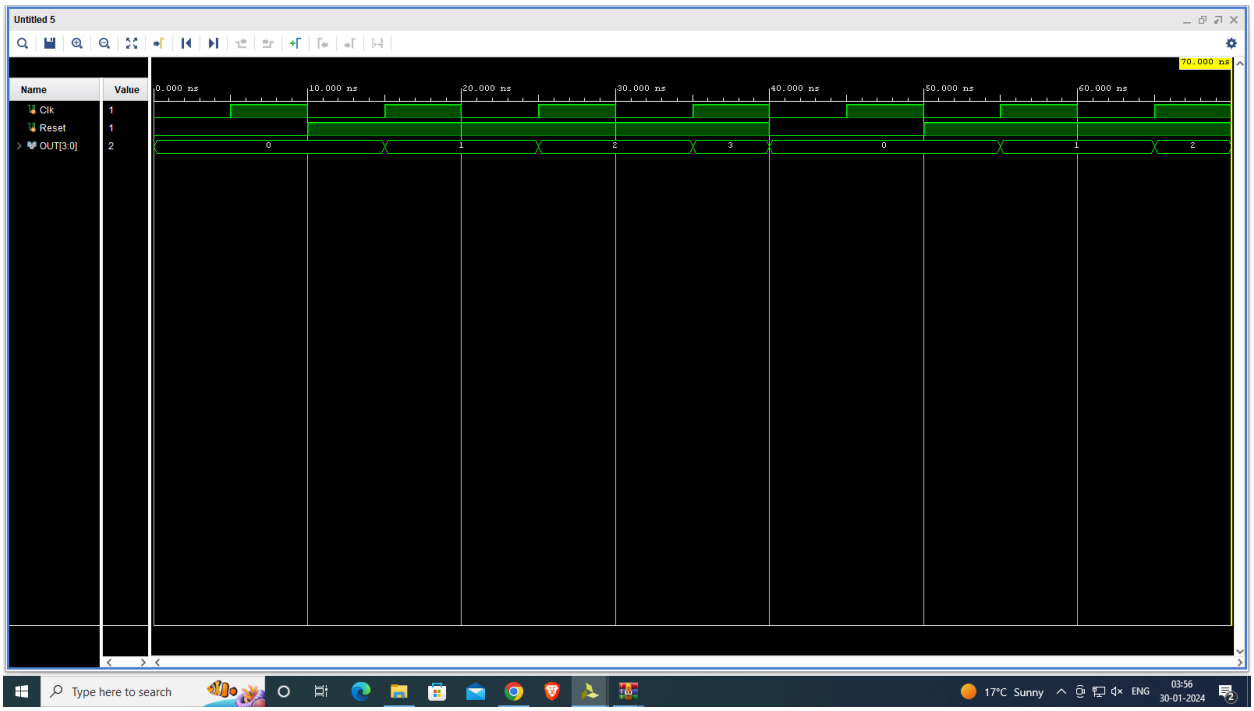
```
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////


module Ascounter(
    input Clk,
    input Reset,
    output [3:0] OUT
    );

    Tff f1(.T(1), .Clk(Clk), .Reset(Reset), .Q(OUT[0]));
    Tff f2(.T(1), .Clk(~OUT[0]), .Reset(Reset), .Q(OUT[1]));
    Tff f3(.T(1), .Clk(~OUT[1]), .Reset(Reset), .Q(OUT[2]));
    Tff f4(.T(1), .Clk(~OUT[2]), .Reset(Reset), .Q(OUT[3]));


endmodule
```

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 30.01.2024 03:36:56
// Design Name:
// Module Name: Ascounter_tb
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
```

```
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////


module Ascounter_tb();
    reg Clk, Reset;
    wire [3:0] OUT;
    Ascounter uut(Clk, Reset, OUT);
    initial
    begin
    Clk = 0;
        forever #5 Clk = ~Clk;
    end
    initial begin
        Reset = 0;
        #10;
        Reset = 1;
        #10;
        Reset = 1;
        #10;
        Reset = 1;
        #10;
        Reset = 1;
        #10;
        Reset = 1;
        #10;
        Reset = 1;
        #10;
        Reset = 1;
        #10;
    $finish();
    end
endmodule
```

Final Simulation Results :


Untitled 3
Name
Value
Clk
Reset
OUT[3:0]
1
1
6
0.000 ns
10.000 ns
20.000 ns
30.000 ns
40.000 ns
50.000 ns
60.000 ns
70.000 ns
0
1
2
3
4
5
6
Type here to search
17°C Sunny
ENG
03:42
30-01-2024


Untitled 5
Name
Value
Clk
Reset
OUT[3:0]
1
1
2
0.000 ns
10.000 ns
20.000 ns
30.000 ns
40.000 ns
50.000 ns
60.000 ns
70.000 ns
0
1
2
3
0
1
2
Type here to search
17°C Sunny
ENG
03:56
30-01-2024