ES204 Digital Systems
LAB Assignment - 1

Indian Institute of Technology, Gandhinagar
January 9, 2024
Time & Venue: Tuesday 8:30-9:50am [7/108]

Submission deadline: Jan 9, 2024 (9:50 am)
Marks : 20

For each of the questions, write a Verilog code. You also need to create a **testbench** and show the simulation results.

1. **[20 Marks]** Implement the following function using

   (a) Structural code
   (b) continuous assignment

$$f(a,b,c,d) = \sum m(0,2,5,9,11,13,15)$$

Question a.
Srucutral Code :

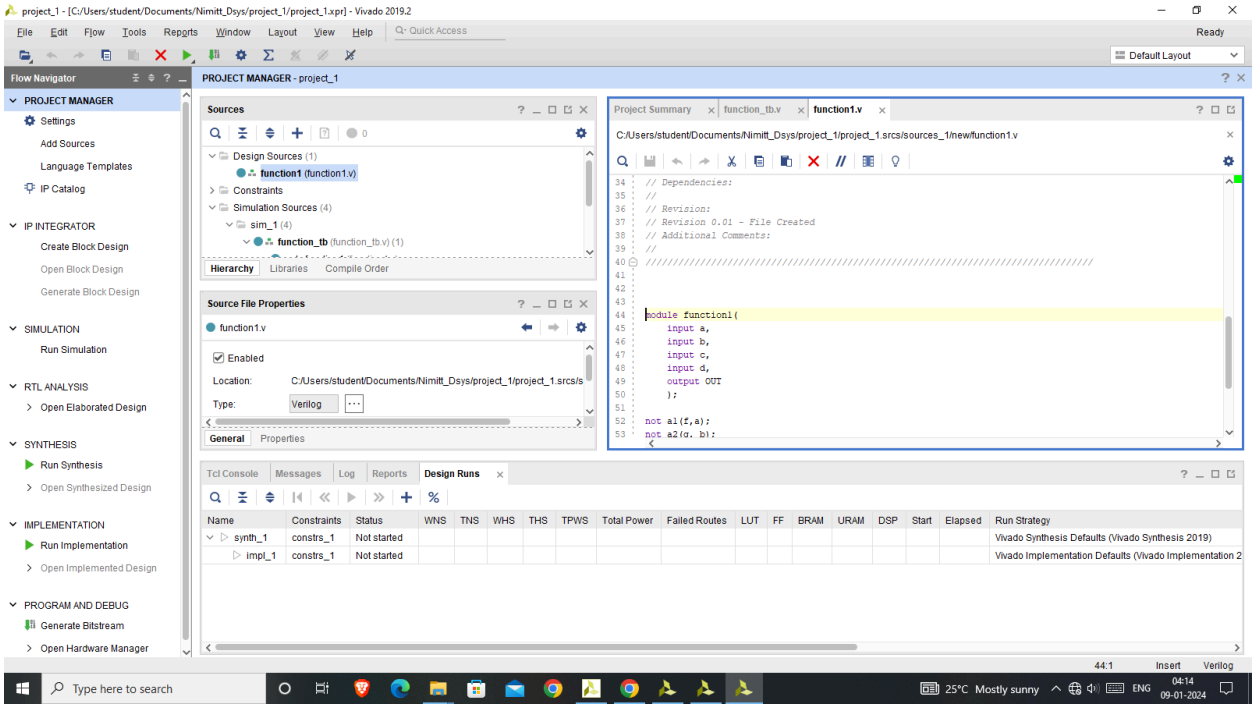
```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 09.01.2024 03:35:43
// Design Name:
// Module Name: function1
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
```

```
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 09.01.2024 03:22:10
// Design Name:
// Module Name: function_1
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////



module function1(
    input a,
    input b,
    input c,
    input d,
    output OUT
    );

not a1(f,a);
not a2(g, b);
not a3(h, c);
not a4(i, d);
and a5(j, a, d);
and a6(k, f, g, i);
and a7(l, b, h, d);
or a8( OUT, j, k, l);
endmodule
```


project_1 - [C:/Users/student/Documents/Nimitt_Dsys/project_1/project_1.xpr] - Vivado 2019.2
File Edit Flow Tools Reports Window Layout View Help
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Ready
Default Layout
Flow Navigator
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IP INTEGRATOR
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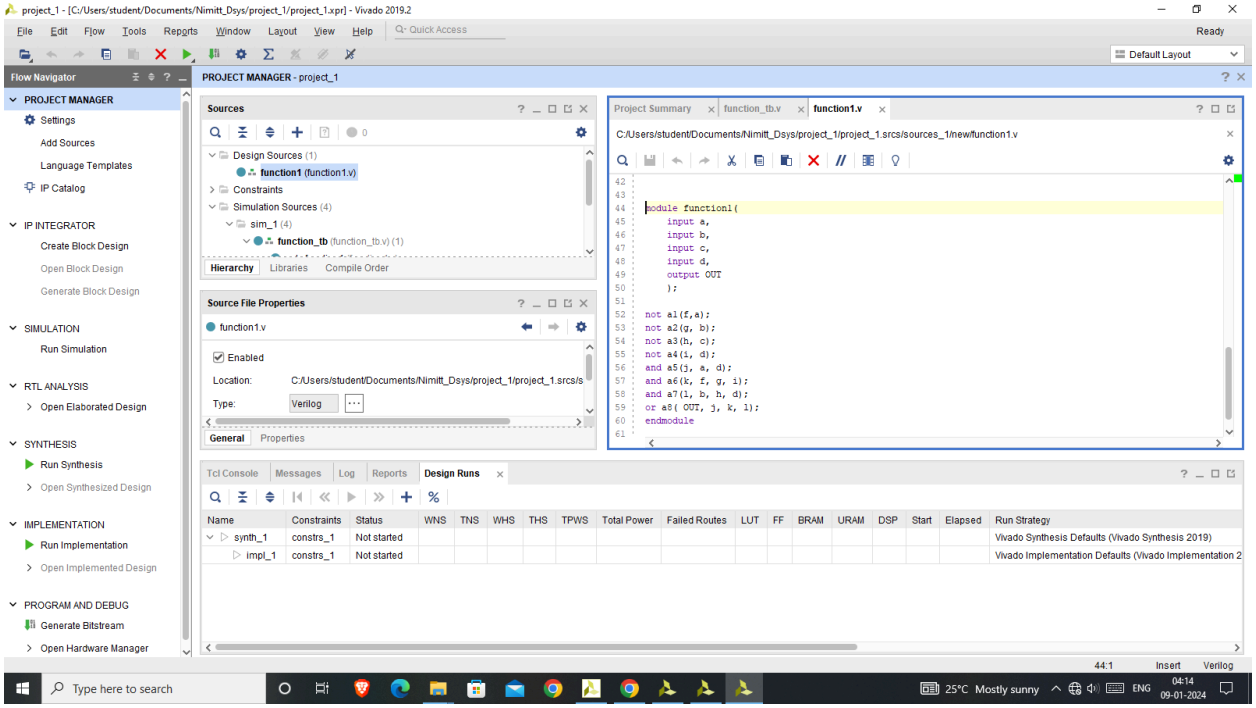
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
PROJECT MANAGER - project_1
Sources
Design Sources (1)
function1 (function1.v)
Constraints
Simulation Sources (4)
sim_1 (4)
function_tb (function_tb.v) (1)
Hierarchy Libraries Compile Order
Source File Properties
function1.v
Enabled
Location: C:/Users/student/Documents/Nimitt_Dsys/project_1/project_1.srcs/s
Type: Verilog
General Properties
Project Summary
function_tb.v
function1.v
C:/Users/student/Documents/Nimitt_Dsys/project_1/project_1.srcs/sources_1/new/function1.v
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
module function1(
input a,
input b,
input c,
input d,
output OUT
);
not a1(f,a);
not a2(g, b);
Tcl Console Messages Log Reports Design Runs
Name Constraints Status WNS TNS WHS THS TPWS Total Power Failed Routes LUT FF BRAM URAM DSP Start Elapsed Run Strategy
synth_1 constrs_1 Not started Vivado Synthesis Defaults (Vivado Synthesis 2019)
impl_1 constrs_1 Not started Vivado Implementation Defaults (Vivado Implementation 2
44:1 Insert Verilog
Type here to search
25°C Mostly sunny
ENG
04:14
09-01-2024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module function1(
input a,
input b,
input c,
input d,
output OUT
);
not a1(f,a);
not a2(g, b);
not a3(h, c);
not a4(i, d);
and a5(j, a, d);
and a6(k, f, g, i);
and a7(l, b, h, d);
or a8(OUT, j, k, l);
endmodule
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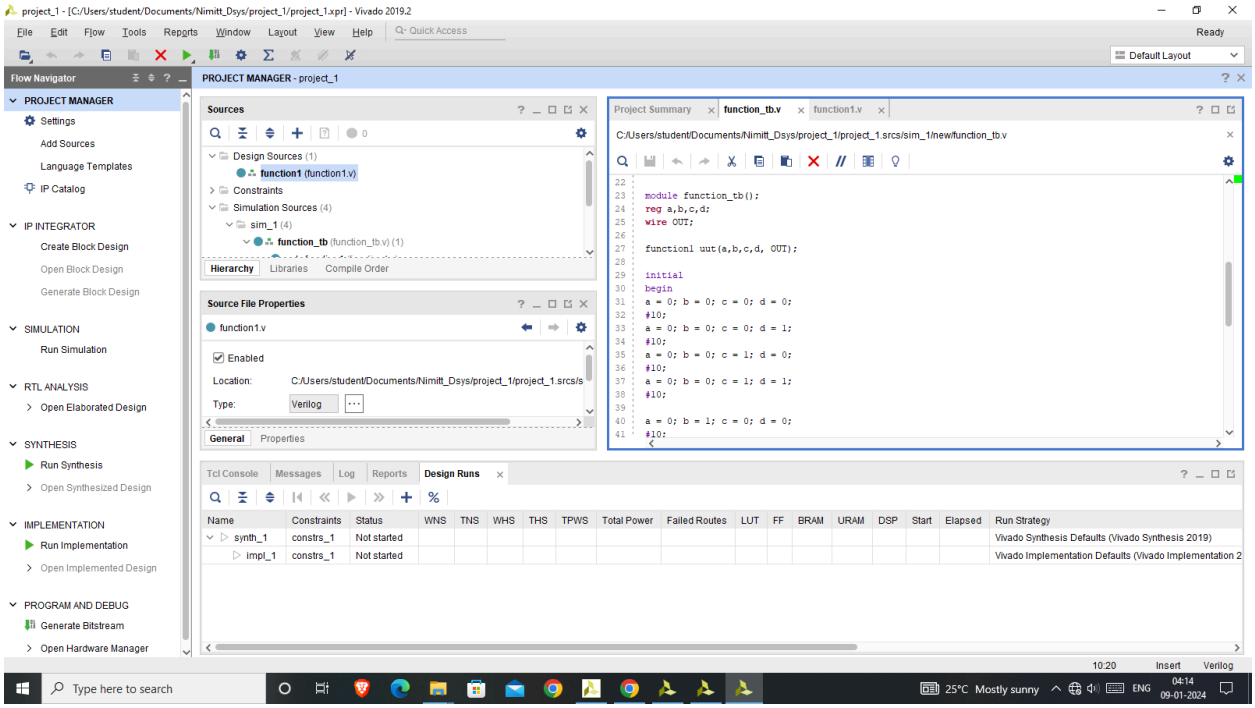
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function1.v
C:/Users/student/Documents/Nimitt_Dsys/project_1/project_1.srcs/sim_1/new/function_tb.v
module function_tb();
reg a,b,c,d;
wire OUT;
function1 uut(a,b,c,d, OUT);
initial
begin
a = 0; b = 0; c = 0; d = 0;
#10;
a = 0; b = 0; c = 0; d = 1;
#10;
a = 0; b = 0; c = 1; d = 0;
#10;
a = 0; b = 0; c = 1; d = 1;
#10;
a = 0; b = 1; c = 0; d = 0;
#10;
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impl_1 constrs_1 Not started Vivado Implementation Defaults (Vivado Implementation 2
10:20 Insert Verilog
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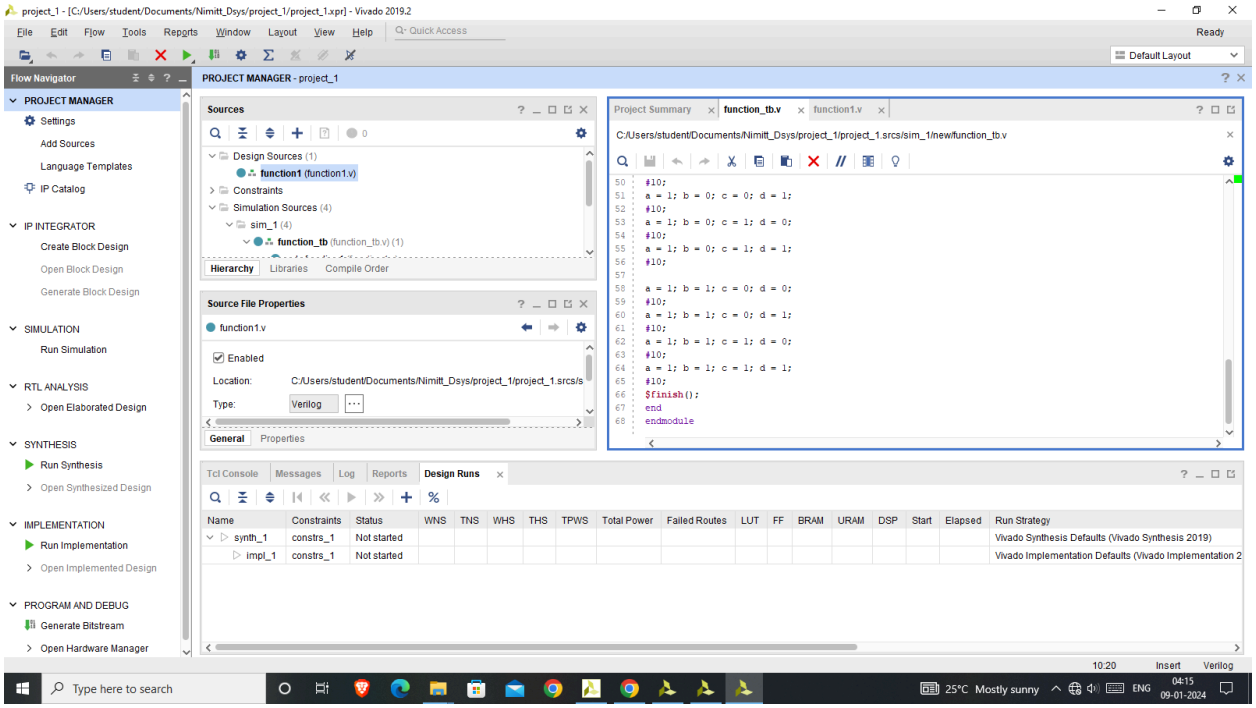
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#10;
a = 1; b = 0; c = 0; d = 1;
#10;
a = 1; b = 0; c = 1; d = 0;
#10;
a = 1; b = 0; c = 1; d = 1;
#10;
a = 1; b = 1; c = 0; d = 0;
#10;
a = 1; b = 1; c = 0; d = 1;
#10;
a = 1; b = 1; c = 1; d = 0;
#10;
a = 1; b = 1; c = 1; d = 1;
#10;
$finish();
end
endmodule
Tcl Console Messages Log Reports Design Runs
Name Constraints Status WNS TNS WHS THS TPWS Total Power Failed Routes LUT FF BRAM URAM DSP Start Elapsed Run Strategy
synth_1 constrs_1 Not started Vivado Synthesis Defaults (Vivado Synthesis 2019)
impl_1 constrs_1 Not started Vivado Implementation Defaults (Vivado Implementation 2
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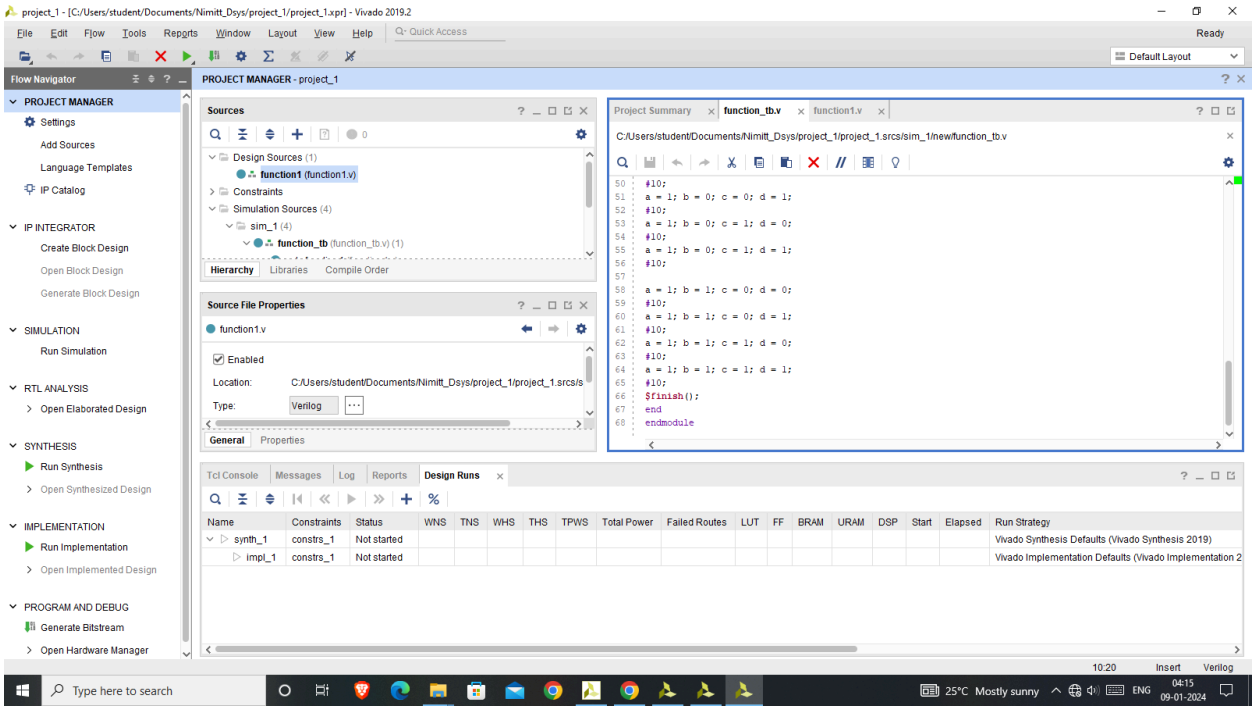
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function1.v
C:/Users/student/Documents/Nimitt_Dsys/project_1/project_1.srcs/sim_1/new/function_tb.v
#10;
a = 1; b = 0; c = 0; d = 1;
#10;
a = 1; b = 0; c = 1; d = 0;
#10;
a = 1; b = 0; c = 1; d = 1;
#10;
a = 1; b = 1; c = 0; d = 0;
#10;
a = 1; b = 1; c = 0; d = 1;
#10;
a = 1; b = 1; c = 1; d = 0;
#10;
a = 1; b = 1; c = 1; d = 1;
#10;
$finish();
end
endmodule
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impl_1 constrs_1 Not started Vivado Implementation Defaults (Vivado Implementation 2
10:20 Insert Verilog
Type here to search
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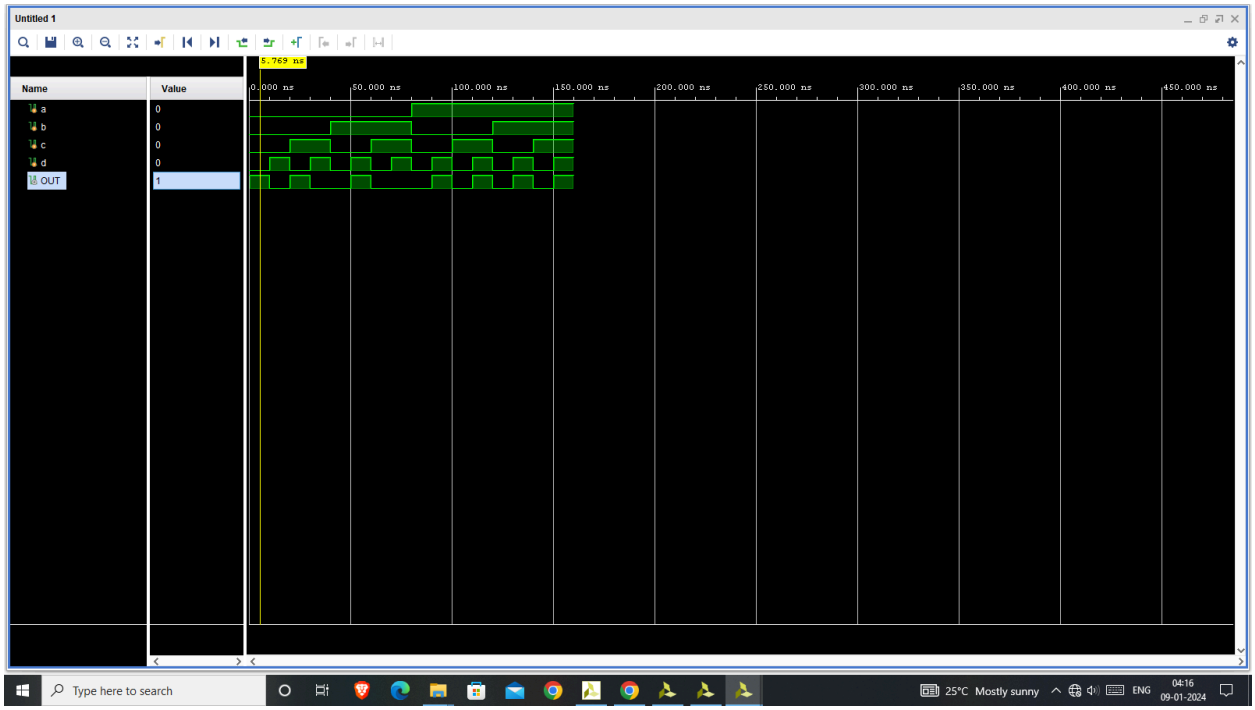
09-01-2024


Untitled 1
Name
Value
a
b
c
d
OUT
0
0
0
0
1
5.769 ns
0.000 ns
50.000 ns
100.000 ns
150.000 ns
200.000 ns
250.000 ns
300.000 ns
350.000 ns
400.000 ns
450.000 ns
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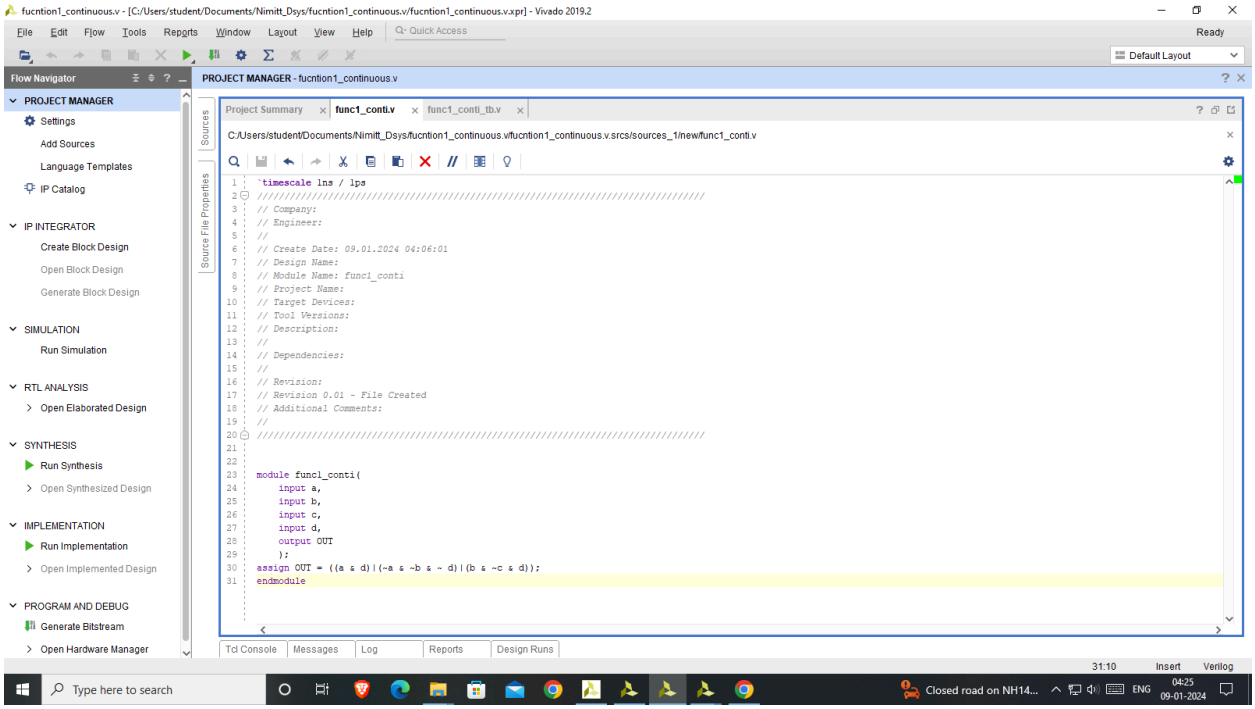
25°C Mostly sunny
ENG
04:16
09-01-2024

Question B


fucntion1_continuous.v - [C:/Users/student/Documents/Nimitt_Dsys/fucntion1_continuous.v/fucntion1_continuous.v.xpr] - Vivado 2019.2
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PROJECT MANAGER - fucntion1_continuous.v
Project Summary
func1_conti.v
func1_conti_tb.v
C:/Users/student/Documents/Nimitt_Dsys/fucntion1_continuous.v/fucntion1_continuous.v.srcs/sources_1/new/func1_conti.v
Sources
Source File Properties
`timescale 1ns / 1ps
// Company:
// Engineer:
// Create Date: 09.01.2024 04:06:01
// Design Name:
// Module Name: func1_conti
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
// Dependencies:
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
module func1_conti(
input a,
input b,
input c,
input d,
output OUT
);
assign OUT = ((a & d)|(~a & ~b & ~ d)|(b & ~c & d));
endmodule
Tcl Console
Messages
Log
Reports
Design Runs
31:10
Insert
Verilog
Type here to search
Closed road on NH14...
ENG
04:25
09-01-2024