# Digital Systems : LAB 3

*Pratham Sharda (22110203)*

*Nimitt (22110169)*

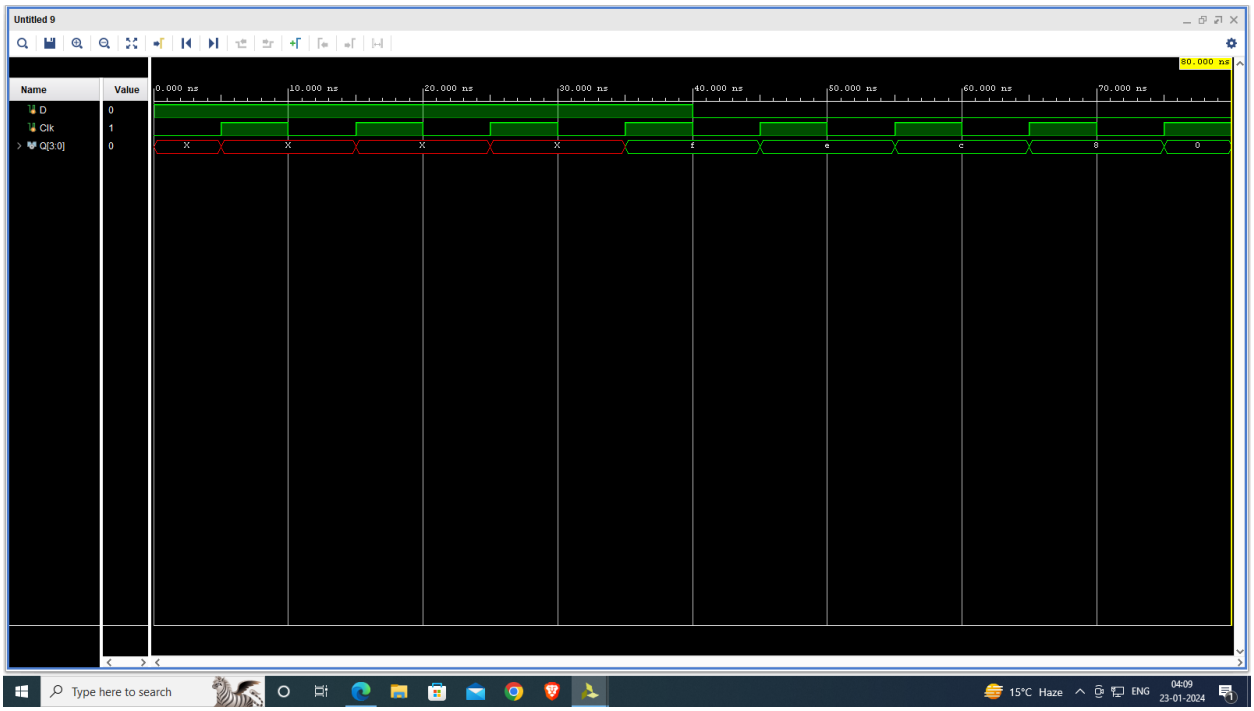
## Shift Register Blocking

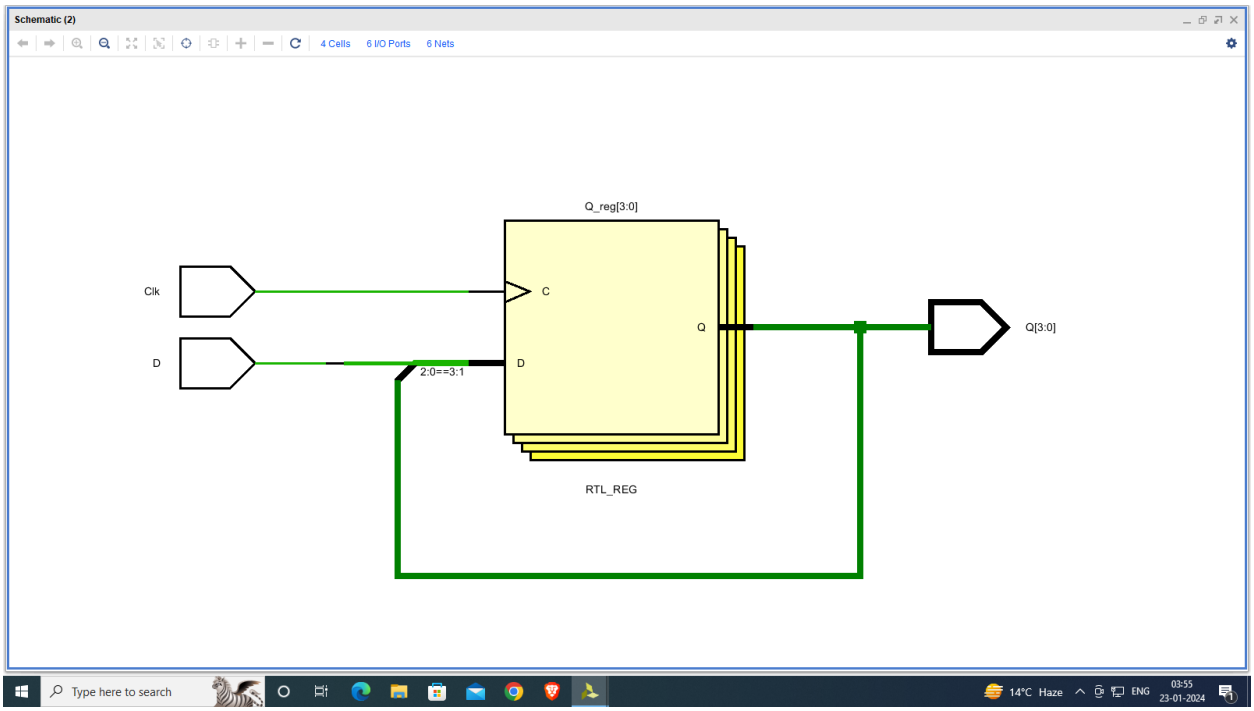
```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 23.01.2024 03:17:03
// Design Name:
// Module Name: ShiftRegister
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module ShiftRegister(
    input D,
    input Clk,
    output reg [3:0] Q
    );
```

```
    always @(posedge Clk)
    begin
        Q[3] = Q[2];
        Q[2] = Q[1];
        Q[1] = Q[0];
        Q[0] = D;
    end
endmodule
```

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 23.01.2024 03:42:38
// Design Name:
// Module Name: tb
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module tb();
    reg D, Clk;
    wire [3:0] Q;
    ShiftRegister uut(D, Clk, Q);
```

```
    initial
    begin
        Clk = 0;
        forever #5 Clk = ~ Clk;
    end
    initial
    begin
        D = 1;
        #10;
        D = 1;
        #10;
        D = 1;
        #10;
        D = 1;
        #10;
        D = 0;
        #10;
        D = 0;
        #10;
        D = 0;
        #10;
        D = 0;
        #10;
    $finish();
    end

endmodule
```



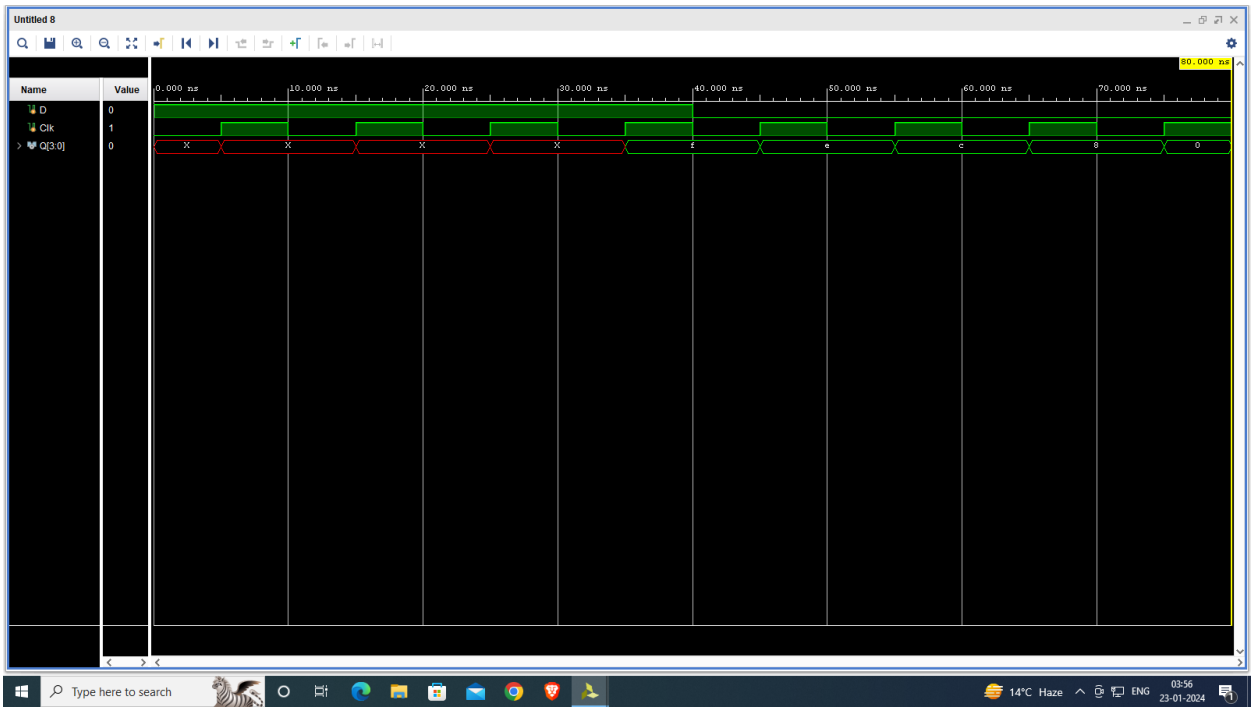

# Shift Register Non Blocking

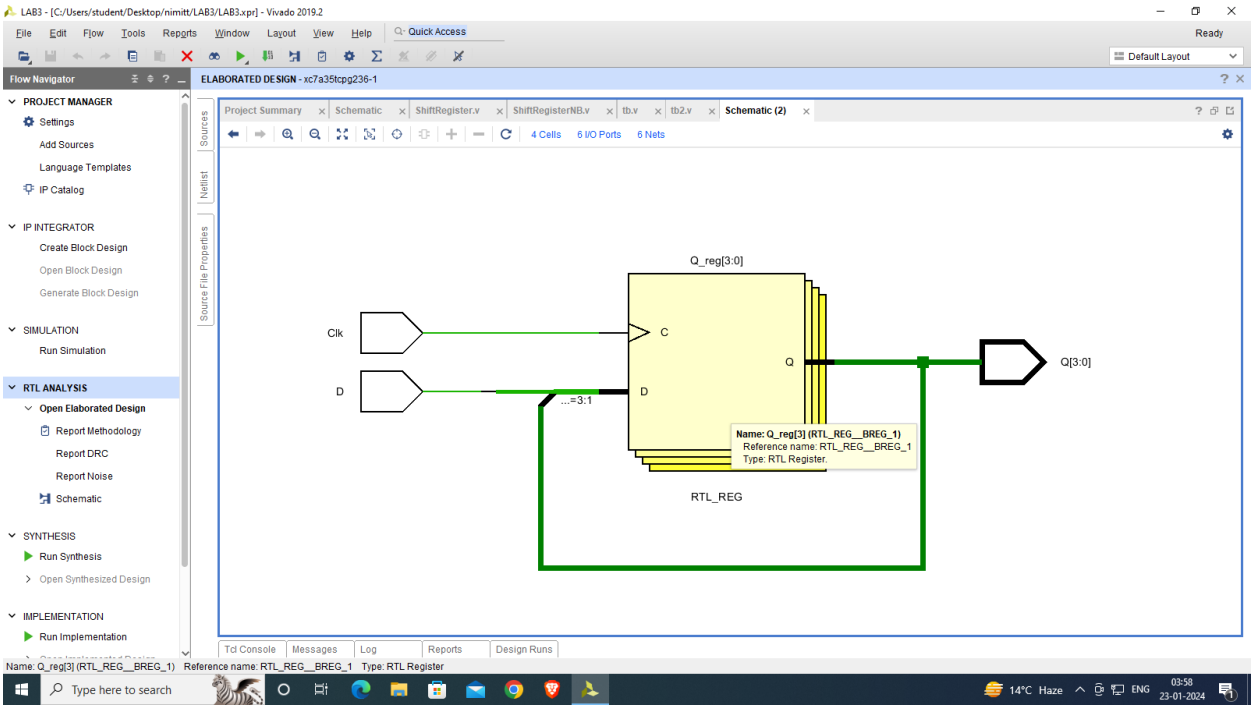
```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 23.01.2024 03:44:35
// Design Name:
// Module Name: ShiftRegisterNB
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module ShiftRegisterNB(
    input D,
    input Clk,
    output reg [3:0] Q
    );
        always @(posedge Clk)
    begin
        Q[3] <= Q[2];
        Q[2] <= Q[1];
        Q[1] <= Q[0];
        Q[0] <= D;
```

```
    end
endmodule
```

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 23.01.2024 03:48:43
// Design Name:
// Module Name: tb2
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module tb2();
    reg D, Clk;
    wire [3:0] Q;
    ShiftRegisterNB uut(D, Clk, Q);
    initial
    begin
        Clk = 0;
        forever #5 Clk = ~ Clk;
    end
    initial
```

```
    begin
        D = 1;
        #10;
        D = 1;
        #10;
        D = 1;
        #10;
        D = 1;
        #10;
        D = 0;
        #10;
        D = 0;
        #10;
        D = 0;
        #10;
        D = 0;
        #10;
    $finish();
    end
endmodule
```


Untitled 8
Name
Value
D
Clk
Q[3:0]
0
1
0
0.000 ns
10.000 ns
20.000 ns
30.000 ns
40.000 ns
50.000 ns
60.000 ns
70.000 ns
80.000 ns
Type here to search
14°C Haze
ENG
03:56
23-01-2024


LAB3 - [C:/Users/student/Desktop/nimitt/LAB3/LAB3.xpr] - Vivado 2019.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
ELABORATED DESIGN - xc7a35tcpg236-1
Project Summary
Schematic
ShiftRegister.v
ShiftRegisterNB.v
tb.v
tb2.v
Schematic (2)
4 Cells
6 I/O Ports
6 Nets
Q_reg[3:0]
Clk
D
C
D
Q
...=3:1
Q[3:0]
Name: Q_reg[3] (RTL_REG__BREG_1)
Reference name: RTL_REG__BREG_1
Type: RTL Register
RTL_REG
Tcl Console
Messages
Log
Reports
Design Runs
Name: Q_reg[3] (RTL_REG__BREG_1) Reference name: RTL_REG__BREG_1 Type: RTL Register
Type here to search
14°C Haze
ENG
03:58
23-01-2024