

Digital Systems : LAB 2

Nimitt

Pratham Sharda

Question 1

```
/// Full Adder Strucutral Code
`timescale 1ns / 1ps
/////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 16.01.2024 03:09:56
// Design Name:
// Module Name: question1
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
/////////////////////////////////////////////////////////////////

module question1(
    input Cin,
    input A,
    input B,
    output Cout,
```

```

        output Sum
    );

    and a1(f, Cin,A);
    and a2(g, A, B);
    and a3(h, B, Cin);
    or a4(Cout, f, g, h);

    xor a5(i, A, B);
    xor a6(Sum,i,Cin);

endmodule

```

```

// TestBench
`timescale 1ns / 1ps
/////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 16.01.2024 03:13:26
// Design Name:
// Module Name: question1_tb
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
/////////////////////////////////////////////////////////////////

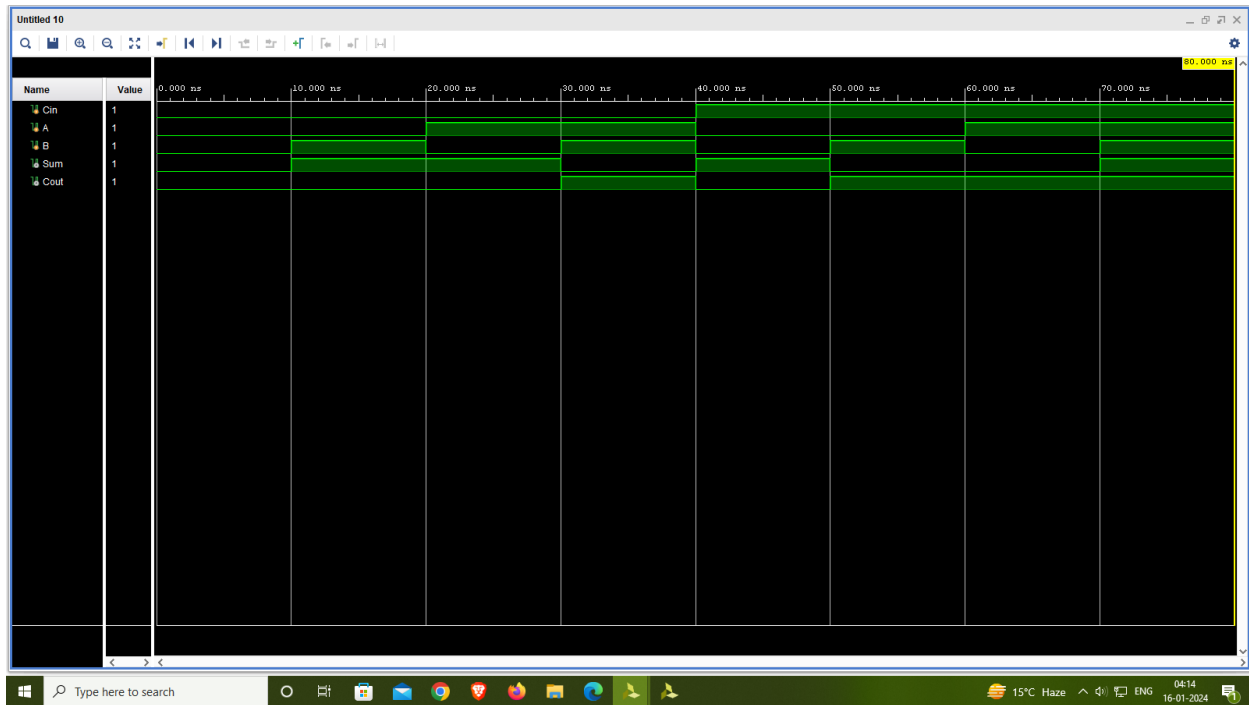
```

```

module question1_tb();
    reg Cin, A, B;
    wire Sum, Cout;
    question1 uut(Cin, A, B, Cout, Sum);
    initial
    begin
        Cin = 0; A = 0; B = 0;
        #10
        Cin = 0; A = 0; B = 1;
        #10
        Cin = 0; A = 1; B = 0;
        #10
        Cin = 0; A = 1; B = 1;
        #10
        Cin = 1; A = 0; B = 0;
        #10
        Cin = 1; A = 0; B = 1;
        #10
        Cin = 1; A = 1; B = 0;
        #10
        Cin = 1; A = 1; B = 1;
        #10
        $finish();
    end
endmodule

```

Simulations Results :



Question 2 :

```

/// 4 bit Adder
`timescale 1ns / 1ps
/////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 16.01.2024 03:38:37
// Design Name:
// Module Name: question2
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:

```

```

//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
////////////////////////////////////

module question2(
    input [3:0] A,
    input [3:0] B,
    output [3:0] OUT,
    output Cout
);
    wire w1, w2, w3;
    question1 inst1 (.Cin(0), .A(A[0]), .B(B[0]), .Cout(w1), .Sum
    question1 inst2 (.Cin(w1), .A(A[1]), .B(B[1]), .Cout(w2), .Sum
    question1 inst3 (.Cin(w2), .A(A[2]), .B(B[2]), .Cout(w3), .Sum
    question1 inst4 (.Cin(w3), .A(A[3]), .B(B[3]), .Cout(Cout),

endmodule

```

```

// TestBench
`timescale 1ns / 1ps
////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 16.01.2024 03:56:46
// Design Name:
// Module Name: Question2_tb
// Project Name:
// Target Devices:
// Tool Versions:
// Description:

```

```

//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
////////////////////////////////////

module Question2_tb();
    reg [3:0] A;
    reg [3:0] B;
    wire [3:0] OUT;
    wire Cout;

    question2 uut(A , B, OUT, Cout);
    initial
    begin
        A = 4'b0000; B = 4'b0000;
        #10;
        A = 4'b0001; B = 4'b0001;
        #10;
        A = 4'b0100; B = 4'b0010;
        #10;
        A = 4'b1010; B = 4'b1001;
        #10;
        A = 4'b1000; B = 4'b0100;
        #10;
        $finish();
    end
endmodule

```

Simulation Results :

