

Digital Systems : LAB 3

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Shift Register Blocking

```
`timescale 1ns / 1ps
/////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 23.01.2024 03:17:03
// Design Name:
// Module Name: ShiftRegister
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
/////////////////////////////////////////////////////////////////

module ShiftRegister(
    input D,
    input Clk,
    output reg [3:0] Q
);
```

```

always @(posedge Clk)
begin
    Q[3] = Q[2];
    Q[2] = Q[1];
    Q[1] = Q[0];
    Q[0] = D;
end
endmodule

```

```

`timescale 1ns / 1ps
/////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 23.01.2024 03:42:38
// Design Name:
// Module Name: tb
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
/////////////////////////////////////////////////////////////////

module tb();
    reg D, Clk;
    wire [3:0] Q;
    ShiftRegister uut(D, Clk, Q);

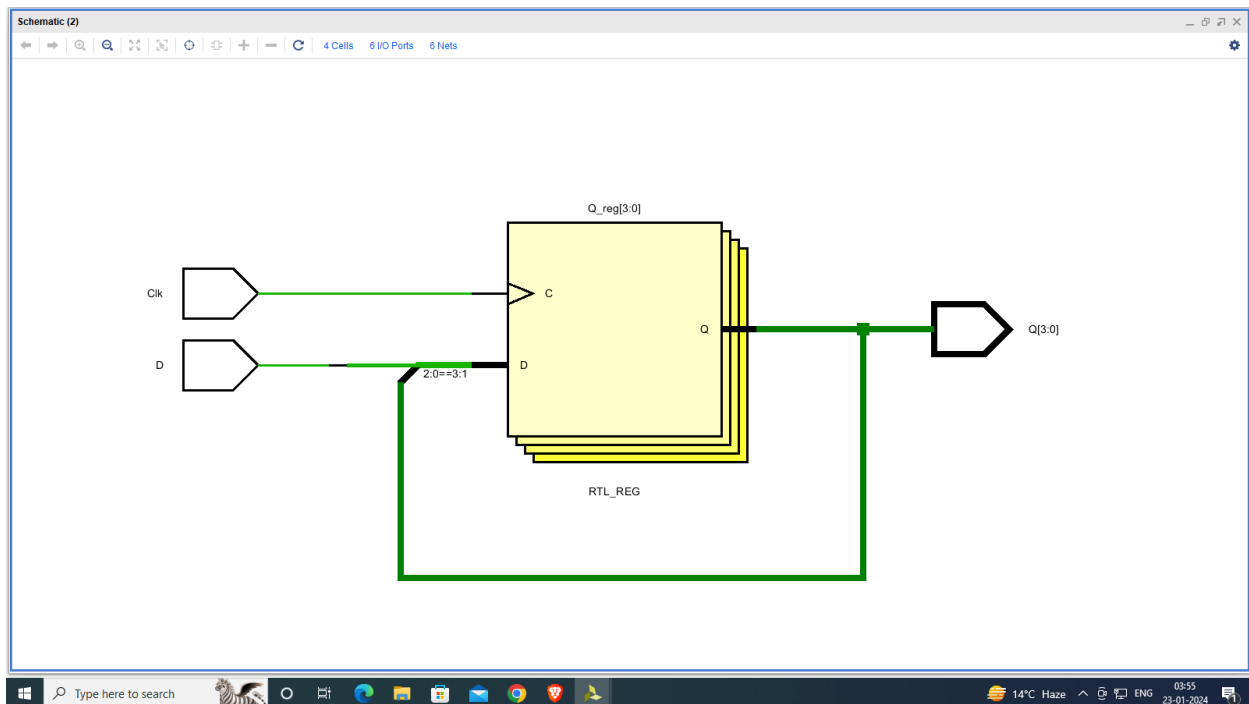
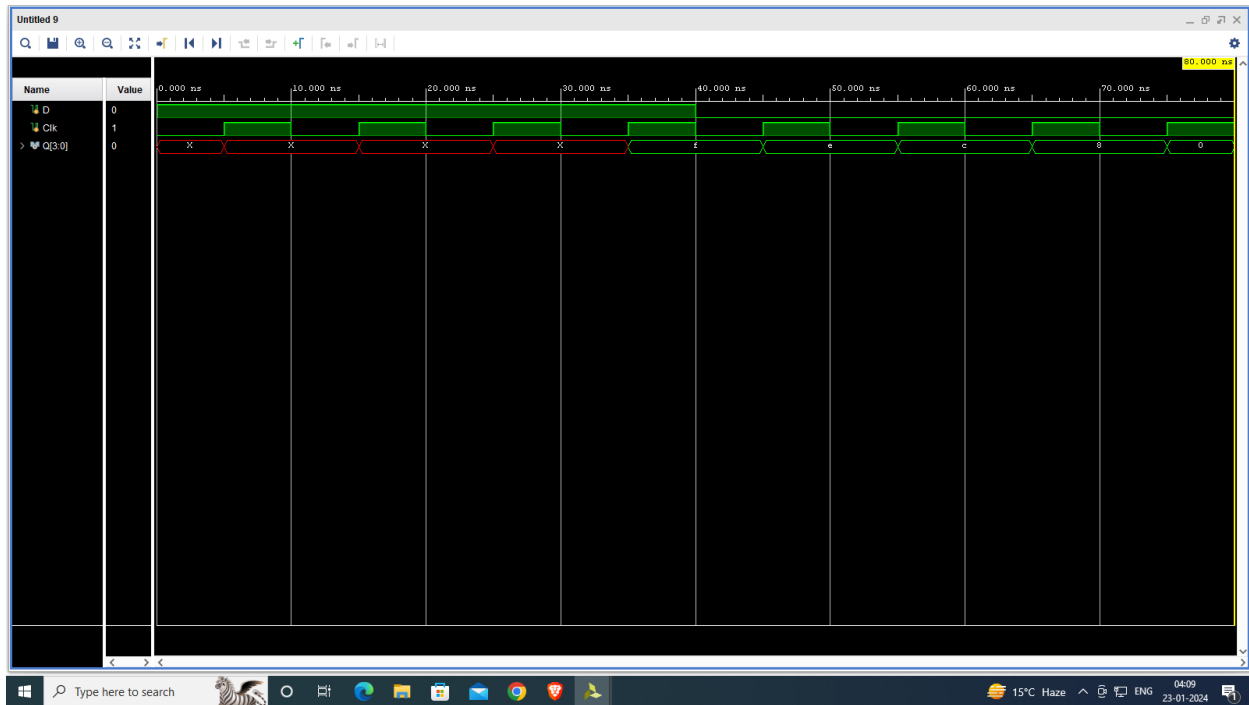
```

```

initial
begin
    Clk = 0;
    forever #5 Clk = ~ Clk;
end
initial
begin
    D = 1;
    #10;
    D = 1;
    #10;
    D = 1;
    #10;
    D = 1;
    #10;
    D = 0;
    #10;
    D = 0;
    #10;
    D = 0;
    #10;
    D = 0;
    #10;
    $finish();
end

endmodule

```



Shift Register Non Blocking

```

`timescale 1ns / 1ps
/////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 23.01.2024 03:44:35
// Design Name:
// Module Name: ShiftRegisterNB
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
/////////////////////////////////////////////////////////////////

module ShiftRegisterNB(
    input D,
    input Clk,
    output reg [3:0] Q
);
    always @(posedge Clk)
    begin
        Q[3] <= Q[2];
        Q[2] <= Q[1];
        Q[1] <= Q[0];
        Q[0] <= D;
    end

```

```
end  
endmodule
```

```
`timescale 1ns / 1ps  
/////////////////////////////////////////////////////////////////  
// Company:  
// Engineer:  
//  
// Create Date: 23.01.2024 03:48:43  
// Design Name:  
// Module Name: tb2  
// Project Name:  
// Target Devices:  
// Tool Versions:  
// Description:  
//  
// Dependencies:  
//  
// Revision:  
// Revision 0.01 - File Created  
// Additional Comments:  
//  
/////////////////////////////////////////////////////////////////  
  
module tb2();  
    reg D, Clk;  
    wire [3:0] Q;  
    ShiftRegisterNB uut(D, Clk, Q);  
    initial  
    begin  
        Clk = 0;  
        forever #5 Clk = ~ Clk;  
    end  
    initial
```

```
begin
    D = 1;
    #10;
    D = 1;
    #10;
    D = 1;
    #10;
    D = 1;
    #10;
    D = 0;
    #10;
    D = 0;
    #10;
    D = 0;
    #10;
    D = 0;
    #10;
    $finish();
end
endmodule
```

