Digital Systems : LAB 4

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a. Array Multiplier

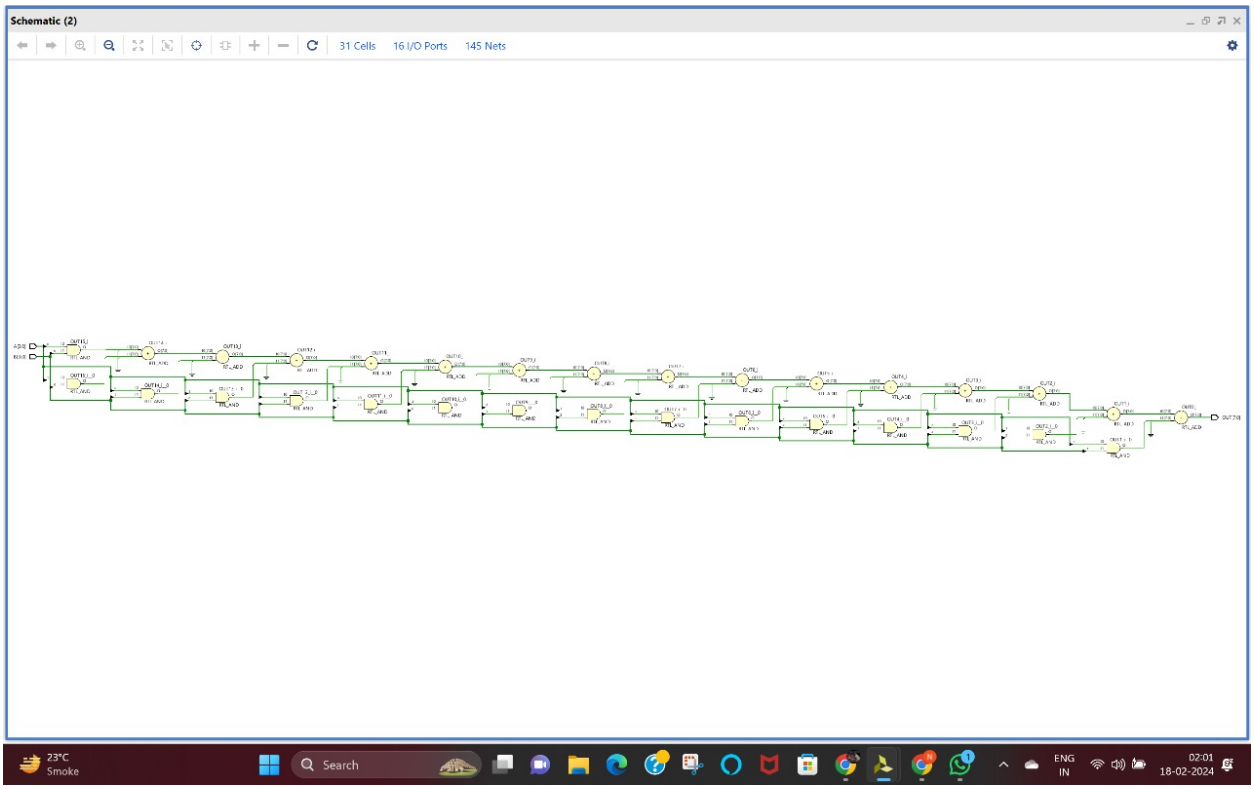
```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 02/17/2024 01:19:26 PM
// Design Name:
// Module Name: array_multiplier
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module array_multiplier(
    input [7:0] A,
    input [7:0] B,
    output reg [15:0] OUT
);
```

```
    reg [15:0] temp;
    parameter n = 8;
    parameter l = 16;
    integer i = 0;
    integer j = 0;

    always @(*)
        begin
        OUT = 0;
        for (i = 0; i < n; i=i+1)
            for (j = 0; j < i+1; j=j+1)
                begin
                temp = 0;
                temp[i] = (A[i-j] & B[j]);
                OUT = OUT + temp;
                end

        for (i = n; i < l; i=i+1)
            for (j = n - 1; j > i-n; j=j-1)
            begin
                temp = 0;
                temp[i] = (A[i-j] & B[j]);
                OUT = OUT + temp;
            end
        end
endmodule
```

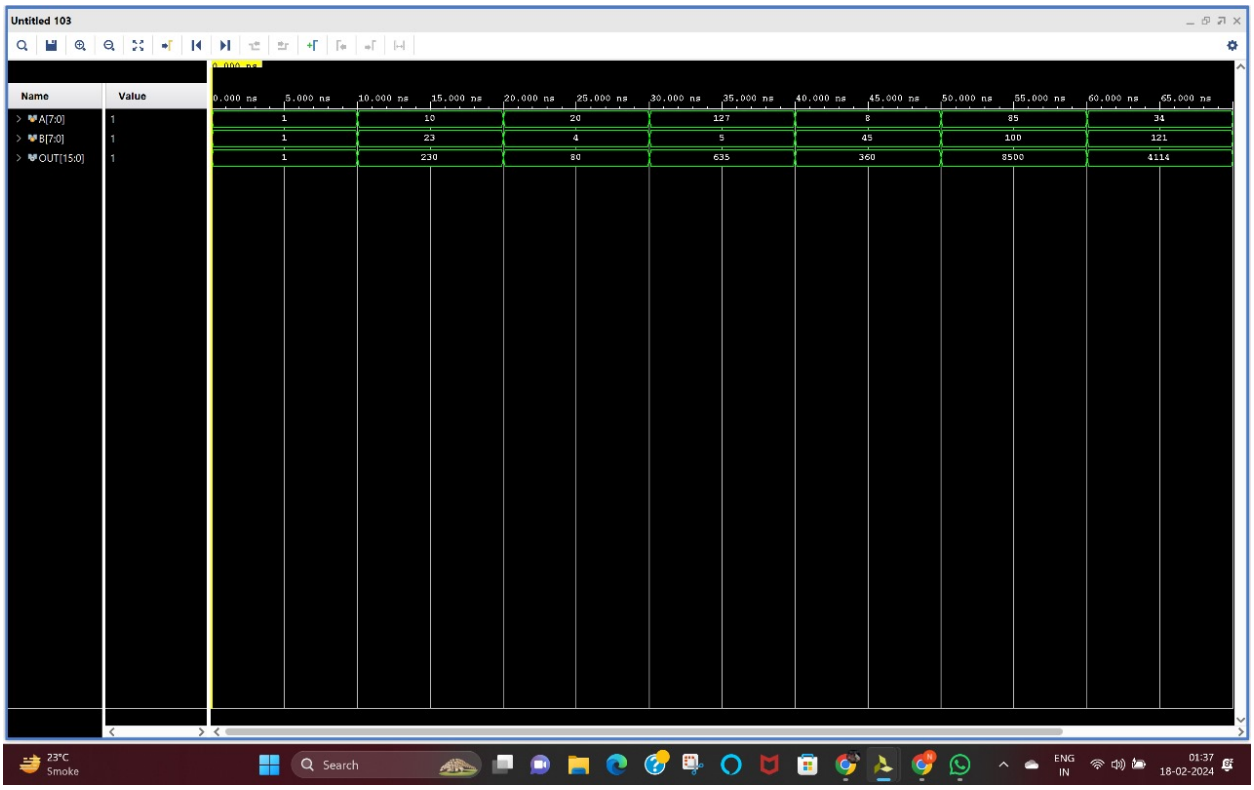
```
TestBench
module array_multiplier_tb();
    reg [7:0] A;
    reg [7:0] B;
    wire [15:0] OUT;

    array_multiplier uut(A,B,OUT);
```

```
        A = 1; B = 1;
        #10;
        A = 10; B = 23;
        #10;
        A = 20; B = 4;
        #10;
        A = 127; B = 5;
        #10;
        A = 8; B = 45;
        #10;
        A = 85; B = 100;
        #10;
        A = 34; B = 121;
        #10;
    endmodule
```

Schematic



Simulation Results :



b. Binary Mutiplier

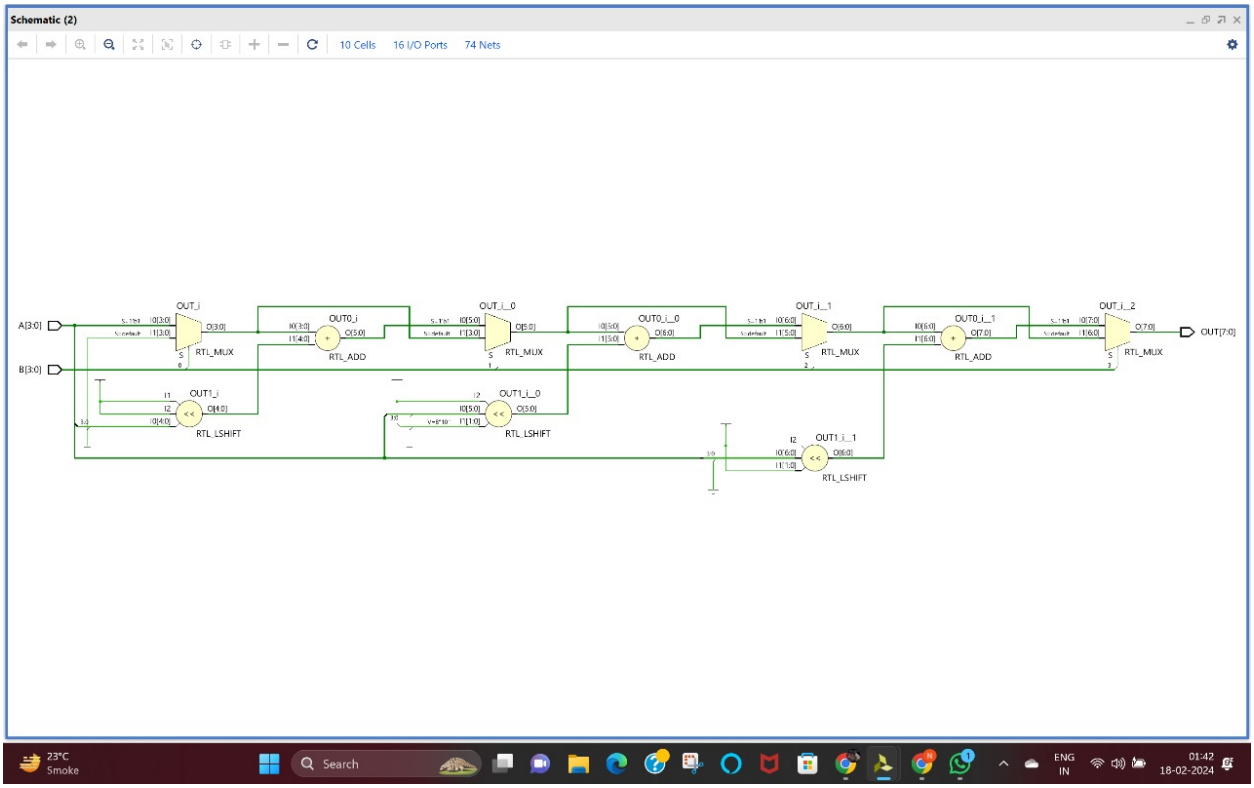
```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 02/17/2024 01:19:26 PM
// Design Name:
// Module Name: binary_multiplier
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
```

```
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////

module binary_multiplier(
    input [7:0] A,
    input [7:0] B,
    output reg [15:0] OUT
    );
    parameter n = 8;
    integer i;
    reg  [15:0]t;
    always @(*) begin
        OUT = 16'b0;
        for (i = 0; i < n; i = i + 1) begin
            if (B[i]) begin
                t = (A << i);
                OUT = OUT+t;
            end
        end
    end
endmodule
```

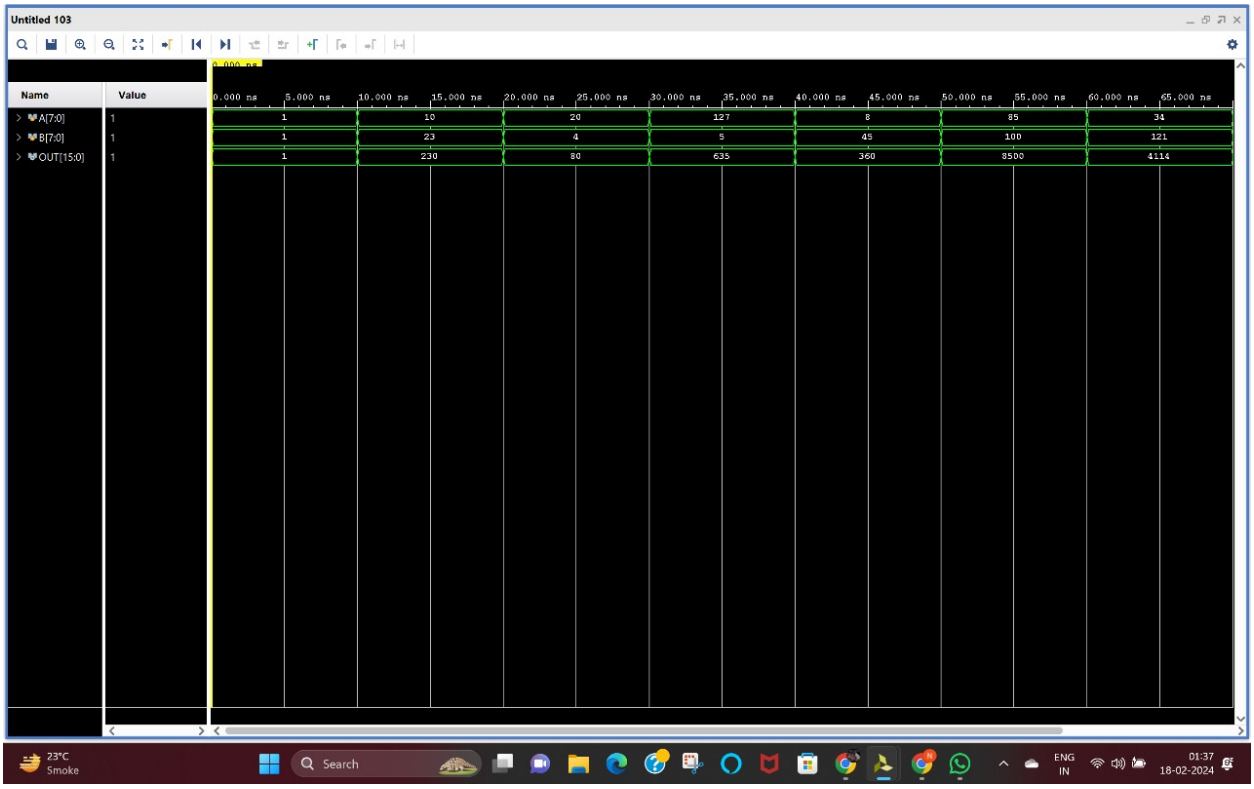
```
TestBench
TestBench
module binary_multiplier_tb();
    reg [7:0] A;
    reg [7:0] B;
    wire [15:0] OUT;
```

```
    binary_multiplier uut(A,B,OUT);
    A = 1; B = 1;
    #10;
    A = 10; B = 23;
    #10;
    A = 20; B = 4;
    #10;
    A = 127; B = 5;
    #10;
    A = 8; B = 45;
    #10;
    A = 85; B = 100;
    #10;
    A = 34; B = 121;
    #10;
endmodule
```

Schematic:



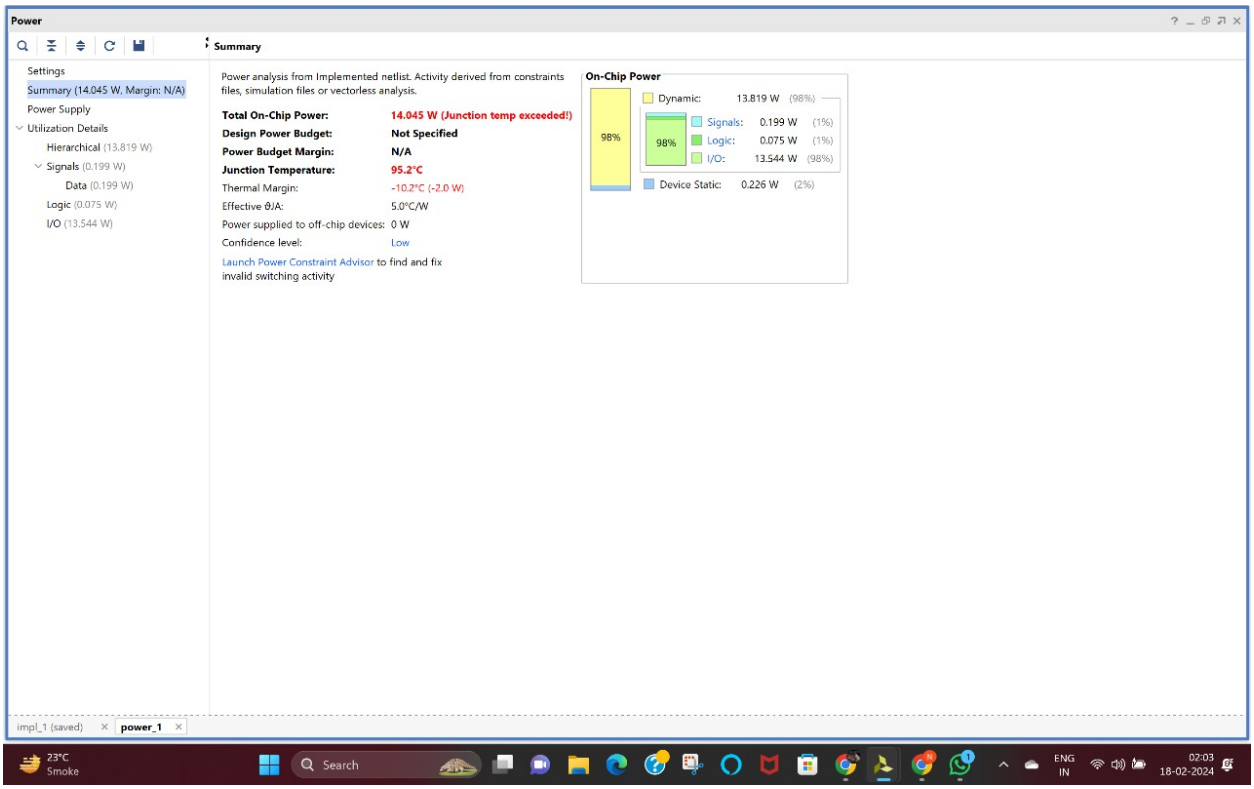
Simulations Results :

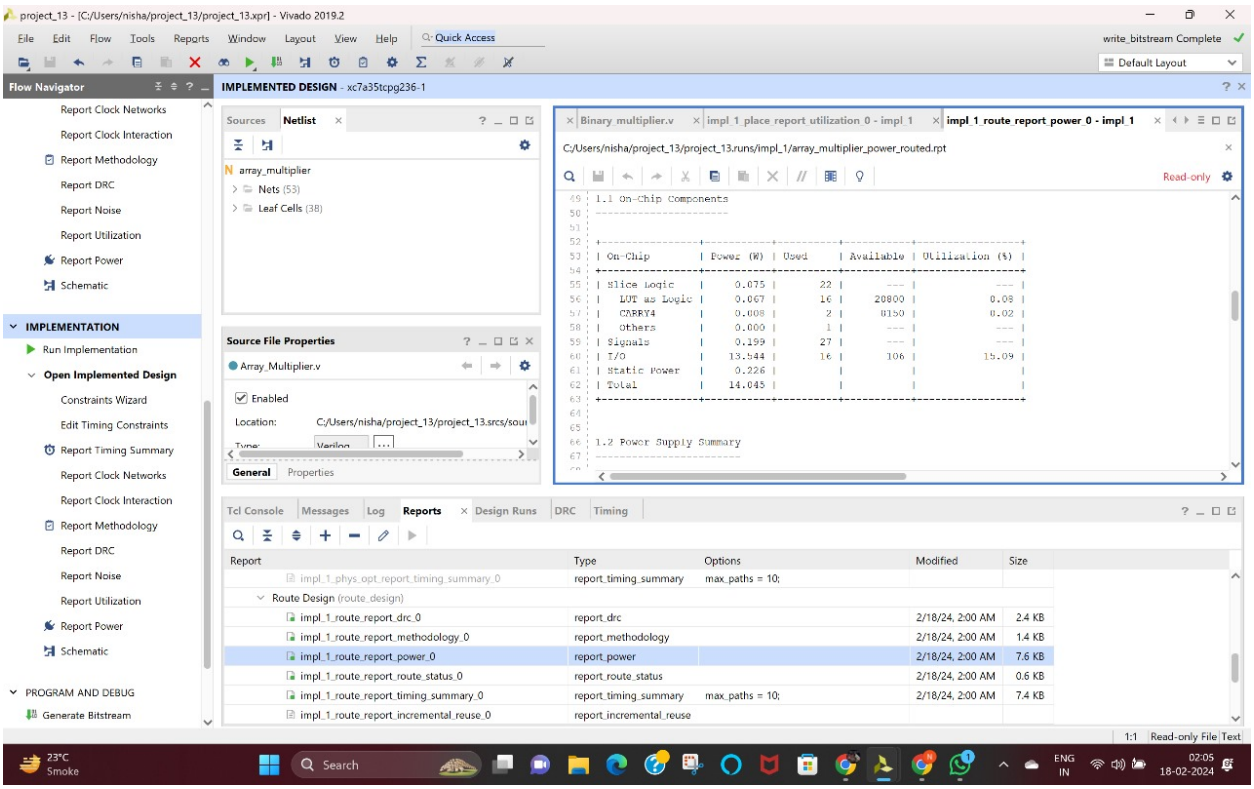


Comparison of a. Array multipliers and b. Binary multiplier

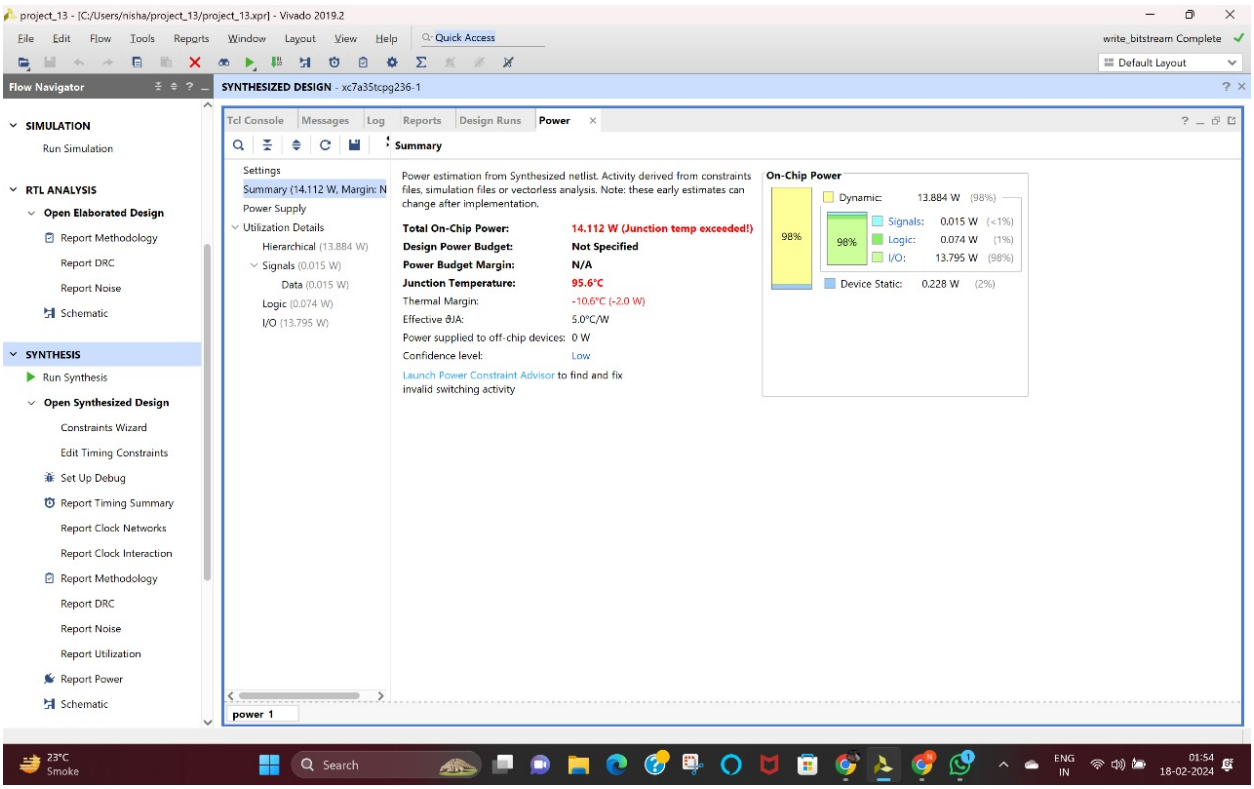
Power and Comparison

Array multiplier

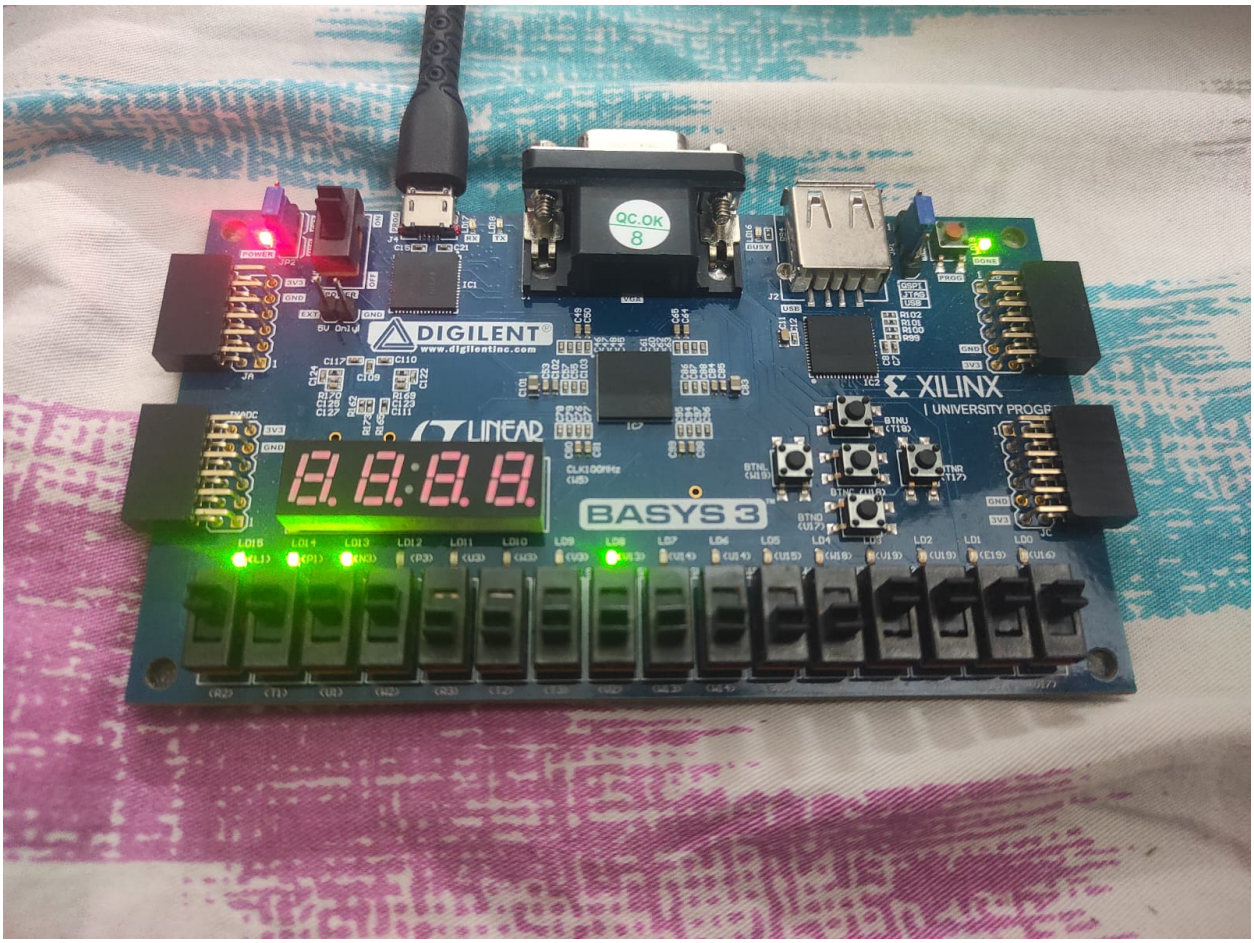




Binary multiplier



FPGA results:



We can see the programmed FPGA gives correct output.