BAHRIA UNIVERSITY (KARACHI CAMPUS)

FINAL EXAMINATION –SPRING SEMESTER – 2020

(Computer Organization and Assembly Language: CEN-323)

Class: **BS (CS)–3(A/B)** **(Morning)**

Course Instructor: **Aisha Danish** Time Allowed: **08 Hours**

Date:**4-July-2020** **Session: I** Max Marks: **50**

Student Name:_____ **Enrolment #**_____

Note: Attempt all questions in sequence
In addition to upload the solution on LMS, please also email it to course instructor. In order to avoid any run time electricity and internet unavailability situation, it is suggested that keep your laptop charged. Also activate 3G/4G connection as an alternative of Wifi/internet option to upload your solution.

Question 1 **[5+3]**

(a) Suppose you have to design a 32-bit instruction set architecture. Show the format of atleast 6 instructions. Specify the following fields (in number of bits) for each instruction that you will design:

Opcode

Addressing mode

Addresses (may be 0,1 or 2)

You are allowed to use any type of instruction for your design purpose e.g. arithmetic, logical, transfer of control etc.

(b) With reference to the instruction set that you design, answer the following:

i. How many total number of instructions can be present in your instruction set?

ii. How many addressing modes you have used in your instructions?

iii. How many positive integers can be stored in the address field that you have designed.

Question 2 **[3+3]**

(a) Use the Booth algorithm to multiply 20 (multiplicand) by 19 (multiplier), where each number is represented using 6 bits.

(b) Express the following numbers in IEEE 32-bit floating-point format:

i. -12

ii. 237

Question 3 **[3+3]**

(a) Briefly describe why Level 3 Cache was first introduced. In which processor it was implemented first? Show the complete organization of that system.

(b) The Intel Core i9 family of processors has a built in cache, identify which cache mapping technique is used in these processors. Elaborate the mapping technique with the help of diagram.

Question 4 **[3+3]**

(a) List any five mobile device Operating Systems supported by 32-bit ARM architecture. Which one is most widely used and why?

(b) With the help of diagram, show the abstraction of a network provided by an operating system.

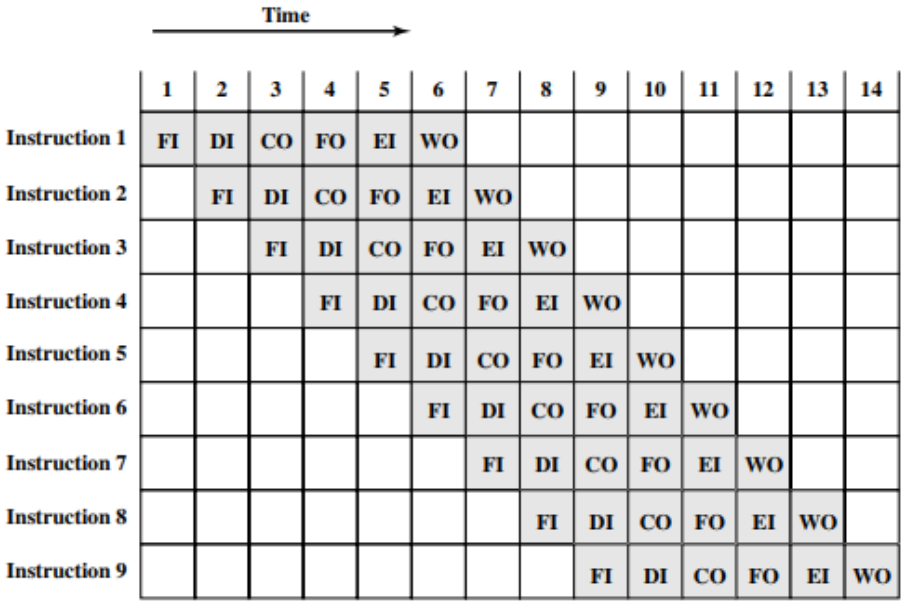
Question 5 **[3+3]**

(a) In MIMD processor architecture which one is best suited for enterprise server applications, shared memory or distributed memory? Justify your answer.

(b) Elaborate the concept of context switching**.**

Question 6 **[3+3]**

(a) Assume a pipeline with four stages: fetch instruction (FI), decode instruction and calculate addresses (DA), fetch operand (FO), and execute (EX). Draw a diagram similar to Figure 1 for a sequence of 8 instructions, in which the fourth instruction is a branch that is taken and in which there are no data dependencies.



Timing Diagram for Instruction Pipeline Operation

Figure 1

(b) How many number of pipeline stages are currently implemented in processors? Identify and list down any three processors and their respective number of pipeline stages.

Question 7 **[6x2]**

Give short answers to the following questions:

i. What is the benefit of using biased representation for the exponent portion of a floating-point number?

ii. Define Unified cache and split cache.

iii. List five major applications of vector processors.

iv. Why does x86 ISA has a segmented memory model?

v. Differentiate between Failover and Failback in multiprocessor organization.

vi. What is Assembler directive?