FINAL EXAM PAPER

BAHRIA UNIVERSITY (KARACHI CAMPUS)

FINAL EXAMINATION –SPRING SEMESTER – 2020

(Computer Organization and Assembly Language: CEN-323)

Class: **BS (CS)–3(A/B)** **(Morning)**

Course Instructor: **Aisha Danish** Time Allowed: **08 Hours**

Date:**4-July-2020** **Session: I** Max Marks: **50**

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Class: BSCS-3A

Note: Attempt all questions in sequence

Q1

(a) Suppose you have to design a 32-bit instruction set architecture. Show the format of atleast 6 instructions. Specify the following fields (in number of bits) for each instruction that you will design:

Opcode Addressing mode

Addresses (may be 0,1 or2)

You are allowed to use any type of instruction for your design purpose e.g. arithmetic, logical, transfer of control etc.

Ans.

X=(A*B*C)+D/(F-E)

Instruction Stack Contents	Content	Operand of Addressing mode
MOV R1,A	R1<-M[A]	0100
MUL R1,B	R1<-R1*B	1111
MUL R1,C	R1<-R1*C	1111
MOV R2,D	R2<-M[D]	0100
ADDR1,R2	R1<-R1+R2	0101
MOVR3,F	R3<-M[F]	0100
SUBR3,E	R3<-R3 E	1000

DIV R1,R3	R1<-R1/R3	
MOV Y, R1		0100

(b) With reference to the instruction set that you design, answer the following:

i. How many total number of instructions can be present in your instruction set?

Ans. There are total nine instruction that are present in my instruction set.

ii. How many addressing modes you have used in your instructions?

Ans. I have only used Director Addressing in my instruction set.

iii. How many positive integers can be stored in the address field that you have designed?

Ans. The range is 0 through 4,294,967,295(2^{11} -1) for representation as an unsigned binary number and -2,147,483,640(-2^{11}) through 2,147,483,647 (2^{11} -1) for representation as two's complement.

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Q2

(a). Use the Booth algorithm to multiply 20 (multiplicand) by 19 (multiplier), where each number is represented using 6 bits

Ans.

Let A = multiplicand = 20 = 010100

Let X = multiplier = 19 = 010011

A		0	1	0	1	0	0				20
Xx		0	1	0	0	1	1				19
Y		1	-1	0	1	0	-1		recoded multiplier		
Add -A	+	1	0	1	1	0	0				
Shift		1	1	0	1	1	0	0			
Shift Only				1	1	1	0	1	1	0	0
Add A	+	0	1	0	1	0	0				
		0	0	1	1	1	1	0	0		
Shift		0	0	0	1	1	1	1	0	0	
Shift Only				0	0	0	0	1	1	1	1
0	0										
Add -A	+	1	0	1	1	0	0				
	1	0	1	1	1	1	1	1	0	0	
Shift	1	1	0	1	1	1	1	1	1	0	0
Add A	+	0	1	0	1	0	0				
	0	0	1	0	1	1	1	1	1	0	0
Shift	0	0	0	1	0	1	1	1	1	1	0
0	=	380									

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(b). Express the following numbers in IEEE 32-bit floating-point format:

i. -12

ii. 237

Ans. i. -12

Step 1:
-12 conversion into binary form = 0100

Step 2: Normalize the number:
0.100 * 23

Step 3: Finding the exponent.
E – 127 = 3
So E = 130.

Step 4: Floating Point Representation:
Sign(1 bit) + exponent (8 bits) + Mantissa (23 bits).
Answer = 11000001010000000000000000000000

ii. 237

Step 1: Conversion into binary
237 = 11101101

Step 2: Normalize the number:
1.1101101 * 27

Step 3: Finding the exponent.
E – 127 = 7.
So E = 134.

Step 4: Floating point Representation.
Sign (1 bit) + exponent (8 bit) + Mantissa (23 bit)
Answer = 01000011011011010000000000000000

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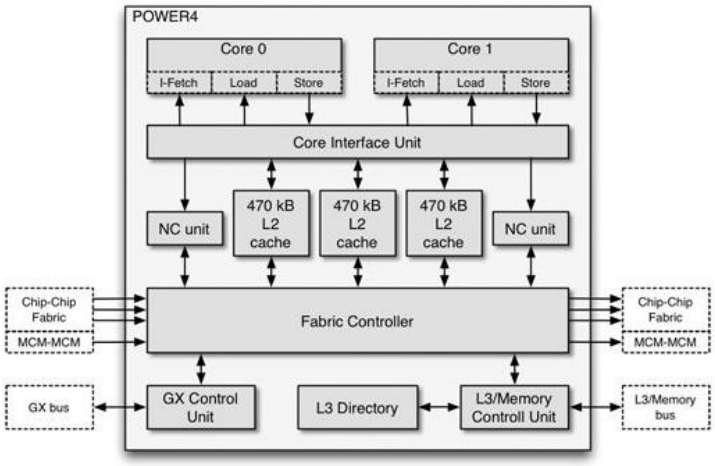
Q3

(a). Briefly describe why Level 3 Cache was first introduced. In which processor it was implemented first? Show the complete organization of that system.

Ans. A CPU cache is a hardware cache used by CPU of a computer to reduce the average cost (time or energy) to access data from main memory. A level 3 cache is a specialized cache that is used by the CPU and is usually built onto the motherboard and in certain special processors, within the CPU module itself. Level 3 cache was introduced to improve the performance of the CPU. It is usually slower than L2 cache but it can hold more data which makes it more efficient. The first consumer CPU to include Level 3 cache was Pentium 3 Extreme Edition which had a mammoth 2 MB of L3 cache back in 2003.



IBM POWER 4 ORGAN DIAGRAM

(b). The Intel Core i9 family of processors has a built in cache, identify which cache mapping technique is used in these processors. Elaborate the mapping technique with the help of diagram.

Ans. Intel core i9 have had multiple iterations the one we're going to be discussing is the 7900X core i9 released in 2018, this includes 10x1024 KB of 12 cache and 13.75 MB the implementation of the cache mapping technique is associative mapping as direct isn't used in most modern architectures as it is very hard to implement with multiple levels of cache with different transfer rates and different sizes.

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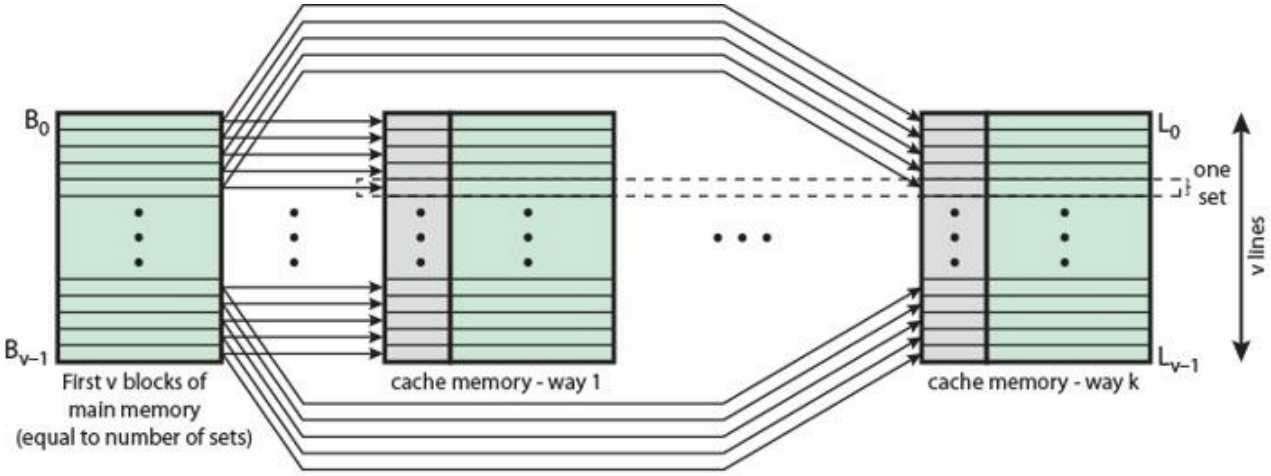

Following is the diagram showing how a CPU architecture is implemented of a core i9, in this we can see the L3 cache is outside and shared between all the cores as it should be, also L1 and L2 caches are present within the cores hence they're not shown separately.

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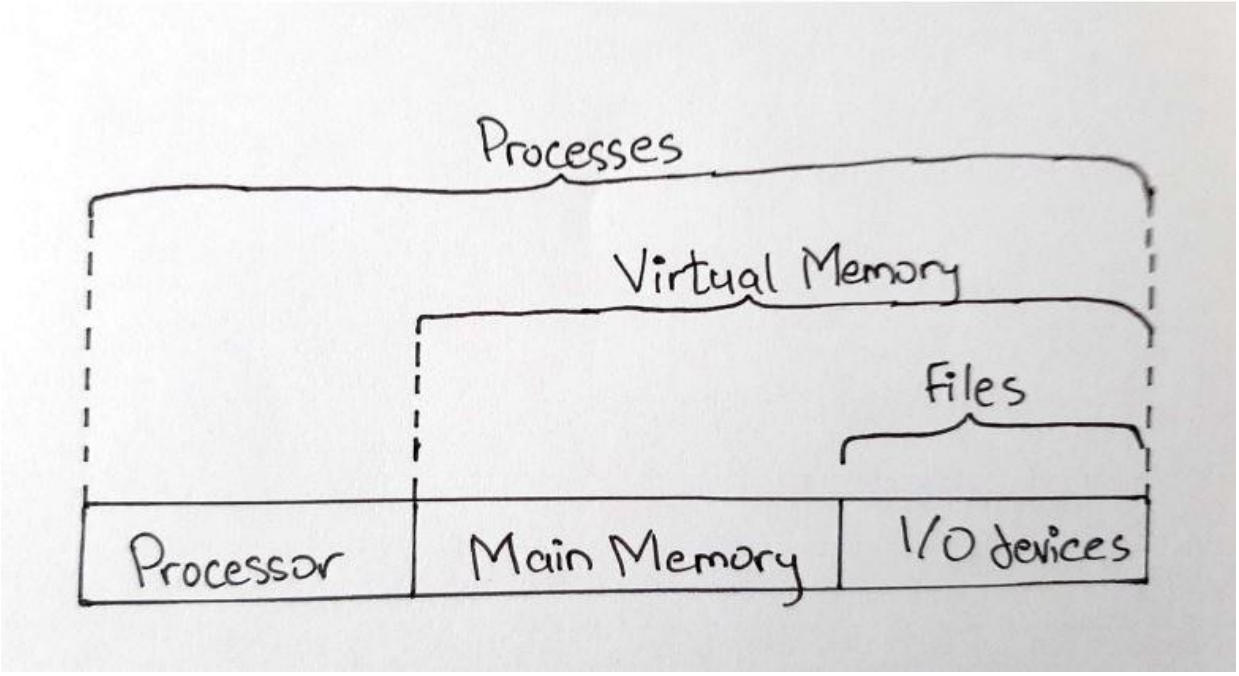
Q4

(a) List any five mobile device Operating Systems supported by 32-bit ARM architecture. Which one is most widely used and why?

Ans. Android, Tizen, Chrome Os, Blackberry 10 and ios10.

Android is most widely used due to the Global Partnerships And Large Installed Base, low cost of android phones but Quality smartphones, new features every often to attract new crowd, open source technology while also building on the contributions of the open-source Linux community and more than 300 hardware, software, and carrier partners, Android has rapidly become the fastest-growing mobile OS.

(b). With the help of diagram, show the abstraction of a network provided by an operating system.



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Q5

(a) In MIMD processor architecture which one is best suited for enterprise server applications, shared memory or distributed memory? Justify your answer.

Ans. Distributed Memory.

All processors in the system are directly connected to own memory and caches. Any processor can't directly access another processor's memory. Each mode has a network interface (NI). All communication and synchronization between processors happens via messages passed through the NI.

Transparency: Achieving the image of a single system image without concealing the details of the location, access, migration, concurrency, failure, relocation, persistence and resources to the users.

Openness: Making the network easier to configure and modify.

(b) Elaborate the concept of context switching**.**

Ans. In Operating System, Context Switching involves storing a context or state of a process so that it can be reloaded when required and execution can be resumed from the same point as earlier.

The steps involved in context switching are:

- Save the context of the process that is currently running on the CPU.
- Move the process control block of the above process to the relevant queue.
- Select a new process for execution.
- Update the process control block of the selected process.
- Update the memory management data structure as required.
- Restore the context of the process that was previously running when it is loaded on the processor.

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Q6

(a) Assume a pipeline with four stages: fetch instruction (FI), decode instruction and calculate addresses (DA), fetch operand (FO), and execute (EX). Draw a diagram similar to Figure 1 for a sequence of 8 instructions, in which the fourth instruction is a branch that is taken and in which there are no data dependencies.

Instructions	1	2	3	4	5	6	7	8	9	10	11
Inst 1	FI	DA	FO	EX							
Inst 2		FI	DA	FO	EX						
Inst 3			FI	DA	FO	EX					
Inst 4				FI	DA	FO	EX				
Inst 5					FI	DA	FO				
Inst 6						FI	DA				
Inst 7							FI				
Inst 16								FI	DA	FO	EX

(b). How many number of pipeline stages are currently implemented in processors? Identify and list down any three processors and their respective number of pipeline stages.

Ans. There are commonly 5 stages in pipeline stages currently implemented in processors.

1. Instruction Fetch (IF): Retrieval of Instructions from cache.
2. Instruction Decoding (ID): Identification of the operation to be performed.
3. Operand Fetch (OF): Decoding and retrieval of any required operands.
4. Execution (EX): Performing the operation on the operands.
5. Write-back (WB): Updating the destination operands.

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Q7

(i) What is the benefit of using biased representation for the exponent portion of a floating-point number?

Ans**.** Nonnegative floating-point numbers can be treated as integers for comparison purpose is the benefit of using biased representation for the exponent portion of a floating-point number.

(ii) Define Unified cache and split cache.

Ans. A split cache consists of two physically separate parts, where one part is called the instruction cache which is dedicated for holding instructions and the other is data cache for holding data. A unified cache consists of data and instructions in the same cache. It balances the load between instructions and data automatically

(iii) List five major applications of vector processors.

Ans**.** Image processing, artificial intelligence, mapping the human genome, hurricane predictions and space simulations.

(iv) Why does x86 ISA has a segmented memory model?

Ans. x86 ISA has a segmented memory model because it is based on a combination of two numbers; a memory segment and an offset within that segment. To support old software, the processor starts up in real mode in which it uses segmented addressing model.

(v) Differentiate between Failover and Failback in multiprocessor organization.

Ans. Failover is the process of shifting I/O and its processes from a primary location to a secondary disaster recovery location. Failback is the process of re-synchronizing the data back to the primary location, halting I/O and application activity and cutting over to the original location.

(vi) What is Assembler directive?

Ans. Assembler Directives are instructions that direct the assembler to do any task. This is used to set the program or register address during assembly. ORG (origin), EQU (equate) and DSB (define space for a byte) are some examples of assembler directives.

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