

UNIT-2 REGISTER TRANSFER AND MICROOPERATIONS (REF. CH-5 MORRIS MANO EDITED 3RD

Gaurang Patel

ED.)

OUTLINE

Digital Systems and Microoperations

Register Transfer Language

Register Transfer

Bus and Memory Transfers

Arithmetic Microoperations

Logic Microoperations

Shift Microoperations

Arithmetic Logic Shift Unit

DIGITAL SYSTEM

Combinational and sequential circuits can be used to create simple digital systems.

Digital System: An interconnection of hardware modules that do a certain task on the information.

Modules are interconnected with common data and control paths to form a digital computer system

DIGITAL SYSTEM

Simple digital systems are frequently characterized in terms of

- the registers they contain
- the operations that they perform
- the control that initiates the sequence of microoperations

Digital Module= Registers + Microoperations Hardware + Control Functions

MICROOPERATIONS

The operations executed on the data in registers are called microoperations

Examples of microoperations:

- Shift
- Load
- Clear
- Increment
- Add
- Subtract
- Complement
- • • •

MICROOPERATIONS

For any function of the computer, a sequence of microoperations is used to describe it

The result of the operation may be:

replace the previous binary information of a register or transferred to another register

Shift Right Operation

101101110011

Shift Right Operation

010110111001

REGISTER TRANSFER LANGUAGE

Register Transfer Language (RTL): a symbolic notation to describe the microoperation transfers among registers

Register transfer => the availability of hardware logic circuits that can perform a stated microoperation and transfer the result to the same or another register

Language => programming language

A convenient tool for describing the internal organization of digital computers

Can also be used to facilitate the design process of digital systems.

REGISTER TRANSFER (OUR FIRST MICROOPERATION)

Computer registers are designated by capital letters (sometimes followed by numerals) to denote the function of the register

R1: processor register

MAR: Memory Address Register (holds an address for a memory unit)

PC: Program Counter

IR: Instruction Register

SR: Status Register

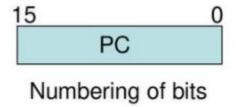
The individual flip-flops in an n-bit register are numbered in sequence from 0 to n-1 (from the right position toward the left position)

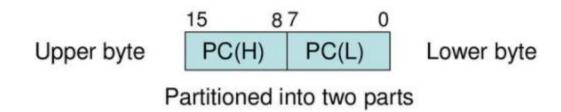
R1 7 6 5 4 3 2 1 0

Register R1 Showing individual bits

A block diagram of a register

Other ways of drawing the block diagram of a register:





Information transfer from one register to another is described by a replacement operator: $R2 \leftarrow R1$

This statement denotes a transfer of the content of register R1 into register R2

The transfer happens in one clock cycle

The content of the R1 (source) does not change

The content of the R2 (destination) will be lost and replaced by the new data transferred from R1

We are assuming that the circuits are available from the outputs of the source register to the inputs of the destination register, and that the destination register has a parallel load capability

Conditional transfer occurs only under a control condition

Representation of a (conditional) transfer

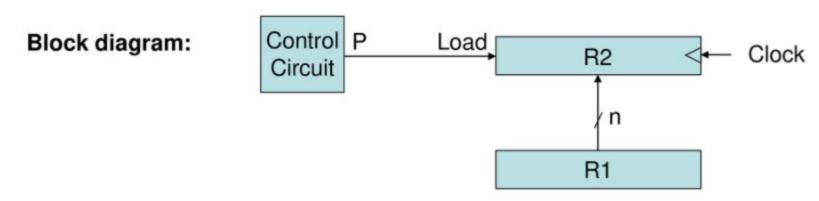
• P: R2 ← R1

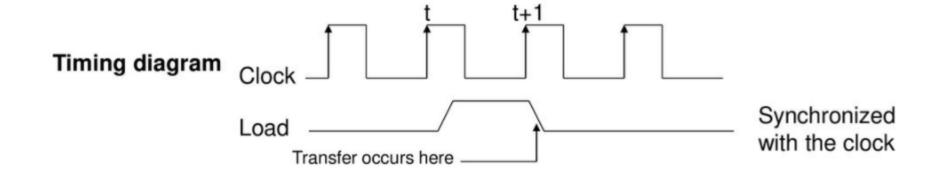
A binary condition (P equals to 0 or 1) determines when the transfer occurs

The content of R1 is transferred into R2 only if P is 1

Note: P is called control function (Boolean variable that is equal to 0 or 1)

Hardware implementation of a controlled transfer: $P: R2 \leftarrow R1$





Basic Symbols for Register Transfers				
Symbol	Description	Examples		
Letters & numerals	Denotes a register	MAR, R2		
Parenthesis ()	Denotes a part of a register	R2(0-7), R2(L)		
Arrow ← Denotes transfer of information		R2 ← R1		
Comma,	Separates two microoperations	R2 ← R1, R1 ← R2		

BUS AND MEMORY TRANSFERS

Paths must be provided to transfer information from one register to another

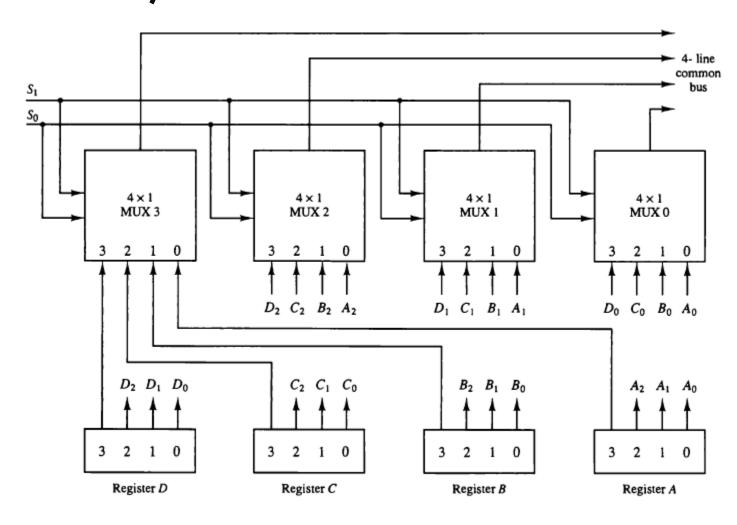
The number of wires will be excessive if separate lines are used between each register and all other registers in the system

A **Common Bus System** is a scheme for transferring information between registers in a multiple-register configuration

A bus: set of common lines, one for each bit of a register, through which binary information is transferred one at a time

Control signals determine which register is selected by the bus during each particular register transfer

BUS AND MEMORY TRANSFERS (BUS SYSTEM FOR 4 REGISTERS)



BUS AND MEMORY TRANSFERS

The transfer of information from a bus into one of many destination registers is done:

- By connecting the bus lines to the inputs of all destination registers and then:
- activating the load control of the particular destination register selected

We write: $R2 \leftarrow C$ to symbolize that the content of register C is loaded into the register R2 using the common system bus

It is equivalent to: BUS \leftarrow C, (select C)R2 \leftarrow BUS (Load R2)

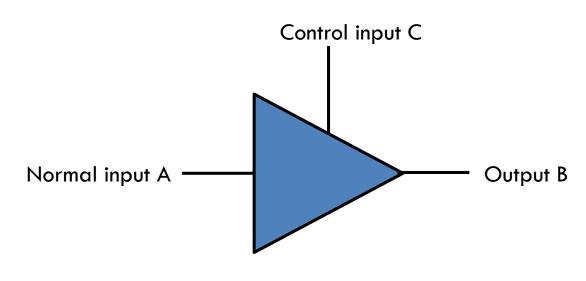
BUS AND MEMORY TRANSFERS: THREE-STATE BUS BUFFERS

A bus system can be constructed with three-state buffer gates instead of multiplexers

A three-state buffer is a digital circuit that exhibits three states: logic-0, logic-1, and high-impedance (Hi-Z)

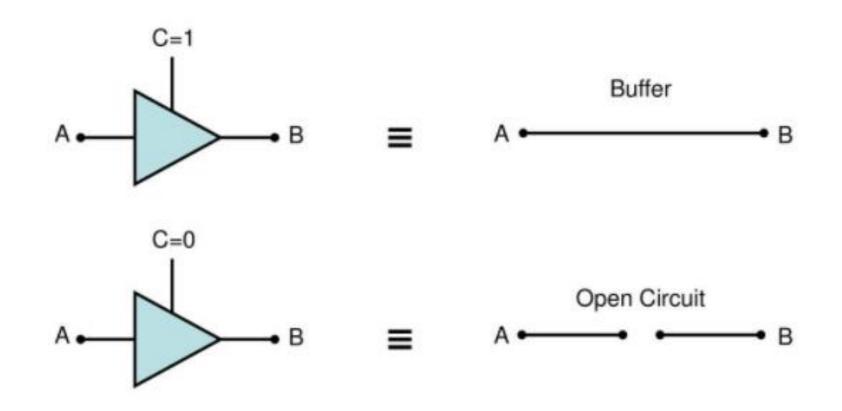
The Hi-Z state behaves like an open circuit

The output is disconnected and does not have a logic significance

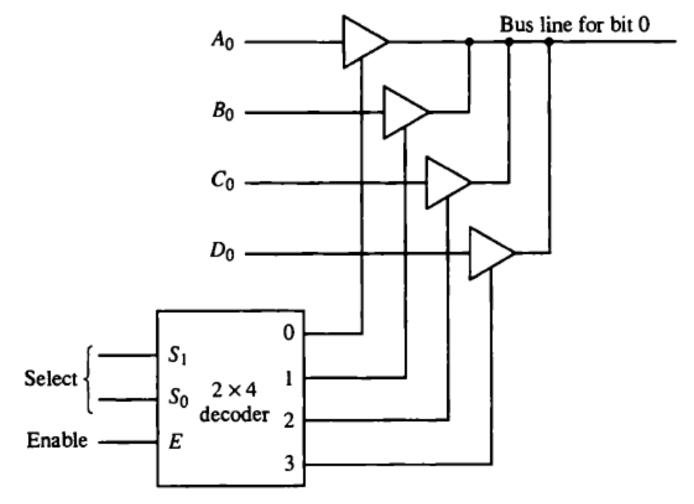


Three-State Buffer

BUS AND MEMORY TRANSFERS: THREE-STATE BUS BUFFERS



BUS AND MEMORY TRANSFERS: THREE-STATE BUS BUFFERS



BUS AND MEMORY TRANSFERS: MEMORY TRANSFER

Memory read: Transfer from memory

Memory write: Transfer to memory

Data being read or wrote is called a memory word (called M)It is necessary to specify the address of M when writing /reading memory

This is done by enclosing the address in square brackets following the letter M

Example: M[0016]: the memory contents at address 0x0016

BUS AND MEMORY TRANSFERS: MEMORY TRANSFER

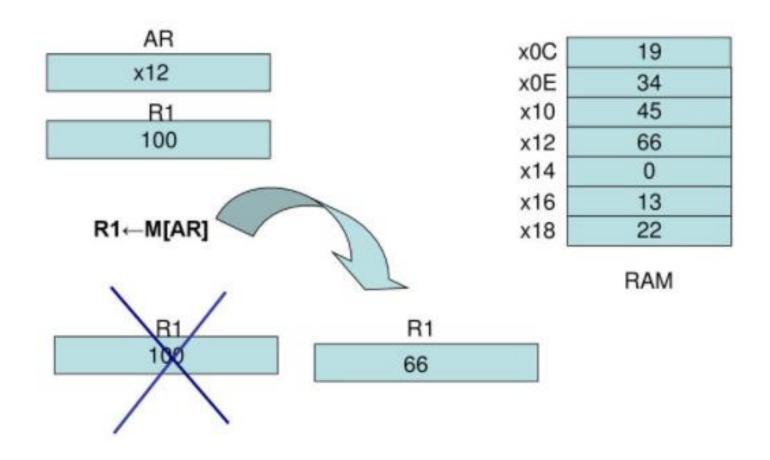
Assume that the address of a memory unit is stored in a register called the Address Register AR

Lets represent a Data Register with DR, then:

• Read: DR \leftarrow M[AR]

 \bullet Write: M[AR] ← DR

BUS AND MEMORY TRANSFERS: MEMORY TRANSFER



ARITHMETIC MICROOPERATIONS

The microoperations most often encountered in digital computers are classified into four categories:

- Register transfer microoperations
- Arithmetic microoperations (on numeric data stored in the registers)
- Logic microoperations (bit manipulations on non-numeric data)
- Shift microoperations

ARITHMETIC MICROOPERATIONS

The basic arithmetic microoperations are: addition, subtraction, increment and decrement

Addition Microoperation:

Subtraction Microoperation:

$$R3 \leftarrow R1-R2 \text{ or } :$$

 $R3 \leftarrow R1 + R2' + 1$ (with 2's complement)

ARITHMETIC MICROOPERATIONS

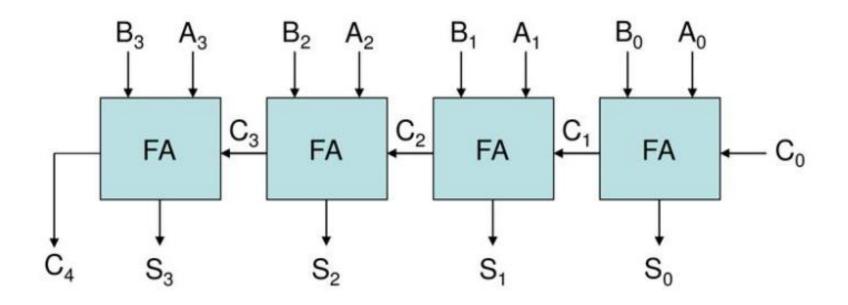
One's Complement Microoperation:

Two's Complement Microoperation:

Increment Microoperation:

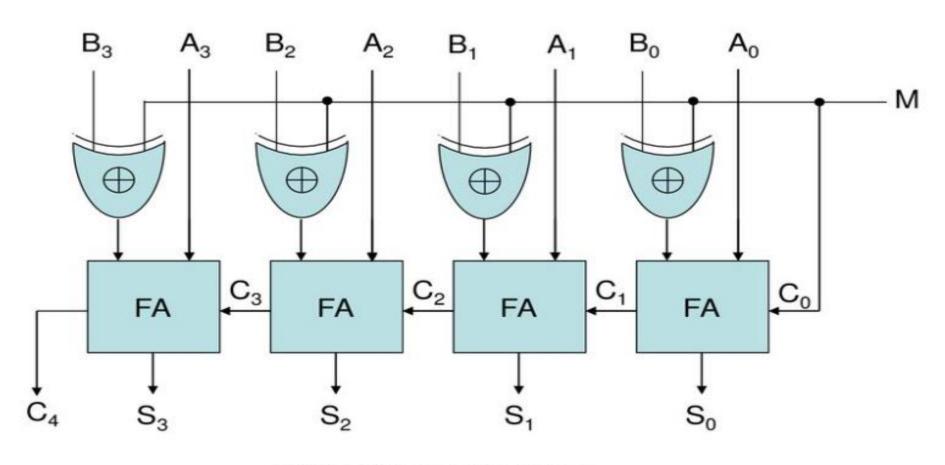
Decrement Microoperation:

BUS AND MEMORY TRANSFERS: BINARY ADDER



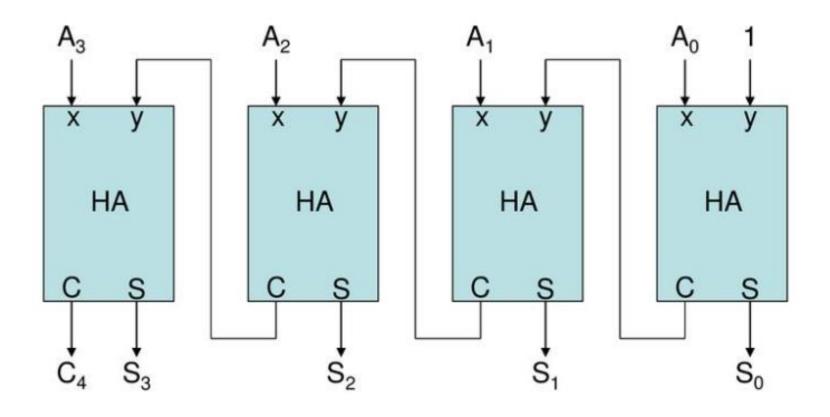
4-bit binary adder (connection of FAs)

BUS AND MEMORY TRANSFERS: BINARY ADDER-SUBTRACTOR



4-bit adder-subtractor

BUS AND MEMORY TRANSFERS: BINARY INCREMENTER



4-bit Binary Incrementer

BUS AND MEMORY TRANSFERS: BINARY INCREMENTER

Binary Incrementer can also be implemented using a counter

A binary decrementer can be implemented by adding 1111 to the desired register each time!

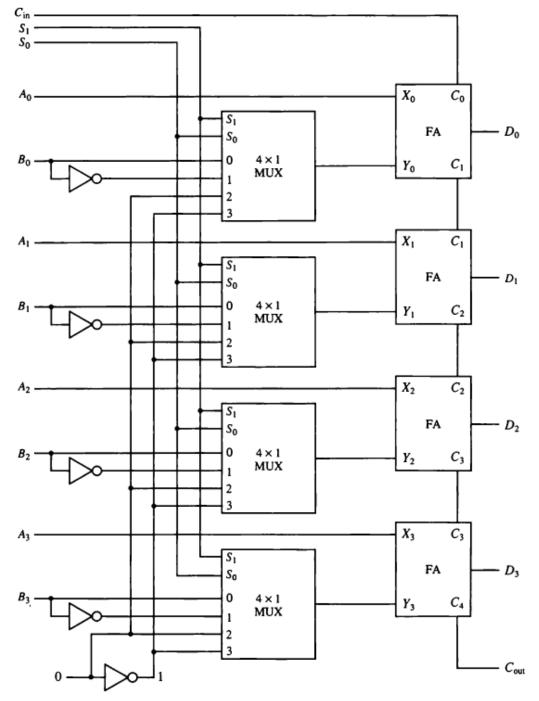


Figure 4-9 4-bit arithmetic circuit.

 TABLE 4-4 Arithmetic Circuit Function Table

Select		Innut	Output		
$\overline{S_1}$	So	C_{in}	Input Y	Output $D = A + Y + C_{in}$	Microoperation
0	0	0	В	D = A + B	Add
0	0	1	В	D = A + B + 1	Add with carry
0	1	0	\overline{B}	$D = A + \overline{B}$	Subtract with borrow
0	1	1	\overline{B}	$D=A+\overline{B}+1$	Subtract
1	0	0	0	D = A	Transfer A
1	0	1	0	D=A+1	Increment A
1	1	0	1	D=A-1	Decrement A
1	1	1	1	D = A	Transfer A

OR Microoperation

Symbol: ∨, +

· Gate:

• Example: $100110_2 \lor 1010110_2 = 1110110_2$

P+Q: R1←R2+R3, R4←R5 √R6

AND Microoperation

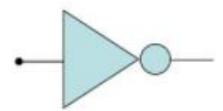
Symbol: ∧

• Gate:

• Example: $100110_2 \land 1010110_2 = 0000110_2$

Complement (NOT) Microoperation

· Gate:

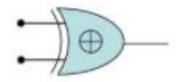


• Example: $\overline{1010110}_2 = 0101001_2$

XOR (Exclusive-OR) Microoperation

Symbol: ⊕

Gate:



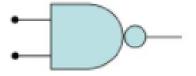
Example: 100110₂ ⊕ 1010110₂ = 1110000₂

LOGIC MICROOPERATIONS: OTHER LOGIC MICROOPERATIONS

NAND Microoperation

Symbols: ∧ and ¯

· Gate:



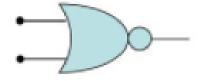
• Example: $100110_2 \land 1010110_2 = 1111001_2$

LOGIC MICROOPERATIONS: OTHER LOGIC MICROOPERATIONS

NOR Microoperation

Symbols: ∨ and ¯

Gate:



• Example: $1\overline{00110_2} \lor 1010110_2 = 0001001_2$

LOGIC MICROOPERATIONS: OTHER LOGIC MICROOPERATIONS

Set (Preset) Microoperation

Force all bits into 1's by ORing them with a value in which all its bits are being assigned to logic-1

Example: $100110_2 \text{ v } 1111111_2 = 1111111_2$

Clear (Reset) Microoperation

Force all bits into 0's by ANDing them with a value in which all its bits are being assigned to logic-0

Example: $100110_2 \land 000000_2 = 0000000_2$

TABLE 4-6 Sixteen Logic Microoperations

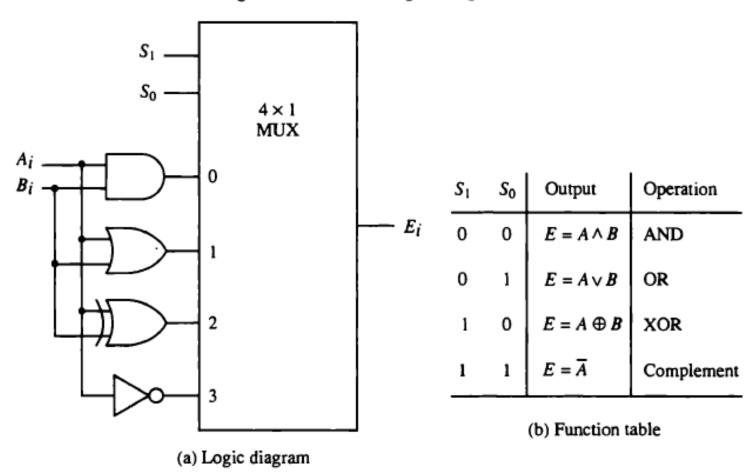
Boolean function	Microoperation	Name
$F_0 = 0$	<i>F</i> ←0	Clear
$F_1 = xy$	$F \leftarrow A \land B$ $F \leftarrow A \land \overline{B}$	AND
$F_2 = xy'$ $F_3 = x$	$F \leftarrow A$	Transfer A
$F_4 = x'y$ $F_5 = y$	$F \leftarrow \overline{A} \land B$ $F \leftarrow B$	Transfer B
$F_6 = x \oplus y$	$F \leftarrow A \oplus B$	Exclusive-OR
$F_7 = x + y$ $F_8 = (x + y)'$	$F \leftarrow A \vee B \\ F \leftarrow \overline{A \vee B}$	OR NOR
$F_9=(x\oplus y)'$	$F \leftarrow \overline{A \oplus B}$	Exclusive-NOR
$F_{10} = y'$ $F_{11} = x + y'$	$F \leftarrow \overline{B} \\ F \leftarrow A \lor \overline{B}$	Complement B
$F_{12}=x'$	$F \leftarrow \overline{A}$	Complement A
$F_{13} = x' + y$ $F_{14} = (xy)'$	$F \leftarrow \overline{A} \vee B \\ F \leftarrow \overline{A} \wedge \overline{B}$	NAND
$F_{15}=1$	$F \leftarrow \text{all 1's}$	Set to all 1's

LOGIC MICROOPERATIONS: HARDWARE IMPLEMENTATION

The hardware implementation of logic microoperations requires that logic gates be inserted for each bit or pair of bits in the registers to perform the required logic function

Most computers use only four (AND, OR, XOR, and NOT) from which all others can be derived.

Figure 4-10 One stage of logic circuit.



SHIFT MICROOPERATIONS

Used for serial transfer of data

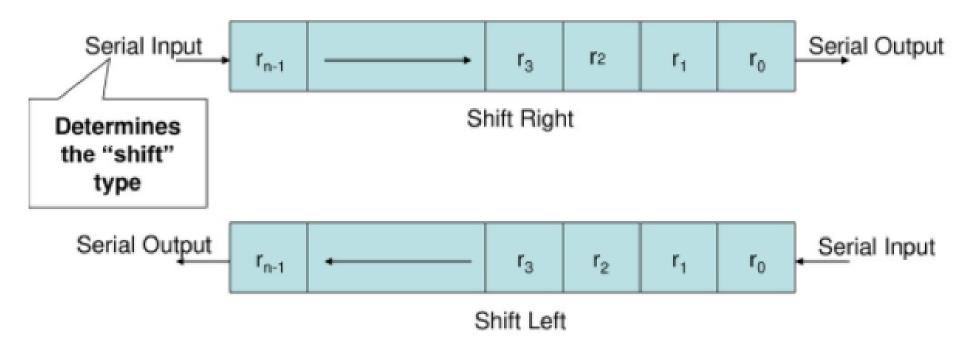
Also used in conjunction with arithmetic, logic, and other dataprocessing operations

The contents of the register can be shifted to the left or to the right

As being shifted, the first flip-flop receives its binary information from the serial input

Three types of shift: Logical, Circular, and Arithmetic

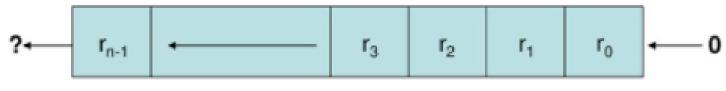
SHIFT MICROOPERATIONS



^{**}Note that the bit ri is the bit at position (i) of the register

SHIFT MICROOPERATIONS: LOGICAL SHIFTS

- Transfers 0 through the serial input
- Logical Shift Right: R1←shr R1

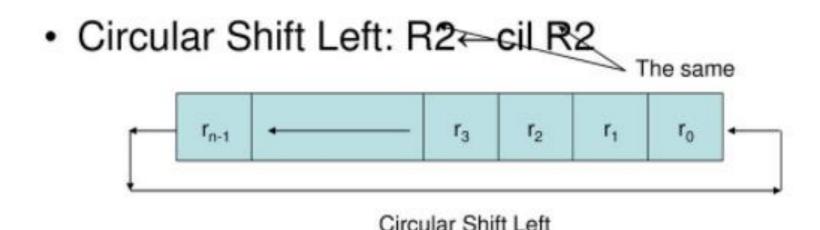


Logical Shift Left

SHIFT MICROOPERATIONS: CIRCULAR SHIFTS (ROTATE OPERATION)

- Circulates the bits of the register around the two ends without loss of information
- Circular Shift Right: R⁴←cir R¹

 The same



SHIFT MICROOPERATIONS: ARITHMETIC SHIFTS

Shifts a signed binary number to the left or right

An arithmetic shift-left multiplies a signed binary number by 2:

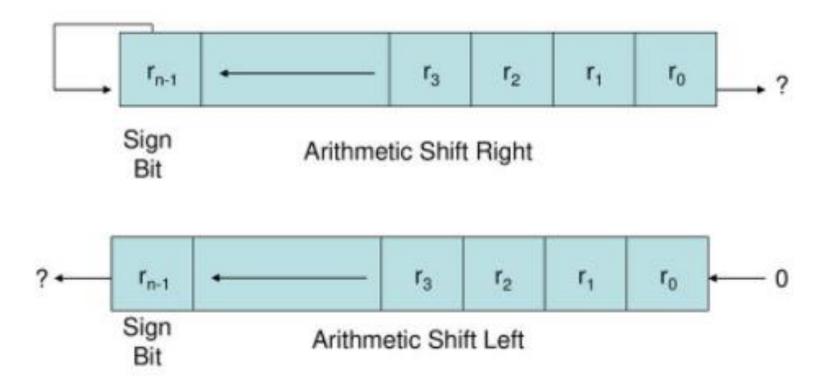
• ashl (00100):

An arithmetic shift-right divides the number by 2:

ashr (00100): 00010

An overflow may occur in arithmetic shift-left, and occurs when the sign bit is changed (sign reversal)

SHIFT MICROOPERATIONS: ARITHMETIC SHIFTS



SHIFT MICROOPERATIONS: ARITHMETIC SHIFTS

An overflow flip-flop Vs can be used to detect an arithmetic shiftleft overflow

$$V_s = R_{n-1} \oplus R_{n-2}$$

$$R_{n-2}$$
 $V_s = \begin{cases} 1 \rightarrow \text{overflow} \\ 0 \rightarrow \text{no overflow} \end{cases}$

SHIFT MICROOPERATIONS

Circular shift left once

```
Example: Assume R1=11001110, then:

    Arithmetic shift right once : R1 = 11100111

    Arithmetic shift right twice : R1 = 11110011

    Arithmetic shift left once : R1 = 10011100

- Arithmetic shift left twice : R1 = 00111000
- Logical shift right once : R1 = 01100111
- Logical shift left once : R1 = 10011100
- Circular shift right once : R1 = 01100111
```

: R1 = 10011101

SHIFT MICROOPERATIONS: HARDWARE IMPLEMENTATION

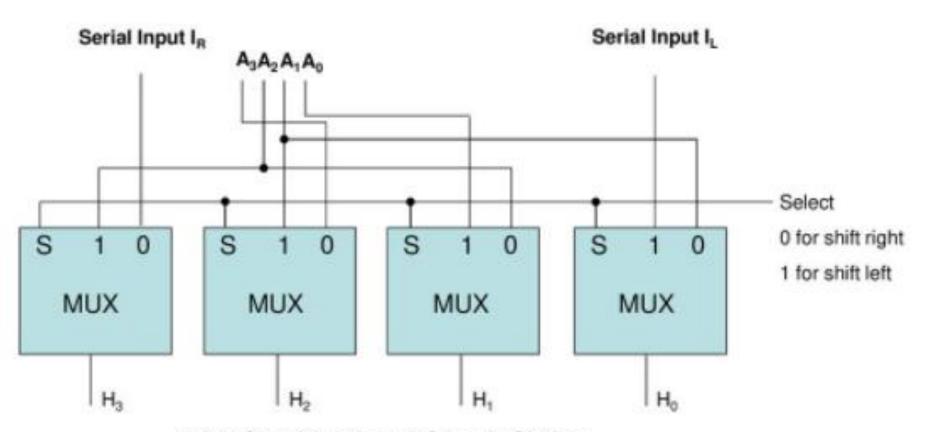
A possible choice for a shift unit would be a bidirectional shift register with parallel load (refer to Fig 2-9). Has drawbacks:

Needs two pulses (the clock and the shift signal pulse)

Not efficient in a processor unit where multiple number of registers share a common bus

It is more efficient to implement the shift operation with a combinational circuit

SHIFT MICROOPERATIONS: HARDWARE IMPLEMENTATION



Function table							
Output							
H_0	H_1	H ₂	Н3				
I_R	A_0	A_1	A_2				
A_1	A ₂	A ₃	I _L				
	${H_0}$ I_R	$\frac{\text{Outp}}{H_0 H_1}$ $I_R A_0$	$ \begin{array}{c cccc} \hline Output \\ \hline H_0 & H_1 & H_2 \\ \hline I_R & A_0 & A_1 \end{array} $				

4-bit Combinational Circuit Shifter

ARITHMETIC LOGIC SHIFT UNIT

Instead of having individual registers performing the microoperations directly, computer systems employ a number of storage registers connected to a common operational unit called an Arithmetic Logic Unit (ALU)

ARITHMETIC LOGIC SHIFT UNIT

Fig.A-> slide no. 31 Fig.B-> slide no. 41

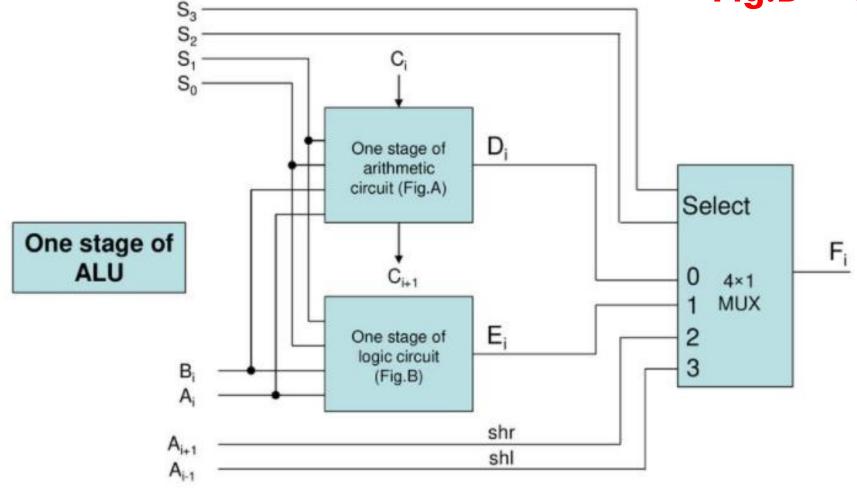


TABLE 4-8 Function Table for Arithmetic Logic Shift Unit

Operation select						
S_3	S_2	S_1	S _o	C_{in}	Operation	Function
0	0	0	0	0	F = A	Transfer A
0	0	0	0	1	F = A + 1	Increment A
0	0	0	1	0	F = A + B	Addition
0	0	0	1	1	F = A + B + 1	Add with carry
0	0	1	0	0	$F = A + \overline{B}$	Subtract with borrow
0	0	1	0	1	$F = A + \overline{B} + 1$	Subtraction
0	0	1	1	0	F = A - 1	Decrement A
0	0	1	1	1	F = A	Transfer A
0	1	0	0	×	$F = A \wedge B$	AND
0	1	0	1	×	$F = A \vee B$	OR
0	1	1	0	×	$F = A \oplus B$	XOR
0	1	1	1	×	$F = \overline{A}$	Complement A
1	0	×	×	×	$F = \operatorname{shr} A$	Shift right A into F
1	1	×	x	×	$F = \operatorname{shl} A$	Shift left A into F

Thonk You