

# UNIT-1 INTRODUCTION TO DIGITAL CIRCUITS (REF. CH-1 MORRIS MANO EDITED 3<sup>RD</sup> ED.)

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### DIGITAL COMPUTERS

A Digital system that performs various computational tasks

The word digital implies that the information in the computer is represented by variables that take a limited number od discrete values

These values are processed internally by components that can maintain a limited number of discrete states

Eg. Decimal digits 0...9 provide 10 discrete values

The first electronic digital computers were primarily used for numerical computations

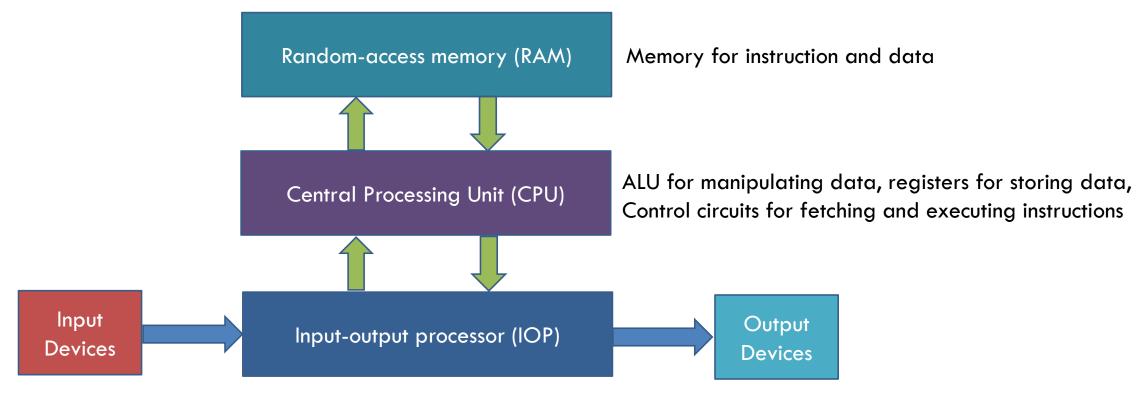
In this case, the discrete elements are digits

From this, the term digital computers has emerged

### DIGITAL COMPUTERS

Because of physical restrictions of components, and human logic tends to be binary, digital components are constrained to take only two values i.e. Binary

### BLOCK DIAGRAM OF A DIGITAL COMPUTER



Communicating and controlling transfer of information between the computer and the outside world

### LOGIC GATES

Binary information is represented in digital computers by physical quantities called **signals** 

Electrical signals such as voltage exist throughout the computer in either of one of two recognizable states i.e. 0 and 1

Signal 3 volts to represent binary 1

Signal 0.5 volt to represent binary 0

The manipulation of the binary information is done by logic circuits called **gates** 

Gates are blocks of hardware that produce signals of binary 1 or 0 when input logic requirements are satisfied

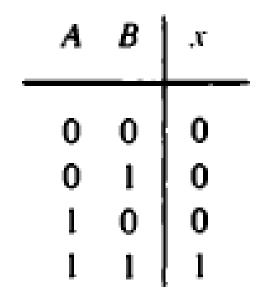
### AND GATE

#### **Symbol**



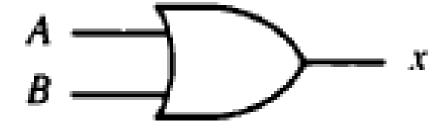
#### **Algebraic function**

$$x = A \cdot B$$
  
or  
 $x = AB$ 



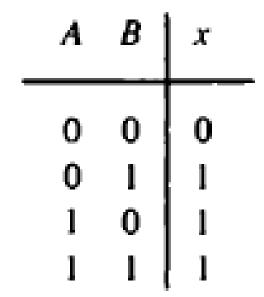
### **OR GATE**

#### **Symbol**



#### **Algebraic function**

$$x = A + B$$



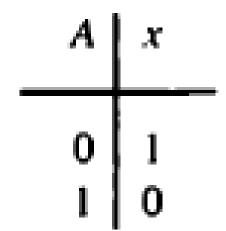
### **INVERTER**

#### **Symbol**



#### **Algebraic function**

$$x = A'$$



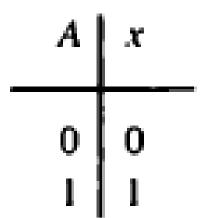
### **BUFFER**

#### **Symbol**



#### **Algebraic function**

$$x = A$$



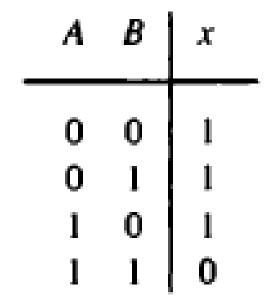
### NAND GATE

#### **Symbol**



#### **Algebraic function**

$$x = (AB)'$$



### NOR GATE

#### **Symbol**



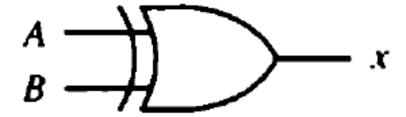
#### **Algebraic function**

$$x = (A + B)'$$

| <br>Α | В | х |
|-------|---|---|
| 0     | 0 | 1 |
| 0     | 1 | 0 |
| 1     | 0 | 0 |
| 1     | 1 | 0 |

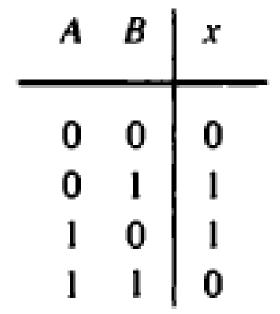
### X-OR GATE

#### **Symbol**



#### **Algebraic function**

$$x = A \oplus B$$
  
or  
 $x = A'B + AB'$ 



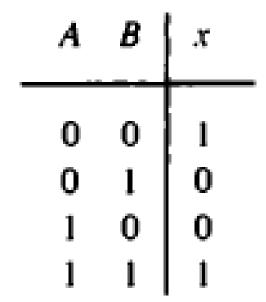
### X-NOR GATE

#### **Symbol**



#### Alashraic function

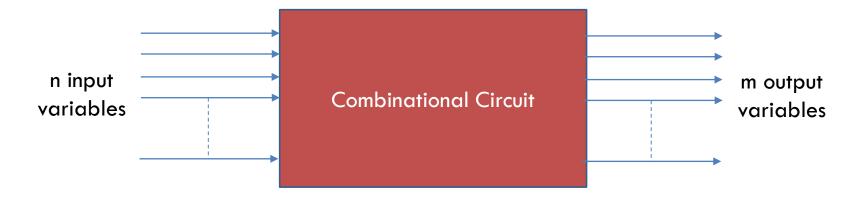
$$x = (A \oplus B)'$$
or
$$x = A'B' + AB$$



### COMBINATIONAL CIRCUITS

A **Combinational circuit** is a connected arrangement of logic gates with a set of inputs and outputs

At any given time, the binary values of the outputs are a function of the binary combination of the inputs



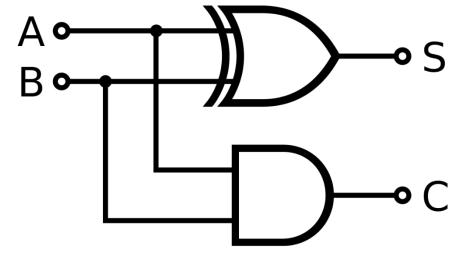
### **COMBINATIONAL CIRCUITS**

Design procedure of a Combinational Circuit

- 1. The problem is stated
- 2. The input and output variables are assigned letter symbols
- 3. The truth table that defines the relationship between inputs and outputs is derived
- 4. The simplified Boolean functions for each output are obtained
- 5. The logic diagram is drawn

### HALF ADDER

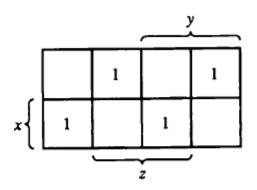
| Inp | uts | Outputs |       |  |
|-----|-----|---------|-------|--|
| Α   | В   | Sum     | Carry |  |
| 0   | 0   | 0       | 0     |  |
| 0   | 1   | 1       | 0     |  |
| 1   | 0   | 1       | 0     |  |
| 1   | 1   | 0       | 1     |  |



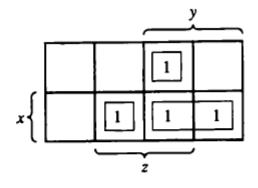
$$S = A' B + A B' = A \bigoplus B$$
  
 $C = A B$ 

### FULL ADDER

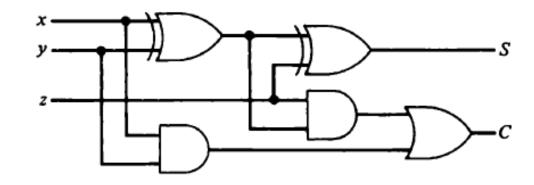
| Inputs |   |                 | Outputs |       |
|--------|---|-----------------|---------|-------|
| Α      | В | C <sub>in</sub> | Sum     | Carry |
| 0      | 0 | 0               | 0       | 0     |
| 0      | 0 | 1               | 1       | 0     |
| 0      | 1 | 0               | 1       | 0     |
| 0      | 1 | 1               | 0       | 1     |
| 1      | 0 | 0               | 1       | 0     |
| 1      | 0 | 1               | 0       | 1     |
| 1      | 1 | 0               | 0       | 1     |
| 1      | 1 | 1               | 1       | 1     |



$$S = x'y'z + x'yz' + xy'z' + xyz$$
$$= x \oplus y \oplus z$$



C = xy + xz + yz= xy + (x'y + xy')z



### FLIP-FLOPS

In case of combinational circuits, the outputs at any given time are entirely dependent on inputs that are present at that time

The combinational circuits do not have storage elements

The circuit which includes combinational circuit with storage elements are called **Sequential Circuit** 

The most common type of sequential circuit is the synchronous type

Synchronous circuits employ signals that affect the storage elements only at discrete instants of time

This is achieved by timing device called clock pulse generator which produces a periodic train of clock pulses

### FLIP-FLOPS

The storage elements employed in clocked sequential circuits are called **flip-flops** 

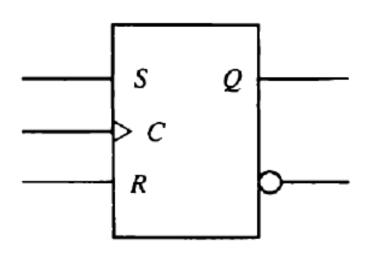
A flip-flop is a binary cell capable of storing one bit of information

Having two outputs

- Normal value
- Complement value of the bit stored

Maintains a binary state until directed by a clock pulse to switch states

### SR FLIP-FLOP

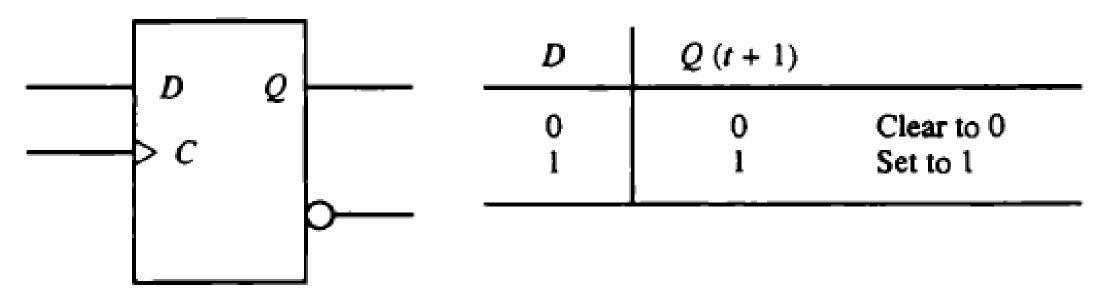


(a) Graphic symbol

| S R | Q(t+1) |               |
|-----|--------|---------------|
| 0 0 | Q(t)   | No change     |
| 0 1 | 0      | Clear to 0    |
| 1 0 | 1      | Set to 1      |
| 1 1 | ?      | Indeterminate |

(b) Characteristic table

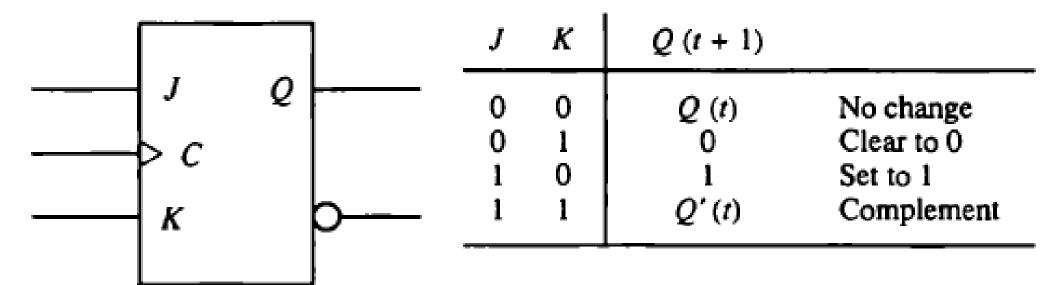
### D FLIP-FLOP



(a) Graphic symbol

(b) Characteristic table

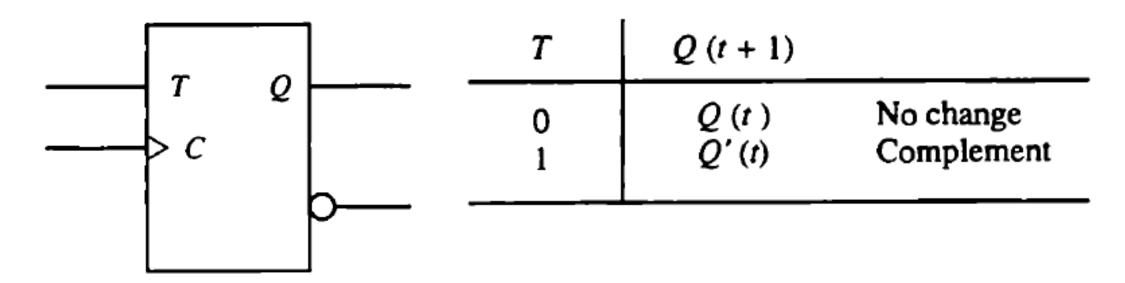
### JK FLIP-FLOP



(a) Graphic symbol

(b) Characteristic table

### T FLIP-FLOP



(a) Graphic symbol

(b) Characteristic table

### EDGE TRIGGERED

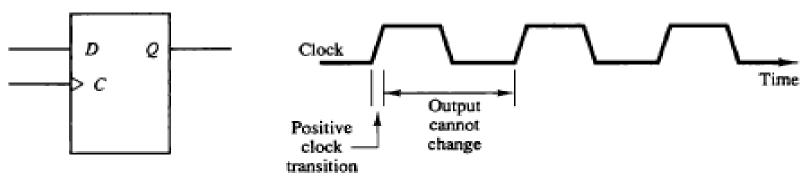
In this type of flip-flop, output transitions occur at a specific level of the clock pulse

When the clock pulse level exceeds this threshold level, the inputs are locked out so that the flip-flop is irresponsive to further changes in inputs until the clock pulse returns to 0 and another pulse occurs

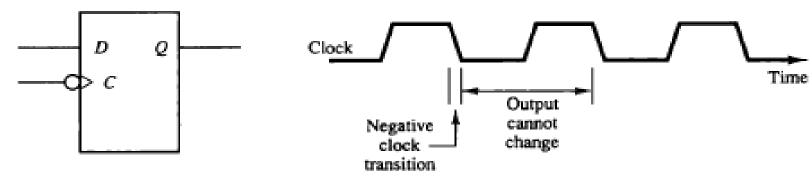
Some edge-triggered flip-flops cause transition on the rising edge of the clock signal

Others cause transition on the falling edge

### EDGE TRIGGERED



(a) Positive-edge-triggered D flip-flop.



(b) Negative-edge-triggered D flip-flop.

## Thank You