Candidate Seat No…….

CHAROTAR UNIVERSITY OF SCIENCE & TECHNOLOGY

Fourth Semester of B. Tech (CE/CSE) Examination May 2022

CE258 Microprocessor and Computer Organization

Date: 04.05.2022, Wednesday **Time: 10.00 a.m. To 01.00 p.m.** **Maximum Marks: 70**

Instructions:

1. The question paper comprises of two sections.
2. Section I and II must be attempted in separate answer sheets.
3. Make and Mention suitable assumptions and draw neat figures wherever required.
4. Use of scientific calculator is allowed.

SECTION – I

Q - 1 Do as Directed. **[09]**

[A] Answer the following questions. [05]

1. Convert given number into octal representation. $(10101110111010010110.10111)_2$.

2. What is the minimum value possible with the Sign Magnitude representation in 6 bits register?

3. Each stage in pipelining should be completed within ____ clock cycle.

4. What is 10's complement of $(489)_{11}$?

5. ADD B is which type of address instruction? where B is the memory location.

[B] Answer the following questions. [04]

1. Which are the major component of the CPU? How they are interconnected?

2. Draw a memory hierarchy.

Q - 2 Answer the following questions. (Attempt Any Three) **[12]**

[A] Consider 1MB cache and 4 GB Main Memory are partitioned into 32KB blocks and word size is 2B. (Note: Consider Memory as word addressable not byte addressable.)
How many bits are required for Physical address and word offset? How many TAG bits are required for Direct mapping and 4-Way Set Associative Mapping?

[B] What is interrupt and subroutine? Differentiate interrupt and subroutine.

[C] Give a function table of 256 × 8 RAM. (Show Memory function and State of the databus)

[D] What is instruction pipeline? Derive the equation for speedup with necessary assumption and solve below example.

A non-pipeline system takes 50ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10 ns. Determine the speedup of the pipeline for 100 tasks over non pipeline.

Q - 3 Answer the following questions.(Attempt Any Two) **[14]**

[A] Draw a Flow chart of Booth Algorithm and perform following Multiplication operation using Booth Algorithm. Show each and every steps in the form of table. $(-27)_{10} \times (18)_{10}$

[B] What is addressing modes? List and explain six addressing modes (which involve any type of register) with example.

[C] What is instruction pipeline conflicts? Explain the solutions of branch difficulties in detail.

SECTION – II

Q - 4 Do as Directed. **[09]**

[A] Answer the following questions. [05]

1. Define Sequential circuit.

2. Perform 1-bit logical shift right operation on 101101110011.

3. What is immediate addressing mode?

4. 80186 microprocessor contains _____ bits address bus.

5. 80386 has the ability to address _____ GB of physical memory.

[B] Answer the following questions. [04]

1. Draw the circuit diagram of full adder.

2. List out the registers available in a basic computer.

Q - 5 Answer the following questions. (Attempt Any Three) **[12]**

[A] Draw a block diagram of a common bus system for transferring data from four registers using multiplexers.

[B] Explain direct and indirect addressing modes with appropriate diagram.

[C] Explain any four functional parts of 80186 microprocessor.

[D] List out the operating modes in 80386 and Explain.

Q - 6 Answer the following questions. (Attempt Any Two) **[14]**

[A] What is three-state buffer? Explain with diagram. Draw a block diagram of common bus system for ‘bit 0’ line using three-state buffers.

[B] Which are the different types of instructions available in a basic computer? Draw the flowchart of determining the type of an instruction.

[C] Draw the architecture of 8086.

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