Candidate Seat no…….

CHAROTAR UNIVERSITY OF SCIENCE & TECHNOLOGY

Third Semester of B. Tech (CE) Examination

Fourth Semester of B. Tech (CE/IT) Examination

May 2016

CE216/CE216.02 Computer Organization and Peripherals

Date: 06.05.2016, Friday **Time: 10.00 am To 01.00 pm** **Maximum Marks: 70**

Instructions:

1) The question paper comprises two sections.
2) Section I and II must be attempted in separate answer sheets.
3) Make suitable assumptions and draw neat figures wherever required.
4) Use of scientific calculator is allowed.

SECTION – I

Q - 1	**Answer the question below. (A to E)**	**[11]**
A	What is instruction Cycle?	[1]
B	What is mnemonics in assembly language?	[1]
C	What is Selective Clear? Take 1010 Value for your explanation.	[1]
D	What is use of control function in Register Transfer language?	[1]
E	In which addressing mode, the operand is implicitly part of instruction.	[1]
	State True OR False. (F to K)	
F	Tristate buffer is used to implement Common bus system.	[1]
G	Hardware interlock is a straightforward method to solve processor dependency in Instruction pipeline.	[1]
H	Operand Fetch is one of the phases of Instruction Execution.	[1]
I	In micrpprogram control, the control logic is implemented with gates, flip-flops, decoders and other digital Circuits.	[1]
J	Microprocessor understands Higher Level language only.	[1]
K	N X 1 Encoder has 1 input lines and N output lines.	[1]

Q – 2.A What are the different types of Instruction Format? **[04]**

OR

Q – 2.A Draw Common Bus System diagram of 4-bit, 4 Registers. Explain the function of Selection lines to transfer data from Registers to Common Bus. **[04]**

Q – 2.B **Answer any TWO questions.** **[08]**

(i) What are the addressing modes used in Basic Computer?

(ii) What is RISC? What are the characteristics of CPU which is based on RISC?

(iii) Design Circuit for logic Micro Operations.

(iv) Provide the significance of following registers in CPU.
PC, AR, DR, IR, INPR, OUTR, AC, TR

Q - 3	**Answer any TWO.**	**[12]**
A	By taking suitable example, explain Direct Address and Indirect Address.	
B	Write and Explain: memory reference instructions.	
C	Design Circuit for Arithmetic Micro Operations.	
D	What are the Machine Language, Assembly Language and higher Level Language?	

SECTION – II

Q - 4 **Answer the question below. (A to E)** **[11]**

A Explain use of Decoder in Processor functionality. [1]

B What is Hexadecimal Representation of $(10)_{10.}$ [1]

C How does Branch and Save Return Address facilitate subroutine or function call? [1]

D Which of the following binary pattern is 2's complement of 1101. [1]

a) 1001 b) 1000 c) 1101 d) 1100

E What will be the value if $(1011001110001111001 0)_2$ is converted to base 16? [1]

State True OR False. (F to K)

F Computer uses 2's complement for Multiplication. [1]

G A "word" is the natural unit of organization of memory. Different computer types may have different word lengths (in bits). [1]

H Current Computers are also known as SISD. [1]

I Physical address is generated by user. [1]

J ROM consists of DRAM. [1]

K Multicore means more than one ALU on single processor die. [1]

Q – 5.A Instruction pipelining is a technique that implements a form of parallelism called instruction-level parallelism within a single processor. How does it increase throughput of CPU? **[04]**

OR

Q – 5.A Draw diagram of register based microprocessor. Explain how the addition operation is performed? **[04]**

Q – 5.B **Answer any TWO.** **[08]**

(i) Convert the following arithmetic expression to postfix notation
(1) A+B/C
(2) A*B*(C+(D/F))
(3) A+B*C/(G*H)/K
(4) A *(C +D *D)/F

(ii) Write a short description of Vector Processors.

(iii) Differentiate between CISC and RISC architecture.

Q – 6. **Answer any TWO.** **[12]**

A Write a short note on: Array Processors

B Draw and explain: Flow chart of Addition & Subtraction algorithm.

C Explain in short with respect to cache memory mapping techniques.
Direct Mapping,
Associative Mapping,
Set-associative Mapping.

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