Exam Date & Time: 28-May-2021 (10:00 AM - 01:45 PM)

CHAROTAR UNIVERSITY OF SCIENCE AND TECHNOLOGY

MICROPROCESSOR AND COMPUTER ORGANIZATION [CE258]

Marks: 70 **Duration: 225 mins.**

Section-1

Answer all the questions.

These are MCQ-type questions. All questions are compulsory

1 If $(XY)_Z = (51)_8$ and X, Y and Z are threeconsecutive numbers then What are the possible values of X , Y andZ? (1)

1) 1, 2, 3 2) 6, 4, 5 3) 8, 9, 10 4) 5, 6, 7

2 What is 10's complement of $(299)_{11}$ (1)

1) 701 2) 811 3) 922 4) 700

3 What will be the value if $(1001001110001110010)_2$ isconverted to base 32? (Note: Use digit 1 to 31) (1)

1) 9 3 8 15 2 2) 2 2 3 4 3 6 2 3) 18 7 14 18 4) 18 14 7 18

4 What is the minimum value possible with the Sign Magnituderepresentation in 6 bits register. (1)

1) -31 2) -32 3) -63 4) -64

5 Which of the following binary pattern is having identical values in2's complement and sign magnitude? (1)

1) 1001 2) 1000 3) 1101 4) 1100

6 The overflow in addition of 4 bits($C_3C_2C_1C_0$) number canbe detected by applying addition of (1)

1) C_0 and C_1 2) C_3 and C_2 3) C_4 and C_3 4) Only C_4

7 Which number is not possible in base 6 number system? (1)

1) 101001 2) 4534645 3) 324334 4) 12345

8 A non pipeline system takes 50ns to process a task. The same taskcan be processed in a six-segment pipeline with a clock cycle of 10ns. Determine the speedup of the pipeline for 100 tasks over nonpipeline. (1)

1) 4.9 2) 4.76 3) 3.90 4) 5.0

9 Each stage in pipelining should be completed within ____ cycle. (1)

1) 1 2) 2 3) 3 4) 4

10 Determine the Number of clock cycles that it takes to process 200tasks in a six-segment pipeline (1)

1) 205 2) 208 3) 206 4) 200

11 Which conflicts below code will generate?

LOAD R1

LOAD R2

ADD R3 R1 R2

STORE R3 (1)

1)	Data conflicts		2)	Branch conflicts		3)	No Conflicts		4)	Resource conflicts					

12 In which category of flyn's classification, all processor receivesthe same instruction from the control unit but operate on differentdata? (1)

1)	SISD		2)	SIMD		3)	MISD		4)	MIMD					

13 Which Pipeline conflicts arise due to the instruction which changesthe value of Program Counter?

1: Resource Conflicts

2: Branch Difficulties

3: Data Dependency (1)

1)	Only 1		2)	Only 2		3)	Both 2 & 3		4)	Only 3					

14 If you have a register stack of 64 words, Address 0 to 63. Initialvalue of SP=0.

The operations of Push are:

SP < --SP+1

(2) M[SP]=DR

(3)_____

(4)EMTY< --0. (1)

What will be the third operation?

1)	IF(SP=63) then (FULL < --0)		2)	IF(SP=63) then (FULL < --1)		3)	IF(SP=0) then (FULL < --0)		4)	IF(SP=0) then (FULL < --1)					

15 Which instruction set is belonging to Single Accumulator CPUOrganization? (1)

1)	Three Address Instruction		2)	Two Address Instruction		3)	One Address Instruction		4)	Zero Address Instruction					

16 Which is correct Assembly program to perform following operation?S= (D + E) * F (1)

1)	PUSH E, PUSH D, PUSH F, ADD, MUL, POP S		2)	PUSH D, PUSH E, ADD, PUSH F, MUL, POP S		3)	PUSH E, PUSH D, ADD, PUSH F, MUL, POP S		4)	PUSH D, PUSH E, ADD, PUSH F, MUL					

17 The addressing mode used in an instruction of the form ADD al[1234X], is _____. (1)

1)	Absolute		2)	Direct		3)	Indirect		4)	Indexed					

18 What will be the value of x if AND operation between 101x1 and mask00010 set the Z status bit? (1)

1)	0		2)	1		3)	Can't determine from Z only								

19 Consider 1MB cache and 4 GB Main Memory are partitioned into 32KBblocks and word size is 2B. (Note: Consider Memory as wordaddressable not byte addressable.) How many TAG bits are requiredfor 4-Way Set Associative Mapping? (1)

1)	20		2)	12		3)	13		4)	14					

20 Consider 1MB cache and 4 GB Main Memory are partitioned into 32KBblocks and word size is 2B. (Note: Consider Memory as wordaddressable not byte addressable.) How many bits are required forPhysical address? (1)

1)	32		2)	31		3)	30		4)	28					

21 Consider 1MB cache and 4 GB Main Memory are partitioned into 32KBblocks and word size is 2B. (Note: Consider Memory as wordaddressable not byte addressable.) How many bits are required forword offset? (1)

1)	12	2)	13	3)	14	4)	15

22 Which memory is efficient to store temporary data while performingarithmetic operation? (1)

1)	Register	2)	Cache memory	3)	Main Memory	4)	Auxiliary Memory

23 What is the Average memory access time with cache if cache memoryaccess time is 10 micro second and main memory access time is 10milli second. The hit ratio is 10%. (1)

1)	9.009 milli second	2)	0.901 milli second	3)	9.001 milli second	4)	9.01 milli second

24 Which flip-flop does store (give output) 0 and 1 with reference tofirst bit of input pin value? (1)

1)	JK Flip flop only	2)	SR Flip flop only	3)	T Flip flop only	4)	JK & SR Flip flop

25 _____ is included in combinational circuit then it isclassified as sequential circuit. (1)

1)	Multiplexer	2)	Flip flop	3)	Decoder	4)	Adder

26 The internal hardware organization of digital computer is bestdefined by (1)

1)	The set of registers it contains and their functions	2)	The sequence of microoperations performed on the binary information stored in the registers	3)	The control lines that initiate the sequence of microoperations	4)	All of the above

27 Which one is not a flag in basic computer design? (1)

1)	FGI	2)	FGO	3)	IEN	4)	INT

28 Instruction Fetch stands for _____ (1)

1)	Transfer of instruction from keyboard	2)	Transfer of instruction from memory to IR	3)	Transfer of instructions to display	4)	Transfer of instruction from IR to Memory

29 With respect to basic computer, in memory read operation, addresswill be transferred to _____register before sending to memory. (1)

1)	PC	2)	MAR	3)	DR	4)	ALU

30 Binary incrementor circuit can be created using Full adder (1)

1)	TRUE	2)	FALSE

31 To implement common bus system using multiplexer for 4 registerseach of length 8 bit, we need _____number of multiplexer and_____ dimension of each multiplexer (1)

1)	8 multiplexer, 8 X 1	2)	8 multiplexer, 4 X 1	3)	4 multiplexer, 8 X 1	4)	4 multiplexer, 4 X 1

32 With respect to basic computer, which Instruction having a correctsyntax? (1)

1)	AC< -AC+TR	2)	IR< -M[PC]	3)	DR< -DR+AC	4)	DR< -M[AR]

33 Which one of the following is memory Read operation? (1)

1)	M[AR]< -- AC	2)	DR< --M[AR]	3)	AC< --DR	4)	M[TR]< --AC

34 Two of the states of three state buffer are logic 1 and 0. What isthird state (1)

1)	Close Circuit State		2)	High-Impedance		3)	Cross Circuit State		4)	Normal Impedance	

35 When an instruction itself contains the operand (data) rather thanthe address of the operand, the technique is known as _____addressing. (1)

1)	Direct		2)	Indirect		3)	Immediate		4)	Memory	

36 What is the meaning of following statement:T0'T1'T2'(IEN)(FGI+FGO): R< --1

1)	R will be set to 1, if T0,T1 are 1 and T2,IEN,FGI,FGO are 0		2)	R will be set to 1, if T0,T1,T2 are 0 and IEN,either FGI or FGO are 1		3)	R will be set to 1, if T0,T1,T2 are 1 and IEN,either FGI or FGO are 0		4)	R will be set to 1, if T0,T1 are 0 and T2,IEN,FGI,FGO are 1	

(1)

37 If data stored in AC=5FH and DR=C2H what is value of AC after AC^DRoperation? (1)

1)	9D		2)	42		3)	DF		4)	DE	

38 Which one of the following is 32-bit microprocessor (1)

1)	8085		2)	8086		3)	80286		4)	Intel Core i3	

39 Which one of the following have Bus Interface Unit and Executionunit only? (1)

1)	8085		2)	8086		3)	80286		4)	80386	

40 80286 processor operates in two different modes, which are knownas_____

1)	Real memory mode, and protected RAM mode		2)	Real address mode and protected virtual address mode		3)	Virtual address mode and protected Real address mode		4)	Real RAM mode and protected virtual address mode	

(1)

41 In _____ address mode, value of segment address is shiftedleft side 4 times and added with offset address to generatephysical address. (1)

1)	Real RAM mode		2)	Real address mode		3)	Protected virtual address mode		4)	Protected Real address mode	

42 In 80286,_____ unit is responsible to pre-fetchinstruction byte. (1)

1)	Execution Unit		2)	Bus Interface Unit		3)	Address Unit		4)	Instruction Unit	

43 Purpose of separate instruction cache and data cache is_____

1)	To increase more efficient access to the caches by accessing data and instruction simultaneously		2)	To reduce data transfer		3)	To speedup execution		4)	To increase I/O	

(1)

44 In 80386, during _____ translation , logical address istranslated/mapped into linear address (1)

1)	Segment		2)	Page		3)	Address		4)	Both Segment and Page	

45 Descriptors are created by _____ not byapplications programme. (1)

1)	Compilers		2)	Loaders		3)	Linkers		4)	All of the above	

46 Granularity bit: Specifies the units with which the LIMIT field isinterpreted. When the bit is zero, the limit is interpreted inunits of one byte; when value is 1, the limit is interpreted inunits of 4 Kilobytes. (1)

1)	False		2)	True	

47 The segment translation and page-translation steps are mandatory in80386. (1)

1)	True		2)	False			

48 _____ technology is equivalent to 3d Transistors (1)

1)	Feen Fat		2)	Fin Fet		3)	Thin Fet		4)	Thick Fat	

49 Which technology of intel supports connecting co-processor throughport (1)

1)	Turbo boost		2)	Thunder bolt		3)	Hyper Threading		4)	Virtualization	

50 AMD uses 16-way set associative memory in L1cache memory. (1)

1)	True		2)	False	

Section-2

Answer 4 out of 6 questions.

These are descriptive-type questions. Write your answer on blank paper and upload the answers.

1 Perform following Multiplication operation using Booth Algorithm.Show each and every steps in the form of table. $(-42)_{10} \times (13)_{10}$ (Note: Flow chart is not required forevaluation) (5)

2 Suppose you require total 256 Bytes of RAM and 512 Bytes of ROM.The available RAM and ROM configurations are 128 × 8 and 512 × 8respectively. How many RAMs and ROMs are required? Also show theCPU and Memory connection with neat diagram. (5)

3 Evaluate and write the instructions to perform the arithmeticstatement Z = P * (Q - R) using Zero, One, Two, Three type addressInstructions. Also give the instruction set for RISC processor.Operands are in memory address P, Q and R. Use registers R1 to R5and temporary memory location T whenever required. (5)

4 Design and explain the combinational circuit for four-bitarithmetic circuit. (5)

5 Draw a circuit diagram which shows Gate structure for controllingthe LD, INR and CLR pins of PC Register. Instruction detail isattached herewith. (5)

6 By Taking suitable diagram, explain logical address to physicaladdress mapping in 80386 including segmentation and paging. (5)

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