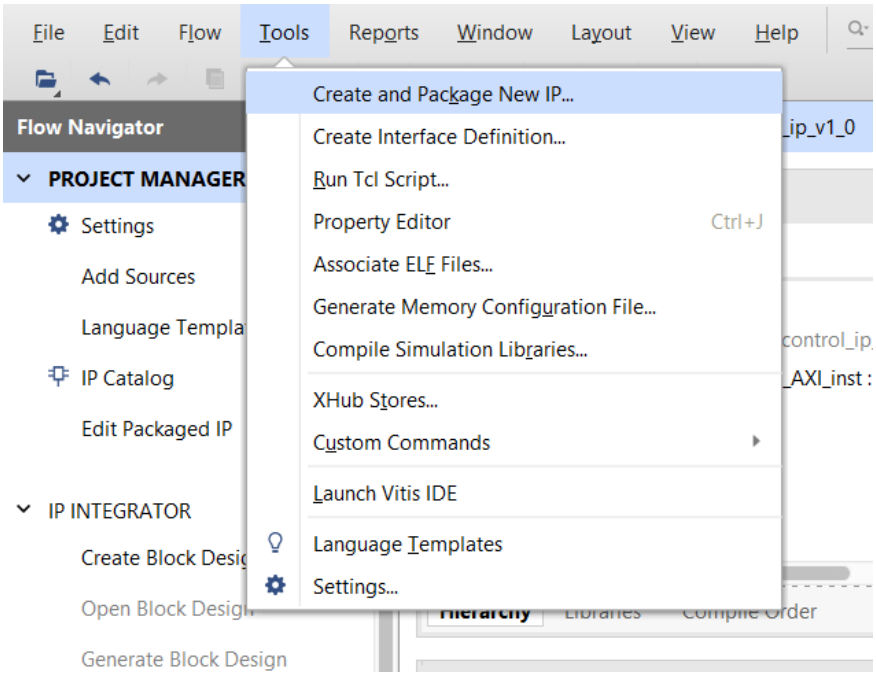
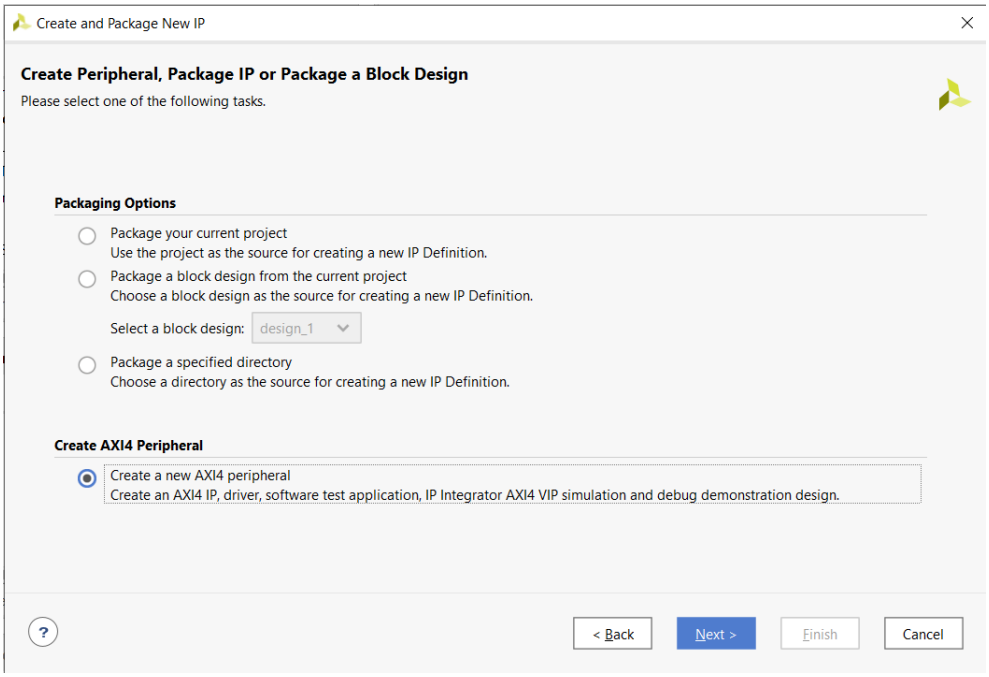
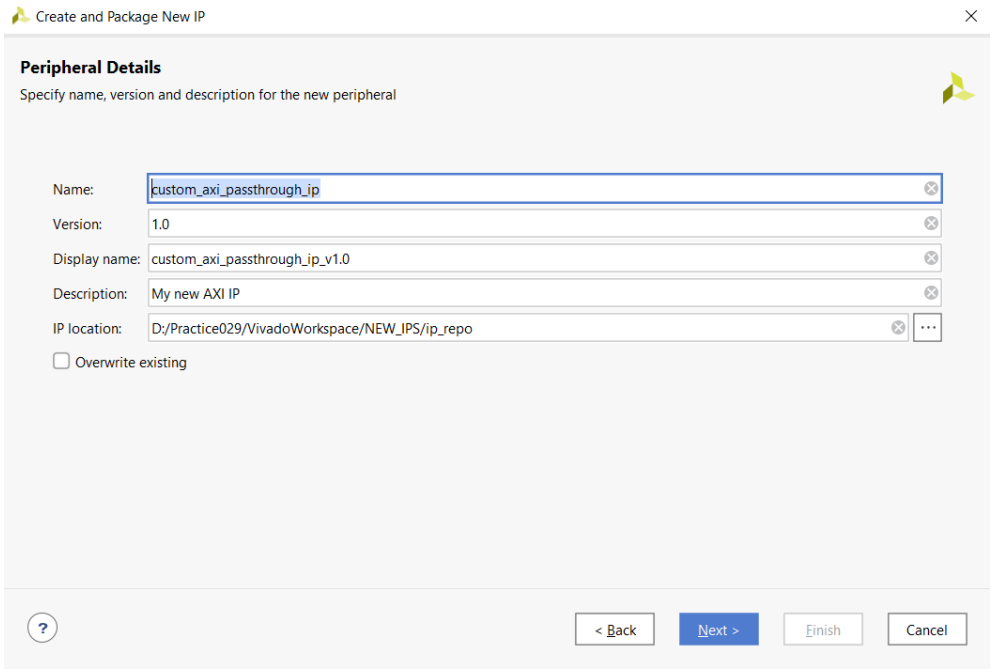
==INSTALLATION PROCEDURE==

1. Create a new IP:

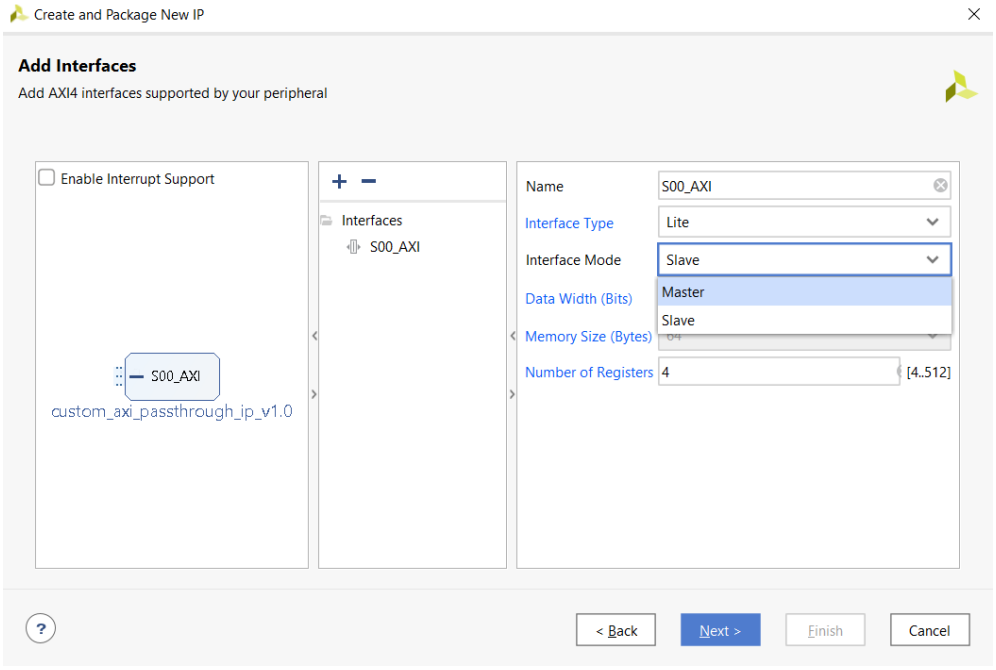




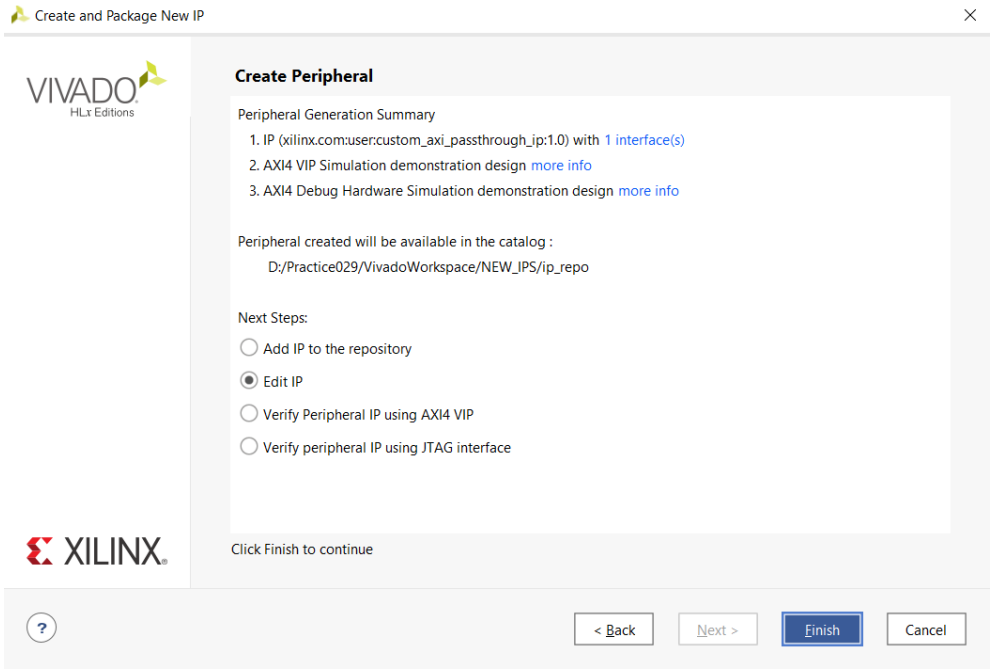
- It must be an AXI4 peripheral.



- It must be named «custom_axi_passthrough_ip» specifically.

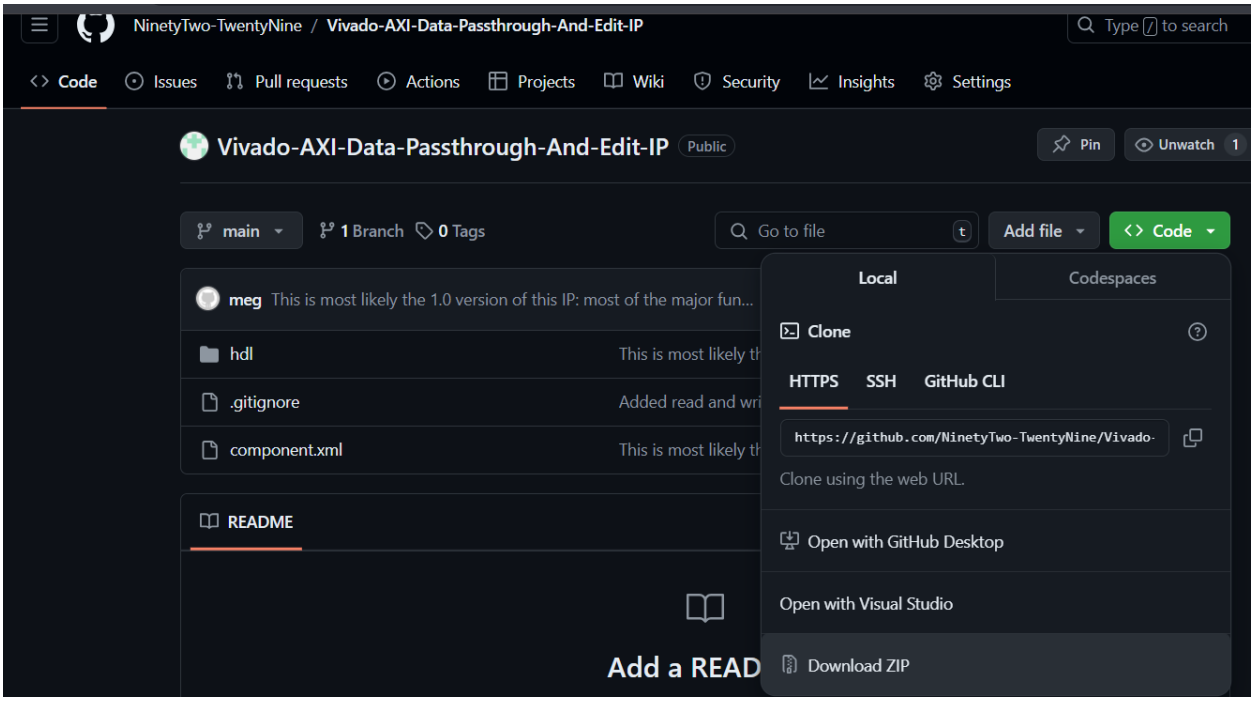


- Switch the default slave AXI interface to master and click «Next».

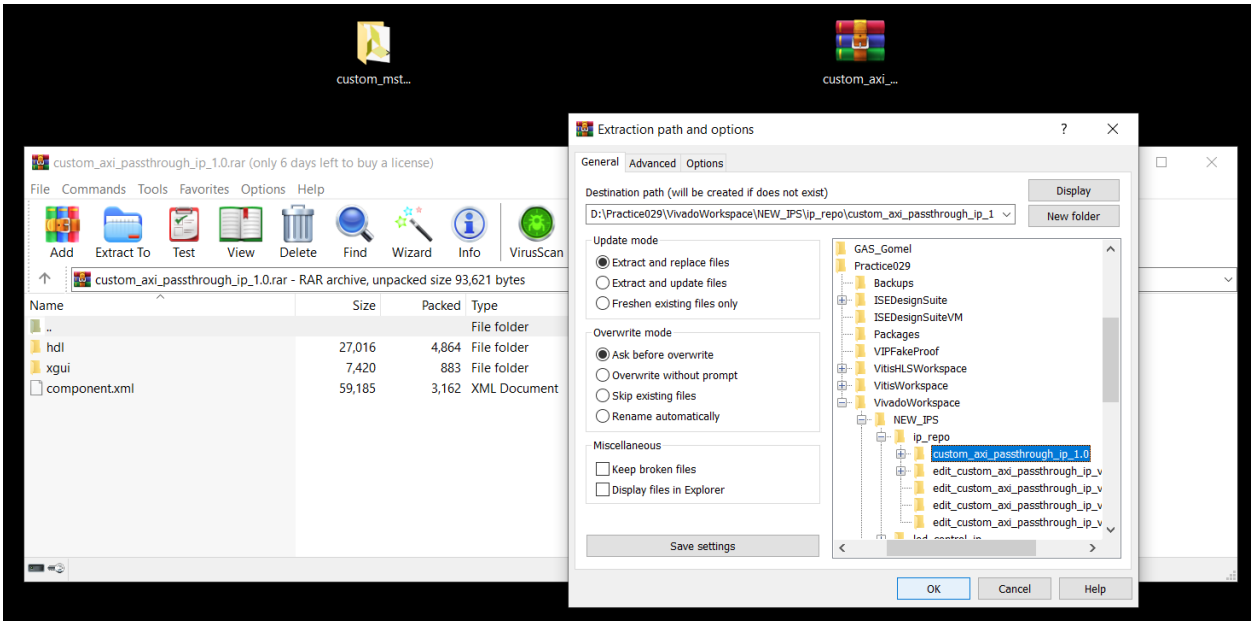


- Choose «Edit IP», click «Finish». After the project window opens, close it.

2. Download the entire project:

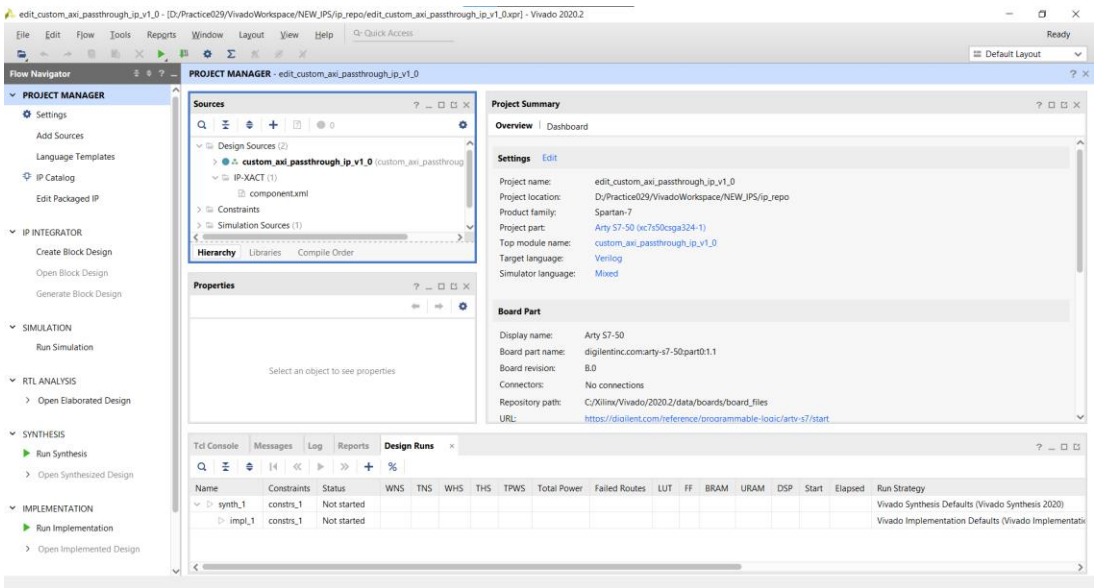


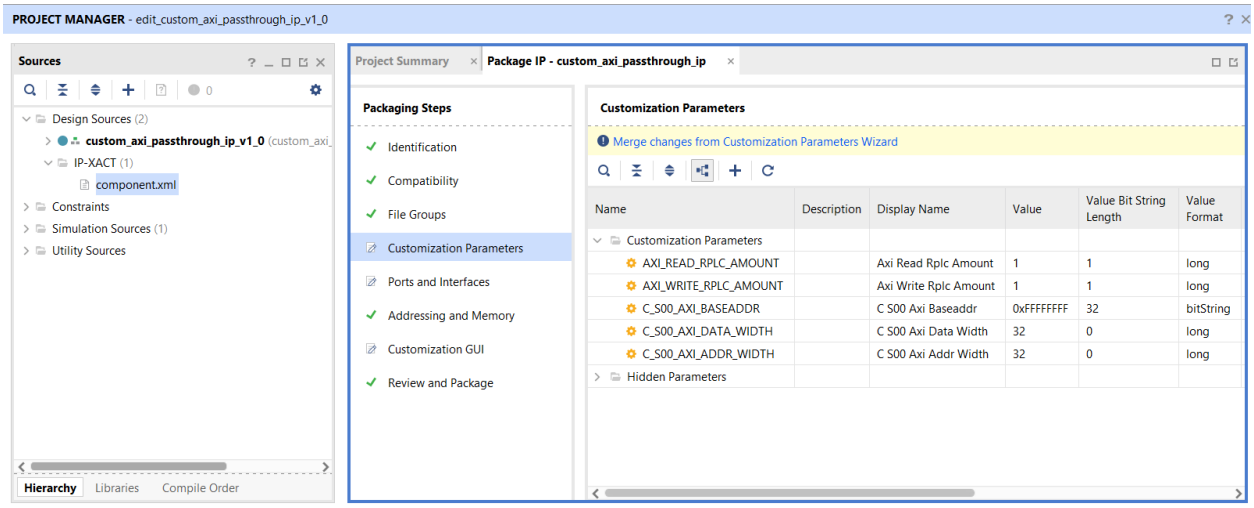
3. Extract the files into the main IP folder:



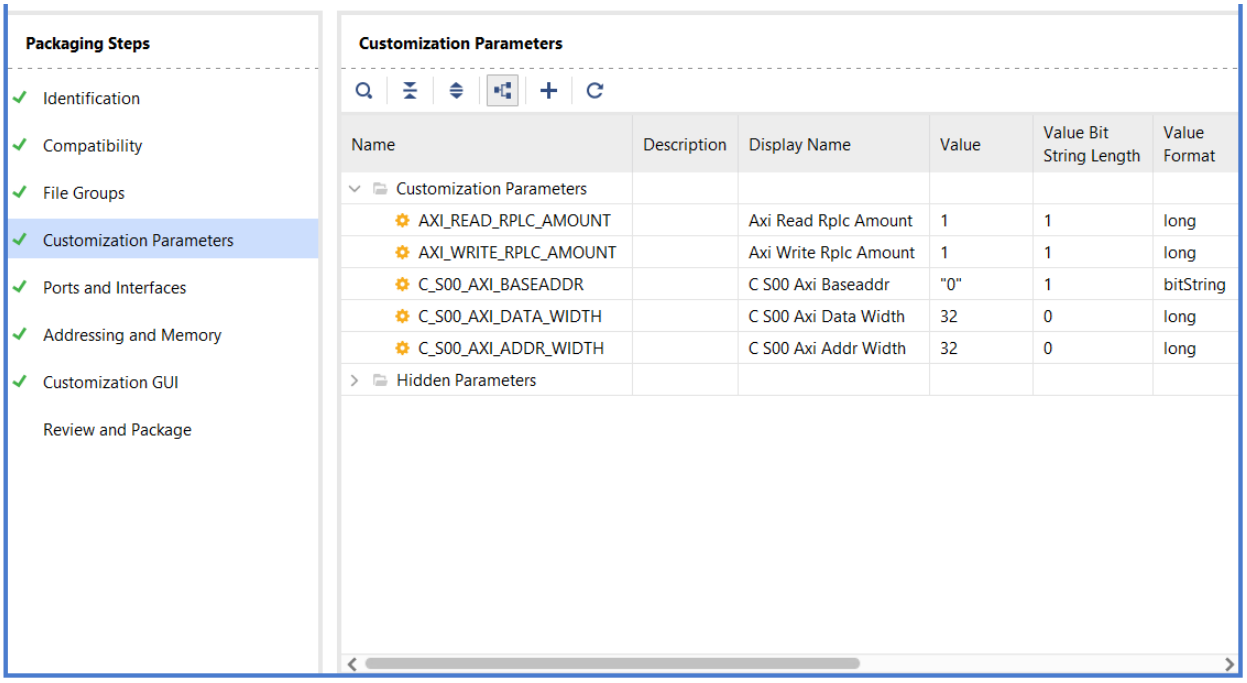
- If everything was done properly, then 4 files in the IP folder should get replaced (unless the IP project's HDL language is VHDL).
- In case the language is set to VDHL and not Verilog: delete the automatically created VHDL files and select the Verilog versions of those files as the main HDL code (can be done in the IP project itself).

4. Open the IP project again and set it up:

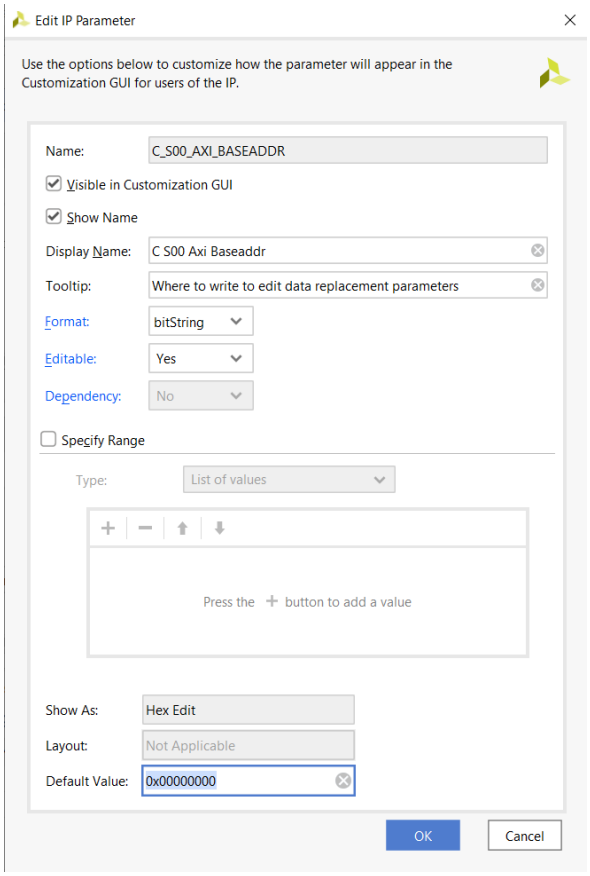




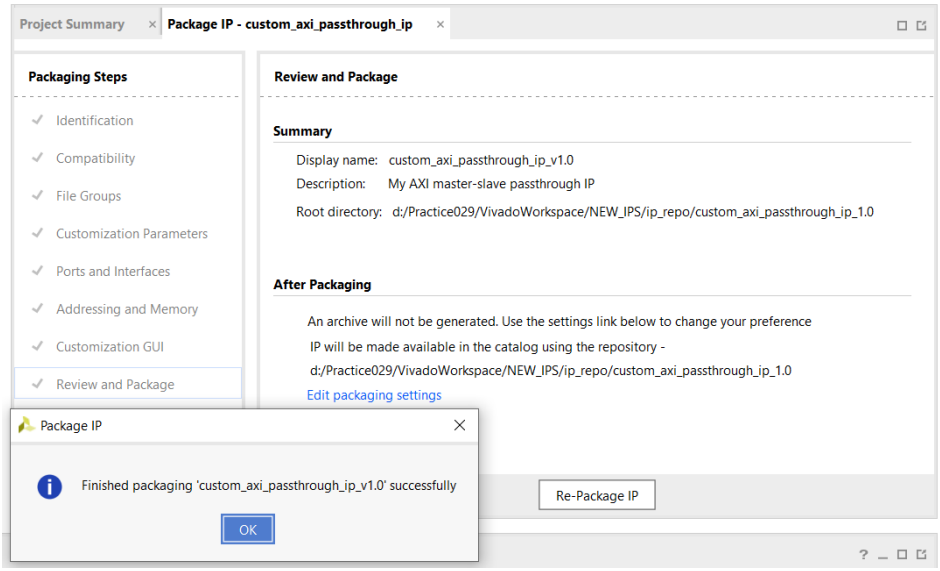
- Set these 5 parameters («C_S00_AXI_ADDR_WIDTH» could be left out) as UI-visible if they weren't already automatically set as visible.



- After pressing the «Merge changes» button, the width and default value of the «C_S00_AXI_BASEADDR» parameter might get reset. It has to be fixed manually.

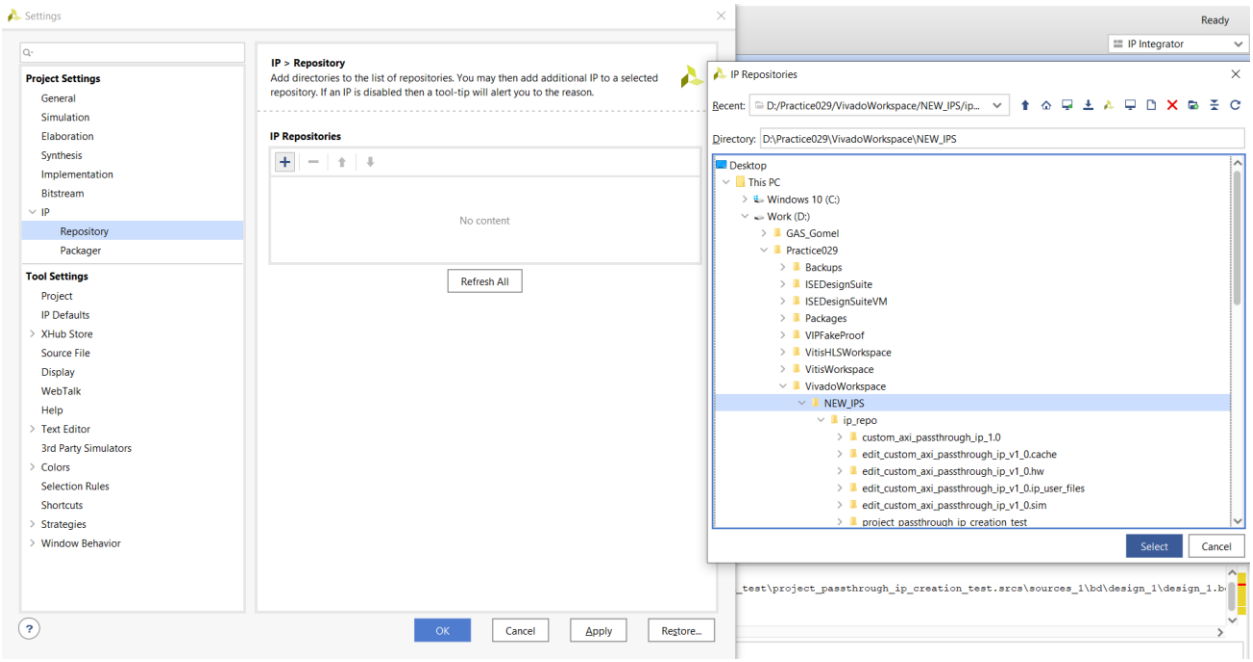


- Set the default value of this parameter to «0xFFFFFFFF» (or anything else of 32-bit width) and click «OK».



- Repackage the IP.

5. Include necessary directories (with the IP) in any of your projects:



6. The IP can now be used in that project: