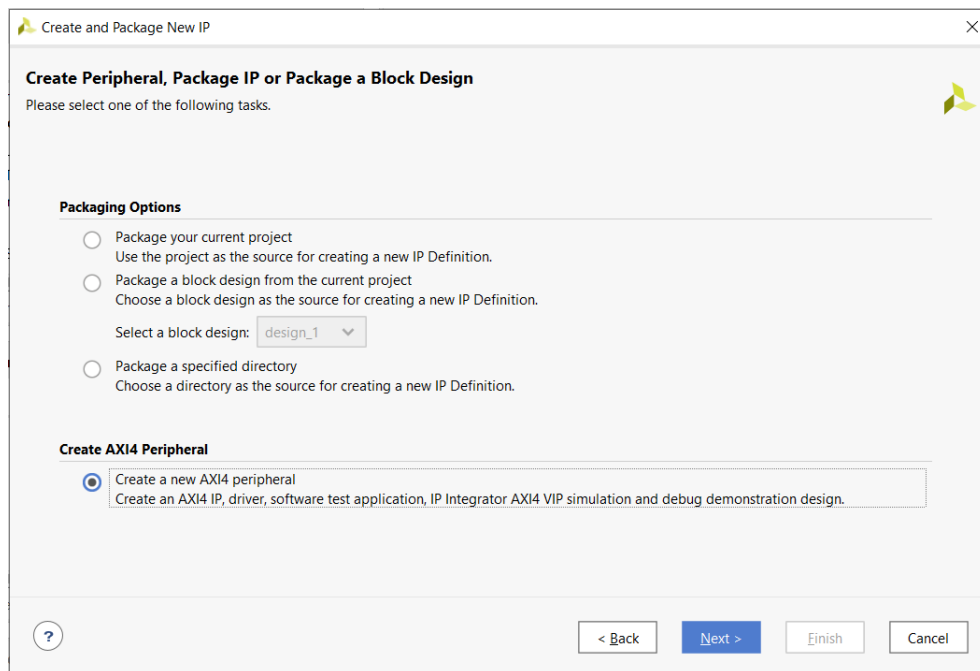
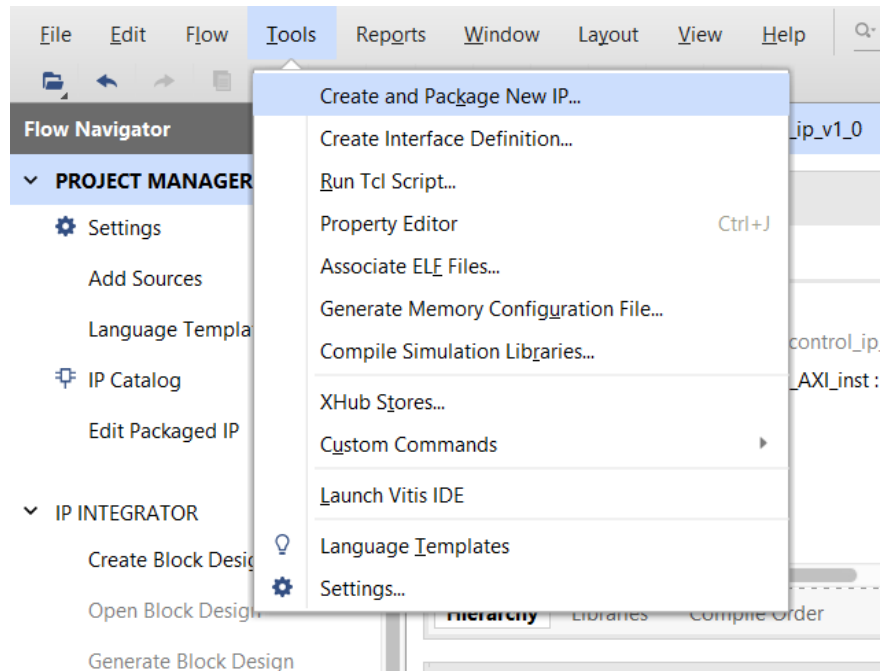


==INSTALLATION PROCEDURE==

1. Create a new IP:



- It must be an AXI4 peripheral.

Create and Package New IP

Peripheral Details

Specify name, version and description for the new peripheral

Name:

Version:

Display name:

Description:

IP location:

☐ Overwrite existing

< Back Next > Finish Cancel

- It must be named «custom_axi_passthrough_2bus_input» specifically.

Create and Package New IP

Add Interfaces

Add AXI4 interfaces supported by your peripheral

☐ Enable Interrupt Support

Interfaces

- S00_AXI

custom_axi_passthrough_2bus_input_v1.0

Name:

Interface Type:

Interface Mode:

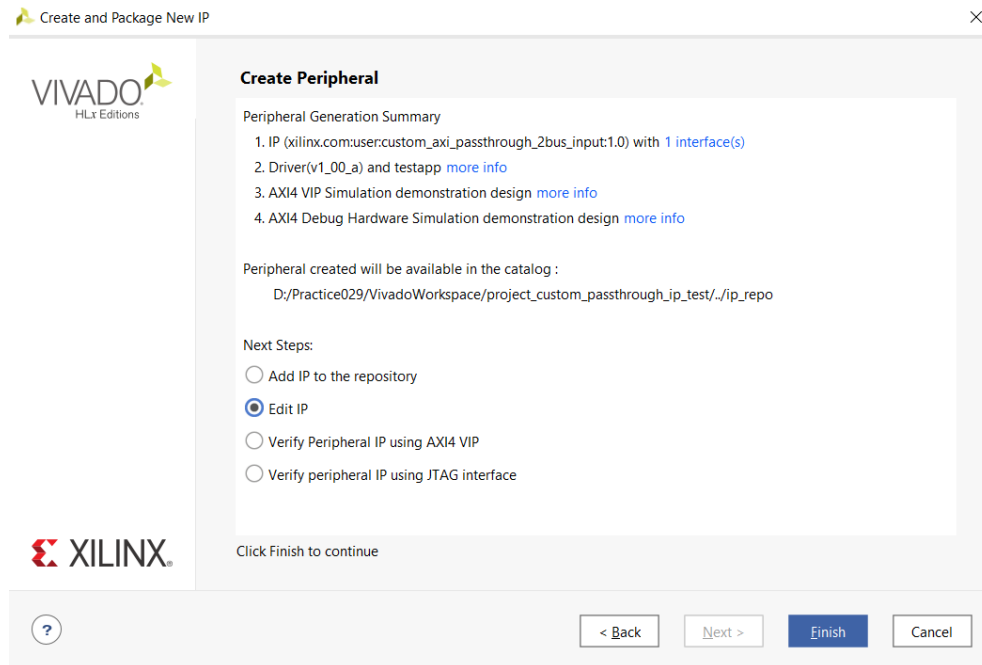
Data Width (Bits):

Memory Size (Bytes):

Number of Registers: [4..512]

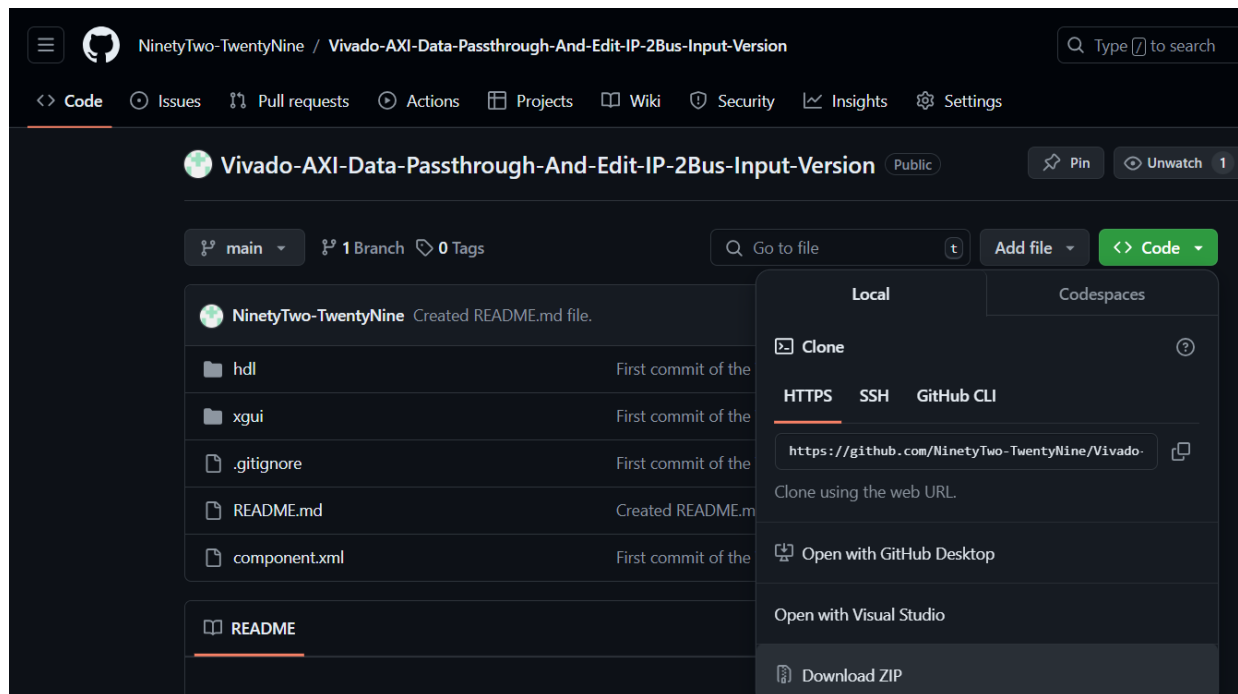
< Back Next > Finish Cancel

- Switch the default slave AXI interface to master and click «Next».

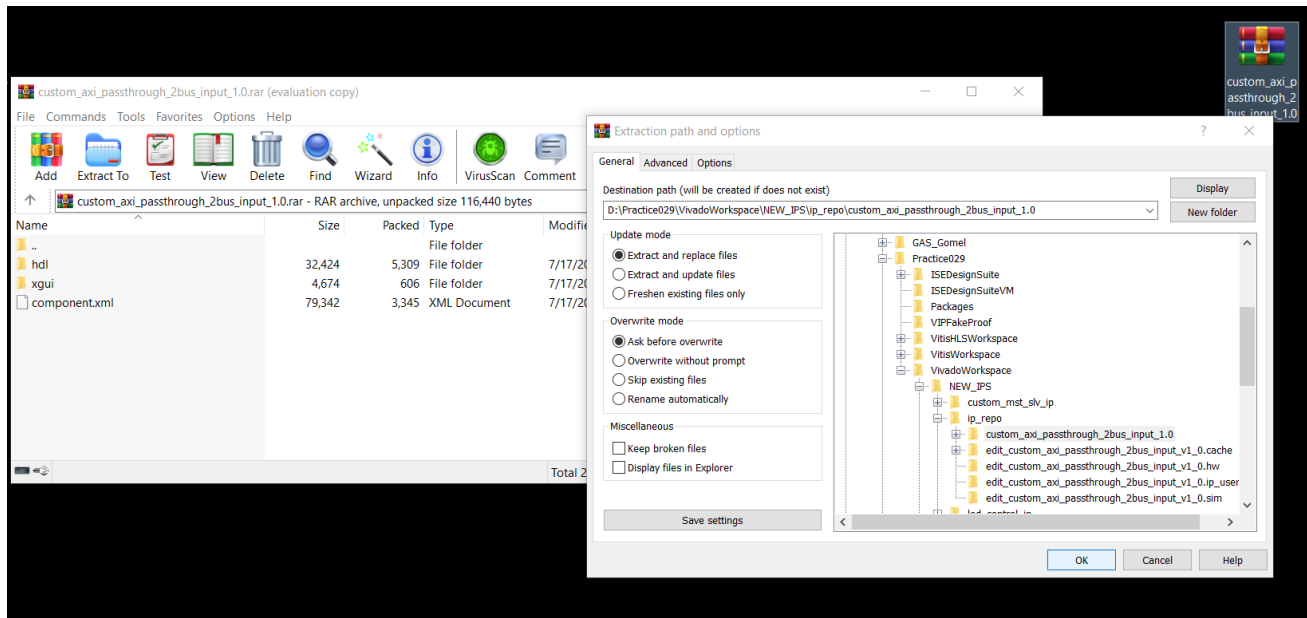


- Choose «Edit IP», click «Finish». After the project window opens, close it.

2. Download the entire project:

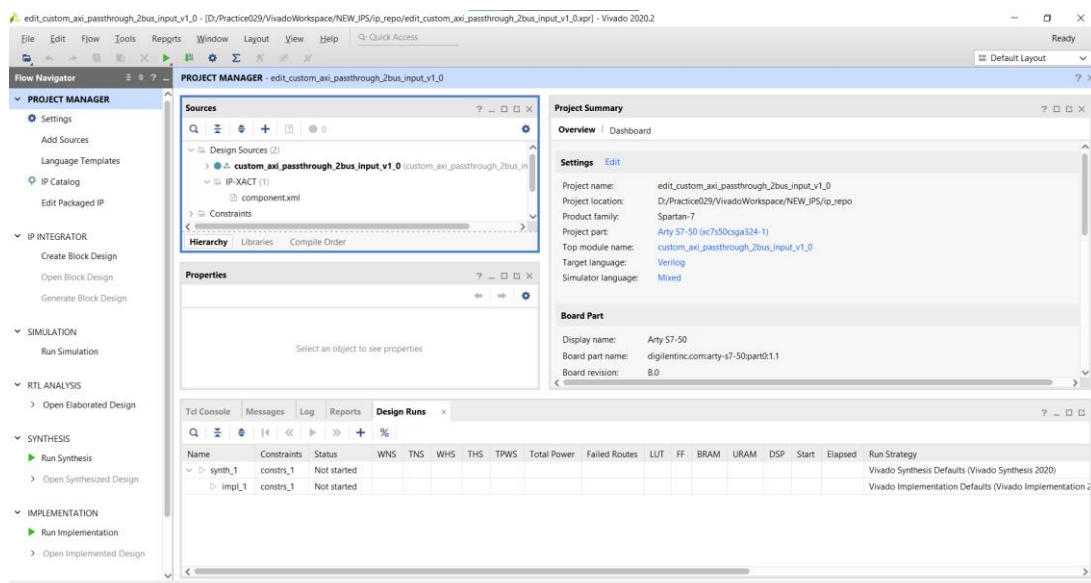


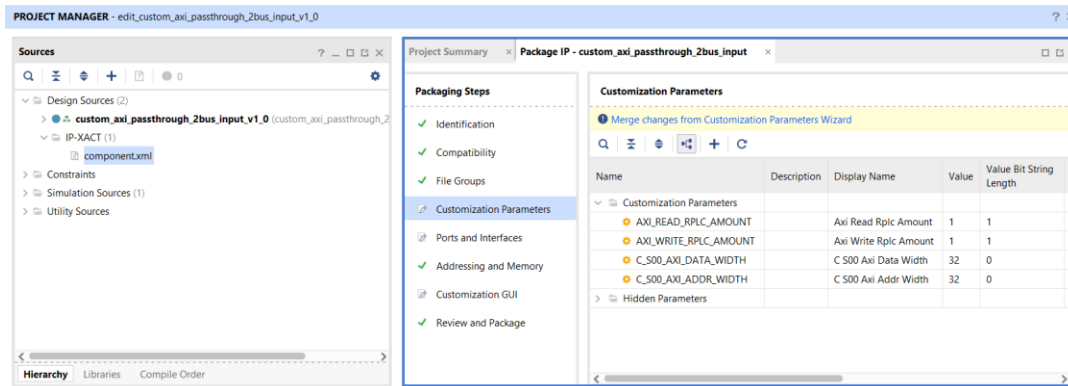
3. Extract the files into the main IP folder:



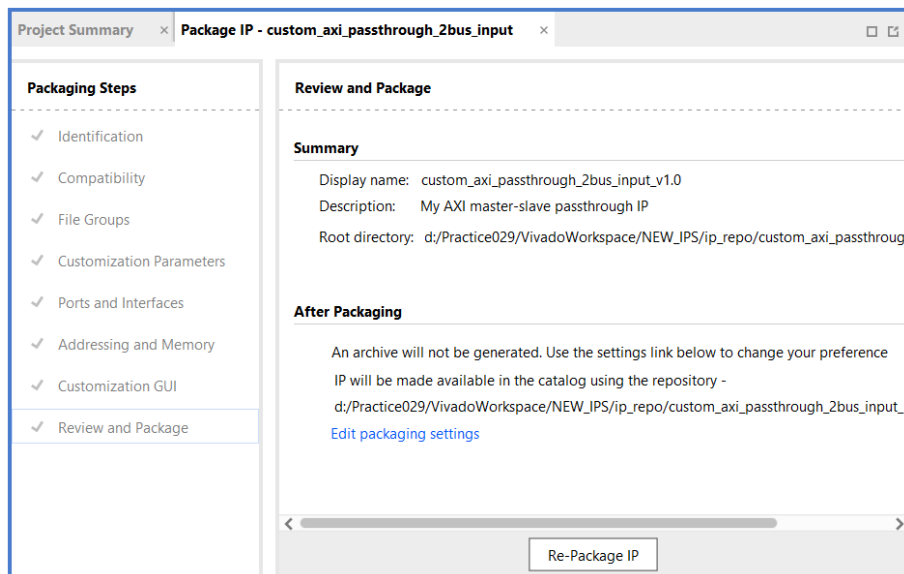
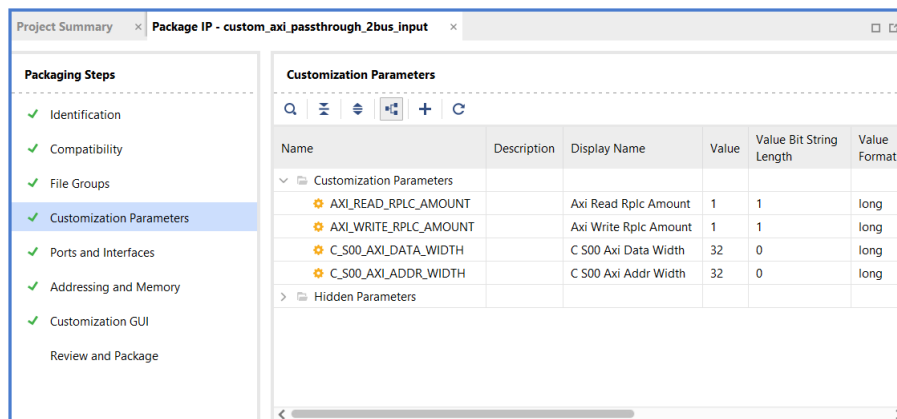
- If everything was done properly, then 4 files in the IP folder should get replaced (unless the IP project's HDL language is VHDL).
- In case the language is set to VHDL and not Verilog: delete the automatically created VHDL files and select the Verilog versions of those files as the main HDL code (can be done in the IP project itself).

4. Open the IP project again and set it up:



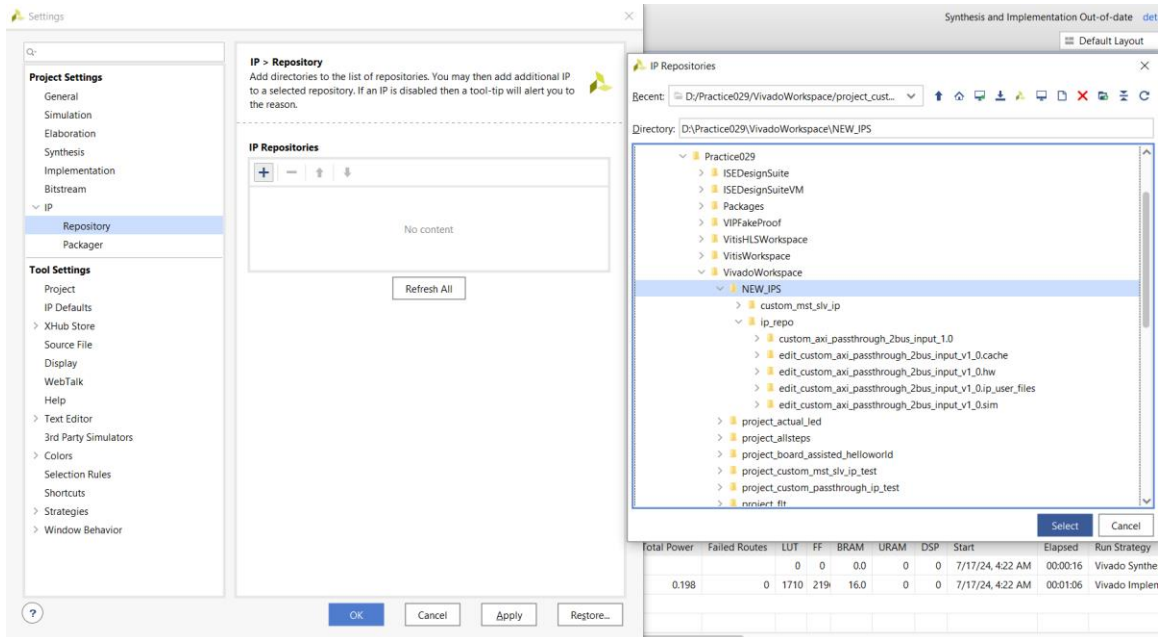


- Set these 4 parameters («C_S00_AXI_ADDR_WIDTH» could be left out) as UI-visible if they weren't already automatically set as visible.



- Repackage the IP.

5. Include necessary directories (with the IP) in any of your projects:



6. The IP can now be used in that project:

