具有集成电流检测、1/256 微步进和失速检测功能的 DRV8889-Q1 汽车步进驱动器

1 特性

- 符合汽车应用 要求
- 具有符合 AEC-Q100 标准的下列结果：
  - 器件温度 1 级：-40°C 至 125°C 的环境运行温度范围
  - 器件 HBM ESD 分类等级 3A
  - 器件 CDM ESD 分类等级 C4B
- 脉宽调制 (PWM) 微步进电机驱动器
  - 最大 1/256 微步进
- 集成式电流检测功能
  - 无需使用检测电阻器
- 智能调优衰减技术、固定缓慢和混合衰减选项
- 4.5V 至 45V 的工作电源电压范围
- 低 $R_{DS(ON)}$：900mΩ HS + LS（在 13.5V 和 25°C 条件下）
- 每个桥都具有高电流容量
  - 2.5A 峰值、1.5A 满量程、1.1A rms
- 可配置的关断时间 PWM 斩波
  - 7μs、16μs、24μs 或 32μs。
- 简单的 STEP/DIR 接口
- 支持菊花链的 SPI
- 低电流睡眠模式 (2μA)
- 扩频时钟和输出压摆率控制可最大限度降低 EMI
- 小型封装和外形尺寸
- 保护 功能
  - VM 欠压锁定 (UVLO)
  - 电荷泵欠压 (CPUV)
  - 过流保护 (OCP)
  - 失速检测
  - 开路负载检测
  - 过热警告 (OTW)
  - 欠热警告 (UTW)
  - 热关断 (OTSD)
  - 故障条件指示引脚 (nFAULT)

2 应用

- 汽车双极步进电机
- 前照灯位置调节
- 抬头显示 (HUD)
- HVAC 步进电机
- 电子燃油喷射 (EFI)

3 说明

DRV8889-Q1 是一款适用于汽车 应用的步进电机驱动器。该器件与两个 N 沟道功率金属氧化物半导体场效应晶体管 (MOSFET) H 桥驱动器、一个微步进分度器以及集成电流检测功能完全集成。DRV8889-Q1 能够驱动高达 1.5A 的满量程电流或 1.1A rms 输出电流（电压为 13.5V 且 T_A = 25°C，取决于 PCB 设计）。

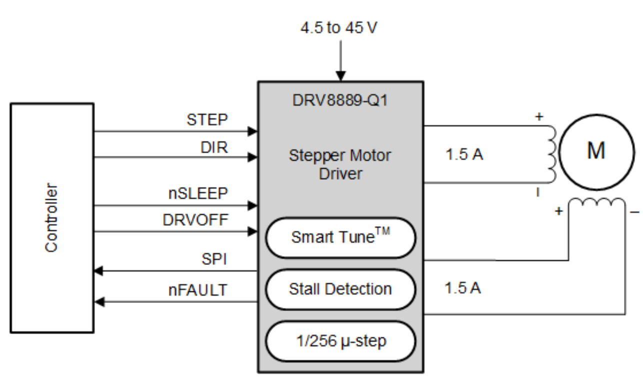
DRV8889-Q1 采用内部电流检测架构，无需使用两个外部功率检测电阻器，因此减小了 PCB 面积并降低了系统成本。DRV8889-Q1 使用能够在智能调优、缓慢和混合衰减选项之间进行选择的内部 PWM 电流调节方案。智能调优衰减技术可自动调节，以实现最佳电流调节性能并对电机变化和老化效应进行补偿。扭矩 DAC 功能使控制器无需调节 VREF 电压基准即可调节输出电流。

简易 STEP/DIR 接口允许外部控制器管理步进电机的方向和步进速率。该器件可以配置为不同步进模式，范围涵盖整步至 1/256 微步。凭借专用 nSLEEP 引脚，该器件可提供一种低功耗休眠模式，从而实现超低静态待机电流。该器件 具有 全双工、4 线同步 SPI 通信功能，并允许通过菊花链方式串联最多 63 个器件以实现可配置性和提供详细故障报告。

器件信息[(1)]

器件型号	封装	封装尺寸（标称值）
DRV8889QPWPRQ1	HTSSOP (24)	7.80mm × 4.40mm
DRV8889QRGERQ1	VQFN (24)（可湿性侧面）	4.00mm × 4.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化原理图

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
4 月2019 年	*	初始发行版。

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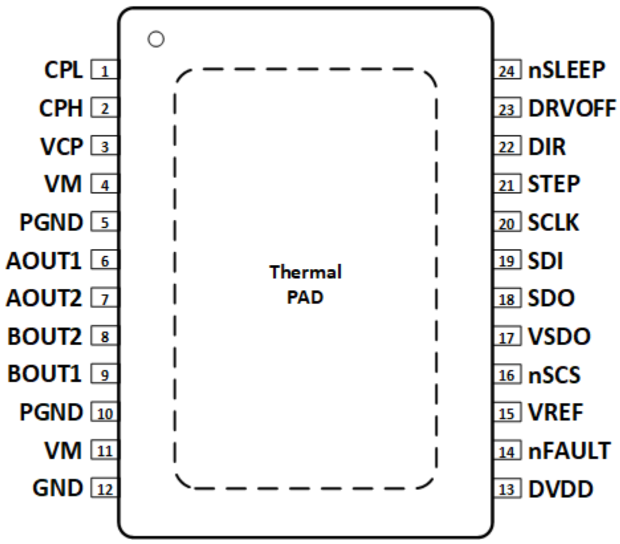
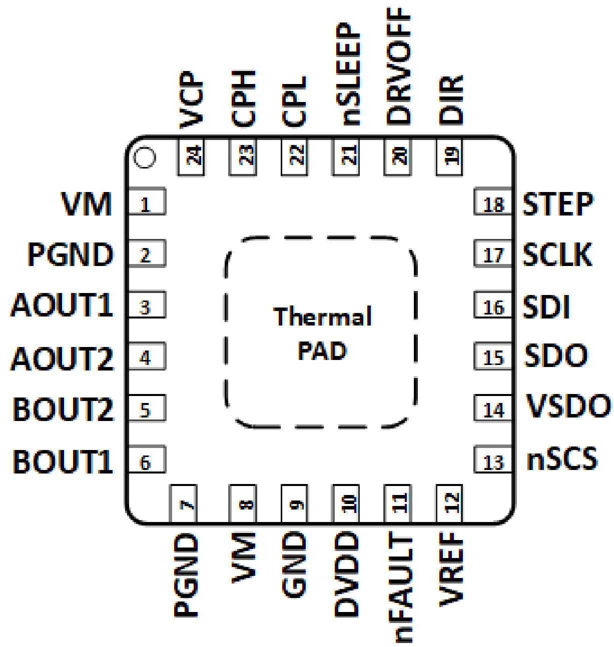
5 Pin Configuration and Functions

PWP PowerPAD™ Package
24-Pin HTSSOP
Top View



RGE Package
24-Pin VQFN With Wettable Flank and Exposed Thermal Pad
Top View



Pin Functions

PIN			I/O	TYPE	DESCRIPTION
NAME	NO.				
	HTSSOP	VQFN			
AOUT1	6	3	O	Output	Winding A output. Connect to stepper motor winding.
AOUT2	7	4	O	Output	Winding A output. Connect to stepper motor winding.
PGND	5, 10	2, 7	—	Power	Power ground. Connect to system ground.
BOUT1	9	6	O	Output	Winding B output. Connect to stepper motor winding
BOUT2	8	5	O	Output	Winding B output. Connect to stepper motor winding
CPH	2	23	—	Power	Charge pump switching node. Connect a X7R, 0.022-µF, VM-rated ceramic capacitor from CPH to CPL.
CPL	1	22			
DIR	22	19	I	Input	Direction input. Logic level sets the direction of stepping; internal pulldown resistor.
DRVOFF	23	20	I	Input	Logic high to disable device outputs; logic low to enable; internal pullup to DVDD.
DVDD	13	10		Power	Logic supply voltage. Connect a X7R, 0.47-µF, 6.3-V or 10-V rated ceramic capacitor to GND.
GND	12	9	—	Power	Device ground. Connect to system ground.
VREF	15	12	I	Input	Current set reference input. Maximum value 3.3 V. DVDD can be used to provide VREF through a resistor divider.
SCLK	20	17	I	Input	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin.
SDI	19	16	I	Input	Serial data input. Data is captured on the falling edge of the SCLK pin
SDO	18	15	O	Push Pull	Serial data output. Data is shifted out on the rising edge of the SCLK pin.
STEP	21	18	I	Input	Step input. A rising edge causes the indexer to advance one step; internal pulldown resistor.

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Pin Functions (continued)

PIN			I/O	TYPE	DESCRIPTION
NAME	NO.				
	HTSSOP	VQFN			
VCP	3	24	—	Power	Charge pump output. Connect a X7R, 0.22-µF, 16-V ceramic capacitor to VM.
VM	4, 11	1, 8	—	Power	Power supply. Connect to motor supply voltage and bypass to GND with two 0.01-µF ceramic capacitors (one for each pin) plus a bulk capacitor rated for VM.
VSDO	17	14		Power	Supply pin for SDO output. Connect to 5-V or 3.3-V depending on the desired logic level.
nFAULT	14	11	O	Open Drain	Fault indication. Pulled logic low with fault condition; open-drain output requires an external pullup resistor.
nSCS	16	13	I	Input	Serial chip select. An active low on this pin enables the serial interface communications. Internal pullup to DVDD.
nSLEEP	24	21	I	Input	Sleep mode input. Logic high to enable device; logic low to enter low-power sleep mode; internal pulldown resistor.
PAD	-	-	-	-	Thermal pad. Connect to system ground.

Errata: The QFN package for the prototype version samples does not have wettable flanks. The final version samples will be in wettable flank QFN package.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Power supply voltage (VM)	–0.3	50	V
Charge pump voltage (VCP, CPH)	–0.3	VM + 7	V
Charge pump negative switching pin (CPL)	–0.3	VM	V
Internal regulator voltage (DVDD)	–0.3	5.5	V
SDO output reference voltage (VSDO)	–0.3	5.5	V
Control pin voltage (STEP, DIR, DRVOFF, nFAULT, nSLEEP, SDI, SDO, SCLK, nSCS)	–0.3	5.5	V
Open drain output current (nFAULT)	0	10	mA
Reference input pin voltage (VREF)	–0.3	5.5	V
Continuous phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	–1.0	VM + 1.0	V
Transient 100 ns phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	–3.0	VM + 3.0	V
Peak drive current (AOUT1, AOUT2, BOUT1, BOUT2)	Internally Limited		A
Operating ambient temperature, T_A	–40	125	°C
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100–002(1)		±2000	V
		Charged device model (CDM), per AEC Q100–011	Corner pins for PWP (1, 12, 13, and 24)	±750	
			Other pins	±500	

(1) AECQ100–002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS–001specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VM}	Supply voltage range for normal (DC) operation	4.5	45	V
V_I	Logic level input voltage	0	5.3	V
V_{SDO}	SDO buffer supply voltage	2.9	5.3	V
V_{VREF}	VREF voltage	0.05	3.3	V
f_{PWM}	Applied STEP signal (STEP)	0	100 (1)	kHz
I_{FS}	Motor full-scale current (xOUTx)	0	1.5 (2)	A
I_{rms}	Motor RMS current (xOUTx)	0	1.1 (2)	A
T_A	Operating ambient temperature	–40	125	°C
T_J	Operating junction temperature	–40	150	°C

(1) STEP input can operate up to 500 kHz, but system bandwidth is limited by the motor load
(2) Power dissipation and thermal limits must be observed

6.4 Thermal Information

THERMAL METRIC (1)		DRV8889-Q1		UNIT
		PWP (HTSSOP)	RGE (VQFN)	
		24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.9	40.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.2	31.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.3	17.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.3	17.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.1	4.3	°C/W

(1) For more information about traditional and new thermalmetrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics

Over recommended operating conditions unless otherwise noted. Typical limits apply for T_J = 25°C and V_{VM} = 13.5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, DVDD, VSDO)						
V_{VM}	VM operating voltage	Supply voltage range for normal (DC) operation	4.5		45	V
I_{VM}	VM operating supply current	DRVOFF = 0, nSLEEP = 1, No motor load		5	6.5	mA
I_{VMQ}	VM sleep mode supply current	nSLEEP = 0		2	4	µA
t_{SLEEP}	Sleep time	nSLEEP = 0 to sleep-mode	75			µs
t_{RESET}	nSLEEP reset pulse	nSLEEP low to only clear fault registers	5		20	µs
t_{WAKE}	Wake-up time	nSLEEP = 1 to output transition		0.6	0.9	ms
t_{ON}	Turn-on time	VM > UVLO to output transition		0.6	0.9	ms
V_{DVDD}	Internal regulator voltage	No external load	4.5	5	5.5	V
CHARGE PUMP (VCP, CPH, CPL)						
V_{VCP}	VCP operating voltage			VM + 5		V
$f_{(VCP)}$	Charge pump switching frequency	V_{VM} > UVLO; nSLEEP = 1		400		kHz
LOGIC-LEVEL INPUTS (STEP, DIR, nSLEEP, nSCS, SCLK, SDI, DRVOFF)						
V_{IL}	Input logic-low voltage		0		0.6	V
V_{IH}	Input logic-high voltage		1.5		5.3	V
V_{HYS}	Input logic hysteresis			150		mV
I_{IL1}	Input logic-low current	VIN = 0 V (nSCS, DRVOFF)	8		12	µA
I_{IL2}	Input logic-low current	VIN = 0 V	–1		1	µA
I_{IH1}	Input logic-high current	VIN = DVDD (nSCS, DRVOFF)			200	nA
I_{IH2}	Input logic-high current	VIN = 5 V			100	µA
PUSH-PULL OUTPUT (SDO)						
$R_{PD,SDO}$	Internal pull-down resistance	5mA load, with respect to GND		40	65	Ω
$R_{PU,SDO}$	Internal pull-up resistance	5mA load, with respect to VSDO		30	50	Ω
I_{SDO}	SDO Leakage Current	SDO = VSDO and 0V	-1		1	µA
CONTROL OUTPUTS (nFAULT)						
V_{OL}	Output logic-low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output logic-high leakage	V_{VM} = 13.5 V	–1		1	µA

Electrical Characteristics (continued)

Over recommended operating conditions unless otherwise noted. Typical limits apply for T_J = 25°C and V_{VM} = 13.5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MOTOR DRIVER OUTPUTS (AOUT1, AOUT2, BOUT1, BOUT2)						
$R_{DS(ON)}$	High-side FET on resistance	VM = 13.5 V, I_O = 0.5 A		450	850	mΩ
$R_{DS(ON)}$	Low-side FET on resistance	VM = 13.5 V, I_O = 0.5 A		450	850	mΩ
t_{SR}	Output slew rate	SR = 00b, VM = 13.5 V, I_O = 0.5 A		10		V/µs
		SR = 01b, VM = 13.5 V, I_O = 0.5 A		35		
		SR = 10b, VM = 13.5 V, I_O = 0.5 A		50		
		SR = 11b, VM = 13.5 V, I_O = 0.5 A		105		
PWM CURRENT CONTROL (VREF)						
K_V	Transimpedance gain			2.2		V/A
t_{OFF}	PWM off-time	TOFF = 00b		7		µs
		TOFF = 01b		16		
		TOFF = 10b		24		
		TOFF = 11b		32		
ΔI_{TRIP}	Current trip accuracy	I_O = 1.5 A, 10% to 20% current setting	–12		12	%
		I_O = 1.5 A, 20% to 100% current setting	–7.5		7.5	
$I_{O,CH}$	AOUT and BOUT current matching	I_O = 1.5 A	–2.5		2.5	%
PROTECTION CIRCUITS						
V_{UVLO}	VM UVLO lockout	VM falling, UVLO falling	4.15	4.25	4.35	V
		VM rising, UVLO rising	4.25	4.35	4.45	
$V_{UVLO,HYS}$	Undervoltage hysteresis	Rising to falling threshold		100		mV
V_{RST}	VM UVLO reset	VM falling, device reset, no SPI communications			3.9	V
V_{CPUV}	Charge pump undervoltage	VCP falling; CPUV report		VM + 2		V
I_{OCP}	Overcurrent protection	Current through any FET	2.5			A
t_{OCP}	Overcurrent deglitch time	V_{VM} < 37 V		3		µs
		V_{VM} >= 37 V		0.5		
t_{RETRY}	Overcurrent retry time	OCP_MODE = 1b		4		ms
t_{OL}	Open load detection time	EN_OL = 1b			200	ms
I_{OL}	Open load current threshold			30		mA
T_{OTW}	Overtemperature warning	Die temperature T_J	135	150	165	°C
T_{UTW}	Undertemperature warning	Die temperature T_J	-25	-10	5	°C
T_{OTSD}	Thermal shutdown	Die temperature T_J	150	165	180	°C
T_{HYS_OTSD}	Thermal shutdown hysteresis	Die temperature T_J		20		°C
T_{HYS_OTW}	Overtemperature warning hysteresis	Die temperature T_J		20		°C
T_{HYS_UTW}	Undertemperature warning hysteresis	Die temperature T_J		10		°C

6.6 SPI Timing Requirements

		MIN	NOM	MAX	UNIT
$t_{(READY)}$	SPI ready, VM > V_{RST}		1		ms
$t_{(CLK)}$	SCLK minimum period	100			ns
$t_{(CLKH)}$	SCLK minimum high time	50			ns
$t_{(CLKL)}$	SCLK minimum low time	50			ns
$t_{su(SDI)}$	SDI input setup time	20			ns

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SPI Timing Requirements (continued)

		MIN	NOM	MAX	UNIT
$t_{h(SDI)}$	SDI input hold time	30			ns
$t_{d(SDO)}$	SDO output delay time, SCLK high to SDO valid, C_L = 20 pF			30	ns
$t_{su(nSCS)}$	nSCS input setup time	50			ns
$t_{h(nSCS)}$	nSCS input hold time	50			ns
$t_{(HI\_nSCS)}$	nSCS minimum high time before active low			2	µs
$t_{dis(nSCS)}$	nSCS disable time, nSCS high to SDO high impedance		10		ns

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6.7 Indexer Timing Requirements

Over recommended operating conditions unless otherwise noted. Typical limits apply for T_J = 25°C and V_{VM} = 13.5 V

NO.			MIN	MAX	UNIT
1	f_{STEP}	Step frequency		500(1)	kHz
2	$t_{WH(STEP)}$	Pulse duration, STEP high	970		ns
3	$t_{WL(STEP)}$	Pulse duration, STEP low	970		ns
4	$t_{SU(DIR, Mx)}$	Setup time, DIR to STEP rising	200		ns
5	$t_{H(DIR, Mx)}$	Hold time, DIR to STEP rising	200		ns

(1) STEP input can operate up to 500 kHz, but system bandwidth islimited by the motor load.

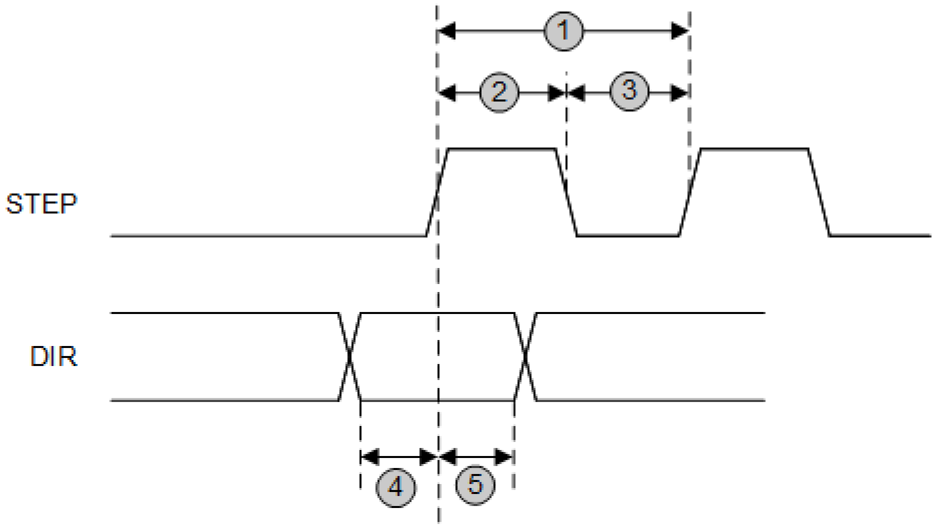

图 1. STEP and DIR Timing Diagram

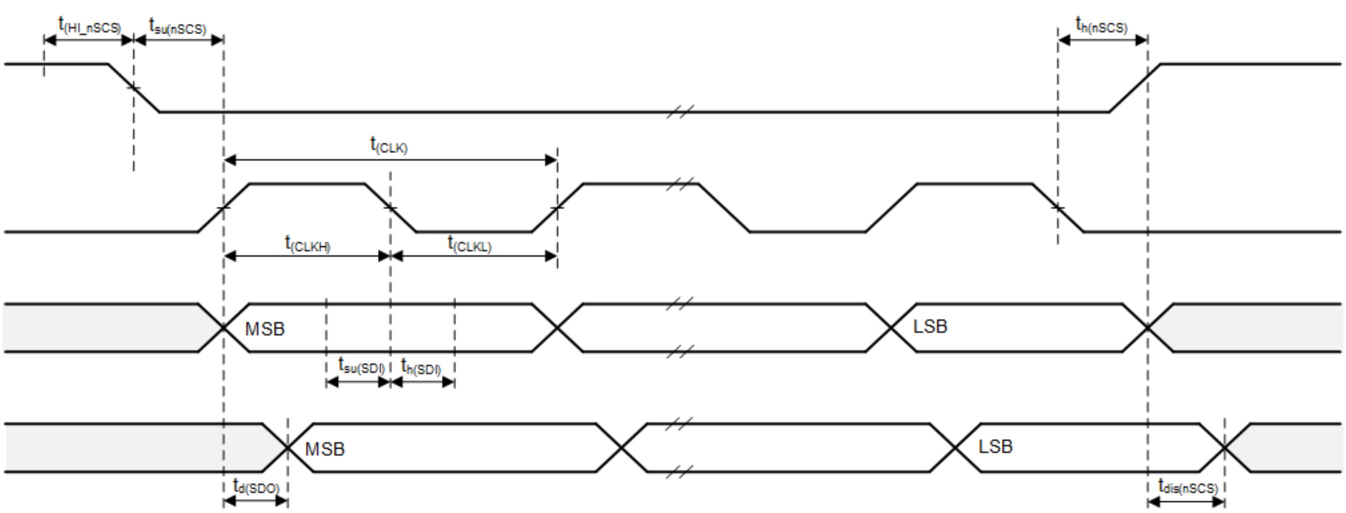

图 2. SPI Slave-Mode Timing Definition

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7 Detailed Description

7.1 Overview

The DRV8889-Q1 device is an integrated motor-driver solution for bipolar stepper motors. The device integrates two N-channel power MOSFET H-bridges, integrated current sense and regulation circuitry, and a microstepping indexer. The DRV8889-Q1 device can be powered with a supply voltage from 4.5 to 45 V and is capable of providing an output current up to 2.5-A peak, 1.5-A full-scale, or 1.1-A root mean square (rms). The actual full-scale and rms current depends on the ambient temperature, supply voltage, and PCB thermal capability.

The device uses an integrated current-sense architecture which eliminates the need for two external power sense resistors. This architecture removes the power dissipated in the sense resistors by using a current mirror approach and using the internal power MOSFETs for current sensing. The current regulation set point is adjusted by the voltage at the VREF pin. These features reduces external component cost, board PCB size, and system power consumption.

A simple STEP/DIR interface allows for an external controller to manage the direction and step rate of the stepper motor. The internal indexer can execute high-accuracy microstepping without requiring the external controller to manage the winding current level. The indexer is capable of full step, half step, and 1/4, 1/8, 1/16, 1/32, 1/64, 1/128 and 1/256 microstepping. In addition to a standard half stepping mode, a noncircular half stepping mode is available for increased torque output at higher motor RPM.

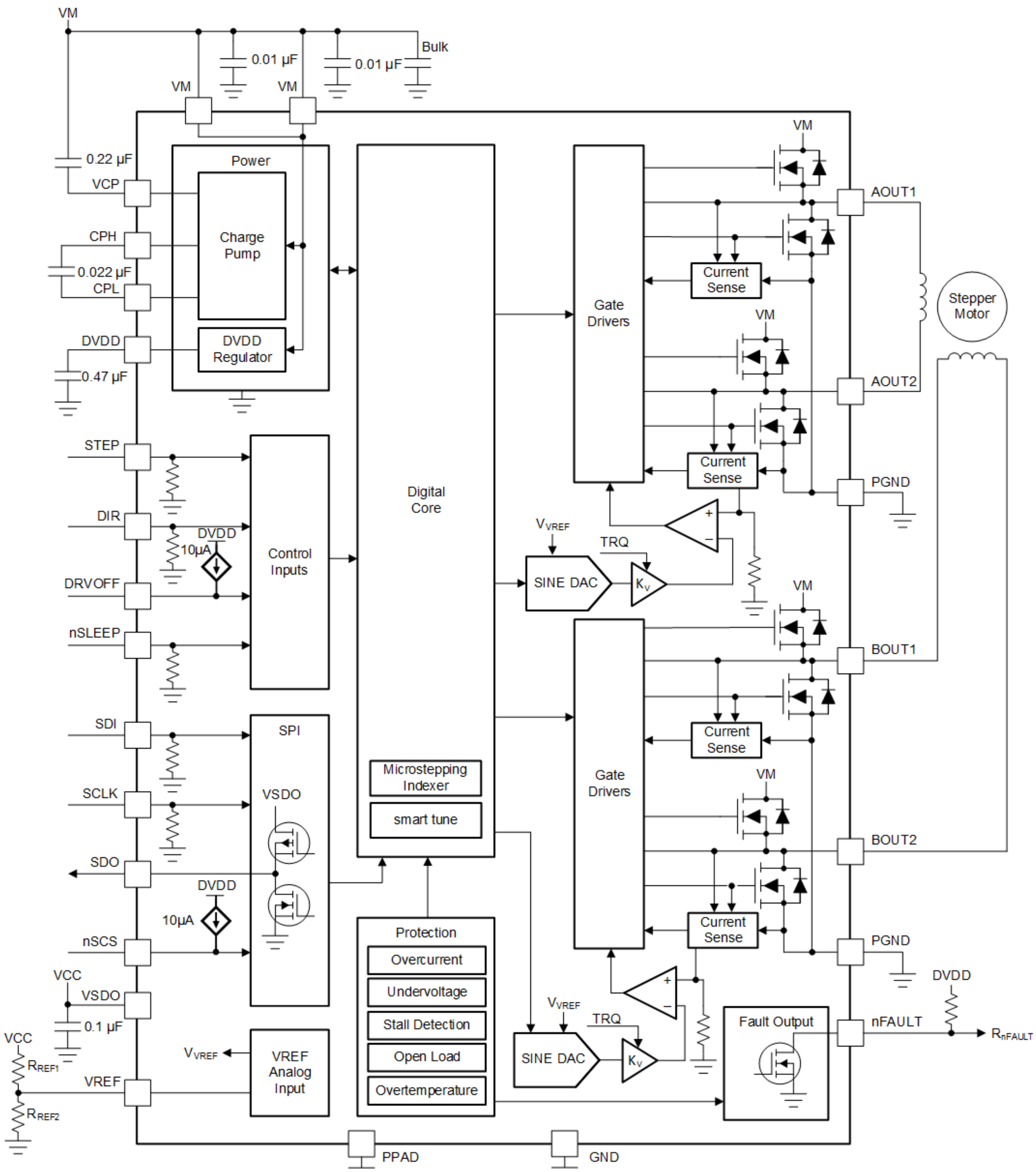
The current regulation is configurable between several decay modes. The decay mode can be selected as a slow-mixed, mixed decay, smart tune Ripple Control, or smart tune Dynamic Decay current regulation scheme. The slow-mixed decay mode uses slow decay on increasing steps and mixed decay on decreasing steps. The smart tune decay modes automatically adjust for optimal current regulation performance and compensate for motor variation and aging effects. Smart tune Ripple Control uses a variable off-time, ripple control scheme to minimize distortion of the motor winding current. Smart tune Dynamic Decay uses a fixed off-time, dynamic decay percentage scheme to minimize distortion of the motor winding current while also minimizing frequency content.

The device integrates a spread spectrum clocking feature for both the internal digital oscillator and internal charge pump. This feature combined with output slew rate control minimizes the radiated emissions from the device.

A torque DAC feature allows the controller to scale the output current without needing to scale the VREF voltage reference. The torque DAC is accessed using a digital input pin which allows the controller to save system power by decreasing the motor current consumption when high output torque is not required.

A low-power sleep mode is included which allows the system to save power when not actively driving the motor.

7.2 Functional Block Diagram



7.3 Feature Description

表 1 lists the recommended external components for the DRV8889-Q1 device.

表 1. DRV8889-Q1 External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	GND	Two X7R, 0.01-µF, VM-rated ceramic capacitors
C_{VM2}	VM	GND	Bulk, VM-rated capacitor
C_{VCP}	VCP	VM	X7R, 0.22-µF, 16-V ceramic capacitor
C_{SW}	CPH	CPL	X7R, 0.022-µF, VM-rated ceramic capacitor
C_{DVDD}	DVDD	GND	X7R, 0.47-µF to 1-µF, 6.3-V ceramic capacitor
R_{nFAULT}	VCC [(1)]	nFAULT	>4.7-kΩ resistor
R_{REF1}	VREF	VCC	Resistor to limit chopping current. It is recommended that the value of parallel combination of R_{REF1} and R_{REF2} should be less than 50-kΩ.
R_{REF2} (Optional)	VREF	GND	

(1) VCC is not a pin on the DRV8889-Q1 device, but a VCC supply voltage pullup is required for open-drain output nFAULT; nFAULT may be pulled up to DVDD

7.3.1 Stepper Motor Driver Current Ratings

Stepper motor drivers can be classified using three different numbers to describe the output current: peak, rms, and full-scale.

7.3.1.1 Peak Current Rating

The peak current in a stepper driver is limited by the overcurrent protection trip threshold I_{OCP}. The peak current describes any transient duration current pulse, for example when charging capacitance, when the overall duty cycle is very low. In general the minimum value of I_{OCP} specifies the peak current rating of the stepper motor driver.

For the DRV8889-Q1 device, the peak current rating is 2.5A per bridge.

7.3.1.2 rms Current Rating

The rms (average) current is determined by the thermal considerations of the IC. The rms current is calculated based on the $R_{DS(ON)}$, rise and fall time, PWM frequency, device quiescent current, and package thermal performance in a typical system at 25°C. The actual operating rms current may be higher or lower depending on heatsinking and ambient temperature.

For the DRV8889-Q1 device, the rms current rating is 1.1 A per bridge.

7.3.1.3 Full-Scale Current Rating

The full-scale current describes the top of the sinusoid current waveform while microstepping. Because the sinusoid amplitude is related to the rms current, the full-scale current is also determined by the thermal considerations of the device. The full-scale current rating is approximately $\sqrt{2} \times I_{RMS}$.

For the DRV8889-Q1 device, the full-scale current rating is 1.5 A per bridge.

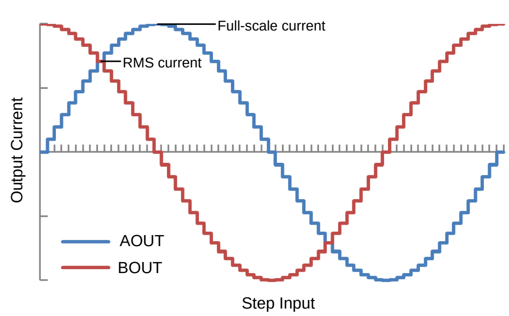


图 3. Full-Scale and RMS Current

7.3.2 PWM Motor Drivers

The device has drivers for two full H-bridges to drive the two windings of a bipolar stepper motor. 图 4 shows a block diagram of the circuitry.

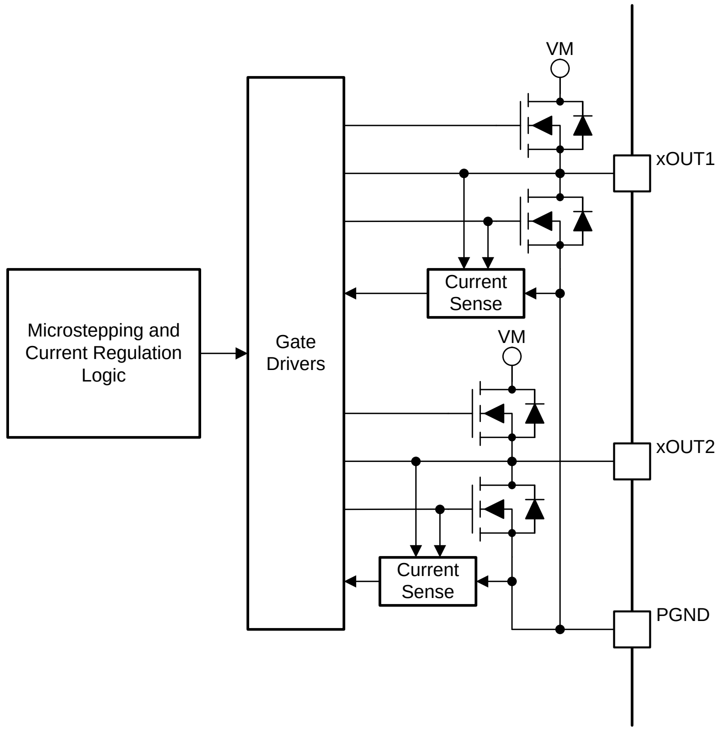


图 4. PWM Motor Driver Block Diagram

7.3.3 Microstepping Indexer

Built-in indexer logic in the device allows a number of different step modes. The MICROSTEP_MODE bits in the SPI register are used to configure the step mode as shown in 表 2.

表 2. Microstepping Settings

MICROSTEP_MODE	STEP MODE
0000b	Full step (2-phase excitation) with 100% current
0001b	Full step (2-phase excitation) with 71% current
0010b	Non-circular 1/2 step
0011b	1/2 step
0100b	1/4 step
0101b	1/8 step
0110b	1/16 step
0111b	1/32 step
1000b	1/64 step
1001b	1/128 step
1010b	1/256 step

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表 3 shows the relative current and step directions for full-step (71% current), 1/2 step, 1/4 step and 1/8 step operation. Higher microstepping resolutions follow the same pattern. The AOUT current is the sine of the electrical angle and the BOUT current is the cosine of the electrical angle. Positive current is defined as current flowing from the xOUT1 pin to the xOUT2 pin while driving.

At each rising edge of the STEP input the indexer travels to the next state in the table. The direction is shown with the DIR pin logic high. If the DIR pin is logic low, the sequence is reversed.

注

If the step mode is changed on the fly while stepping, the indexer advances to the next valid state for the new step mode setting at the rising edge of STEP.

The home state is an electrical angle of 45°. This state is entered after power-up, after exiting logic undervoltage lockout, or after exiting sleep mode.

表 3. Relative Current and Step Directions

1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP 71%	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
1	1	1		0	100	0
2				20	98	11
3	2			38	92	23
4				56	83	34
5	3	2	1	71	71	45
6				83	56	56
7	4			92	38	68
8				98	20	79
9	5	3		100	0	90
10				98	–20	101
11	6			92	–38	113
12				83	–56	124
13	7	4	2	71	–71	135
14				56	–83	146
15	8			38	–92	158
16				20	–98	169
17	9	5		0	–100	180
18				–20	–98	191
19	10			–38	–92	203
20				–56	–83	214
21	11	6	3	–71	–71	225
22				–83	–56	236
23	12			–92	–38	248
24				–98	–20	259
25	13	7		–100	0	270
26				–98	20	281
27	14			–92	38	293
28				–83	56	304
29	15	8	4	–71	71	315
30				–56	83	326
31	16			–38	92	338
32				–20	98	349

表 4 shows the full step operation with 100% full-scale current. This stepping mode consumes more power than full-step mode with 71% current, but provides a higher torque at high motor RPM.

表 4. Full Step with 100% Current

FULL STEP 100%	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
1	100	100	45
2	-100	100	135
3	-100	-100	225
4	100	–100	315

表 5 shows the noncircular 1/2–step operation. This stepping mode consumes more power than circular 1/2-step operation, but provides a higher torque at high motor RPM.

表 5. Non-Circular 1/2-Stepping Current

NON-CIRCULAR 1/2-STEP	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
1	0	100	0
2	100	100	45
3	100	0	90
4	100	–100	135
5	0	–100	180
6	–100	–100	225
7	–100	0	270
8	–100	100	315

7.3.4 Controlling VREF with an MCU DAC

In some cases, the full-scale output current may need to be changed between many different values, depending on motor speed and loading. The voltage of the VREF pin can be adjusted in the system to change the full-scale current.

In this mode of operation, as the DAC voltage increases, the full-scale regulation current increases as well. For proper operation, the output of the DAC should not rise above 3.3 V.

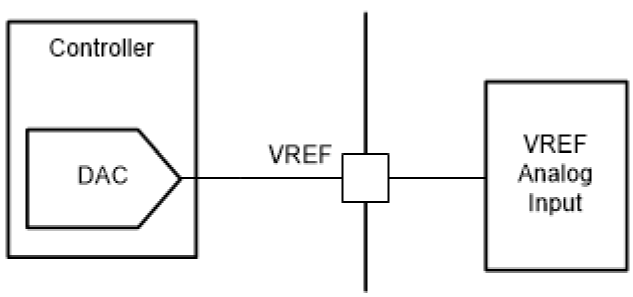

图 5. Controlling VREF with a DAC Resource

The VREF pin can also be adjusted using a PWM signal and low-pass filter.

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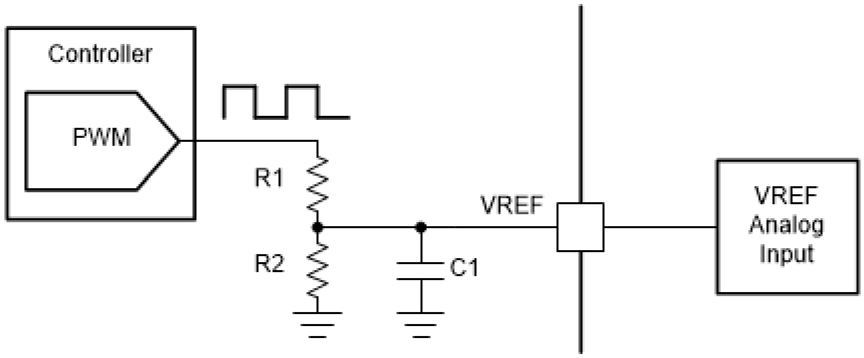

图 6. Controlling VREF With a PWM Resource

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7.3.5 Current Regulation

The current through the motor windings is regulated by a PWM current-regulation circuit. When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage, inductance of the winding, and the magnitude of the back EMF present. When the current hits the current regulation threshold, the bridge enters a decay mode for a period of time determined by the TOFF register setting and the selected decay mode to decrease the current. After the off-time expires, the bridge is re-enabled, starting another PWM cycle.

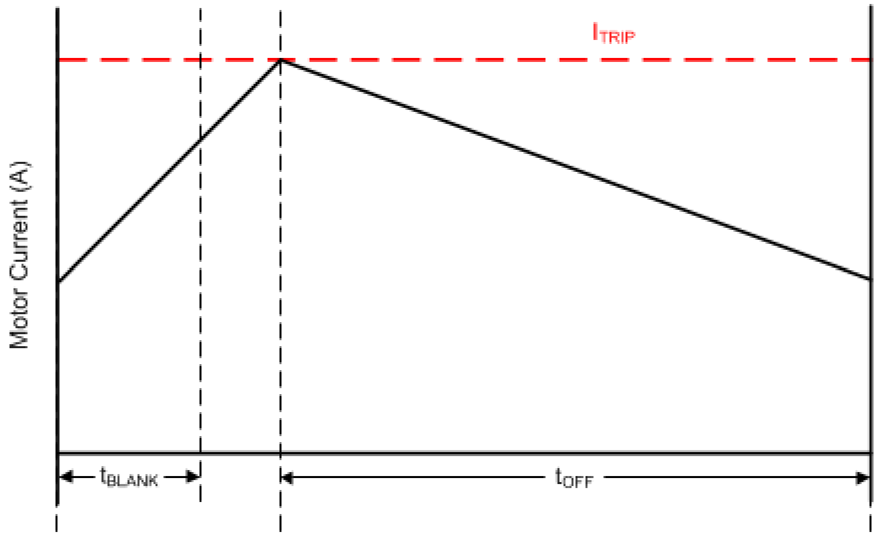

图 7. Current Chopping Waveform

The PWM regulation current is set by a comparator which monitors the voltage across the current sense MOSFETs in parallel with the low-side power MOSFETs. The current sense MOSFETs are biased with a reference current that is the output of a current-mode sine-weighted DAC whose full-scale reference current is set by the voltage at the VREF pin. In addition, the TRQ_DAC register can further scale the reference current.

Use 公式 1 to calculate the full-scale regulation current.

$$I_{FS}(A) = \frac{V_{REF}(V)}{K_V(V/A)} \times TRQ\_DAC(\%) = \frac{V_{REF}(V) \times TRQ\_DAC(\%)}{2.2(V/A)} \quad (1)$$

The TRQ_DAC is adjusted via the SPI register. 表 6 lists the current scalar value for different inputs.

表 6. Torque DAC Settings

TRQ_DAC	CURRENT SCALAR (TRQ)
0000b	100%
0001b	93.75%
0010b	87.5%
0011b	81.25%
0100b	75%
0101b	68.75%
0110b	62.5
0111b	56.25%
1000b	50%
1001b	43.75%
1010b	37.5%
1011b	31.25%

表 6. Torque DAC Settings (接下页)

TRQ_DAC	CURRENT SCALAR (TRQ)
1100b	25%
1101b	18.75%
1110b	12.5%
1111b	6.25%

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7.3.6 Decay Modes

During PWM current chopping, the H-bridge is enabled to drive through the motor winding until the PWM current chopping threshold is reached. This is shown in 图 8, Item 1.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay. In fast decay mode, once the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. The opposite FETs are turned on; as the winding current approaches zero, the bridge is disabled to prevent any reverse current flow. Fast decay mode is shown in 图 8, item 2. In slow decay mode, winding current is re-circulated by enabling both of the low-side FETs in the bridge. This is shown in 图 8, Item 3.

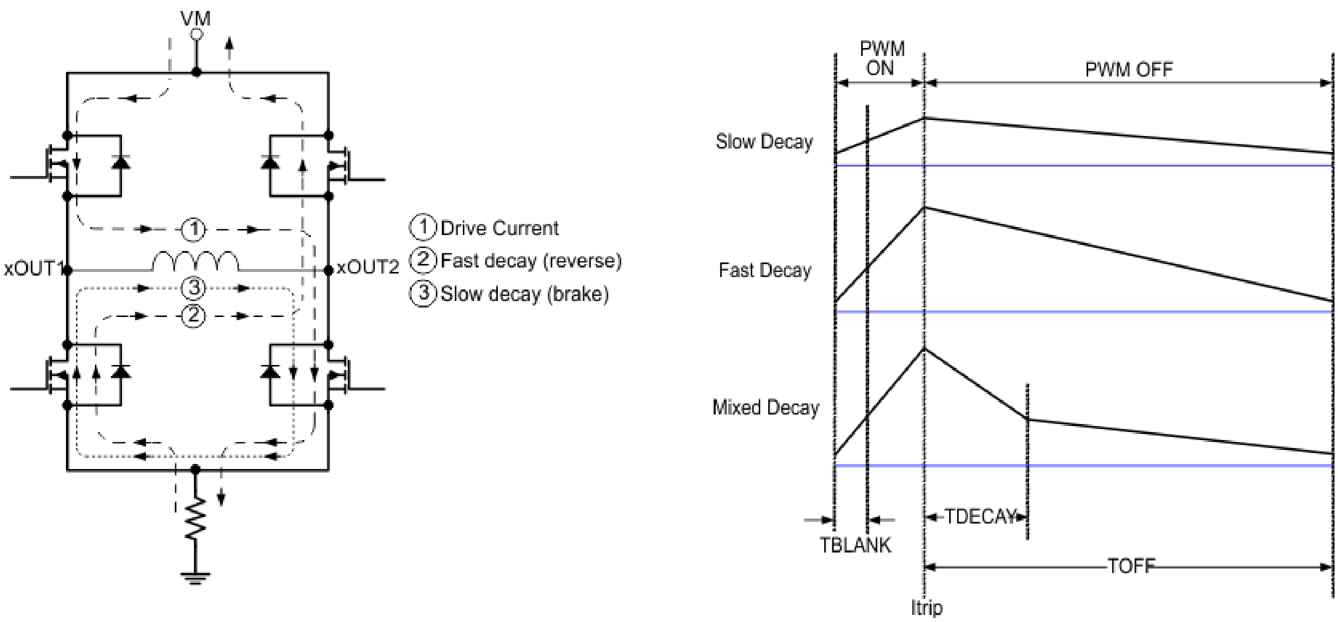

图 8. Decay Modes

The decay mode is selected by the DECAY register as shown in 表 7.

表 7. Decay Mode Settings

DECAY	INCREASING STEPS	DECREASING STEPS
000b	Slow decay	Slow decay
001b	Slow decay	Mixed decay: 30% fast
010b	Slow decay	Mixed decay: 60% fast
011b	Slow decay	Fast decay
100b	Mixed decay: 30% fast	Mixed decay: 30% fast
101b	Mixed decay: 60% fast	Mixed decay: 60% fast
110b	Smart tune Dynamic Decay	Smart tune Dynamic Decay
111b (default)	Smart tune Ripple Control	Smart tune Ripple Control

图 9 defines increasing and decreasing current. For the slow-mixed decay mode, the decay mode is set as slow during increasing current steps and mixed decay during decreasing current steps. In full step and noncircular 1/2-step operation, the decay mode corresponding to decreasing steps is always used.

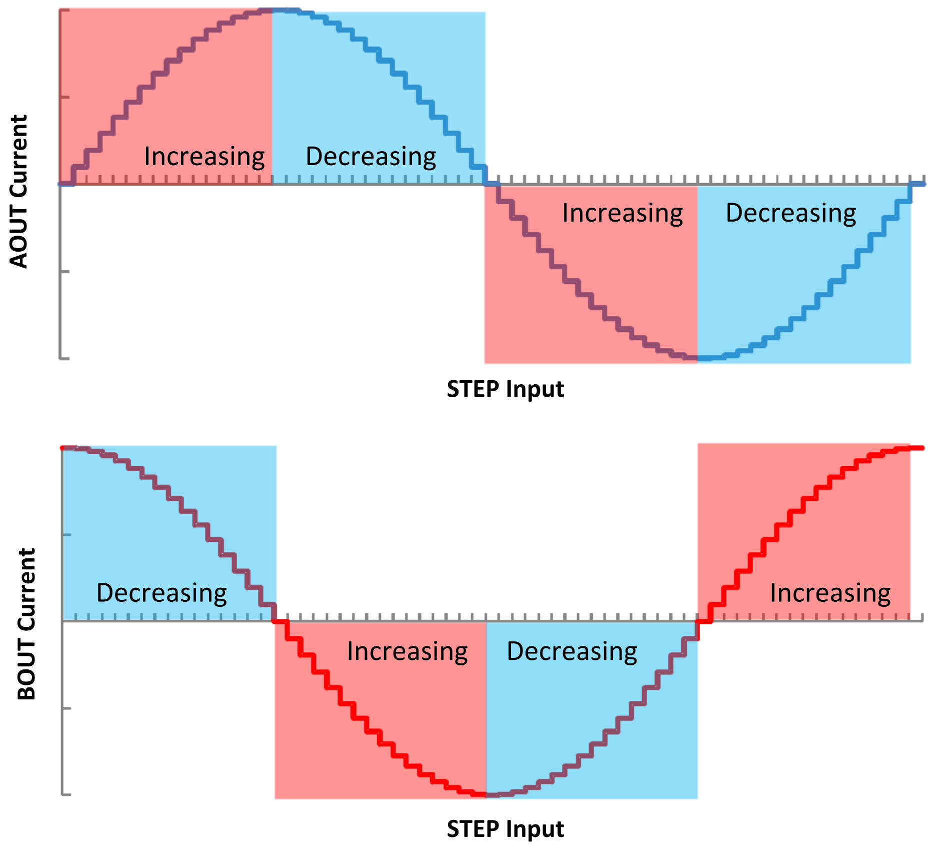

图 9. Definition of Increasing and Decreasing Steps

7.3.6.1 Slow Decay for Increasing and Decreasing Current

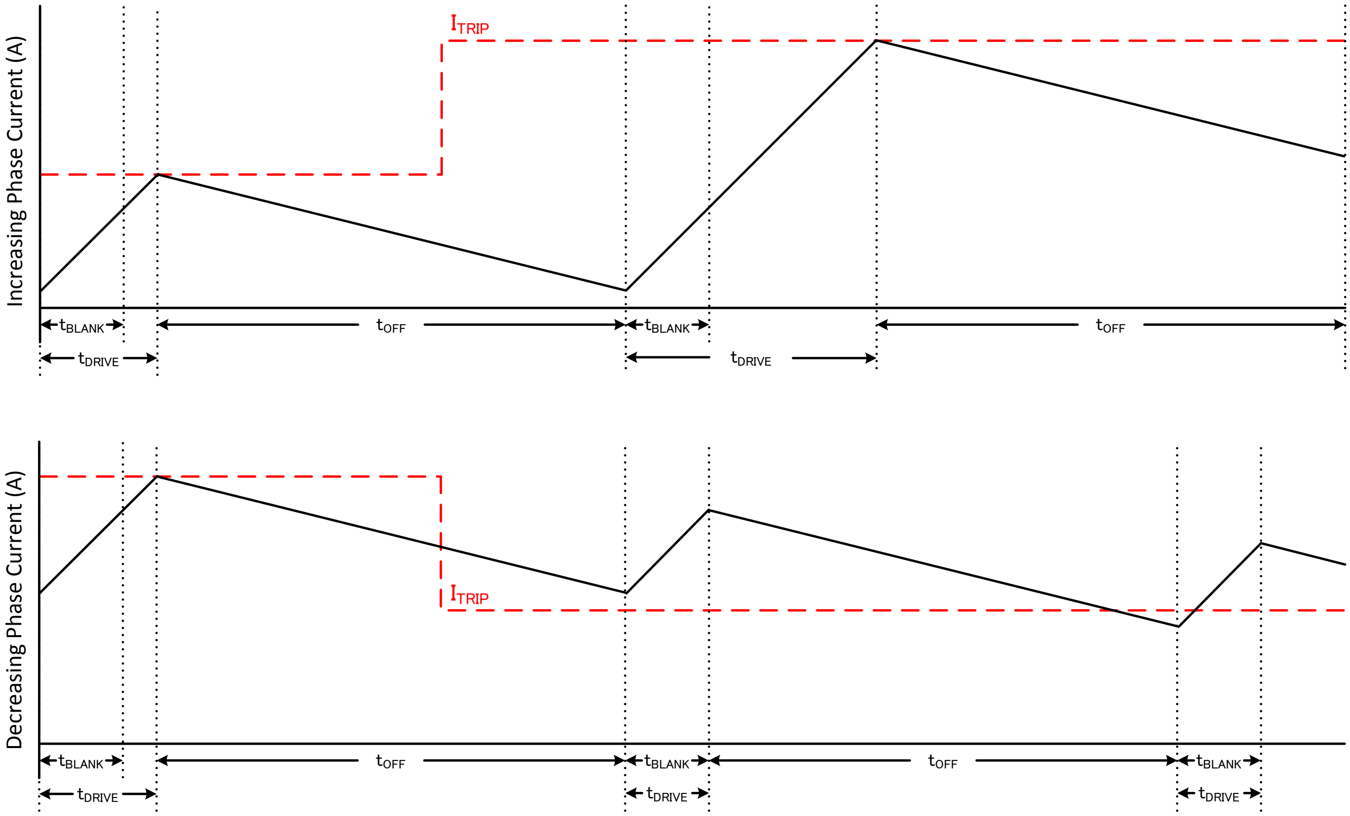

图 10. Slow/Slow Decay Mode

During slow decay, both of the low-side FETs of the H-bridge are turned on, allowing the current to be recirculated.

Slow decay exhibits the least current ripple of the decay modes for a given t_{OFF}. However on decreasing current steps, slow decay will take a long time to settle to the new I_{TRIP} level because the current decreases very slowly.

In cases where current is held for a long time (no input in the STEP pin) or at very low stepping speeds, slow decay may not properly regulate current because no back-EMF is present across the motor windings. In this state, motor current can rise very quickly, and may require a large off-time. In some cases this may cause a loss of current regulation, and a more aggressive decay mode is recommended.

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7.3.6.2 Slow Decay for Increasing Current, Mixed Decay for Decreasing Current

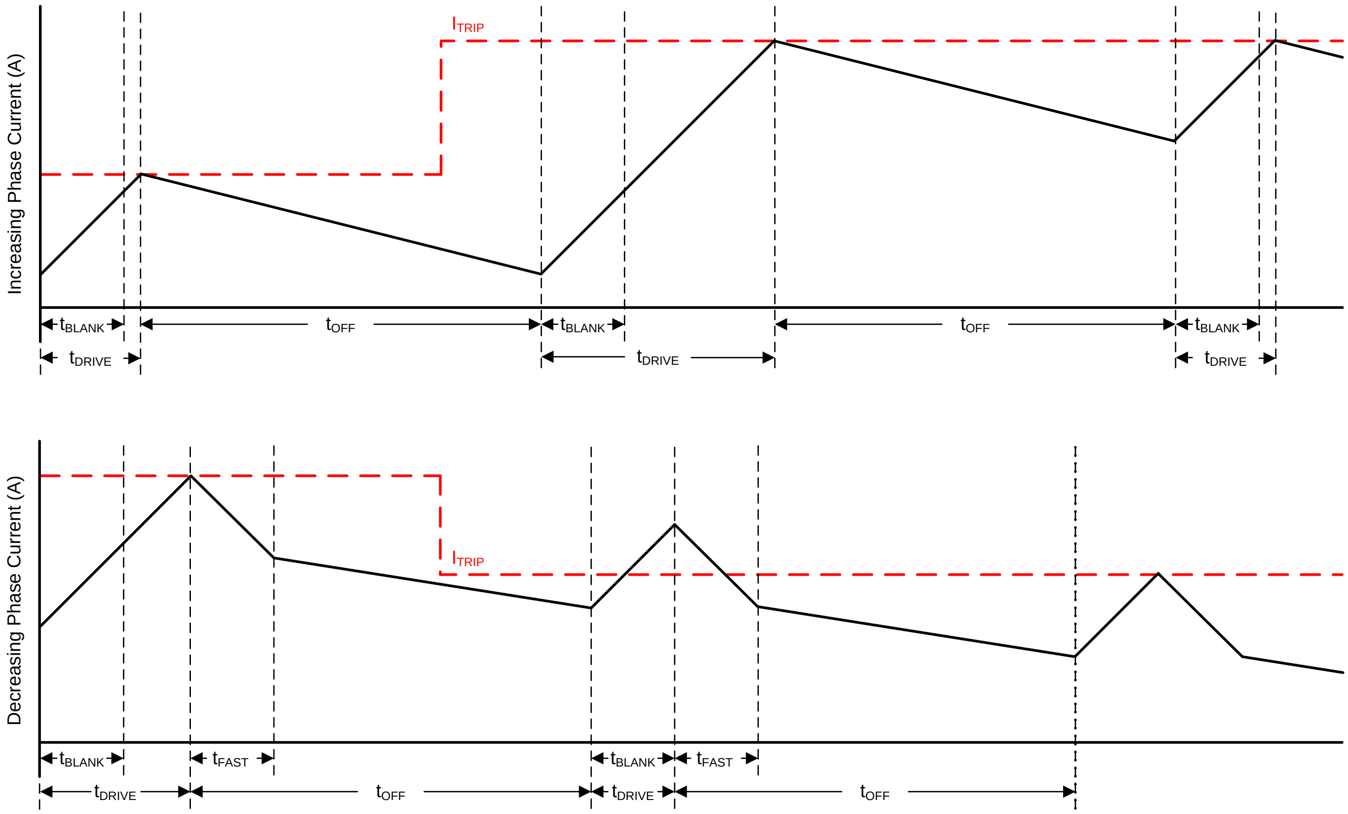

图 11. Slow-Mixed Decay Mode

Mixed decay begins as fast decay for a time, followed by slow decay for the remainder of the t_{OFF} time. In this mode, mixed decay only occurs during decreasing current. Slow decay is used for increasing current.

This mode exhibits the same current ripple as slow decay for increasing current, because for increasing current, only slow decay is used. For decreasing current, the ripple is larger than slow decay, but smaller than fast decay. On decreasing current steps, mixed decay settles to the new I_{TRIP} level faster than slow decay.

7.3.6.3 Mode 4: Slow Decay for Increasing Current, Fast Decay for Decreasing current

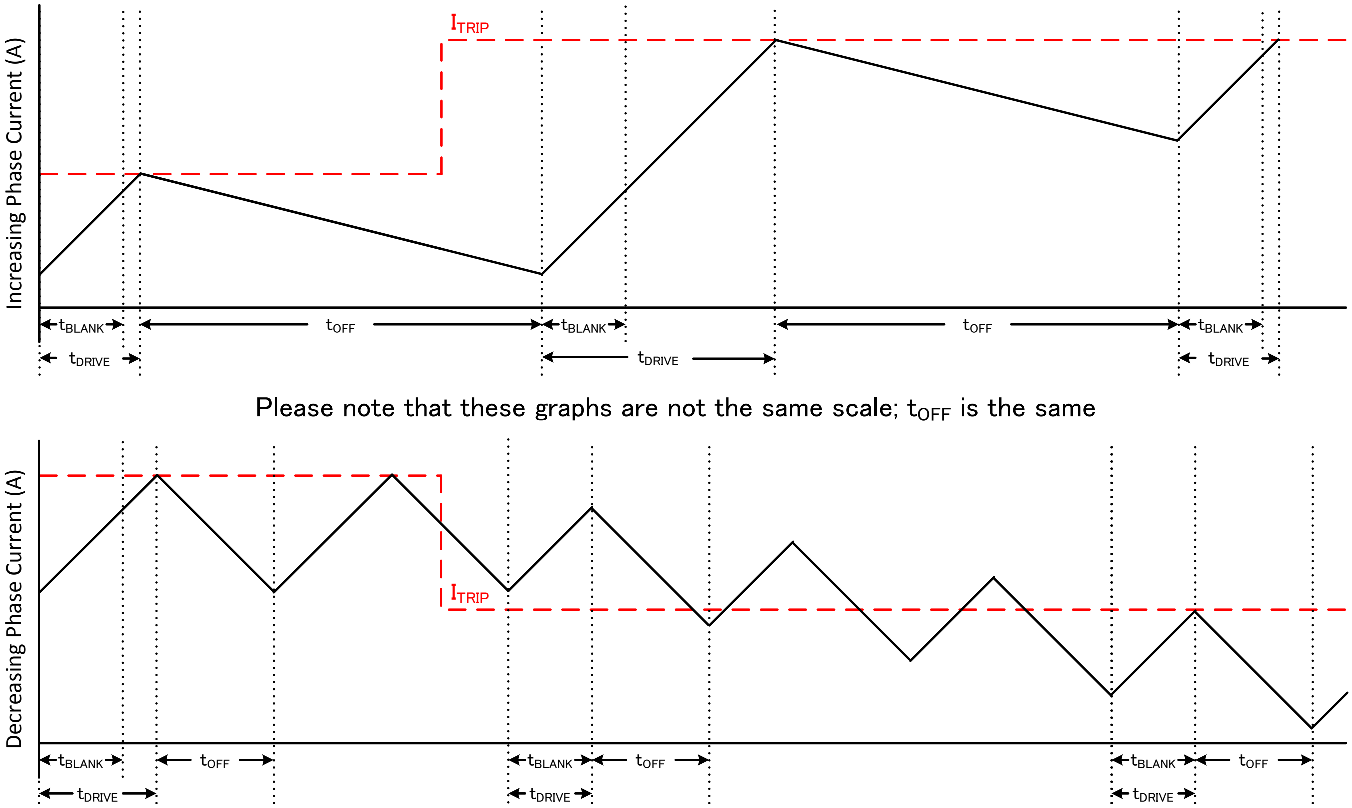

图 12. Slow/Fast Decay Mode

During fast decay, the polarity of the H-bridge is reversed. The H-bridge will be turned off as current approaches zero in order to prevent current flow in the reverse direction. In this mode, fast decay only occurs during decreasing current. Slow decay is used for increasing current.

Fast decay exhibits the highest current ripple of the decay modes for a given t_{OFF}. Transition time on decreasing current steps is much faster than slow decay since the current is allowed to decrease much faster.

7.3.6.4 Mixed Decay for Increasing and Decreasing Current

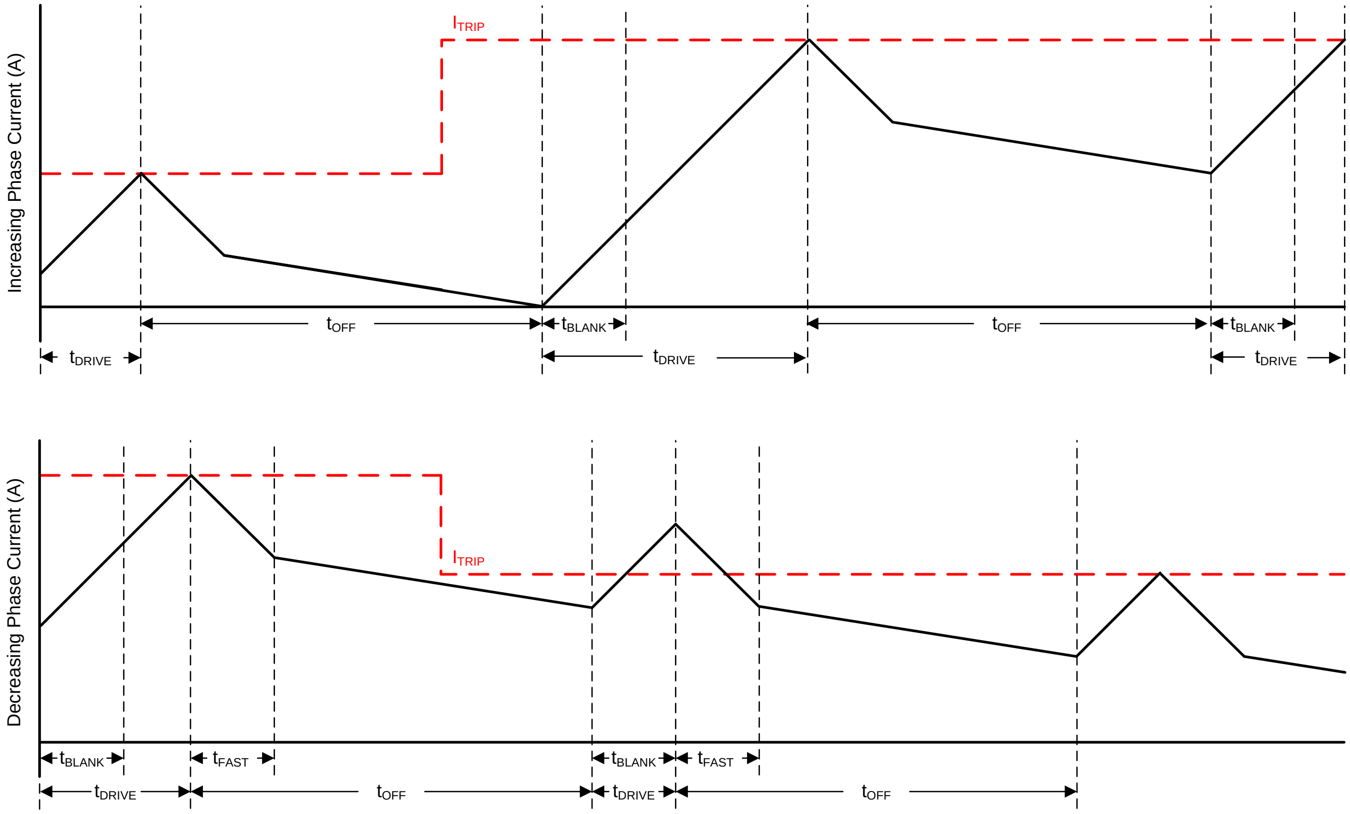

图 13. Mixed-Mixed Decay Mode

Mixed decay begins as fast decay for a time, followed by slow decay for the remainder of t_{OFF}. In this mode, mixed decay occurs for both increasing and decreasing current steps.

This mode exhibits ripple larger than slow decay, but smaller than fast decay. On decreasing current steps, mixed decay settles to the new I_{TRIP} level faster than slow decay.

In cases where current is held for a long time (no input in the STEP pin) or at very low stepping speeds, slow decay may not properly regulate current because no back-EMF is present across the motor windings. In this state, motor current can rise very quickly, and requires an excessively large off-time. Increasing or decreasing mixed decay mode allows the current level to stay in regulation when no back-EMF is present across the motor windings.

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7.3.6.5 Smart tune Dynamic Decay

The smart tune current regulation schemes are advanced current-regulation control methods compared to traditional fixed off-time current regulation schemes. Smart tune current regulation schemes help the stepper motor driver adjust the decay scheme based on operating factors such as the ones listed as follows:

- Motor winding resistance and inductance
- Motor aging effects
- Motor dynamic speed and load
- Motor supply voltage variation
- Motor back-EMF difference on rising and falling steps
- Step transitions
- Low-current versus high-current dI/dt

The device provides two different smart tune current regulation modes, named smart tune Dynamic Decay and smart tune Ripple Control.

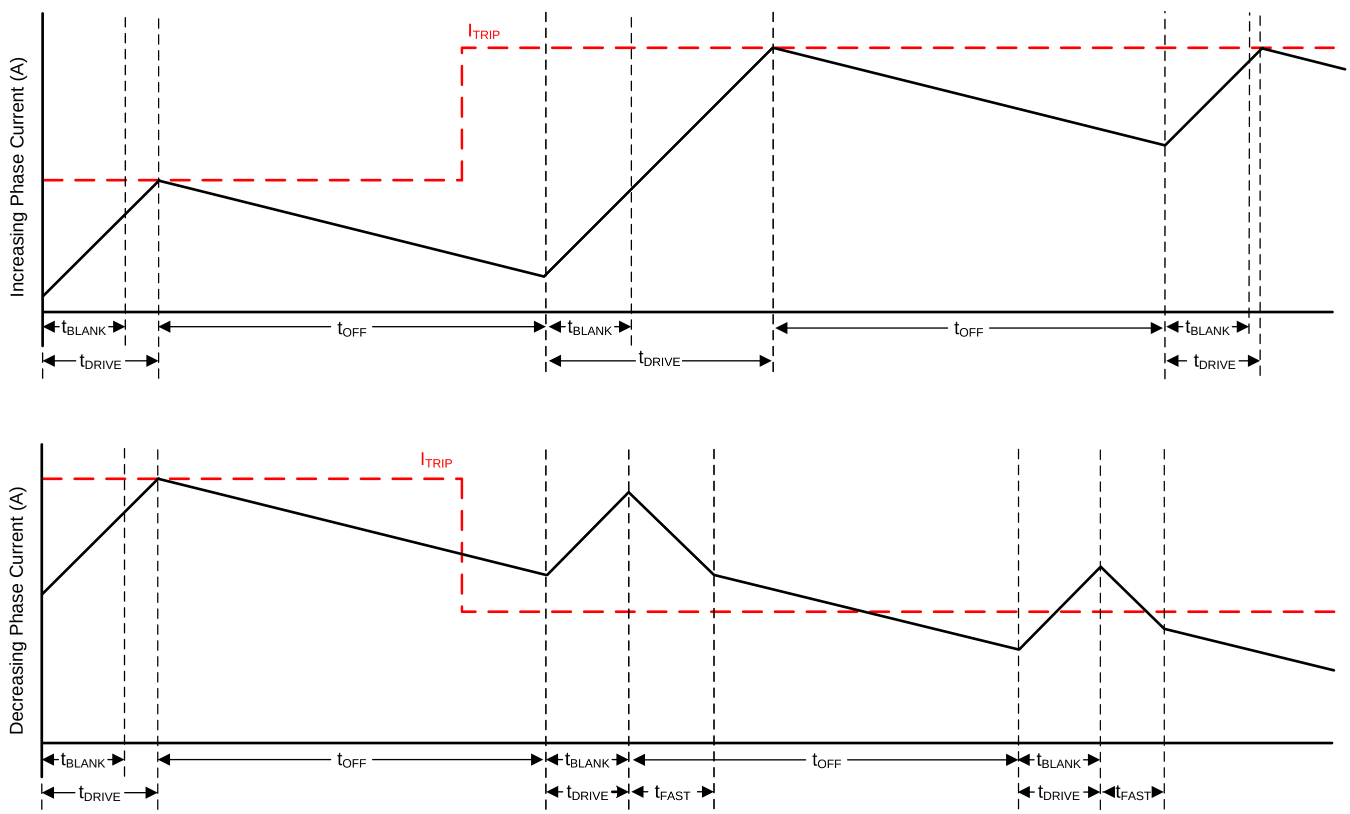

图 14. Smart tune Dynamic Decay Mode

Smart tune Dynamic Decay greatly simplifies the decay mode selection by automatically configuring the decay mode between slow, mixed, and fast decay. In mixed decay, smart tune dynamically adjusts the fast decay percentage of the total mixed decay time. This feature eliminates motor tuning by automatically determining the best decay setting that results in the lowest ripple for the motor.

The decay mode setting is optimized iteratively each PWM cycle. If the motor current overshoots the target trip level, then the decay mode becomes more aggressive (add fast decay percentage) on the next cycle to prevent regulation loss. If a long drive time must occur to reach the target trip level, the decay mode becomes less aggressive (remove fast decay percentage) on the next cycle to operate with less ripple and more efficiently. On falling steps, smart tune Dynamic Decay automatically switches to fast decay to reach the next step quickly.

Smart tune Dynamic Decay is optimal for applications that require minimal current ripple but want to maintain a fixed frequency in the current regulation scheme.

7.3.6.6 Smart tune Ripple Control

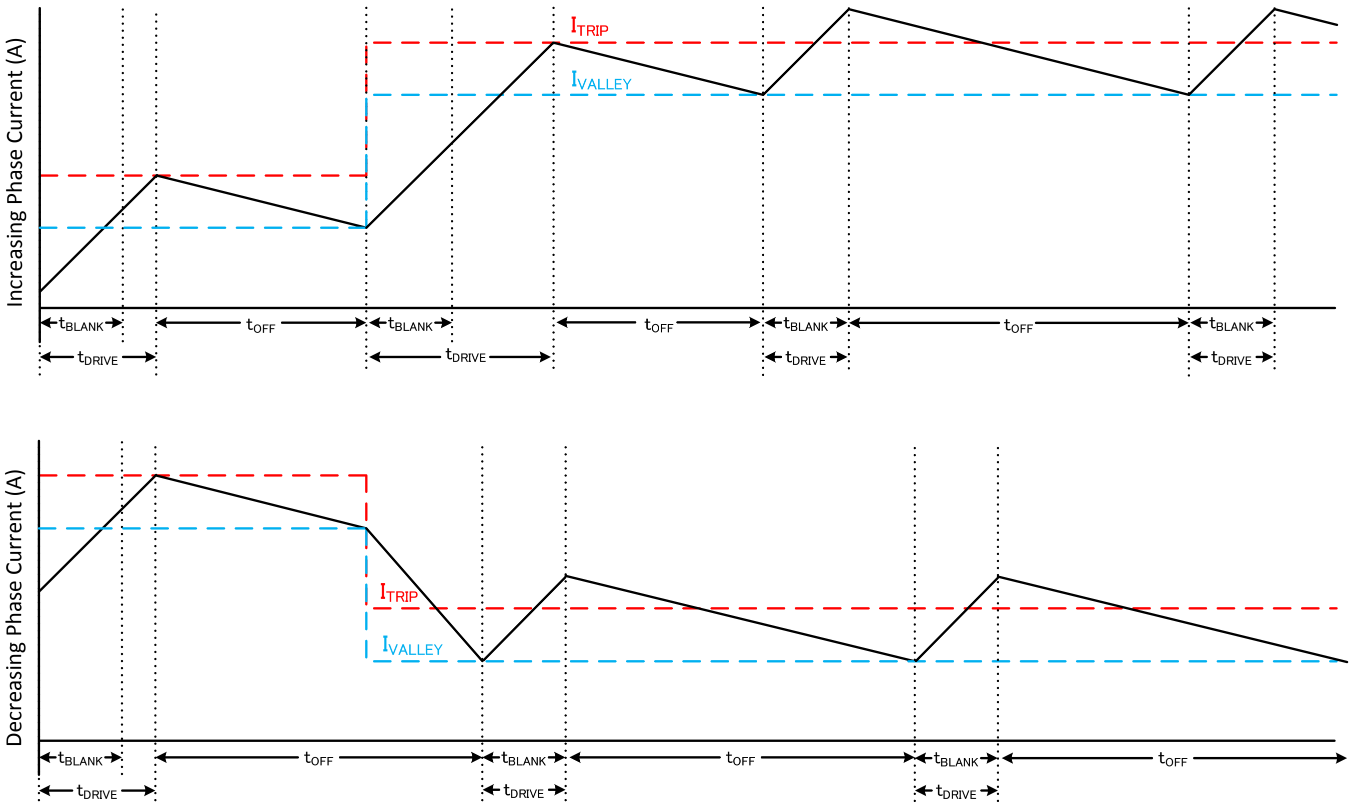

图 15. Smart tune Ripple Control Decay Mode

Smart tune Ripple Control operates by setting an I_{VALLEY} level alongside the I_{TRIP} level. When the current level reaches I_{TRIP}, instead of entering slow decay until the t_{OFF} time expires, the driver enters slow decay until I_{VALLEY} is reached. Slow decay operates similar to mode 1 in which both low-side MOSFETs are turned on allowing the current to recirculate. In this mode, t_{OFF} varies depending on the current level and operating conditions.

This method allows much tighter regulation of the current level increasing motor efficiency and system performance. Smart tune Ripple Control can be used in systems that can tolerate a variable off-time regulation scheme to achieve small current ripple in the current regulation.

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7.3.7 Blanking Time

After the current is enabled (start of drive phase) in an H-bridge, the current sense comparator is ignored for a period of time (t_{BLANK}) before enabling the current-sense circuitry. The blanking time also sets the minimum drive time of the PWM. When the device goes into a drive phase at the end of a slow-decay phase, the blanking time is roughly 500 ns. If the device goes into drive phase at the end of a fast-decay phase, the approximate blanking time is as shown in the following table -

表 8. Blanking Time

SLEW_RATE	Blanking Time (t_{BLANK})
00b	5.6 µs
01b	2 µs
10b	1.5 µs
11b	860 ns

7.3.8 Charge Pump

A charge pump is integrated to supply a high-side N-channel MOSFET gate-drive voltage. The charge pump requires a capacitor between the VM and VCP pins to act as the storage capacitor. Additionally a ceramic capacitor is required between the CPH and CPL pins to act as the flying capacitor.

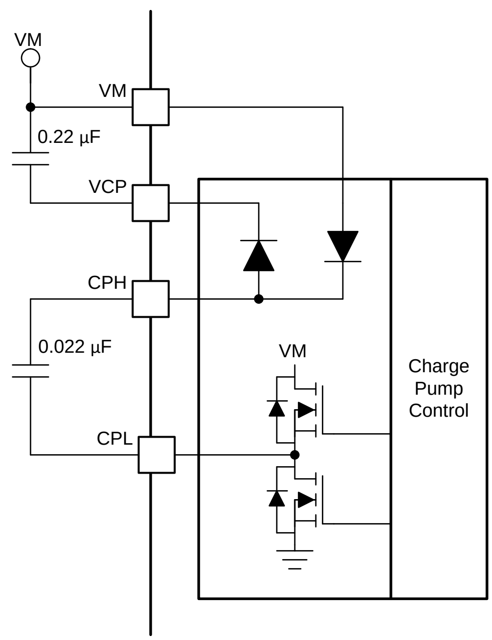

图 16. Charge Pump Block Diagram

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7.3.9 Linear Voltage Regulators

A linear voltage regulator is integrated into the device. The DVDD regulator can be used to provide a reference voltage. DVDD can supply a maximum of 2 mA load. For proper operation, bypass the DVDD pin to GND using a ceramic capacitor.

The DVDD output is nominally 5-V. When the DVDD LDO current load exceeds 2 mA, the output voltage drops significantly.

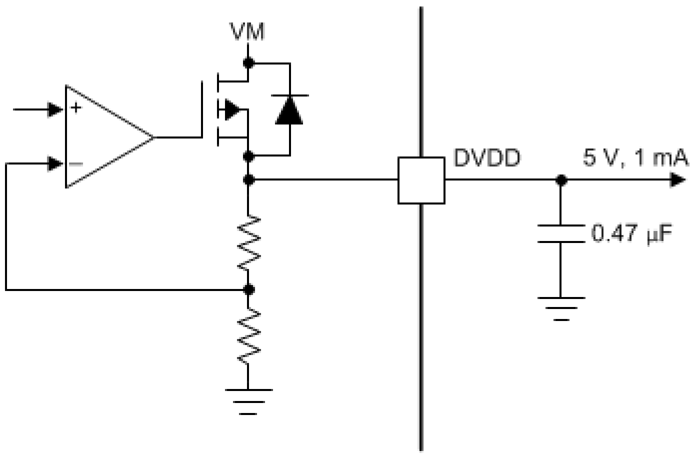

图 17. Linear Voltage Regulator Block Diagram

If logic level inputs must be tied permanently high, tying the input to the DVDD pin instead of an external regulator is preferred. This method saves power when the VM pin is not applied or in sleep mode: the DVDD regulator is disabled and current does not flow through the input pulldown resistors. For reference, logic level inputs have a typical pulldown of 200 kΩ.

The nSLEEP pin cannot be tied to DVDD, else the device will never exit sleep mode.

7.3.10 Logic Level Pin Diagrams

图 18 shows the input structure for the logic-level pins STEP, DIR, nSLEEP, SDI, and SCLK.

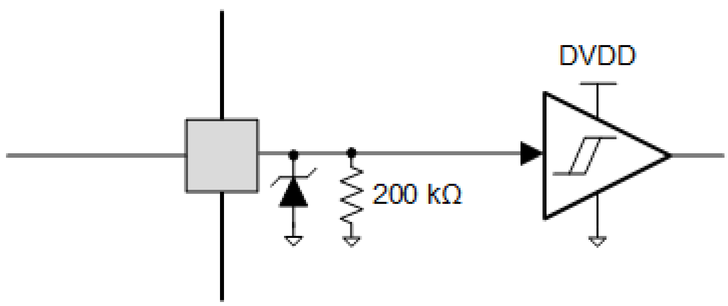

图 18. Logic-Level Input Pin Diagram

图 19 shows the input structure for the logic-level pins DRVOFF, and nSCS.

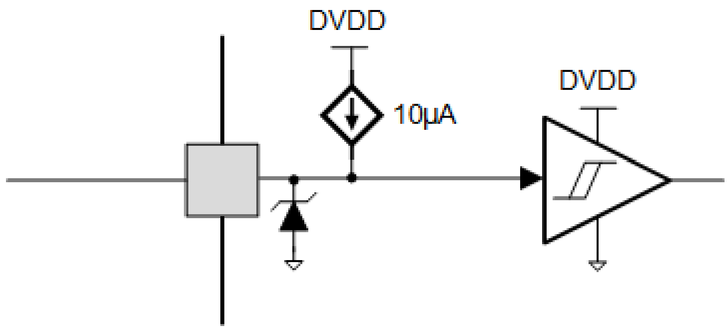

图 19. Logic-Level with Internal Pull-up Input Pin Diagram

7.3.10.1 nFAULT Pin

The nFAULT pin has an open-drain output and should be pulled up to a 5-V or 3.3-V supply. When a fault is detected, the nFAULT pin is logic low. nFAULT pin will be high after power-up. For a 5-V pullup, the nFAULT pin can be tied to the DVDD pin with a resistor. For a 3.3-V pullup, an external 3.3-V supply must be used.

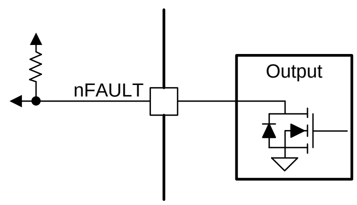

图 20. nFAULT Pin

7.3.11 Protection Circuits

The device is fully protected against supply undervoltage, charge pump undervoltage, output overcurrent, device overtemperature, and open load events.

It provides additional diagnostics in the form of stall detection.

7.3.11.1 VM Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the UVLO-threshold voltage, all the outputs are disabled, and the nFAULT pin is driven low. The charge pump is disabled in this condition. The FAULT and UVLO bits are latched high in the SPI registers. Normal operation resumes (motor-driver operation and nFAULT released) when the VM undervoltage condition is removed. The UVLO bit remains set until it is cleared through the CLR_FLT bit or an nSLEEP reset pulse. Additionally, after power-up, the UVLO bit is latched high in the SPI registers and remains set until it is cleared through the CLR_FLT bit or an nSLEEP reset pulse. SPI communication is available till the voltage on the VM pin falls below the V_{RST} voltage.

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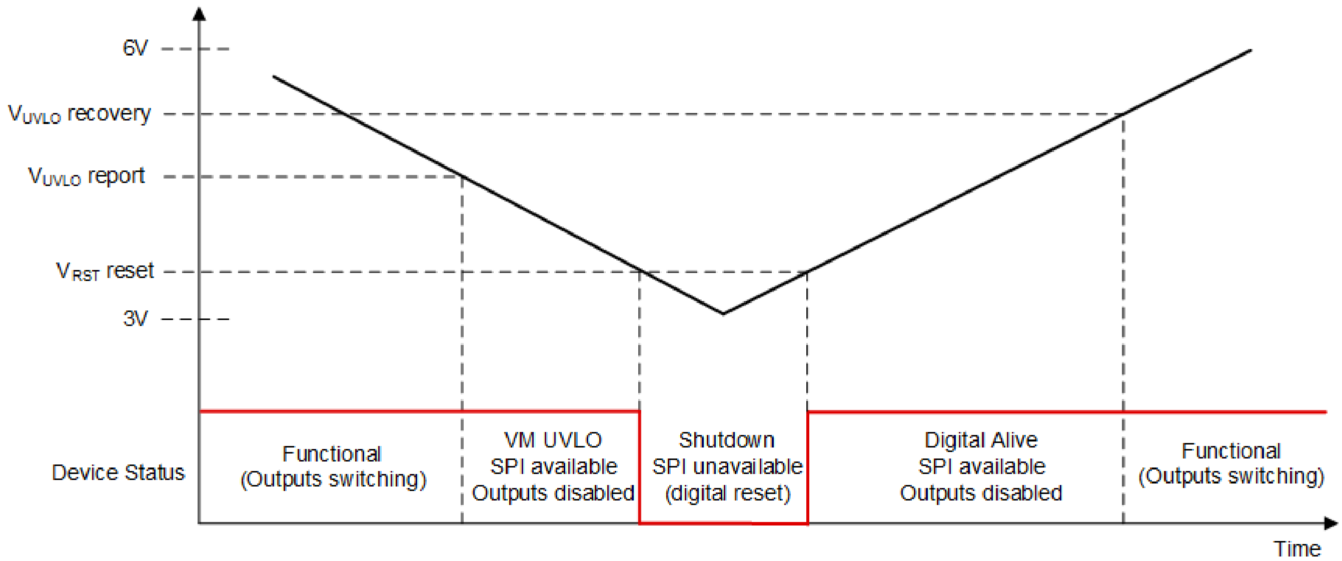

图 21. Supply Voltage Ramp Profile

7.3.11.2 VCP Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin falls below the CPUV voltage, all the outputs are disabled, and the nFAULT pin is driven low. The charge pump remains active during this condition. The FAULT and CPUV bits are latched high in the SPI registers. Normal operation resumes (motor-driver operation and nFAULT released) when the VCP undervoltage condition is removed. The CPUV bit remains set until it is cleared through the CLR_FLT bit or an nSLEEP reset pulse. Additionally, after power-up, the CPUV bit is latched high in the SPI registers and remains set until it is cleared through the CLR_FLT bit or an nSLEEP reset pulse.

Errata: On the prototype version samples, after power-up, the CPUV and UVLO bits are latched high in the SPI registers and remains set until it is cleared through the CLR_FLT bit or an nSLEEP reset pulse. This will be corrected when the final version samples are available.

7.3.11.3 Overcurrent Protection (OCP)

An analog current-limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the t_{OCP} time, all the FETs in the two bridges are disabled and the nFAULT pin is driven low. The FAULT and OCP bits are latched high in the SPI registers. For xOUTx to VM short, corresponding OCP_LSx_x bit goes high in the DIAG Status 1 register. Similarly, for xOUTx to ground short, corresponding OCP_HSx_x bit goes high. For example, for AOUT1 to VM short, OCP_LS1_A bit goes high; and for BOUT2 to ground short, the OCP_HS2_B bit goes high. The charge pump remains active during this condition. The overcurrent protection can operate in two different modes: latched shutdown and automatic retry.

7.3.11.3.1 Latched Shutdown (OCP_MODE = 0b)

In this mode, after an OCP event, all the outputs are disabled and the nFAULT pin is driven low. Normal operation resumes (motor-driver operation and nFAULT released) when the OCP condition is removed and a clear faults command has been issued either through the CLR_FLT bit or an nSLEEP reset pulse. This is the default mode for an OCP event for the device.

7.3.11.3.2 Automatic Retry (OCP_MODE = 1b)

In this mode, after an OCP event all the outputs (AOUTx and BOUTx) are disabled and the nFAULT pin is driven low. Normal operation resumes automatically (motor-driver operation and nFAULT released) after the t_{RETRY} time has elapsed and the fault condition is removed.

7.3.11.4 Open-Load Detection (OL)

If the motor is disconnected from the device while in motion, winding current drops below the open load current threshold (I_{OL}) and an open-load condition is detected. The EN_OL bit must be '1' to enable open load detection. When an open load fault is detected, the OL and FAULT bits are latched high in the SPI register and the nFAULT pin is driven low. Open load detection time is maximum 200 ms. If the OL_A bit is high, it indicates an open load fault in winding A, between AOUT1 and AOUT2. Similarly, an open load fault between BOUT1 and BOUT2 causes the OL_B bit to go high. Normal operation resumes and the nFAULT line is released when the open load condition is removed and a clear faults command has been issued either through the CLR_FLT bit or an nSLEEP reset pulse. The fault also clears when the device is power cycled or comes out of sleep mode.

Errata: On the prototype version samples, an OL fault is detected every time the device detects an OCP event. This will be corrected when the final version samples are available.

7.3.11.5 Stall Detection

Stepper motors have a distinct relation between the winding current, back-EMF, and mechanical torque load of the motor, as shown in 图 22. As motor load approaches the torque capability of the motor at a given winding current, the back-EMF will move in phase with the winding current. By detecting back-emf phase shift between rising and falling current quadrants of the motor current, the DRV8889-Q1 can detect a motor overload stall condition or an end-of-line travel.

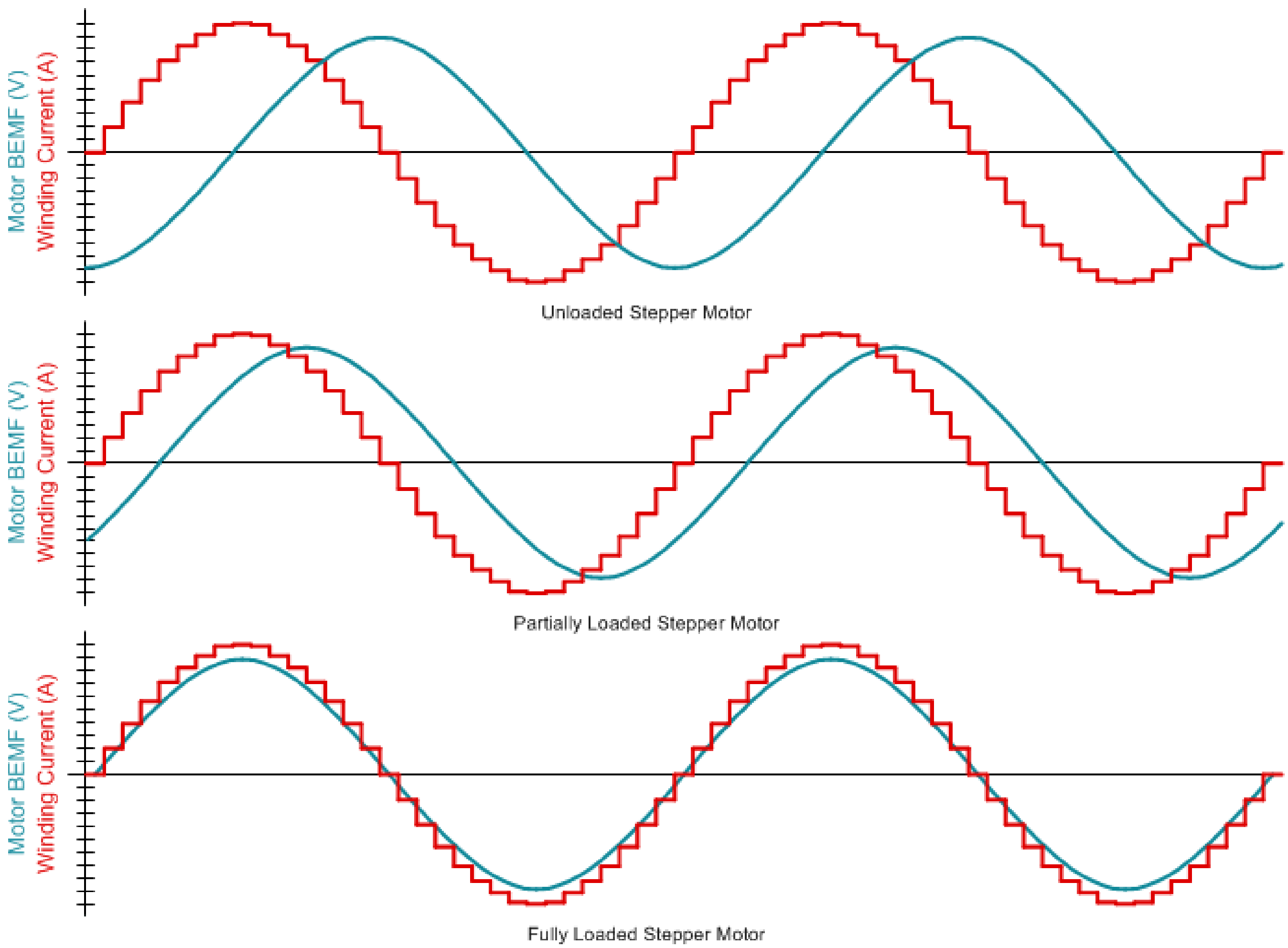

图 22. Stall Detection by Monitoring Motor Back-EMF

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The Stall Detection algorithm works only when the device is programmed to operate in the smart tune Ripple Control decay mode. The DIS_STL bit in CTRL5 register has to be '0' to enable stall detection. The algorithm compares the back-EMF between the rising and falling current quadrants by monitoring PWM off time and generates a value represented by the 8-bit register TRQ_COUNT. The comparison is done in such a way that the TRQ_COUNT value is practically independent of motor current, motor winding resistance, ambient temperature and supply voltage. Full step mode of operation is supported by this algorithm.

For a lightly loaded motor, the TRQ_COUNT will be a non-zero value. As the motor approaches stall condition, TRQ_COUNT will approach zero and can be used to detect stall condition. If anytime TRQ_COUNT falls below the stall threshold (represented by the 8-bit STALL_TH register), device will detect stall and the STALL, STL and FAULT bits are latched high in the SPI register. To indicate stall detection fault on the nFAULT pin, the STL_REP bit in CTRL5 register has to be '1'. When the STL_REP bit is '1', the nFAULT pin will be driven low when stall is detected. In stalled condition, the motor shaft does not spin. The motor starts to spin again when the stall condition is removed and the motor is ramped from zero speed to its target speed. The nFAULT line is released and the fault registers are cleared when a clear faults command has been issued either through the CLR_FLT bit or an nSLEEP reset pulse.

The TRQ_COUNT value is continuously averaged and it gets updated at the end of every half electrical cycle. At the most, it takes two electrical cycles to detect stall.

Stall threshold can be set in two ways – either user can write the STALL_TH bits, or let the algorithm learn the stall threshold value itself through the stall learning process. The stall learning process requires that the STL_LRN bit in CTRL5 register is '1' and the motor is deliberately stalled for some time to allow the algorithm to learn the ideal stall threshold. The process takes 16 electrical cycles and at the end of a successful learning, loads the STALL_TH register with the proper stall threshold bits. Also, the STL_LRN_OK bit goes high at the end of successful learning. It is recommended that users set the stall threshold using the stall learning process for proper stall detection. A stall threshold at one speed may not work well for another speed - therefore it is recommended to re-learn the stall threshold when the motor speed changes.

7.3.11.6 Thermal Shutdown (OTSD)

If the die temperature exceeds the thermal shutdown limit (T_{OTSD}) all MOSFETs in the H-bridge are disabled, and the nFAULT pin is driven low. The charge pump is disabled in this condition. In addition, the FAULT, TF and OTS bits are latched high. This protection feature cannot be disabled. The overtemperature protection can operate in two different modes: latched shutdown and automatic recovery.

7.3.11.6.1 Latched Shutdown (OTSD_MODE = 0b)

In this mode, after a OTSD event all the outputs are disabled and the nFAULT pin is driven low. The FAULT, TF and OTS bits are latched high in the SPI register. Normal operation resumes (motor-driver operation and the nFAULT line released) when the OTSD condition is removed and a clear faults command has been issued either through the CLR_FLT bit or an nSLEEP reset pulse. This mode is the default mode for a OTSD event.

7.3.11.6.2 Automatic Recovery (OTSD_MODE = 1b)

In this mode, after a OTSD event all the outputs are disabled and the nFAULT pin is driven low. The FAULT, TF and OTS bits are latched high in the SPI register. Normal operation resumes (motor-driver operation and the nFAULT line released) when the junction temperature falls below the overtemperature threshold limit minus the hysteresis (T_{OTSD} – T_{HYS_OTSD}). The FAULT, TF and OTS bits remains latched high indicating that a thermal event occurred until a clear faults command is issued either through the CLR_FLT bit or an nSLEEP reset pulse.

7.3.11.7 Overtemperature Warning (OTW)

If the die temperature exceeds the trip point of the overtemperature warning (T_{OTW}), the OTW and TF bits are set in the SPI register. The device performs no additional action and continues to function. When the die temperature falls below the hysteresis point (T_{HYS_OTW}) of the overtemperature warning, the OTW and TF bits clear automatically. The OTW bit can also be configured to report on the nFAULT pin, and set the FAULT bit in the device, by setting the TW_REP bit to 1b through the SPI registers. The charge pump remains active during this condition.

7.3.11.8 Undertemperature Warning (UTW)

If the die temperature falls below the trip point of the undertemperature warning (T_{UTW}), the UTW and TF bits are set in the SPI register. The device performs no additional action and continues to function. When the die temperature exceeds the hysteresis point (T_{HYS_UTW}) of the undertemperature warning, the UTW and TF bits clear automatically. The UTW bit can also be configured to report on the nFAULT pin, and set the FAULT bit in the device, by setting the TW_REP bit to 1b through the SPI registers. The charge pump remains active during this condition.

表 9. Fault Condition Summary

FAULT	CONDITION	CONFIGURATION	ERROR REPORT	H-BRIDGE	CHARGE PUMP	INDEXER	LOGIC	RECOVERY
VM undervoltage (UVLO)	VM < V_{UVLO} (max 4.4 V)	—	nFAULT / SPI	Disabled	Disabled	Disabled	Reset (V_{VM} < 3.9 V)	Automatic: VM > V_{UVLO} (max 4.5 V)
VCP undervoltage (CPUV)	VCP < V_{CPUV} (typ VM + 2.25 V)	—	nFAULT / SPI	Disabled	Operating	Operating	Operating	VCP > V_{CPUV} (typ VM + 2.7 V)
Overcurrent (OCP)	I_{OUT} > I_{OCP} (min 2.5 A)	OCP_MODE = 0b	nFAULT / SPI	Disabled	Operating	Operating	Operating	Latched: CLR_FLT / nSLEEP
		OCP_MODE = 1b	nFAULT / SPI	Disabled	Operating	Operating	Operating	Automatic retry: t_{RETRY}
Open Load (OL)	No load detected	EN_OL = 1b	nFAULT / SPI	Operating	Operating	Operating	Operating	Report only
Stall Detection (STALL)	Stall / stuck motor	STL_REP = 0b	SPI	Operating	Operating	Operating	Operating	No action
		STL_REP = 1b	nFAULT / SPI	Operating	Operating	Operating	Operating	Report only
Overtemperature Warning (OTW)	T_J > T_{OTW}	TW_REP = 1b	nFAULT / SPI	Operating	Operating	Operating	Operating	No action
		TW_REP = 0b	SPI	Operating	Operating	Operating	Operating	Automatic: T_J < T_{OTW} - T_{HYS_OTW}
Undertemperature Warning (UTW)	T_J < T_{UTW}	TW_REP = 1b	nFAULT / SPI	Operating	Operating	Operating	Operating	No action
		TW_REP = 0b	SPI	Operating	Operating	Operating	Operating	Automatic: T_J > T_{UTW} + T_{HYS_UTW}
Thermal Shutdown (OTSD)	T_J > T_{OTSD}	OTSD_MODE = 0b	nFAULT / SPI	Disabled	Disabled	Operating	Operating	Latched: CLR_FLT / nSLEEP
		OTSD_MODE = 1b	SPI	Disabled	Disabled	Operating	Operating	Automatic: T_J < T_{OTSD} - T_{HYS_OTSD}

7.4 Device Functional Modes

7.4.1 Sleep Mode (nSLEEP = 0)

The device state is managed by the nSLEEP pin. When the nSLEEP pin is low, the device enters a low-power sleep mode. In sleep mode, all the internal MOSFETs are disabled, the DVDD regulator is disabled, the charge pump is disabled, and the SPI is disabled. The t_{SLEEP} time must elapse after a falling edge on the nSLEEP pin before the device enters sleep mode. The device is brought out of sleep automatically if the nSLEEP pin is brought high. The t_{WAKE} time must elapse before the device is ready for inputs.

7.4.2 Disable Mode (nSLEEP = 1, DRVOFF = 1)

The DRVOFF pin is used to enable or disable the half bridge in the device. When the DRVOFF pin is high, the output drivers are disabled in the Hi-Z state.

7.4.3 Operating Mode (nSLEEP = 1, DRVOFF = 0)

When the nSLEEP pin is high, the DRVOFF pin is low, and VM > UVLO, the device enters the active mode. The t_{WAKE} time must elapse before the device is ready for inputs. In this mode, the charge pump and low-side gate regulator are enabled.

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Device Functional Modes (接下页)

7.4.4 nSLEEP Reset Pulse

In addition to the CLR_FLT bit in the SPI register, a latched fault can be cleared through a quick nSLEEP pulse. This pulse must be greater than the nSLEEP deglitch time of 5 µs and shorter than 20 µs. If nSLEEP is low for longer than 20 µs, the faults are cleared and the device may or may not shutdown, as shown in the timing diagram (see 图 23). This reset pulse resets any SPI faults and does not affect the status of the charge pump or other functional blocks.

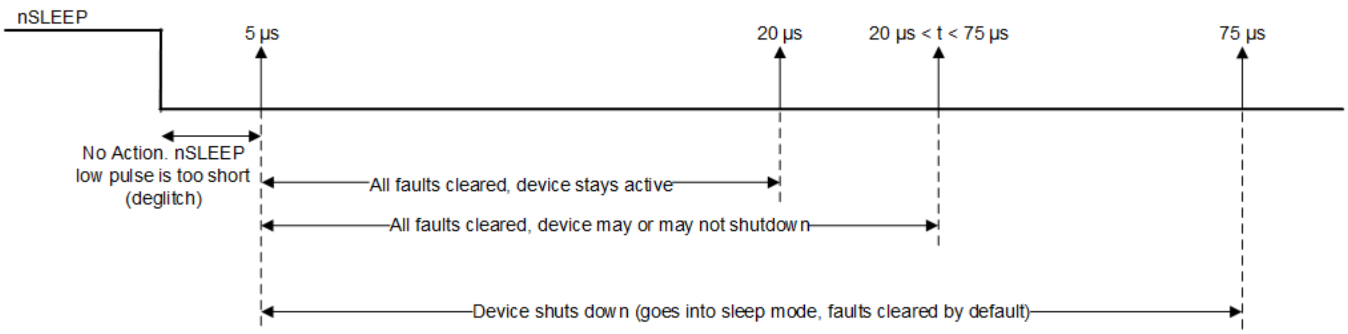

图 23. nSLEEP Reset Pulse

表 10 lists a summary of the functional modes.

表 10. Functional Modes Summary

CONDITION		CONFIGURATION	H-BRIDGE	DVDD Regulator	CHARGE PUMP	INDEXER	Logic
Sleep mode	4.5 V < VM < 45	nSLEEP pin = 0	Disabled	Disbaled	Disabled	Disabled	Disabled
Operating	4.5 V < VM < 45 V	nSLEEP pin = 1 DRVOFF pin = 0	Operating	Operating	Operating	Operating	Operating
Disabled	4.5 V < VM < 45 V	nSLEEP pin = 1 DRVOFF pin = 1	Disabled	Operating	Operating	Operating	Operating

7.5 Programming

7.5.1 Serial Peripheral Interface (SPI) Communication

The device SPI has full duplex, 4-wire synchronous communication. This section describes the SPI protocol, the command structure, and the control and status registers. The device can be connected with the MCU in the following configurations:

- One slave device
- Multiple slave devices in parallel connection
- Multiple slave devices in series (daisy chain) connection

7.5.1.1 SPI Format

The SDI input data word is 16 bits long and consists of the following format:

- 1 read or write bit, W (bit 14)
- 5 address bits, A (bits 13 through 9)
- 8 data bits, D (bits 7 through 0)

The SDO output-data word is 16 bits long and the first 8 bits make up the Status Register (S1). The Report word (R1) is the content of the register being accessed.

Programming (接下页)

For a write command (W0 = 0), the response word on the SDO pin is the data currently in the register being written to.

For a read command (W0 = 1), the response word is the data currently in the register being read.

表 11. SDI Input Data Word Format

	R/W	ADDRESS					DON'T CARE	DATA							
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	W0	A4	A3	A2	A1	A0	X	D7	D6	D5	D4	D3	D2	D1	D0

表 12. SDO Output Data Word Format

STATUS								REPORT							
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
1	1	UVLO	CPUV	OCP	STL	TF	OL	D7	D6	D5	D4	D3	D2	D1	D0

7.5.1.2 SPI for a Single Slave Device

The SPI is used to set device configurations, operating parameters, and read out diagnostic information. The SPI operates in slave mode. The SPI input-data (SDI) word consists of a 16-bit word, with 8 bits command and 8 bits of data. The SPI output data (SDO) word consists of 8 bits of status register with fault status indication and 8 bits of register data. 图 24 shows the data sequence between the MCU and the SPI slave driver.

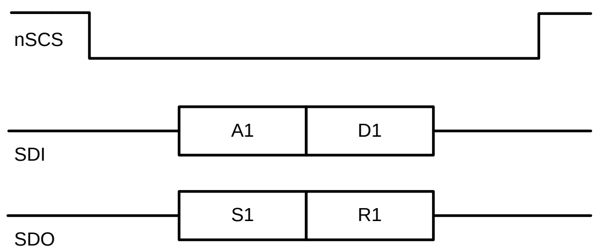

图 24. SPI Transaction Between MCU and the device

A valid frame must meet the following conditions:

- The SCLK pin must be low when the nSCS pin goes low and when the nSCS pin goes high.
- The nSCS pin should be taken high for at least 500 ns between frames.
- When the nSCS pin is asserted high, any signals at the SCLK and SDI pins are ignored, and the SDO pin is in the high-impedance state (Hi-Z).
- Full 16 SCLK cycles must occur.
- Data is captured on the falling edge of the clock and data is driven on the rising edge of the clock.
- The most-significant bit (MSB) is shifted in and out first.
- If the data word sent to SDI pin is less than 16 bits or more than 16 bits, a frame error occurs and the data word is ignored.
- For a write command, the existing data in the register being written to is shifted out on the SDO pin following the 8-bit command data.

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7.5.1.3 SPI for Multiple Slave Devices in Parallel Configuration

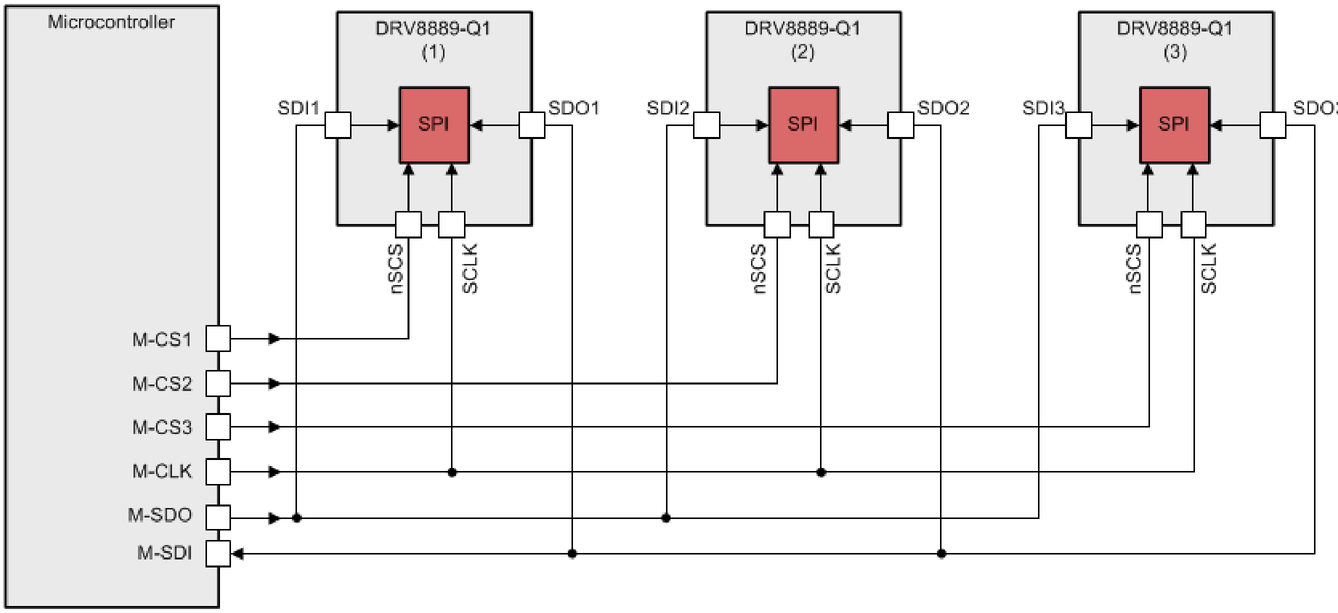

图 25. Three DRV8889-Q1 Devices Connected in Parallel Configuration

7.5.1.4 SPI for Multiple Slave Devices in Daisy Chain Configuration

The DRV8889-Q1 device can be connected in a daisy chain configuration to keep GPIO ports available when multiple devices are communicating to the same MCU. 图 26 shows the topology when three devices are connected in series.

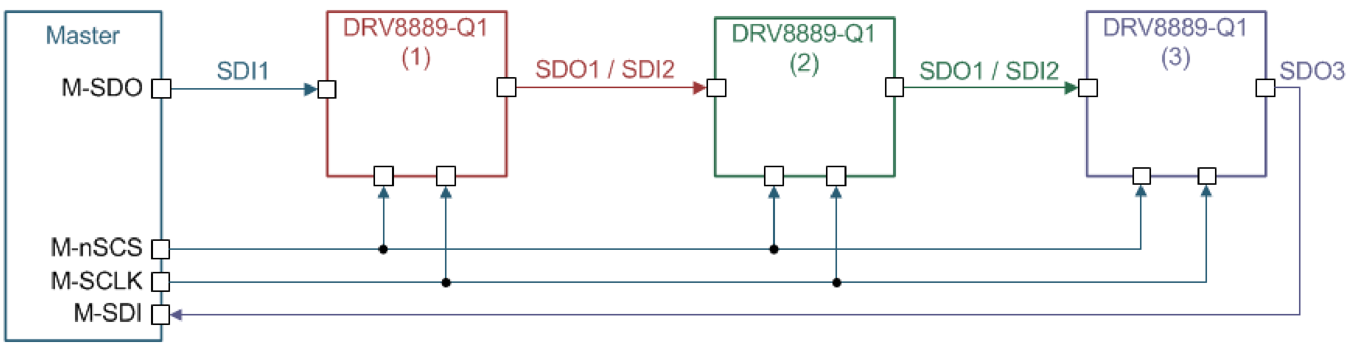

图 26. Three DRV8889-Q1 Devices Connected in Daisy Chain

The first device in the chain receives data from the MCU in the following format for 3-device configuration: 2 bytes of header (HDRx) followed by 3 bytes of address (Ax) followed by 3 bytes of data (Dx).

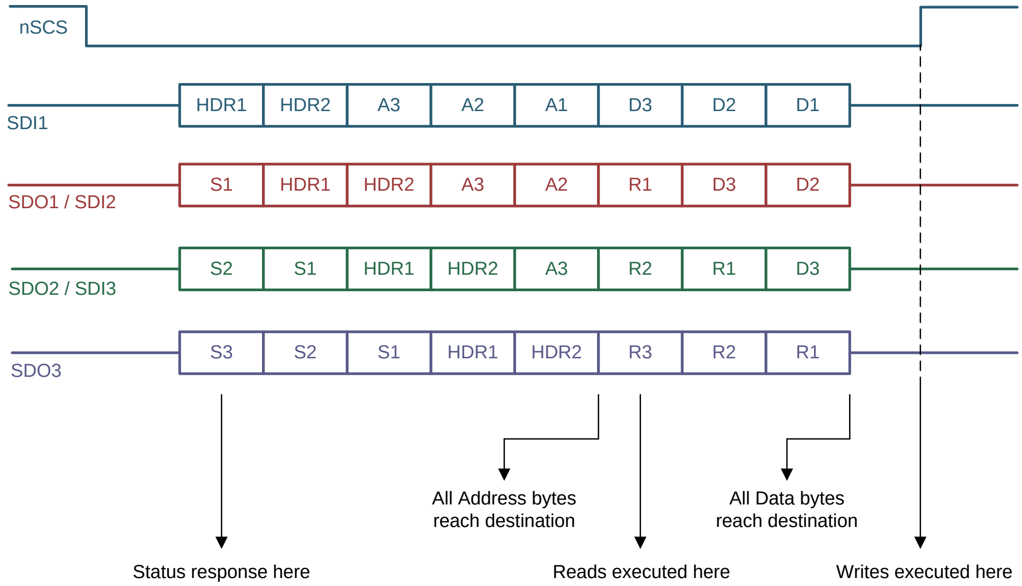

图 27. SPI Frame With Three Devices

After the data has been transmitted through the chain, the MCU receives the data string in the following format for 3-device configuration: 3 bytes of status (Sx) followed by 2 bytes of header followed by 3 bytes of report (Rx).

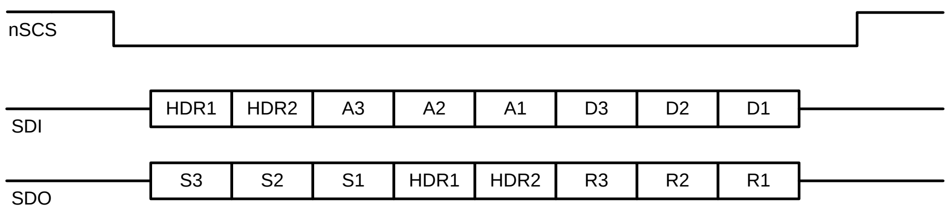

图 28. SPI Data Sequence for Three Devices

The header bytes contain information of the number of devices connected in the chain, and a global clear fault command that will clear the fault registers of all the devices on the rising edge of the chip select (nSCS) signal. Header values N5 through N0 are 6 bits dedicated to show the number of devices in the chain. Up to 63 devices can be connected in series for each daisy chain connection.

The 5 LSBs of the HDR2 register are don't care bits that can be used by the MCU to determine integrity of the daisy chain connection. Header bytes must start with 1 and 0 for the two MSBs.

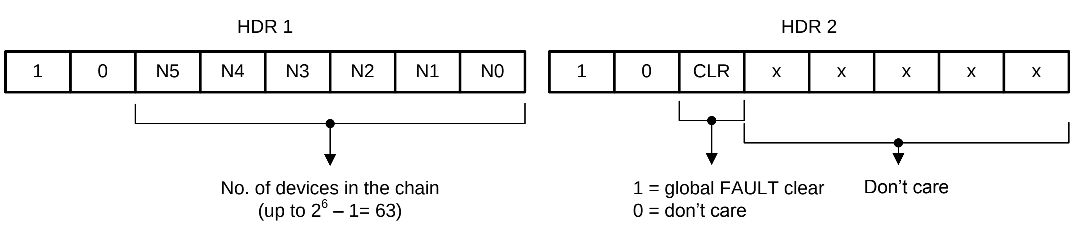

图 29. Header Bytes

The status byte provides information about the fault status register for each device in the daisy chain so that the MCU does not have to initiate a read command to read the fault status from any particular device. This keeps additional read commands for the MCU and makes the system more efficient to determine fault conditions flagged in a device. Status bytes must start with 1 and 1 for the two MSBs.

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Header Bytes (HDRx)	1	0	N5	N4	N3	N2	N1	N0
	1	0	CLR	X	X	X	X	X
Status Byte (Sx)	1	1	UVLO	CPUV	OCP	STL	TF	OL
Address Byte (Ax)	0	R/W	A4	A3	A2	A1	A0	X
Data Byte (Dx)	D7	D6	D5	D4	D3	D2	D1	D0

图 30. Contents of Header, Status, Address, and Data Bytes for DRV8889-Q1

When data passes through a device, it determines the position of itself in the chain by counting the number of status bytes it receives followed by the first header byte. For example, in this 3-device configuration, device 2 in the chain receives two status bytes before receiving the HDR1 byte which is then followed by the HDR2 byte.

From the two status bytes, the data can determine that its position is second in the chain. From the HDR2 byte, the data can determine how many devices are connected in the chain. In this way, the data only loads the relevant address and data byte in its buffer and bypasses the other bits. This protocol allows for faster communication without adding latency to the system for up to 63 devices in the chain.

The address and data bytes remain the same with respect to a 1-device connection. The report bytes (R1 through R3), as shown in 图 28, are the content of the register being accessed.

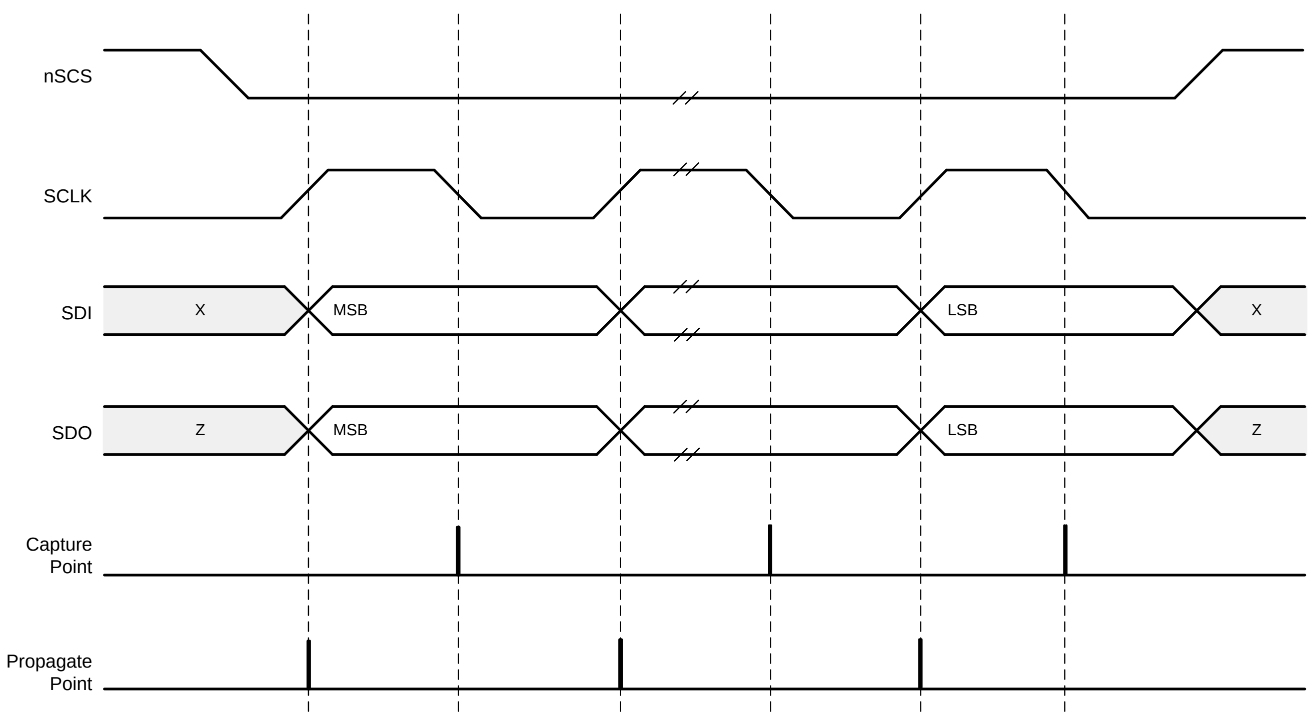

图 31. SPI Transaction

7.6 Register Maps

表 13 lists the memory-mapped registers for the DRV8889-Q1 device. All register addresses not listed in 表 13 should be considered as reserved locations and the register contents should not be modified.

表 13. Memory Map

Register Name	7	6	5	4	3	2	1	0	Access Type	Address
FAULT Status	FAULT	SPI_ERROR	UVLO	CPUV	OCP	STL	TF	OL	R	0x00
DIAG Status 1	OCP_LS2_B	OCP_HS2_B	OCP_LS1_B	OCP_HS1_B	OCP_LS2_A	OCP_HS2_A	OCP_LS1_A	OCP_HS1_A	R	0x01
DIAG Status 2	UTW	OTW	OTS	STL_LRN_OK	STALL	RSVD	OL_B	OL_A	R	0x02
CTRL1	TRQ_DAC [3:0]				RSVD		SLEW_RATE [1:0]		RW	0x03
CTRL2	DIS_OUT	RSVD		TOFF [1:0]		DECAY [2:0]			RW	0x04
CTRL3	DIR	STEP	SPI_DIR	SPI_STEP	MICROSTEP_MODE [3:0]				RW	0x05
CTRL4	CLR_FLT	LOCK [2:0]			EN_OL	OCP_MODE	OTSD_MODE	TW_REP	RW	0x06
CTRL5	RSVD		STL_LRN	DIS_STL	STL_REP	RSVD			RW	0x07
CTRL6	STALL_TH [7:0]								RW	0x08
CTRL7	TRQ_COUNT [7:0]								R	0x09

Complex bit access types are encoded to fit into small table cells. 表 14 shows the codes that are used for access types in this section.

表 14. Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

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7.6.1 Status Registers

The status registers are used to reporting warning and fault conditions. Status registers are read-only registers

表 15 lists the memory-mapped registers for the status registers. All register offset addresses not listed in 表 15 should be considered as reserved locations and the register contents should not be modified.

表 15. Status Registers Summary Table

Address	Register Name	Section
0x00	FAULT status	Go
0x01	DIAG status 1	Go
0x02	DIAG status 2	Go

7.6.1.1 FAULT Status Register Name (address = 0x00)

FAULT status is shown in 图 32 and described in 表 16.

FAULT status is shown in and described in .

Read-only

图 32. FAULT Status Register

7	6	5	4	3	2	1	0
FAULT	SPI_ERROR	UVLO	CPUV	OCP	STL	TF	OL
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 16. FAULT Status Register Field Descriptions

Bit	Field	Type	Default	Description
7	FAULT	R	0b	When nFAULT pin is at 1, FAULT bit is 0. When nFAULT pin is at 0, FAULT bit is 1.
6	SPI_ERROR	R	0b	Indicates SPI protocol errors, such as more SCLK pulses than are required or SCLK is absent even though nSCS is low. Becomes high in fault and the nFAULT pin is driven low. Normal operation resumes when the protocol error is removed and a clear faults command has been issued either through the CLR_FLT bit or an nSLEEP reset pulse.
5	UVLO	R	0b	Indicates an undervoltage lockout fault condition. Latched high after power-up, remains set until it is cleared through the CLR_FLT bit or an nSLEEP reset pulse.
4	CPUV	R	0b	Indicates charge pump undervoltage fault condition. Latched high after power-up, remains set until it is cleared through the CLR_FLT bit or an nSLEEP reset pulse.
3	OCP	R	0b	Indicates overcurrent fault condition
2	STL	R	0b	Indicates motor stall condition.
1	TF	R	0b	Logic OR of the overtemperature warning, undertemperature warning and overtemperature shutdown.
0	OL	R	0b	Indicates open-load condition.

7.6.1.2 DIAG Status 1 (address = 0x01)

DIAG Status 1 is shown in 图 33 and described in 表 17.

Read-only

图 33. DIAG Status 1 Register

7	6	5	4	3	2	1	0
OCP_LS2_B	OCP_HS2_B	OCP_LS1_B	OCP_HS1_B	OCP_LS2_A	OCP_HS2_A	OCP_LS1_A	OCP_HS1_A
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 17. DIAG Status 1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	OCP_LS2_B	R	0b	Indicates overcurrent fault on the low-side FET of half bridge 2 in BOUT
6	OCP_HS2_B	R	0b	Indicates overcurrent fault on the high-side FET of half bridge 2 in BOUT
5	OCP_LS1_B	R	0b	Indicates overcurrent fault on the low-side FET of half bridge 1 in BOUT
4	OCP_HS1_B	R	0b	Indicates overcurrent fault on the high-side FET of half bridge 1 in BOUT
3	OCP_LS2_A	R	0b	Indicates overcurrent fault on the low-side FET of half bridge 2 in AOUT
2	OCP_HS2_A	R	0b	Indicates overcurrent fault on the high-side FET of half bridge 2 in AOUT
1	OCP_LS1_A	R	0b	Indicates overcurrent fault on the low-side FET of half bridge 1 in AOUT
0	OCP_HS1_A	R	0b	Indicates overcurrent fault on the high-side FET of half bridge 1 in AOUT

7.6.1.3 DIAG Status 2 (address = 0x02)

DIAG Status 2 is shown in 图 34 and described in 表 18.

Read-only

图 34. DIAG Status 2 Register

7	6	5	4	3	2	1	0
UTW	OTW	OTS	STL_LRN_OK	STALL	RSVD	OL_B	OL_A
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 18. DIAG Status 2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	UTW	R	0b	Indicates undertemperature warning.
6	OTW	R	0b	Indicates overtemperature warning.
5	OTS	R	0b	Indicates overtemperature shutdown.
4	STL_LRN_OK	R	0b	Indicates stall detection learning is successful
3	STALL	R	0b	Indicates motor stall condition
2	RSVD	R	0b	Reserved.
1	OL_B	R	0b	Indicates open-load detection on BOUT
0	OL_A	R	0b	Indicates open-load detection on AOUT

7.6.2 Control Registers

The IC control registers are used to configure the device. Status registers are read and write capable.

表 19 lists the memory-mapped registers for the control registers. All register offset addresses not listed in 表 19 should be considered as reserved locations and the register contents should not be modified.

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表 19. Control Registers Summary Table

Address	Register Name	Section
0x03	CTRL1	Go
0x04	CTRL2	Go
0x05	CTRL3	Go
0x06	CTRL4	Go
0x07	CTRL5	Go
0x08	CTRL6	Go
0x09	CTRL7	Go

7.6.2.1 CTRL1 Control Register (address = 0x03)

CTRL1 control is shown in 图 35 and described in 表 20.

Read/Write

图 35. CTRL1 Control Register

7	6	5	4	3	2	1	0
TRQ_DAC [3:0]				RSVD		SLEW_RATE [1:0]	
R/W-0000b				R/W-00b		R/W-00b	

表 20. CTRL1 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-4	TRQ_DAC [3:0]	R/W	0000b	**0000b = 100%** 0001b = 93.75% 0010b = 87.5% 0011b = 81.25% 0100b = 75% 0101b = 68.75% 0110b = 62.5% 0111b = 56.25% 1000b = 50% 1001b = 43.75% 1010b = 37.5% 1011b = 31.25% 1100b = 25% 1101b = 18.75% 1110b = 12.5% 1111b = 6.25%
3-2	RSVD	R/W	00b	Reserved
1-0	SLEW_RATE [1:0]	R/W	00b	**00b = 10-V/µs** 01b = 35-V/µs 10b = 50-V/µs 11b = 105-V/µs

7.6.2.2 CTRL2 Control Register (address = 0x04)

CTRL2 is shown in 图 36 and described in 表 21.

Read/Write

图 36. CTRL2 Control Register

7	6	5	4	3	2	1	0
DIS_OUT	RSVD		TOFF [1:0]		DECAY [2:0]		
R/W-0b	R/W-00b		R/W-01b		R/W-111b		

表 21. CTRL2 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7	DIS_OUT	R/W	0b	Write '1' to Hi-Z all outputs. OR'ed with DRVOFF pin.
6-5	RSVD	R/W	00b	Reserved
4-3	TOFF [1:0]	R/W	01b	00b = 7 µs **01b = 16 µs** 10b = 24 µs 11b = 32 µs
2-0	DECAY [2:0]	R/W	111b	000b = Increasing SLOW, decreasing SLOW 001b = Increasing SLOW, decreasing MIXED 30% 010b = Increasing SLOW, decreasing MIXED 60% 011b = Increasing SLOW, decreasing FAST 100b = Increasing MIXED 30%, decreasing MIXED 30% 101b = Increasing MIXED 60%, decreasing MIXED 60% 110b = Smart tune Dynamic Decay **111b = Smart tune Ripple Control**

7.6.2.3 CTRL3 Control Register (address = 0x05)

CTRL3 is shown in 图 37 and described in 表 22.

Read/Write

图 37. CTRL3 Control Register

7	6	5	4	3	2	1	0
DIR	STEP	SPI_DIR	SPI_STEP	MICROSTEP_MODE [3:0]			
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0000b			

表 22. CTRL3 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7	DIR	R/W	0b	Direction input. Logic '1' sets the direction of stepping, when SPI_DIR = 1.
6	STEP	R/W	0b	Step input. Logic '1' causes the indexer to advance one step, when SPI_STEP = 1.
5	SPI_DIR	R/W	0b	**0b = Outputs follow input pin for DIR** 1b = Outputs follow SPI registers DIR
4	SPI_STEP	R/W	0b	**0b = Outputs follow input pin for STEP** 1b = Outputs follow SPI registers STEP

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表 22. CTRL3 Control Register Field Descriptions (接下页)

Bit	Field	Type	Default	Description
3-0	MICROSTEP_MODE [3:0]	R/W	0000b	**0000b = Full step (2-phase excitation) with 100% current** 0001b = Full step (2-phase excitation) with 71% current 0010b = Non-circular 1/2 step 0011b = 1/2 step 0100b = 1/4 step 0101b = 1/8 step 0110b = 1/16 step 0111b = 1/32 step 1000b = 1/64 step 1001b = 1/128 step 1010b = 1/256 step 1011b to 1111b = Reserved

Errata: On the prototype version samples, the STEP bit needs to be cleared after writing '1'. This will be corrected when the final version samples are available - the STEP bit will be self-clearing after a '1' has been written.

7.6.2.4 CTRL4 Control Register (address = 0x06)

CTRL4 is shown in 图 38 and described in 表 23.

Read/Write

图 38. CTRL4 Control Register

7	6	5	4	3	2	1	0
CLR_FLT	LOCK [2:0]			EN_OL	OCP_MODE	OTSD_MODE	TW_REP
R/W-0b	R/W-011b			R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 23. CTRL4 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7	CLR_FLT	R/W	0b	Write '1' to this bit to clear all latched fault bits. This bit automatically resets after being written.
6-4	LOCK [2:0]	R/W	011b	Write 110b to lock the settings by ignoring further register writes except to these bits and address 0x06h bit 7 (CLR_FLT). Writing any sequence other than 110b has no effect when unlocked. Write 011b to this register to unlock all registers. Writing any sequence other than 011b has no effect when locked.
3	EN_OL	R/W	0b	Write '1' to enable open load detection
2	OCP_MODE	R/W	0b	**0b = Overcurrent condition causes a latched fault** 1b = Overcurrent condition causes an automatic retrying fault
1	OTSD_MODE	R/W	0b	**0b = Overtemperature condition will cause latched fault** 1b = Overtemperature condition will cause automatic recovery fault
0	TW_REP	R/W	0b	**0b = Overtemperature or undertemperature warning is not reported on the nFAULT line** 1b = Overtemperature or undertemperature warning is reported on the nFAULT line

7.6.2.5 CTRL5 Control Register (address = 0x07)

CTRL5 control is shown in 图 39 and described in 表 24.

Read/Write

图 39. CTRL5 Control Register

7	6	5	4	3	2	1	0
RSVD		STL_LRN	DIS_STL	STL_REP	RSVD		
R/W-00b		R/W-0b	R/W-0b	R/W-1b	R/W-000b		

表 24. CTRL5 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	RSVD	R/W	00b	Reserved. Should always be '00'.
5	STL_LRN	R/W	0b	Write '1' to learn stall count for stall detection. This bit automatically returns to '0' when the stall learning process is complete.
4	DIS_STL	R/W	0b	**0b = Stall detection is enabled** 1b = Stall detection is disabled
3	STL_REP	R/W	1b	0b = Stall detection is not reported on nFAULT **1b = Stall detection is reported on nFAULT**
2-0	RSVD	R/W	0b	Reserved. Should always be '000'.

Errata: When the final version samples are available, the DIS_STL bit will be changed to EN_STL. Stall detection will be disabled by default, and the bit has to be '1' to enable stall detection.

7.6.2.6 CTRL6 Control Register (address = 0x08)

CTRL6 is shown in 图 40 and described in 表 25.

Read/Write

图 40. CTRL6 Control Register

7	6	5	4	3	2	1	0
STALL_TH [7:0]							
R/W-00001111b							

表 25. CTRL6 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	STALL_TH [7:0]	R/W	00001111b	00000000b = 0 count XXXXXXXXb = 1 to 254 counts 11111111b = 255 counts

7.6.2.7 CTRL7 Control Register (address = 0x09)

CTRL7 is shown in 图 41 and described in 表 26.

Read-only

图 41. CTRL7 Control Register

7	6	5	4	3	2	1	0
TRQ_COUNT [7:0]							
R-11111111b							

表 26. CTRL7 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	TRQ_COUNT [7:0]	R	11111111b	**00000000b = 0 count** XXXXXXXXb = 1 to 254 counts 11111111b = 255 counts

ADVANCE INFORMATION

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8889-Q1 device is used in bipolar stepper control.

8.2 Typical Application

The following design procedure can be used to configure the DRV8889-Q1 device.

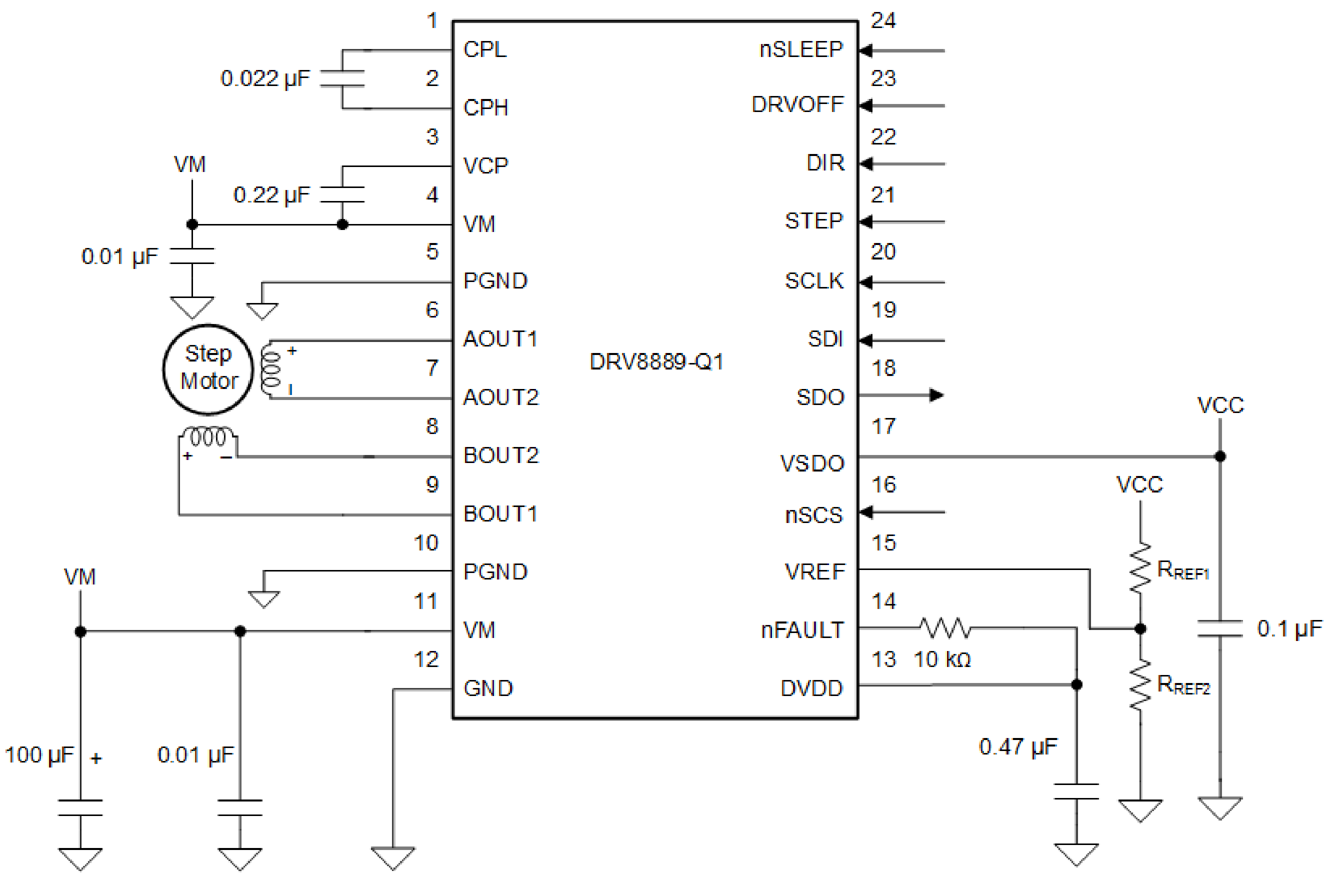

图 42. Typical Application Schematic (HTSSOP package)

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Typical Application (接下页)

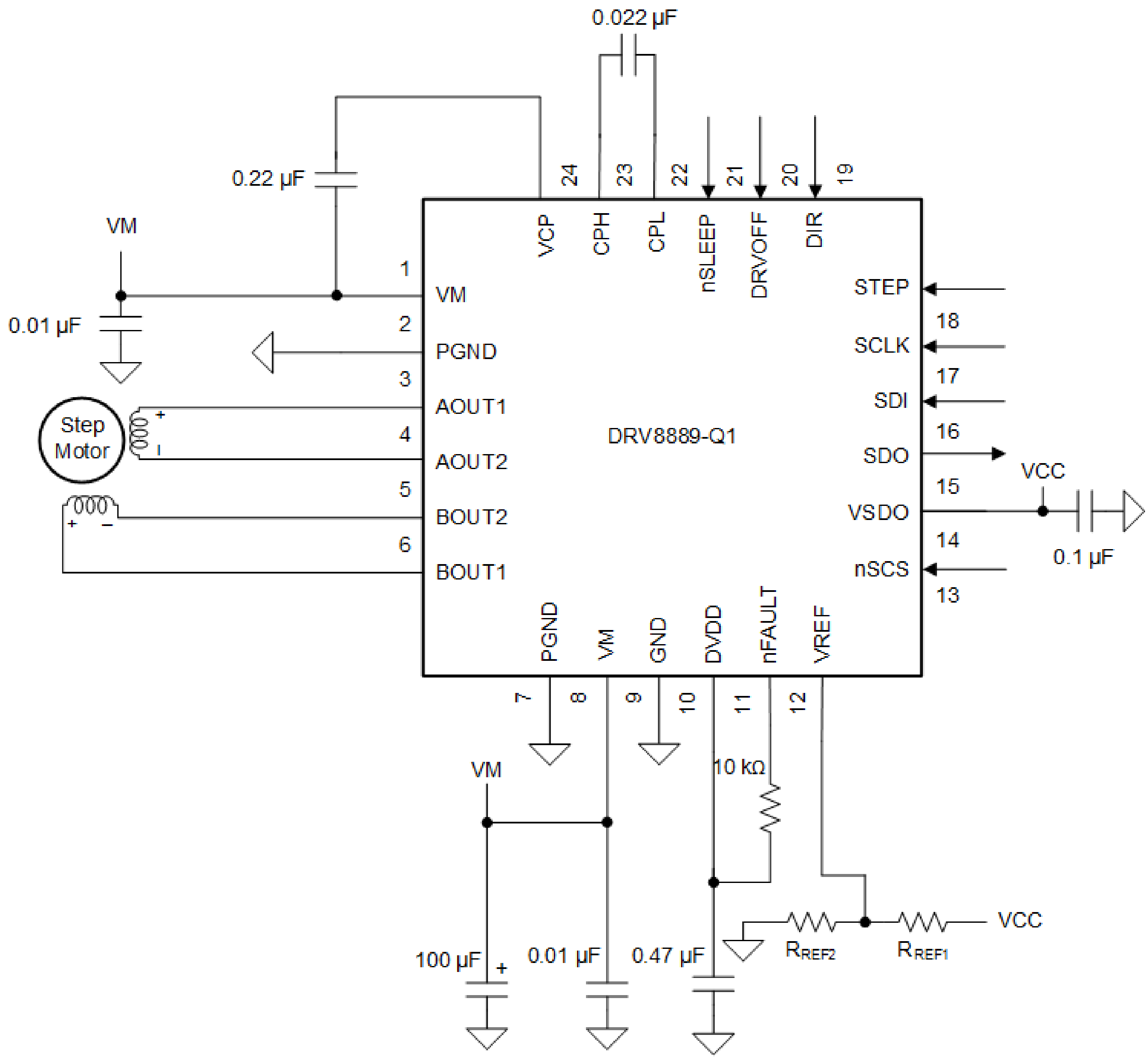

图 43. Typical Application Schematic (VQFN package)

8.2.1 Design Requirements

表 27 lists the design input parameters for system design.

表 27. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	VM	13.5 V
Motor winding resistance	R_L	2.6 Ω/phase
Motor winding inductance	L_L	1.4 mH/phase
Motor full step angle	θ_{step}	1.8°/step
Target microstepping level	n_m	1/8 step

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表 27. Design Parameters (接下页)

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Target motor speed	v	120 rpm
Target full-scale current	I_{FS}	1.5 A

8.2.2 Detailed Design Procedure

8.2.2.1 Stepper Motor Speed

The first step in configuring the device requires the desired motor speed and microstepping level. If the target application requires a constant speed, then a square wave with frequency f_{step} must be applied to the STEP pin. If the target motor speed is too high, the motor does not spin. Make sure that the motor can support the target speed.

Use 公式 2 to calculate f_{step} for a desired motor speed (v), microstepping level (n_m), and motor full step angle (θ_{step})

$$f_{step}\ (\text{steps / s}) = \frac{v\ (\text{rpm}) \times 360\ (° / \text{rot})}{\theta_{step}\ (° / \text{step}) \times n_m\ (\text{steps / microstep}) \times 60\ (\text{s / min})} \tag{2}$$

The value of θ_{step} can be found in the stepper motor data sheet, or written on the motor.

For the DRV8889-Q1 device, the microstepping level is set by the MICROSTEP_MODE bits in the SPI register and can be any of the settings listed in 表 28. Higher microstepping results in a smoother motor motion and less audible noise, but increases switching losses and requires a higher f_{step} to achieve the same motor speed.

表 28. Microstepping Indexer Settings

MICROSTEP_MODE	STEP MODE
0000b	Full step (2-phase excitation) with 100% current
0001b	Full step (2-phase excitation) with 71% current
0010b	Non-circular 1/2 step
0011b	1/2 step
0100b	1/4 step
0101b	1/8 step
0110b	1/16 step
0111b	1/32 step
1000b	1/64 step
1001b	1/128 step
1010b	1/256 step

For example, the motor is 1.8°/step for a target of 120 rpm at 1/8 microstep mode.

$$f_{step}\ (\text{steps / s}) = \frac{120\ \text{rpm} \times 360° / \text{rot}}{1.8° / \text{step} \times 1/8\ \text{steps / microstep} \times 60\ \text{s / min}} = 3.2\ \text{kHz} \tag{3}$$

8.2.2.2 Current Regulation

In a stepper motor, the full-scale current (I_{FS}) is the maximum current driven through either winding. This quantity depends on the VREF voltage and the TRQ setting.

The maximum allowable voltage on the VREF pin is 3.3 V. DVDD can be used to provide VREF through a resistor divider.

During stepping, I_{FS} defines the current chopping threshold (I_{TRIP}) for the maximum current step.

$$I_{FS}\ (A) = \frac{V_{REF}\ (V)}{K_V\ (V/A)} \times TRQ\_DAC\ (\%) = \frac{V_{REF}\ (V) \times TRQ\_DAC\ (\%)}{2.2\ (V/A)} \tag{4}$$

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注

The I_{FS} current must also follow 公式 4 to avoid saturating the motor. VM is the motor supply voltage, and R_L is the motor winding resistance.

$$I_{FS}\ (A) < \frac{VM\ (V)}{R_L\ (\Omega) + 2 \times R_{DS(ON)}\ (\Omega)} \tag{5}$$

8.2.2.3 Decay Modes

The device supports eight different decay modes, as shown in 表 7. The current through the motor windings is regulated using an adjustable fixed-time-off scheme which means that after any drive phase, when a motor winding current has hit the current chopping threshold (I_{TRIP}), the device places the winding in one of the eight decay modes for t_{OFF}. After t_{OFF}, a new drive phase starts.

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9 Power Supply Recommendations

The device is designed to operate from an input voltage supply (VM) range from 4.5 V to 45 V. A 0.01-µF ceramic capacitor rated for VM must be placed at each VM pin as close to the device as possible. In addition, a bulk capacitor must be included on VM.

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

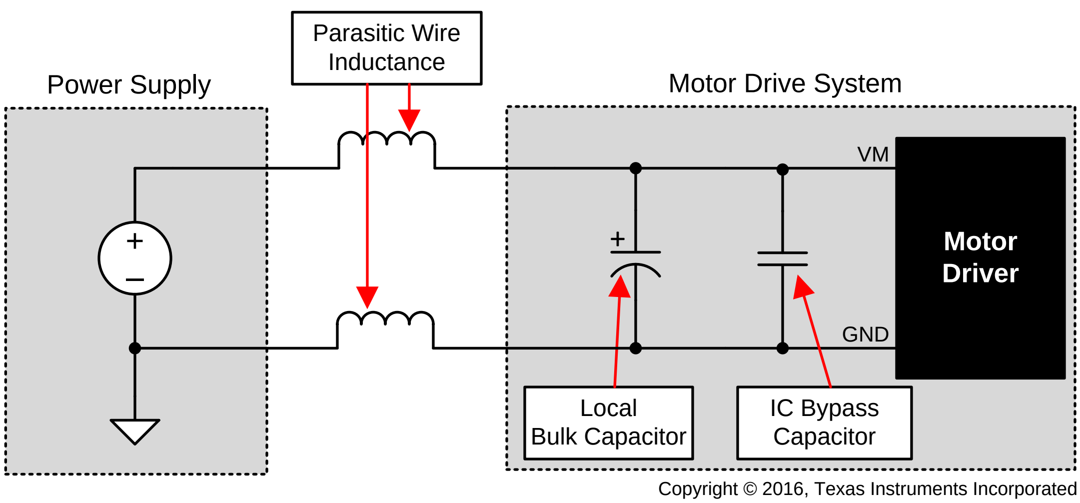

图 44. Example Setup of Motor Drive System With External Power Supply

10 Layout

10.1 Layout Guidelines

The VM pin should be bypassed to GND using a low-ESR ceramic bypass capacitor with a recommended value of 0.01 µF rated for VM. This capacitor should be placed as close to the VM pin as possible with a thick trace or ground plane connection to the device GND pin.

The VM pin must be bypassed to ground using a bulk capacitor rated for VM. This component can be an electrolytic capacitor.

A low-ESR ceramic capacitor must be placed in between the CPL and CPH pins. A value of 0.022 µF rated for VM is recommended. Place this component as close to the pins as possible.

A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. A value of 0.22 µF rated for 16 V is recommended. Place this component as close to the pins as possible.

Bypass the DVDD pin to ground with a low-ESR ceramic capacitor. A value of 0.47 µF rated for 6.3 V is recommended. Place this bypassing capacitor as close to the pin as possible.

The thermal PAD must be connected to system ground.

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10.2 Layout Example

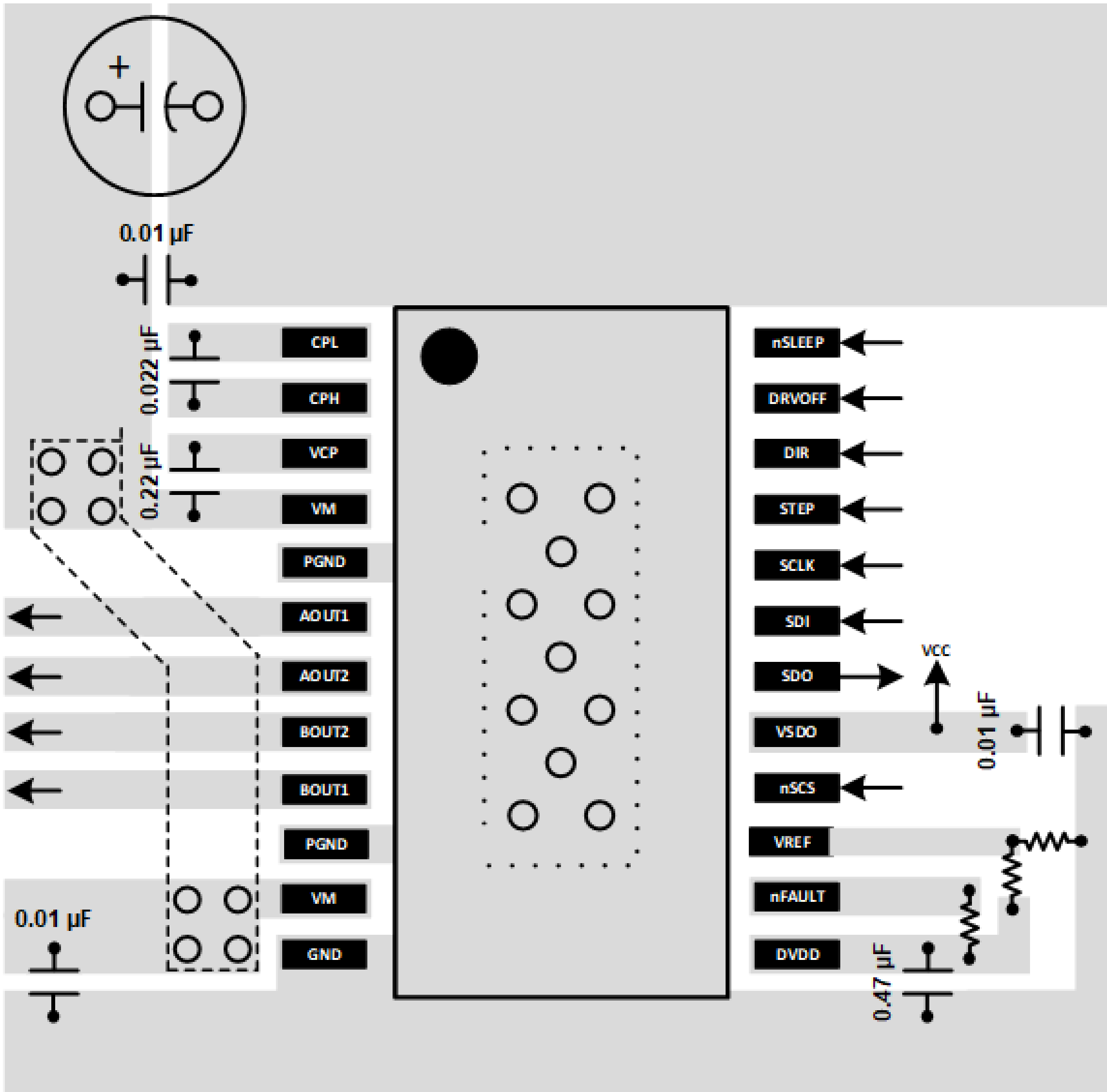

图 45. HTSSOP Layout Recommendation

ADVANCE INFORMATION

Layout Example (接下页)

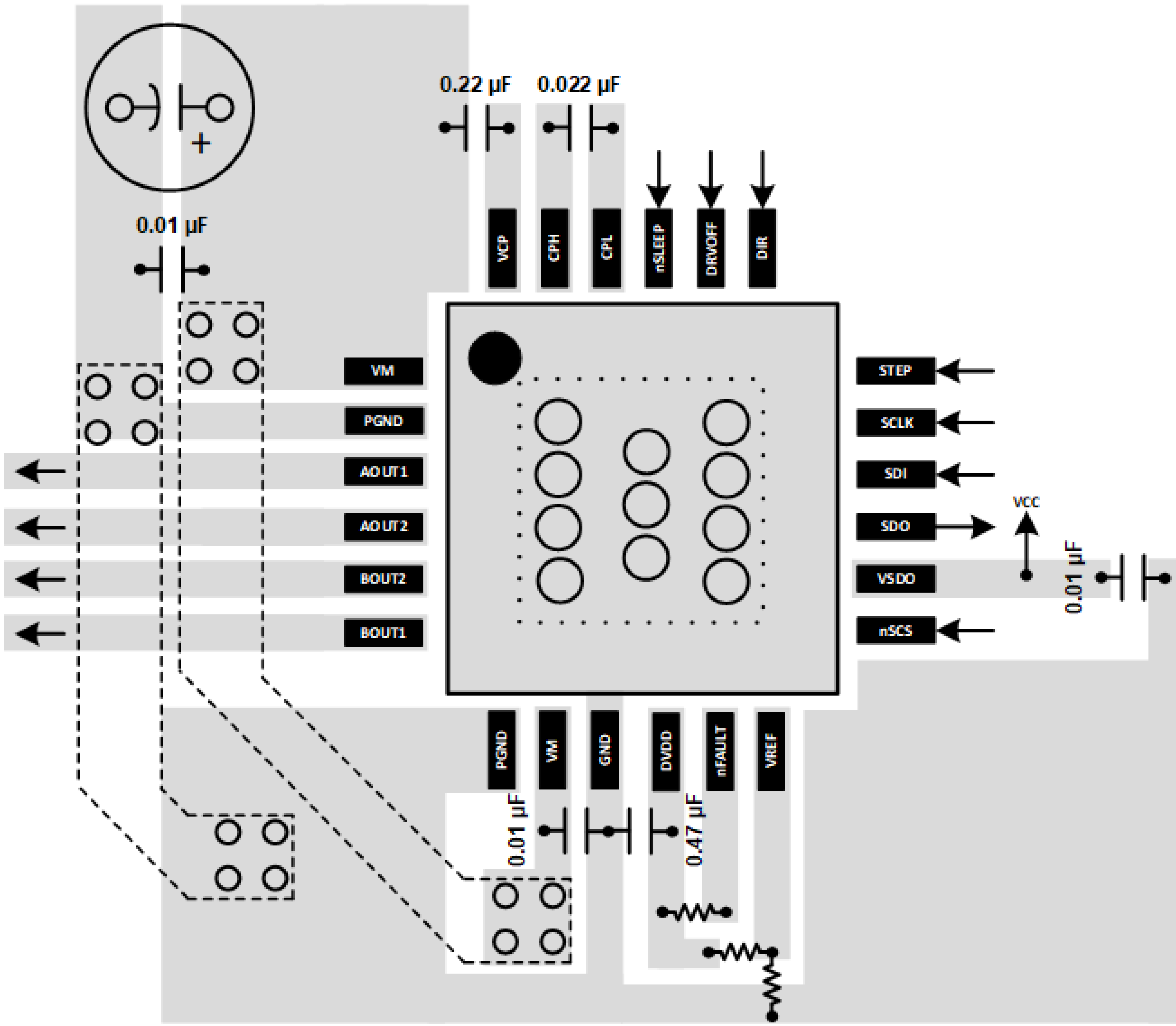

图 46. QFN Layout Recommendation

ADVANCE INFORMATION

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《计算电机驱动器的功耗》*应用报告
- 德州仪器 (TI)，*《电流再循环和衰减模式》*应用报告
- 德州仪器 (TI)，*《AutoTune™ 如何调节步进电机中的电流》* 白皮书
- 德州仪器 (TI)，*《工业电机驱动解决方案指南》*
- 德州仪器 (TI)，*《PowerPAD™ 速成》*应用报告
- 德州仪器 (TI)，*《PowerPAD™ 热增强型封装》*应用报告
- 德州仪器 (TI)，*《使用 AutoTune™ 轻松实现步进电机》* 白皮书
- 德州仪器 (TI)，*《了解电机驱动器电流额定值》*应用报告

11.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商标

E2E is a trademark of Texas Instruments.

11.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

有关器件的机械、封装和可订购信息，请参阅数据表的*机械、封装和可订购信息*部分，此数据表可在 DRV8889-Q1 产品文件夹中找到。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8889QWRGERQ1	PREVIEW	VQFN	RGE	24	3000	TBD	Call TI	Call TI	-40 to 125		
PDRV8889QPWPRQ1	ACTIVE	HTSSOP	PWP	24	2000	TBD	Call TI	Call TI	-40 to 125		Samples
PDRV8889QWRGERQ1	ACTIVE	VQFN	RGE	24	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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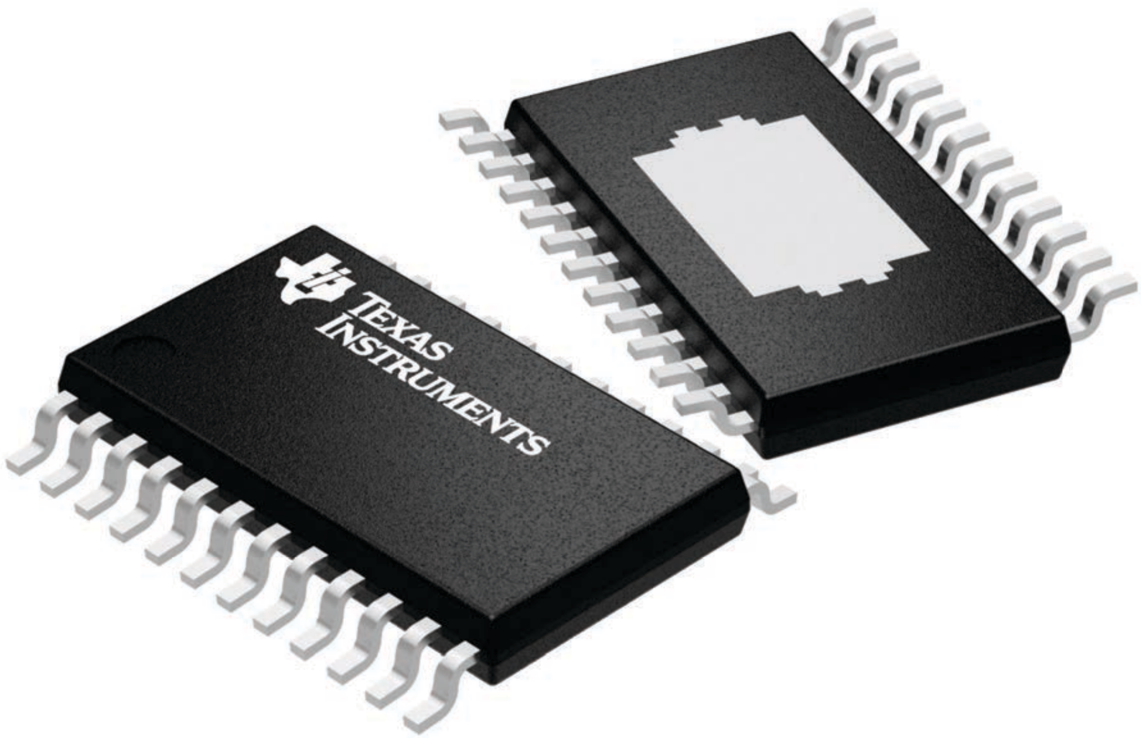
PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 7.6, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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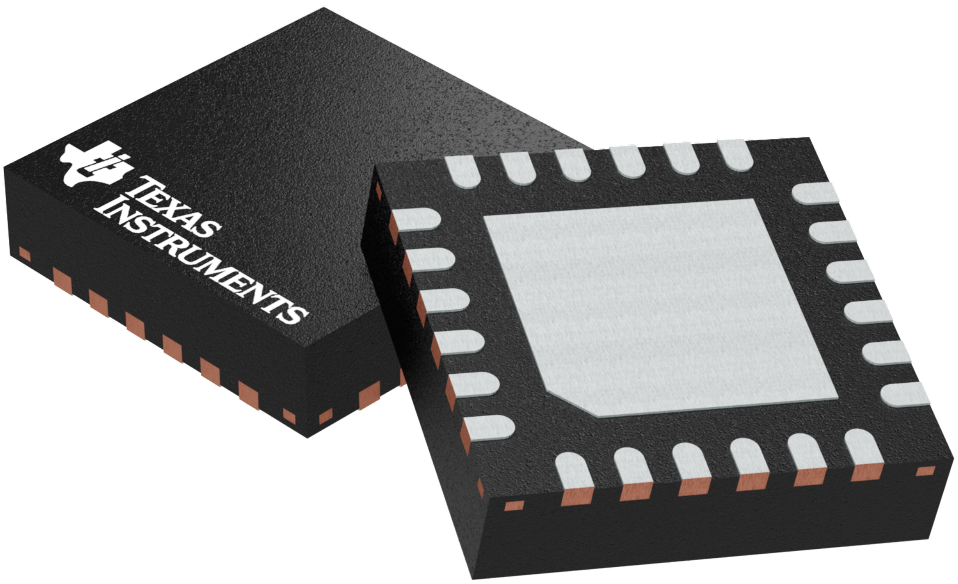

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