



TPS543x 3-A, Wide Input Range, Step-Down Converter

1 Features

- Wide Input Voltage Range:
 - TPS5430: 5.5 V to 36 V
 - TPS5431: 5.5 V to 23 V
- Up to 3-A Continuous (4-A Peak) Output Current
- High Efficiency up to 95% Enabled by 110-mΩ Integrated MOSFET Switch
- Wide Output Voltage Range: Adjustable Down to 1.22 V with 1.5% Initial Accuracy
- Internal Compensation Minimizes External Parts Count
- Fixed 500 kHz Switching Frequency for Small Filter Size
- Improved Line Regulation and Transient Response by Input Voltage Feed Forward
- System Protected by Overcurrent Limiting, Overvoltage Protection and Thermal Shutdown
- –40°C to 125°C Operating Junction Temperature Range
- Available in Small Thermally Enhanced 8-Pin SO PowerPAD™ Package

2 Applications

- Consumer: Set-top Box, DVD, LCD Displays
- Industrial and Car Audio Power Supplies
- Battery Chargers, High Power LED Supply
- 12-V/24-V Distributed Power Systems

3 Description

The TPS543x is a high-output-current PWM converter that integrates a low-resistance, high-side N-channel MOSFET. Included on the substrate with the listed features are a high-performance voltage error amplifier that provides tight voltage regulation accuracy under transient conditions; an undervoltage-lockout circuit to prevent start-up until the input voltage reaches 5.5 V; an internally set slow-start circuit to limit inrush currents; and a voltage feed-forward circuit to improve the transient response. Using the ENA pin, shutdown supply current is reduced to 18 μ A typically. Other features include an active-high enable, overcurrent limiting, over-voltage protection and thermal shutdown. To reduce design complexity and external component count, the TPS543x feedback loop is internally compensated. The TPS5431 is intended to operate from power rails up to 23 V. The TPS5430 regulates a wide variety of power sources including 24 V bus.

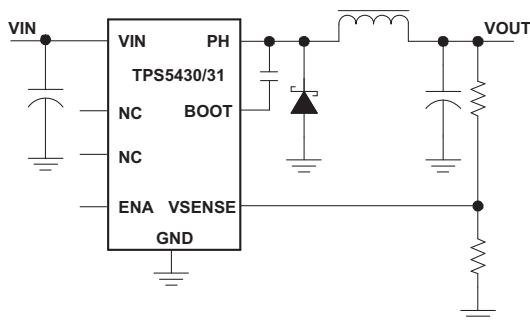
The TPS543x device is available in a thermally enhanced, easy to use 8-pin SOIC PowerPAD™ package. TI provides evaluation modules and the Designer software tool to aid in quickly achieving high-performance power supply designs to meet aggressive equipment development cycles.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	INPUT VOLTAGE
TPS5430	HSOP (8)	5.5 V to 36 V
TPS5431		5.5 V to 23 V

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



Efficiency vs Output Current

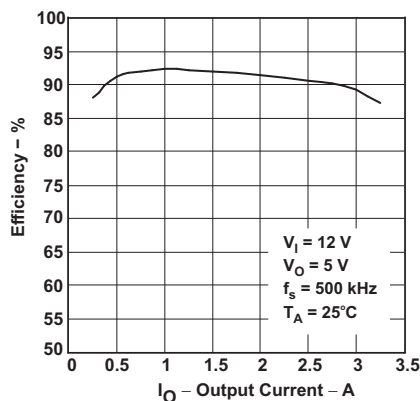


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4 Revision History

Changes from Revision G (February 2015) to Revision H	Page
• Deleted "Recommended Land Pattern" figure from core data sheet. New drawings are furnished in the <i>Mechanical, Packaging, and Orderable Information</i> section.	26
Changes from Revision F (December 2014) to Revision G	Page
• Fixed typo error TPS5430x to TPS513x	1
Changes from Revision E (September 2013) to Revision F	Page
• Added <i>ESD Rating</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	3
Changes from Revision D (January 2013) to Revision E	Page
• Deleted SWIFT from the data sheet Title, Features, and Description	1
Changes from Revision C (November 2006) to Revision D	Page
• Replaced the DISSIPATION RATINGS with the THERMAL INFORMATION table	4
Changes from Revision B (August 2006) to Revision C	Page
• Changed the Efficiency vs Output Current graph	1
• Changed the FUNCTIONAL BLOCK DIAGRAM	9
• Added the Circuit Using Ceramic Output Filter Capacitors section	23

Changes from Revision A (March 2006) to Revision B

Page

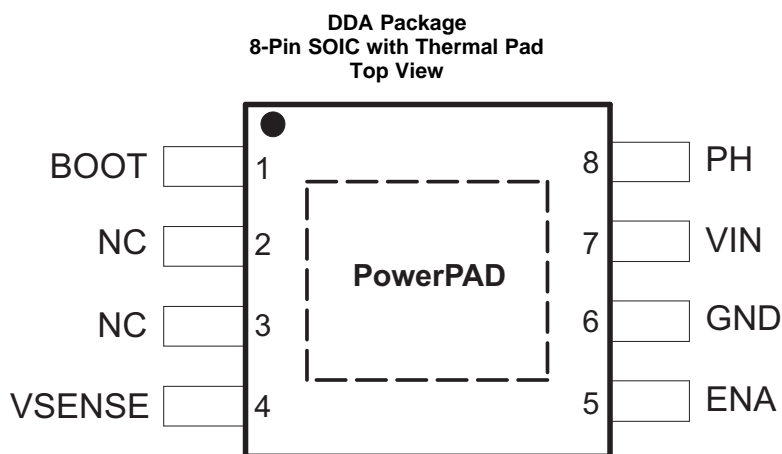
- Added Note 3 to the ABSOLUTE MAXIMUM RATINGS table..... **3**

Changes from Original (January 2006) to Revision A

Page

- Added Added device number TPS5431 **1**
- Changed [Figure 17](#) **21**
- Added [Figure 18](#) **22**

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	1	O	Boost capacitor for the high-side FET gate driver. Connect 0.01 μ F low ESR capacitor from BOOT pin to PH pin.
NC	2, 3	—	Not connected internally.
VSENSE	4	I	Feedback voltage for the regulator. Connect to output voltage divider.
ENA	5	I	On/off control. Below 0.5 V, the device stops switching. Float the pin to enable.
GND	6	—	Ground. Connect to PowerPAD.
VIN	7	—	Input supply voltage. Bypass VIN pin to GND pin close to device package with a high quality, low ESR ceramic capacitor.
PH	8	I	Source of the high side power MOSFET. Connected to external inductor and diode.
PowerPAD		—	GND pin must be connected to the exposed pad for proper operation.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾⁽²⁾

				MIN	MAX	UNIT
V _I	Input voltage range	TPS5430	VIN	−0.3	40 ⁽³⁾	V
			PH (steady-state)	−0.6	40 ⁽³⁾	
	TPS5431	VIN	−0.3	25		
		PH (steady-state)	−0.6	25		
		ENA	−0.3	7		
		BOOT-PH	−0.3	10		
		VSENSE	−0.3	3		
		PH (transient < 10 ns)	−1.2			
I _O	Source current	PH		Internally Limited		
I _{lkg}	Leakage current	PH		10		
T _J	Operating virtual junction temperature range			−40	150	°C
T _{stg}	Storage temperature range			−65	150	°C

- (1) Stresses beyond those listed under [Absolute Maximum Ratings](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.
- (3) Approaching the absolute maximum rating for the VIN pin may cause the voltage on the PH pin to exceed the absolute maximum rating.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
VIN	Input voltage range	TPS5430	5.5	36	V
		TPS5431	5.5	23	
T _J	Operating junction temperature		–40	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾⁽²⁾⁽³⁾		TPS5430 TPS5431	UNIT
		DDA	
		8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance (2-layer custom board) ⁽⁴⁾	33	°C/W
R _{θJA}	Junction-to-ambient thermal resistance (4-layer custom board) ⁽⁵⁾	26	
R _{θJA}	Junction-to-ambient thermal resistance (standard board)	42.3	
Ψ _{JT}	Junction-to-top characterization parameter	4.9	
Ψ _{JB}	Junction-to-board characterization parameter	20.7	
R _{θJC(top)}	Junction-to-case(top) thermal resistance	46.4	
R _{θJC(bottom)}	Junction-to-case(bottom) thermal resistance	0.8	
R _{θJB}	Junction-to-board thermal resistance	20.8	

- (1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, [SPRA953](#).
- (2) Maximum power dissipation may be limited by overcurrent protection
- (3) Power rating at a specific ambient temperature T_A should be determined with a junction temperature of 125°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and long-term reliability. See *Thermal Calculations* in applications section of this data sheet for more information.
- (4) Test boards conditions:
 - (a) 3 in x 3 in, 2 layers, thickness: 0.062 inch.
 - (b) 2 oz. copper traces located on the top and bottom of the PCB.
 - (c) 6 thermal vias in the PowerPAD area under the device package.
- (5) Test board conditions:
 - (a) 3 in x 3 in, 4 layers, thickness: 0.062 inch.
 - (b) 2 oz. copper traces located on the top and bottom of the PCB.
 - (c) 2 oz. copper ground planes on the 2 internal layers.
 - (d) 6 thermal vias in the PowerPAD area under the device package.

TPS5430, TPS5431

SLVS632H – JANUARY 2006 – REVISED APRIL 2016

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6.5 Electrical Characteristics
 $T_J = -40^{\circ}\text{C}$ to 125°C , $V_{IN} = 12\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
I _Q	Quiescent current	VSENSE = 2 V, Not switching, PH pin open		3	4.4	mA
		Shutdown, ENA = 0 V		18	50	μA
UNDERVOLTAGE LOCK OUT (UVLO)						
	Start threshold voltage, UVLO			5.3	5.5	V
	Hysteresis voltage, UVLO			330		mV
VOLTAGE REFERENCE						
	Voltage reference accuracy	T _J = 25°C	1.202	1.221	1.239	V
		I _O = 0 A – 3 A	1.196	1.221	1.245	
OSCILLATOR						
	Internally set free-running frequency		400	500	600	kHz
	Minimum controllable on time			150	200	ns
	Maximum duty cycle		87%	89%		
ENABLE (ENA PIN)						
	Start threshold voltage, ENA				1.3	V
	Stop threshold voltage, ENA		0.5			V
	Hysteresis voltage, ENA			450		mV
	Internal slow-start time (0~100%)		6.6	8	10	ms
CURRENT LIMIT						
	Current limit		4	5	6	A
	Current limit hiccup time		13	16	20	ms
THERMAL SHUTDOWN						
	Thermal shutdown trip point		135	162		°C
	Thermal shutdown hysteresis			14		
OUTPUT MOSFET						
r _{DS(on)}	High-side power MOSFET switch	VIN = 5.5 V		150		mΩ
				110	230	

6.6 Typical Characteristics

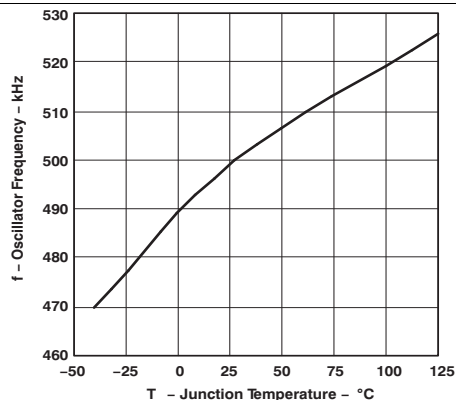


Figure 1. Oscillator Frequency vs. Junction Temperature

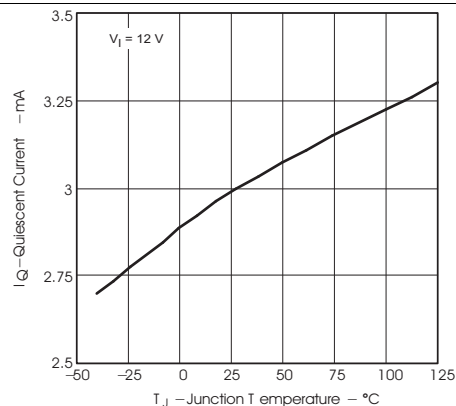


Figure 2. Non-Switching Quiescent Current vs. Junction Temperature

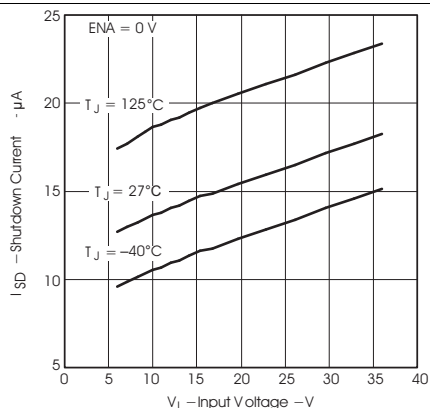


Figure 3. Shutdown Quiescent Current vs. Input Voltage

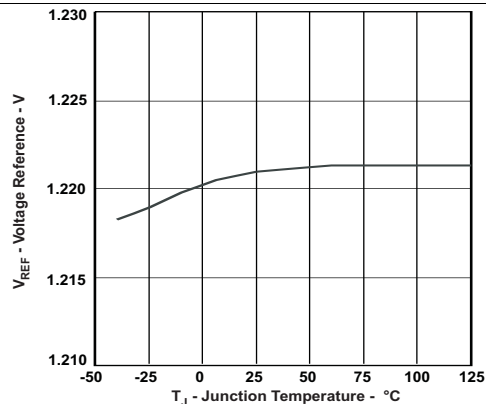


Figure 4. Voltage Reference vs. Junction Temperature

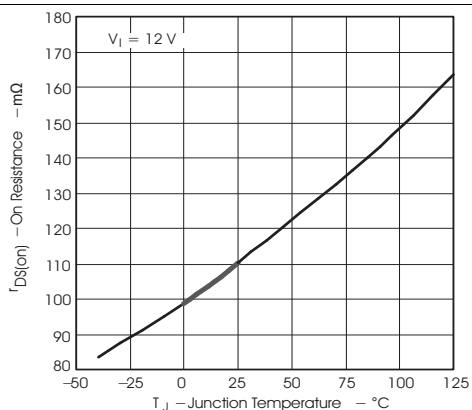


Figure 5. On Resistance vs. Junction Temperature

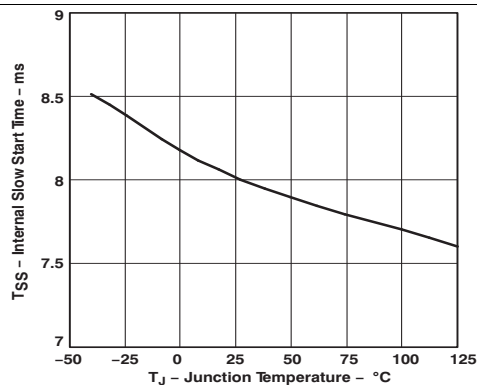


Figure 6. Internal Slow Start Time vs. Junction Temperature

Typical Characteristics (continued)

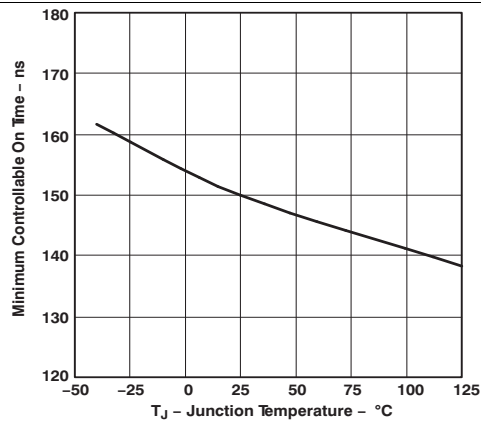


Figure 7. Minimum Controllable On Time vs. Junction Temperature

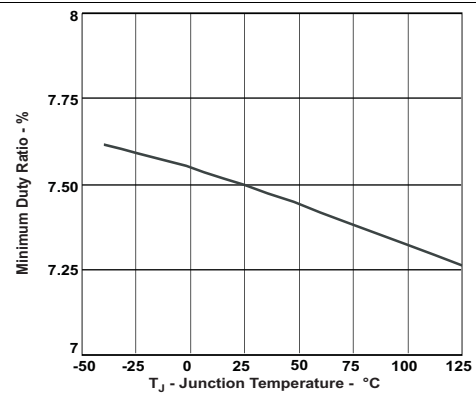


Figure 8. Minimum Controllable Duty Ratio vs. Junction Temperature

7 Detailed Description

7.1 Overview

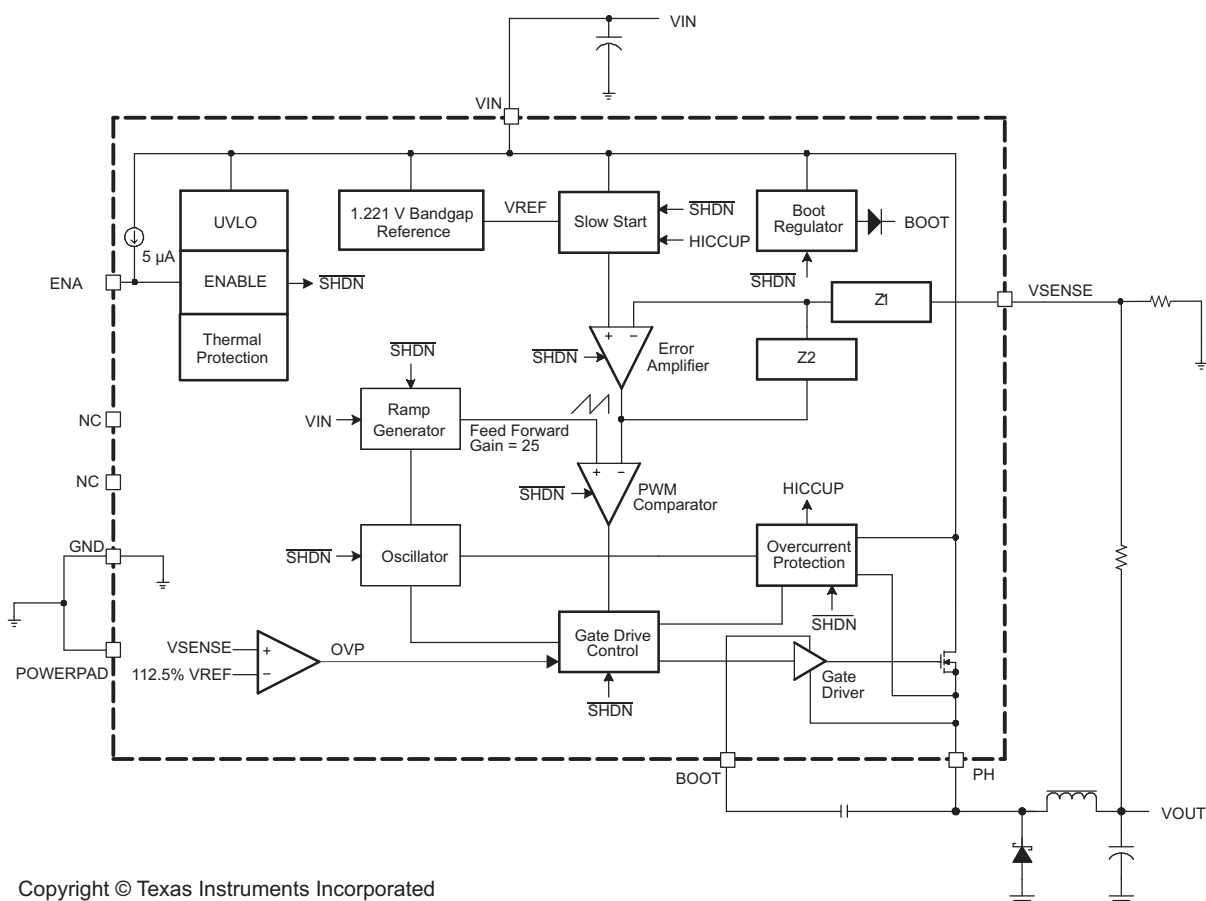
The TPS543x is a 3-A, step-down (buck) regulator with an integrated high-side n-channel MOSFET. The TPS5431 is intended to operate from power rails up to 23 V and the TPS5430 up to 36 V. These devices implement constant-frequency voltage-mode control with voltage feed forward for improved line regulation and line transient response. Internal compensation reduces design complexity and external component count.

The integrated 110-mΩ high-side MOSFET supports high-efficiency power-supply designs capable of delivering 3-A of continuous current to a load. The gate-drive bias voltage for the integrated high-side MOSFET is supplied by a bootstrap capacitor connected from the BOOT to PH pins. The TPS543x reduces the external component count by integrating the bootstrap recharge diode.

The TPS543x has a default input start-up voltage of 5.3 V typical. The ENA pin can be used to disable the TPS543x reducing the supply current to 18 μA. An internal pullup current source enables operation when the ENA pin is floating. The TPS543x includes an internal slow-start circuit that slows the output rise time during start up to reduce inrush current and output voltage overshoot. The minimum output voltage is the internal 1.221-V feedback reference. Output overvoltage transients are minimized by an Overvoltage Protection (OVP) comparator. When the OVP comparator is activated, the high-side MOSFET is turned off and remains off until the output voltage is less than 112.5% of the desired output voltage.

Internal cycle-by-cycle overcurrent protection limits the peak current in the integrated high-side MOSFET. For continuous overcurrent fault conditions the TPS543x will enter hiccup mode overcurrent limiting. Thermal protection protects the device from overheating.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Oscillator Frequency

The internal free running oscillator sets the PWM switching frequency at 500 kHz. The 500 kHz switching frequency allows less output inductance for the same output ripple requirement resulting in a smaller output inductor.

7.3.2 Voltage Reference

The voltage reference system produces a precision reference signal by scaling the output of a temperature stable bandgap circuit. The bandgap and scaling circuits are trimmed during production testing to an output of 1.221 V at room temperature.

7.3.3 Enable (ENA) and Internal Slow Start

The ENA pin provides electrical on/off control of the regulator. Once the ENA pin voltage exceeds the threshold voltage, the regulator starts operation and the internal slow start begins to ramp. If the ENA pin voltage is pulled below the threshold voltage, the regulator stops switching and the internal slow start resets. Connecting the pin to ground or to any voltage less than 0.5 V will disable the regulator and activate the shutdown mode. The quiescent current of the TPS543x in shutdown mode is typically 18 μ A.

The ENA pin has an internal pull-up current source, allowing the user to float the ENA pin. If an application requires controlling the ENA pin, use open drain or open collector output logic to interface with the pin. To limit the start-up inrush current, an internal slow-start circuit is used to ramp up the reference voltage from 0 V to its final value, linearly. The internal slow start time is 8 ms typically.

7.3.4 Undervoltage Lockout (UVLO)

The TPS543x incorporate an undervoltage lockout circuit to keep the device disabled when VIN (the input voltage) is below the UVLO start voltage threshold. During power up, internal circuits are held inactive and the internal slow start is grounded until VIN exceeds the UVLO start threshold voltage. Once the UVLO start threshold voltage is reached, the internal slow start is released and device start-up begins. The device operates until VIN falls below the UVLO stop threshold voltage. The typical hysteresis in the UVLO comparator is 330 mV.

7.3.5 Boost Capacitor (BOOT)

Connect a 0.01 μ F low-ESR ceramic capacitor between the BOOT pin and PH pin. This capacitor provides the gate drive voltage for the high-side MOSFET. X7R or X5R grade dielectrics are recommended due to their stable values over temperature.

7.3.6 Output Feedback (VSENSE) and Internal Compensation

The output voltage of the regulator is set by feeding back the center point voltage of an external resistor divider network to the VSENSE pin. In steady-state operation, the VSENSE pin voltage should be equal to the voltage reference 1.221 V.

The TPS543x implements internal compensation to simplify the regulator design. Since the TPS543x uses voltage mode control, a type 3 compensation network has been designed on chip to provide a high crossover frequency and a high phase margin for good stability. See the *Internal Compensation Network* in the applications section for more details.

7.3.7 Voltage Feed-Forward

The internal voltage feed-forward provides a constant dc power stage gain despite any variations with the input voltage. This greatly simplifies the stability analysis and improves the transient response. Voltage feed forward varies the peak ramp voltage inversely with the input voltage so that the modulator and power stage gain are constant at the feed forward gain, i.e.

$$\text{Feed Forward Gain} = \frac{V_{IN}}{\text{Ramp}_{pk-pk}} \quad (1)$$

The typical feed forward gain of TPS543x is 25.

Feature Description (continued)

7.3.8 Pulse-Width-Modulation (PWM) Control

The regulator employs a fixed frequency pulse-width-modulator (PWM) control method. First, the feedback voltage (VSENSE pin voltage) is compared to the constant voltage reference by the high gain error amplifier and compensation network to produce an error voltage. Then, the error voltage is compared to the ramp voltage by the PWM comparator. In this way, the error voltage magnitude is converted to a pulse width which is the duty cycle. Finally, the PWM output is fed into the gate drive circuit to control the on-time of the high-side MOSFET.

7.3.9 Overcurrent Limiting

Overcurrent limiting is implemented by sensing the drain-to-source voltage across the high-side MOSFET. The drain to source voltage is then compared to a voltage level representing the overcurrent threshold limit. If the drain-to-source voltage exceeds the overcurrent threshold limit, the overcurrent indicator is set true. The system will ignore the overcurrent indicator for the leading edge blanking time at the beginning of each cycle to avoid any turn-on noise glitches.

Once overcurrent indicator is set true, overcurrent limiting is triggered. The high-side MOSFET is turned off for the rest of the cycle after a propagation delay. The overcurrent limiting mode is called cycle-by-cycle current limiting.

Sometimes under serious overload conditions such as short-circuit, the overcurrent runaway may still happen when using cycle-by-cycle current limiting. A second mode of current limiting is used, i.e. hiccup mode overcurrent limiting. During hiccup mode overcurrent limiting, the voltage reference is grounded and the high-side MOSFET is turned off for the hiccup time. Once the hiccup time duration is complete, the regulator restarts under control of the slow start circuit.

7.3.10 Overvoltage Protection

The TPS543x has an overvoltage protection (OVP) circuit to minimize voltage overshoot when recovering from output fault conditions. The OVP circuit includes an overvoltage comparator to compare the VSENSE pin voltage and a threshold of $112.5\% \times V_{REF}$. Once the VSENSE pin voltage is higher than the threshold, the high-side MOSFET will be forced off. When the VSENSE pin voltage drops lower than the threshold, the high-side MOSFET will be enabled again.

7.3.11 Thermal Shutdown

The TPS543x protects itself from overheating with an internal thermal shutdown circuit. If the junction temperature exceeds the thermal shutdown trip point, the voltage reference is grounded and the high-side MOSFET is turned off. The part is restarted under control of the slow start circuit automatically when the junction temperature drops 14°C below the thermal shutdown trip point.

7.4 Device Functional Modes

7.4.1 Operation near Minimum Input Voltage

The TPS543x is recommended to operate with input voltages above 5.5 V. The typical VIN UVLO threshold is 5.3 V and the device may operate at input voltages down to the UVLO voltage. At input voltages below the actual UVLO voltage the device will not switch. If EN is floating or externally pulled up to greater than 1.3 V, when $V_{(VIN)}$ passes the UVLO threshold the TPS543x will become active. Switching is enabled and the slow-start sequence is initiated. The TPS543x starts linearly ramping up the internal reference voltage from 0 V to its final value over the internal slow-start time period.

7.4.2 Operation with ENA control

The enable start threshold voltage is 1.3 V max. With ENA held below the 0.5 V minimum stop threshold voltage the TPS543x is disabled and switching is inhibited even if VIN is above its UVLO threshold. The quiescent current is reduced in this state. If the ENA voltage is increased above the max start threshold while $V_{(VIN)}$ is above the UVLO threshold, the device becomes active. Switching is enabled and the slow-start sequence is initiated. The TPS543x starts linearly ramping up the internal reference voltage from 0 V to its final value over the internal slow-start time period.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS543x is a 3-A, step down regulator with an integrated high side MOSFET. This device is typically used to convert a higher DC voltage to a lower DC voltage with a maximum available output current of 3 A. Example applications are: High Density Point-of-Load Regulators for Set-top Box, DVD, LCD and Plasma Displays, High Power LED Supply, Car Audio, Battery Chargers, and other 12-V and 24-V Distributed Power Systems. Use the following design procedure to select component values for the TPS543x. This procedure illustrates the design of a high frequency switching regulator. Alternatively, use the WEBENCH software to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design.

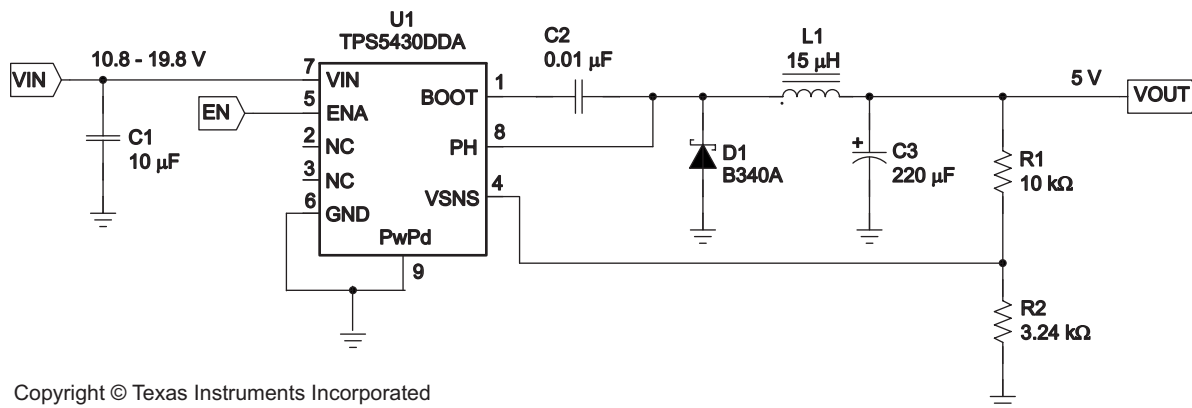
To begin the design process a few parameters must be decided upon. The designer needs to know the following:

- Input voltage range
- Output voltage
- Input ripple voltage
- Output ripple voltage
- Output current rating
- Operating frequency

8.2 Typical Applications

8.2.1 12-V Input to 5.0-V Output

Figure 9 shows the schematic for a typical TPS5430 application. The TPS5430 can provide up to 3 A output current at a nominal output voltage of 5 V. For proper thermal performance, the exposed PowerPAD™ underneath the device must be soldered down to the printed-circuit board.



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Figure 9. Application Circuit, 12 V Input to 5.0 V Output

8.2.1.1 Design Requirements

For this design example, use the following as the input parameters:

DESIGN PARAMETER ⁽¹⁾	EXAMPLE VALUE
Input voltage range	10.8 V to 19.8 V
Output voltage	5 V
Input ripple voltage	300 mV
Output ripple voltage	30 mV
Output current rating	3 A
Operating frequency	500 kHz

(1) As an additional constraint, the design is set up to be small size and low component height.

8.2.1.2 Detailed Design Procedure

The following design procedure can be used to select component values for the TPS5430. This section presents a simplified discussion of the design process.

8.2.1.2.1 Switching Frequency

The switching frequency for the TPS5430 is internally set to 500 kHz. It is not possible to adjust the switching frequency.

8.2.1.2.2 Input Capacitors

The TPS5430 requires an input decoupling capacitor and, depending on the application, a bulk input capacitor. The recommended value for the decoupling capacitor, C1, is 10 μ F. A high quality ceramic type X5R or X7R is required. For some applications, a smaller value decoupling capacitor may be used, so long as the input voltage and current ripple ratings are not exceeded. The voltage rating must be greater than the maximum input voltage, including ripple.

This input ripple voltage can be approximated by [Equation 2](#) :

$$\Delta V_{IN} = \frac{I_{OUT(MAX)} \times 0.25}{C_{BULK} \times f_{sw}} + (I_{OUT(MAX)} \times ESR_{MAX}) \quad (2)$$

Where $I_{OUT(MAX)}$ is the maximum load current, f_{sw} is the switching frequency, C_{IN} is the input capacitor value and ESR_{MAX} is the maximum series resistance of the input capacitor.

The maximum RMS ripple current also needs to be checked. For worst case conditions, this can be approximated by [Equation 3](#) :

$$I_{CIN} = \frac{I_{OUT(MAX)}}{2} \quad (3)$$

In this case the input ripple voltage would be 156 mV and the RMS ripple current would be 1.5 A. The maximum voltage across the input capacitors would be $V_{IN\ max}$ plus $\Delta V_{IN}/2$. The chosen input decoupling capacitor is rated for 25 V and the ripple current capacity is greater than 3 A, providing ample margin. It is very important that the maximum ratings for voltage and current are not exceeded under any circumstance.

Additionally some bulk capacitance may be needed, especially if the TPS5430 circuit is not located within about 2 inches from the input voltage source. The value for this capacitor is not critical but it also should be rated to handle the maximum input voltage including ripple voltage and should filter the output so that input ripple voltage is acceptable.

8.2.1.2.3 Output Filter Components

Two components need to be selected for the output filter, L1 and C2. Since the TPS5430 is an internally compensated device, a limited range of filter component types and values can be supported.

8.2.1.2.3.1 Inductor Selection

To calculate the minimum value of the output inductor, use [Equation 4](#):

$$L_{\text{MIN}} = \frac{V_{\text{OUT(MAX)}} \times (V_{\text{IN(MAX)}} - V_{\text{OUT}})}{V_{\text{IN(max)}} \times K_{\text{IND}} \times I_{\text{OUT}} \times F_{\text{SW}}} \quad (4)$$

K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. Three things need to be considered when determining the amount of ripple current in the inductor: the peak to peak ripple current affects the output ripple voltage amplitude, the ripple current affects the peak switch current and the amount of ripple current determines at what point the circuit becomes discontinuous. For designs using the TPS5430, K_{IND} of 0.2 to 0.3 yields good results. Low output ripple voltages can be obtained when paired with the proper output capacitor, the peak switch current will be well below the current limit set point and relatively low load currents can be sourced before discontinuous operation.

For this design example use $K_{\text{IND}} = 0.2$ and the minimum inductor value is calculated to be 12.5 μH . The next highest standard value is 15 μH , which is used in this design.

For the output filter inductor it is important that the RMS current and saturation current ratings not be exceeded. The RMS inductor current can be found from [Equation 5](#):

$$I_{\text{L(RMS)}} = \sqrt{I_{\text{OUT(MAX)}}^2 + \frac{1}{12} \times \left(\frac{V_{\text{OUT}} \times (V_{\text{IN(MAX)}} - V_{\text{OUT}})}{V_{\text{IN(MAX)}} \times L_{\text{OUT}} \times F_{\text{SW}} \times 0.8} \right)^2} \quad (5)$$

and the peak inductor current can be determined with [Equation 6](#):

$$I_{\text{L(PK)}} = I_{\text{OUT(MAX)}} + \frac{V_{\text{OUT}} \times (V_{\text{IN(MAX)}} - V_{\text{OUT}})}{1.6 \times V_{\text{IN(MAX)}} \times L_{\text{OUT}} \times F_{\text{SW}}} \quad (6)$$

For this design, the RMS inductor current is 3.003 A, and the peak inductor current is 3.31 A. The chosen inductor is a Sumida CDRH104R-150 15 μH . It has a saturation current rating of 3.4 A and a RMS current rating of 3.6 A, easily meeting these requirements. A lesser rated inductor could be used, however this device was chosen because of its low profile component height. In general, inductor values for use with the TPS5430 are in the range of 10 μH to 100 μH .

8.2.1.2.3.2 Capacitor Selection

The important design factors for the output capacitor are dc voltage rating, ripple current rating, and equivalent series resistance (ESR). The dc voltage and ripple current ratings cannot be exceeded. The ESR is important because along with the inductor ripple current it determines the amount of output ripple voltage. The actual value of the output capacitor is not critical, but some practical limits do exist. Consider the relationship between the desired closed loop crossover frequency of the design and LC corner frequency of the output filter. Due to the design of the internal compensation, it is desirable to keep the closed loop crossover frequency in the range 3 kHz to 30 kHz as this frequency range has adequate phase boost to allow for stable operation. For this design example, it is assumed that the intended closed loop crossover frequency will be between 2590 Hz and 24 kHz and also below the ESR zero of the output capacitor. Under these conditions the closed loop crossover frequency is related to the LC corner frequency by:

$$f_{CO} = \frac{f_{LC}^2}{85 V_{OUT}} \quad (7)$$

And the desired output capacitor value for the output filter to:

$$C_{OUT} = \frac{1}{3357 \times L_{OUT} \times f_{CO} \times V_{OUT}} \quad (8)$$

For a desired crossover of 18 kHz and a 15 µH inductor, the calculated value for the output capacitor is 220 µF. The capacitor type should be chosen so that the ESR zero is above the loop crossover. The maximum ESR should be:

$$ESR_{MAX} = \frac{1}{2\pi \times C_{OUT} \times f_{CO}} \quad (9)$$

The maximum ESR of the output capacitor also determines the amount of output ripple as specified in the initial design parameters. The output ripple voltage is the inductor ripple current times the ESR of the output filter. Check that the maximum specified ESR as listed in the capacitor data sheet results in an acceptable output ripple voltage:

$$V_{PP} (MAX) = \frac{ESR_{MAX} \times V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{N_C \times V_{IN(MAX)} \times L_{OUT} \times F_{SW}} \quad (10)$$

Where:

ΔV_{PP} is the desired peak-to-peak output ripple.

N_C is the number of parallel output capacitors.

F_{SW} is the switching frequency.

For this design example, a single 220 µF output capacitor is chosen for C3. The calculated RMS ripple current is 143 mA and the maximum ESR required is 40 mΩ. A capacitor that meets these requirements is a Sanyo Poscap 10TPB220M, rated at 10 V with a maximum ESR of 40 mΩ and a ripple current rating of 3 A. An additional small 0.1 µF ceramic bypass capacitor may also be used, but is not included in this design.

The minimum ESR of the output capacitor should also be considered. For good phase margin, the ESR zero when the ESR is at a minimum should not be too far above the internal compensation poles at 24 kHz and 54 kHz.

The selected output capacitor must also be rated for a voltage greater than the desired output voltage plus one half the ripple voltage. Any derating amount must also be included. The maximum RMS ripple current in the output capacitor is given by Equation 11:

$$I_{COUT(RMS)} = \frac{1}{\sqrt{12}} \times \left[\frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times N_C} \right] \quad (11)$$

Where:

N_C is the number of output capacitors in parallel.

F_{SW} is the switching frequency.

Other capacitor types can be used with the TPS5430, depending on the needs of the application.

8.2.1.2.4 Output Voltage Set-Point

The output voltage of the TPS5430 is set by a resistor divider (R1 and R2) from the output to the VSENSE pin. Calculate the R2 resistor value for the output voltage of 5 V using [Equation 12](#):

$$R2 = \frac{R1 \times 1.221}{V_{OUT} - 1.221} \quad (12)$$

For any TPS5430 design, start with an R1 value of 10 kΩ. R2 is then 3.24 kΩ.

8.2.1.2.5 BOOT Capacitor

The BOOT capacitor should be 0.01 μF.

8.2.1.2.6 Catch Diode

The TPS5430 is designed to operate using an external catch diode between PH and GND. The selected diode must meet the absolute maximum ratings for the application: Reverse voltage must be higher than the maximum voltage at the PH pin, which is $V_{IN(MAX)} + 0.5$ V. Peak current must be greater than $I_{OUT(MAX)}$, plus on half the peak to peak inductor current. Forward voltage drop should be small for higher efficiencies. It is important to note that the catch diode conduction time is typically longer than the high-side FET on time, so attention paid to diode parameters can make a marked improvement in overall efficiency. Additionally, check that the device chosen is capable of dissipating the power losses. For this design, a Diodes, Inc. B340A is chosen, with a reverse voltage of 40 V, forward current of 3 A, and a forward voltage drop of 0.5 V.

8.2.1.2.7 Advanced Information

8.2.1.2.7.1 Output Voltage Limitations

Due to the internal design of the TPS543x, there are both upper and lower output voltage limits for any given input voltage. The upper limit of the output voltage set point is constrained by the maximum duty cycle of 87% and is given by:

$$V_{OUTMAX} = 0.87 \times \left((V_{INMIN} - I_{OMAX} \times 0.230) + V_D \right) - (I_{OMAX} \times R_L) - V_D \quad (13)$$

Where

- V_{INMIN} = minimum input voltage
- I_{OMAX} = maximum load current
- V_D = catch diode forward voltage.
- R_L = output inductor series resistance.

This equation assumes maximum on resistance for the internal high side FET.

The lower limit is constrained by the minimum controllable on time which may be as high as 200 ns. The approximate minimum output voltage for a given input voltage and minimum load current is given by:

$$V_{OUTMIN} = 0.12 \times \left((V_{INMAX} - I_{OMIN} \times 0.110) + V_D \right) - (I_{OMIN} \times R_L) - V_D \quad (14)$$

Where

- V_{INMAX} = maximum input voltage
- I_{OMIN} = minimum load current
- V_D = catch diode forward voltage.
- R_L = output inductor series resistance.

This equation assumes nominal on resistance for the high side FET and accounts for worst case variation of operating frequency set point. Any design operating near the operational limits of the device should be carefully checked to assure proper functionality.

8.2.1.2.7.2 Internal Compensation Network

The design equations given in the example circuit can be used to generate circuits using the TPS543x. These designs are based on certain assumptions and will tend to always select output capacitors within a limited range of ESR values. If a different capacitor type is desired, it may be possible to fit one to the internal compensation of the TPS543x. Equation 15 gives the nominal frequency response of the internal voltage-mode type III compensation network:

$$H(s) = \frac{\left(1 + \frac{s}{2\pi \times F_{z1}}\right) \times \left(1 + \frac{s}{2\pi \times F_{z2}}\right)}{\left(\frac{s}{2\pi \times F_{p0}}\right) \times \left(1 + \frac{s}{2\pi \times F_{p1}}\right) \times \left(1 + \frac{s}{2\pi \times F_{p2}}\right) \times \left(1 + \frac{s}{2\pi \times F_{p3}}\right)} \quad (15)$$

Where

fp0 = 2165 Hz, fz1 = 2170 Hz, fz2 = 2590 Hz

fp1 = 24 kHz, fp2 = 54 kHz, fp3 = 440 kHz

fp3 represents the non-ideal parasitics effect.

Using this information along with the desired output voltage, feed forward gain and output filter characteristics, the closed loop transfer function can be derived.

8.2.1.2.7.3 Thermal Calculations

The following formulas show how to estimate the device power dissipation under continuous conduction mode operations. They should not be used if the device is working at light loads in the discontinuous conduction mode.

Conduction Loss: $P_{con} = I_{OUT}^2 \times R_{ds(on)} \times V_{OUT}/V_{IN}$

Switching Loss: $P_{sw} = V_{IN} \times I_{OUT} \times 0.01$

Quiescent Current Loss: $P_q = V_{IN} \times 0.01$

Total Loss: $P_{tot} = P_{con} + P_{sw} + P_q$

Given $T_A \Rightarrow$ Estimated Junction Temperature: $T_J = T_A + R_{th} \times P_{tot}$

Given $T_{JMAX} = 125^\circ\text{C} \Rightarrow$ Estimated Maximum Ambient Temperature: $T_{AMAX} = T_{JMAX} - R_{th} \times P_{tot}$

8.2.1.3 Application Curves

The performance graphs (Figure 10 through Figure 16) are applicable to the circuit in Figure 9. $T_a = 25^\circ\text{C}$, unless otherwise specified.

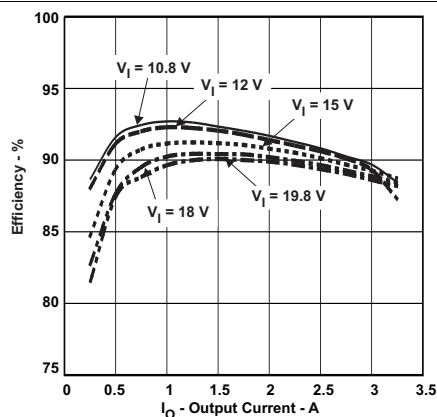


Figure 10. Efficiency vs. Output Current

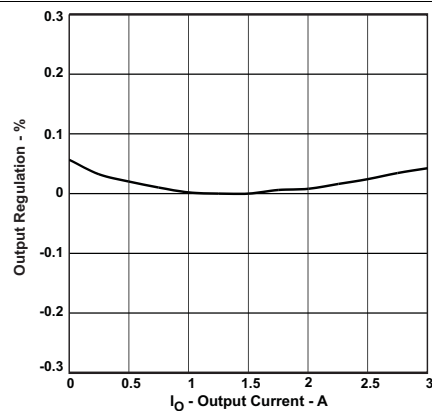


Figure 11. Output Regulation % vs. Output Current

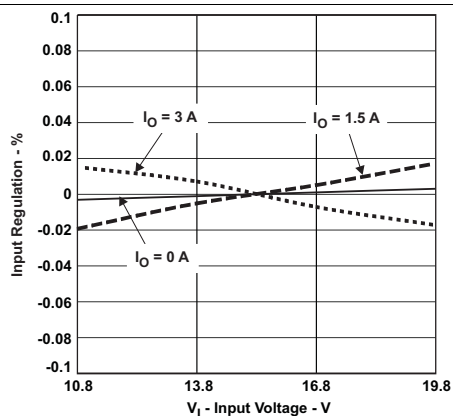


Figure 12. Input Regulation % vs. Input Voltage

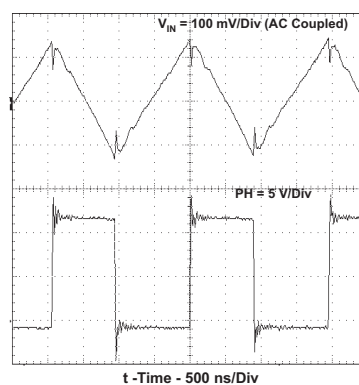


Figure 13. Input Voltage Ripple and PH Node, $I_O = 3\text{ A}$.

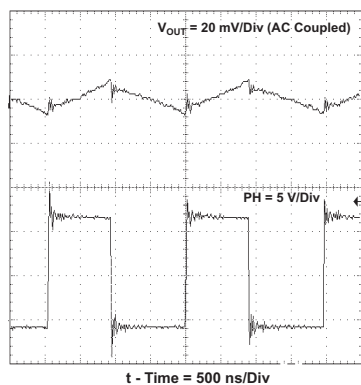


Figure 14. Output Voltage Ripple and PH Node, $I_O = 3\text{ A}$

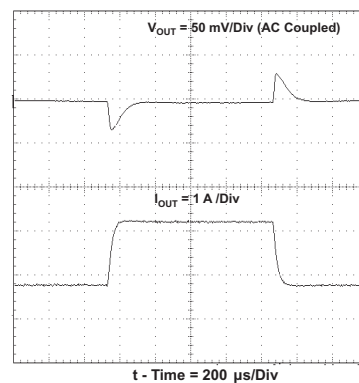


Figure 15. Transient Response, I_O Step 0.75 to 2.25 A.

TPS5430, TPS5431

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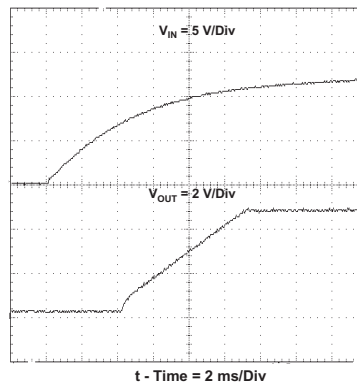
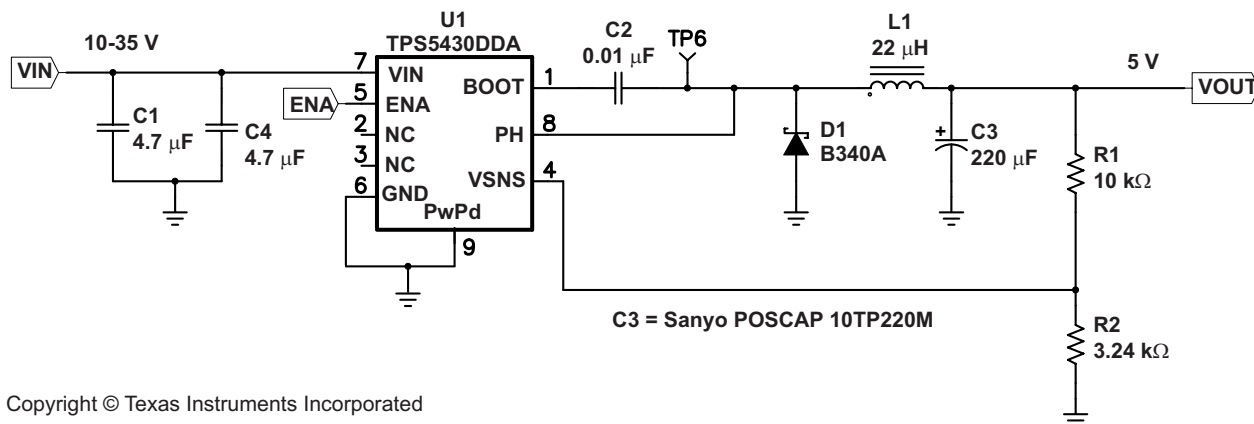


Figure 16. Startup Waveform, V_{IN} and V_{OUT} .

8.2.2 Wide Input Voltage Ranges with TPS5430

Figure 17 shows an application circuit using the wide input voltage range of the TPS5430.



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Figure 17. 10 V– 35 V Input to 5 V Output Application Circuit

8.2.2.1 Design Requirements

For this design example, use the following as the input parameters. This circuit is also designed with a larger value output inductor and a lower closed loop crossover frequency.

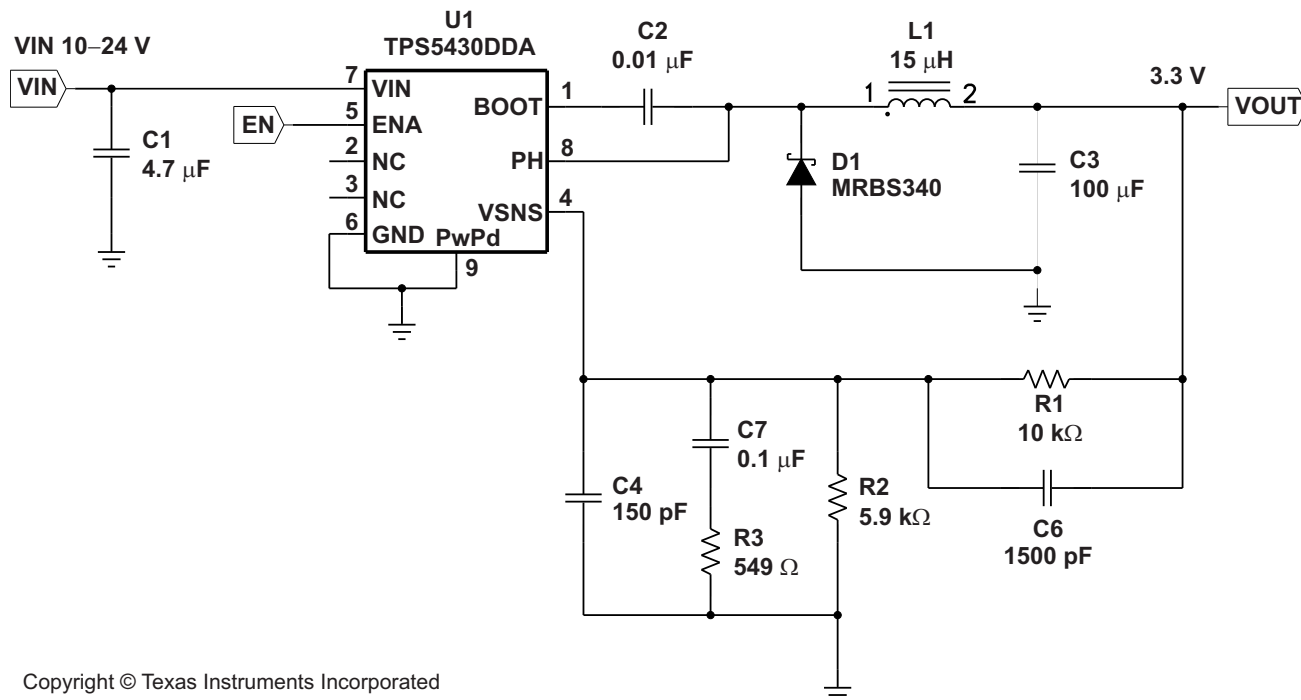
DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	10 V to 35 V
Output voltage	5 V
Input ripple voltage	300 mV
Output ripple voltage	30 mV
Output current rating	3 A
Operating frequency	500 kHz

8.2.2.2 Detailed Design Procedure

The design procedure is similar to what is given for the design example in the [12-V Input to 5.0-V Output Detailed Design Procedure](#) section.

8.2.3 Circuit Using Ceramic Output Filter Capacitors

Figure 19 shows an application circuit using all ceramic capacitors for the input and output filters.



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Figure 19. Ceramic Output Filter Capacitors Circuit

8.2.3.1 Design Requirements

For this design example, use the following as the input parameters. This circuit is also designed with a ceramic output filter capacitor.

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	10 V to 24 V
Output voltage	3.3 V
Input ripple voltage	300 mV
Output current rating	3 A
Operating frequency	500 kHz

8.2.3.2 Detailed Design Procedure

The design procedure is similar to what is given for the design example in the [12-V Input to 5.0-V Output Detailed Design Procedure](#) section, except for the selection of the output filter capacitor values and the design of the additional compensation components required to stabilize the circuit.

8.2.3.2.1 Output Filter Component Selection

Using [Equation 11](#), the minimum inductor value is 12 μ H. A value of 15 μ H is chosen for this design.

When using ceramic output filter capacitors, the recommended LC resonant frequency should be no more than 7 kHz. Since the output inductor is already selected at 15 μ H, this limits the minimum output capacitor value to:

$$C_O \text{ (MIN)} \geq \frac{1}{(2\pi \times 7000)^2 \times L_O} \quad (16)$$

The minimum capacitor value is calculated to be 34 μ F. For this circuit a larger value of capacitor yields better transient response. A single 100 μ F output capacitor is used for C3. It is important to note that the actual capacitance of ceramic capacitors decreases with applied voltage. In this example, the output voltage is set to 3.3 V, minimizing this effect.

8.2.3.2.2 External Compensation Network

When using ceramic output capacitors, additional circuitry is required to stabilize the closed loop system. For this circuit, the external components are R3, C4, C6, and C7. To determine the value of these components, first calculate the LC resonant frequency of the output filter:

$$F_{LC} = \frac{1}{2\pi \sqrt{L_O \times C_O \text{ (EFF)}}} \quad (17)$$

For this example the effective resonant frequency is calculated as 4109 Hz

The network composed of R1, R2, R3, C5, C6, and C7 has two poles and two zeros that are used to tailor the overall response of the feedback network to accommodate the use of the ceramic output capacitors. The pole and zero locations are given by the following equations:

$$F_{p1} = 500000 \times \frac{V_O}{F_{LC}} \quad (18)$$

$$F_{z1} = 0.7 \times F_{LC} \quad (19)$$

$$F_{z2} = 2.5 \times F_{LC} \quad (20)$$

The final pole is located at a frequency too high to be of concern. The second zero, fz2 as defined by [Equation 20](#) uses 2.5 for the frequency multiplier. In some cases this may need to be slightly higher or lower. Values in the range of 2.3 to 2.7 work well. The values for R1 and R2 are fixed by the 3.3 V output voltage as calculated using [Equation 12](#). For this design R1 = 10 k Ω and R2 = 5.90 k Ω . With F_{p1} = 401 Hz, F_{z1} = 2876 Hz and F_{z2} = 10.3 kHz, the values of R3, C6 and C7 are determined using [Equation 21](#), [Equation 22](#), and [Equation 23](#):

$$C7 = \frac{1}{2\pi \times F_{p1} \times (R1 \parallel R2)} \quad (21)$$

$$R3 = \frac{1}{2\pi \times F_{z1} \times C7} \quad (22)$$

$$C6 = \frac{1}{2\pi \times F_{z2} \times R1} \quad (23)$$

For this design, using the closest standard values, C7 is 0.1 μ F, R3 is 549 Ω , and C6 is 1500 pF. C4 is added to improve load regulation performance. It is effectively in parallel with C6 in the location of the second pole frequency, so it should be small in relationship to C6. C4 should be less the 1/10 the value of C6. For this example, 150 pF works well.

For additional information on external compensation of the TPS5430, TPS5431 or other wide voltage range devices, see [SLVA237 Using TPS5410/20/30/31 With Aluminum/Ceramic Output Capacitors](#)

9 Power Supply Recommendations

The TPS5430 is designed to operate from an input voltage supply range between 5.5 V and 36 V. The TPS5431 is designed to operate from an input voltage supply range between 5.5 V and 23 V. This input supply should remain within the input voltage supply range. If the input supply is located more than a few inches from the TPS543x converter bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 100 μ F is a typical choice.

10 Layout

10.1 Layout Guidelines

Connect a low ESR ceramic bypass capacitor to the VIN pin. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pin, and the TPS543x ground pin. The best way to do this is to extend the top side ground area from under the device adjacent to the VIN trace, and place the bypass capacitor as close as possible to the VIN pin. The minimum recommended bypass capacitance is 4.7 μ F ceramic with a X5R or X7R dielectric.

There should be a ground area on the top layer directly underneath the IC, with an exposed area for connection to the PowerPAD. Use vias to connect this ground area to any internal ground planes. Use additional vias at the ground side of the input and output filter capacitors as well. The GND pin should be tied to the PCB ground by connecting it to the ground area under the device as shown below.

The PH pin should be routed to the output inductor, catch diode and boot capacitor. Since the PH connection is the switching node, the inductor should be located very close to the PH pin and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The catch diode should also be placed close to the device to minimize the output current loop area. Connect the boot capacitor between the phase node and the BOOT pin as shown. Keep the boot capacitor close to the IC and minimize the conductor trace lengths. The component placements and connections shown work well, but other connection routings may also be effective.

Connect the output filter capacitor(s) as shown between the VOUT trace and GND. It is important to keep the loop formed by the PH pin, Lout, Cout and GND as small as is practical.

Connect the VOUT trace to the VSENSE pin using the resistor divider network to set the output voltage. Do not route this trace too close to the PH trace. Due to the size of the IC package and the device pin-out, the trace may need to be routed under the output capacitor. Alternately, the routing may be done on an alternate layer if a trace under the output capacitor is not desired.

If using the grounding scheme shown in [Figure 20](#), use a via connection to a different layer to route to the ENA pin.

10.2 Layout Example

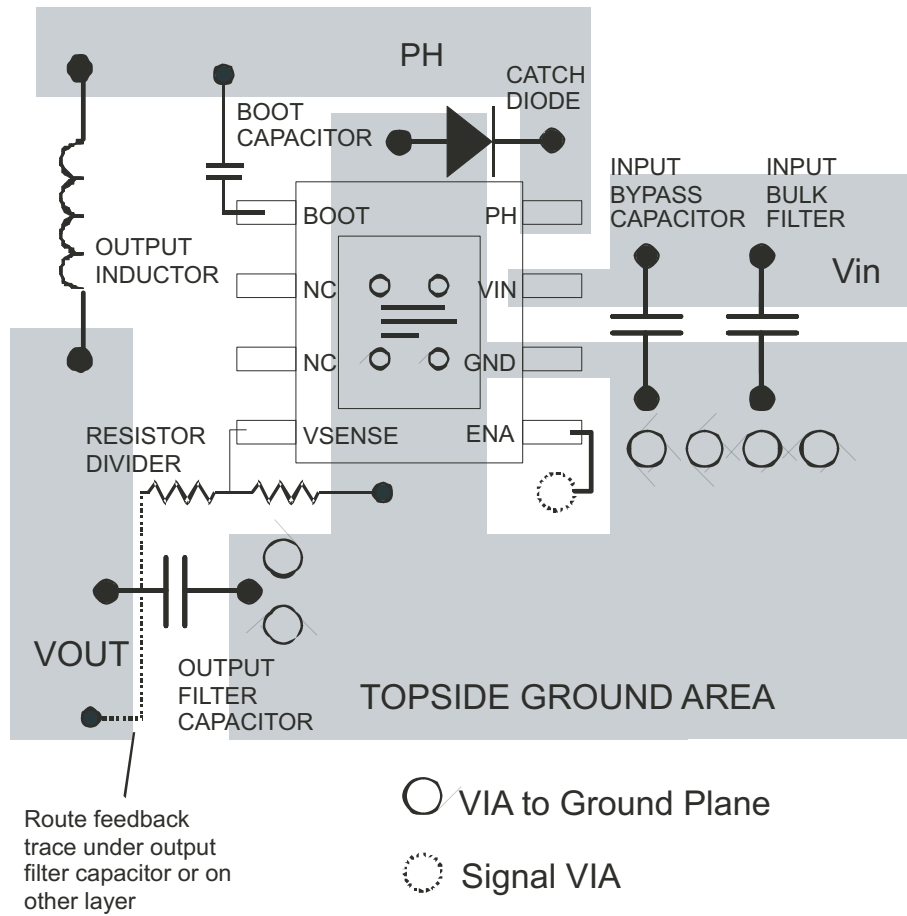


Figure 20. Design Layout

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY	REFERENCE DESIGN
TPS5430	Click here	Click here	Click here	Click here	Click here	
TPS5431	Click here	Click here	Click here	Click here	Click here	

11.2 Trademarks

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

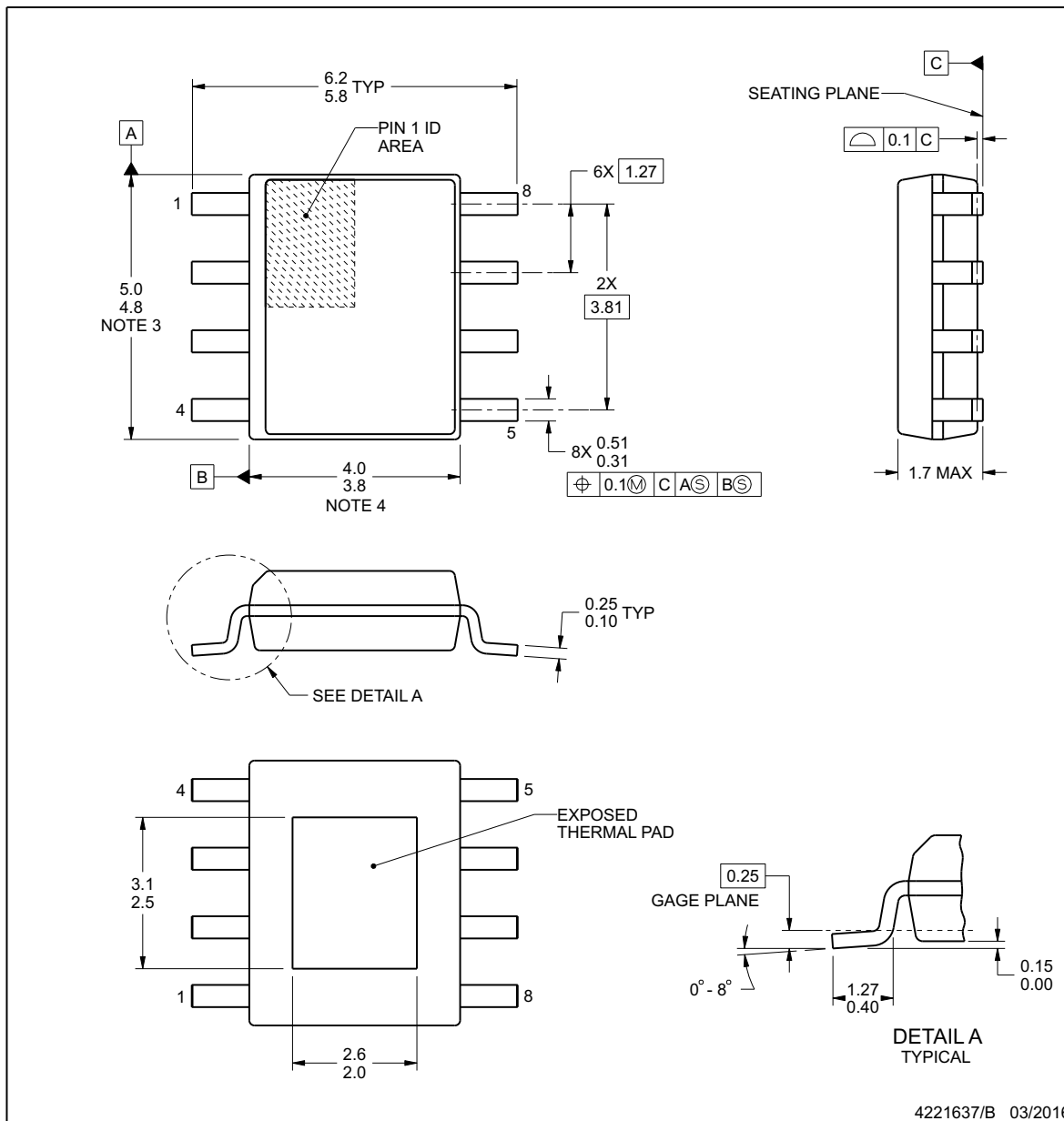
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



PACKAGE OUTLINE

DDA0008J
PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



4221637/B 03/2016

PowerPAD is a trademark of Texas Instruments.

NOTES:

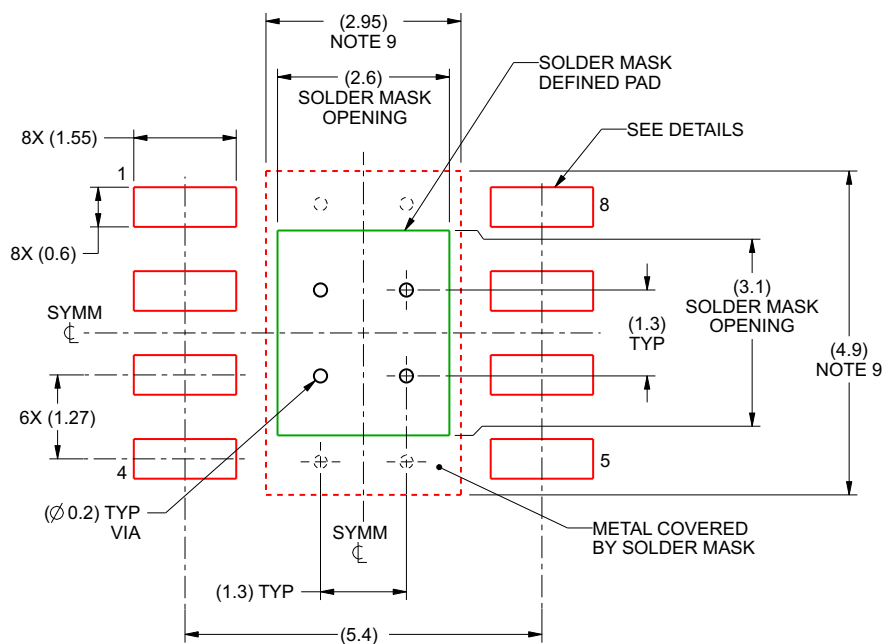
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012, variation BA.

EXAMPLE BOARD LAYOUT

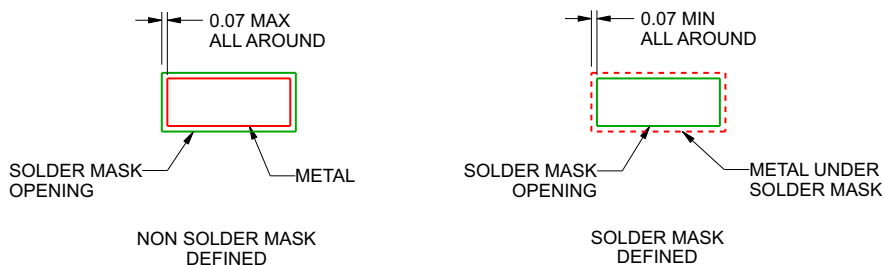
DDA0008J

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS

4221637/B 03/2016

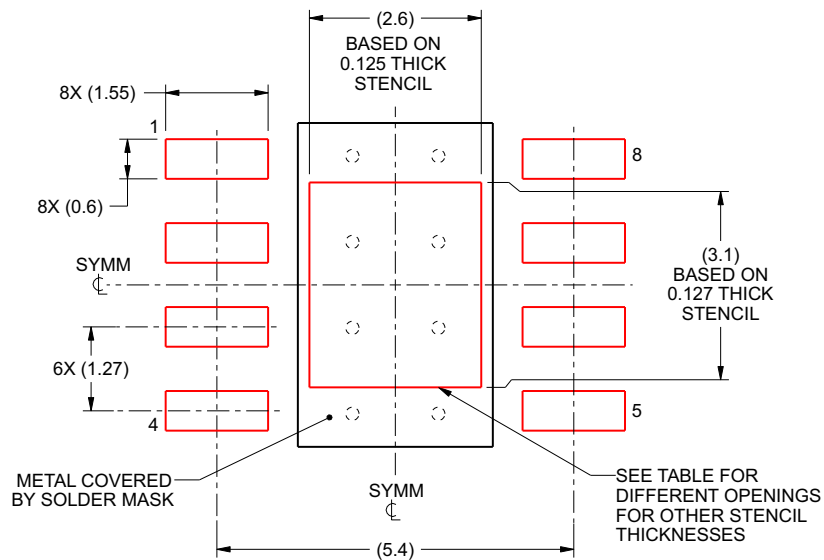
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DDA0008J
PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 3.47
0.125	2.6 X 3.1 (SHOWN)
0.150	2.37 X 2.83
0.175	2.20 X 2.62

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS5430DDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 0	5430	Samples
TPS5430DDAG4	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	5430	Samples
TPS5430DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	5430	Samples
TPS5430DDARG4	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	5430	Samples
TPS5431DDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	5431	Samples
TPS5431DDAG4	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	5431	Samples
TPS5431DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	5431	Samples
TPS5431DDARG4	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	5431	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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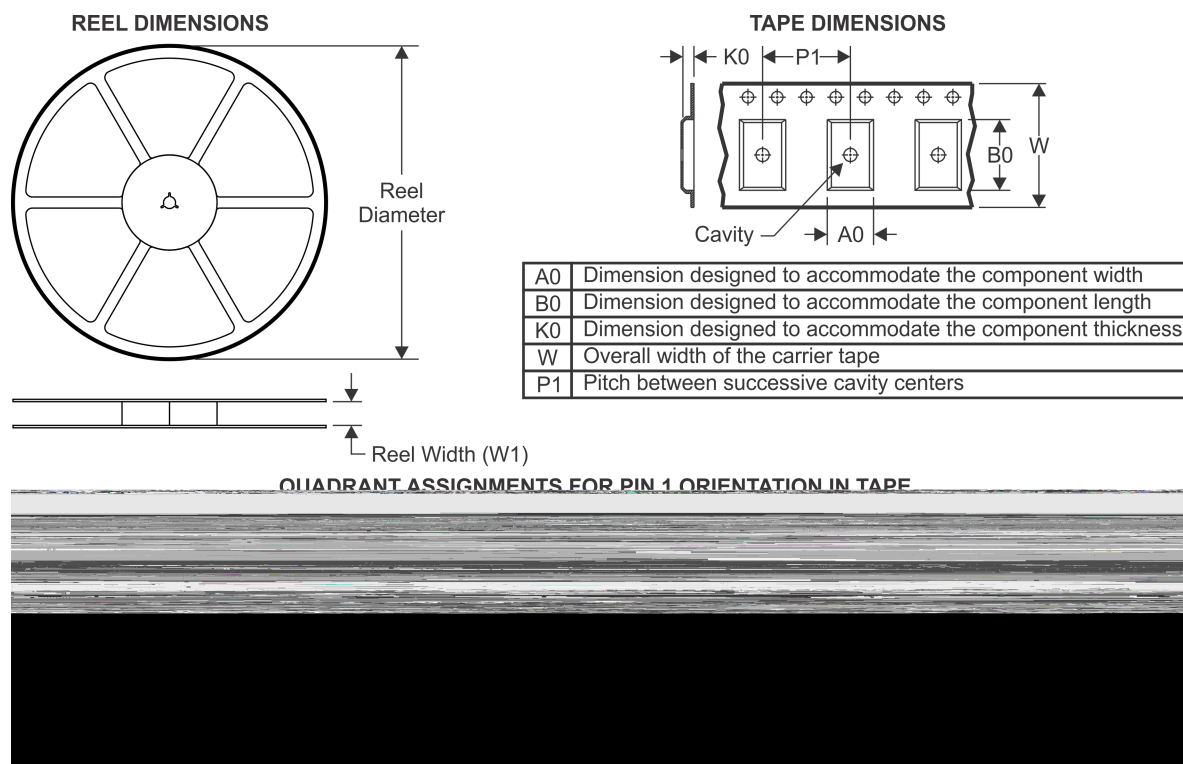
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OTHER QUALIFIED VERSIONS OF TPS5430 :

- Automotive: [TPS5430-Q1](#)
- Enhanced Product: [TPS5430-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS5430DDAR	SO Power PAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS5431DDAR	SO Power PAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS5430DDAR	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0
TPS5431DDAR	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0

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