Electric Transport

Deliverable report 1

EPO-4

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Contents

1 | Assignment 1

The first step in designing our DC/DC converter meant we had to incorporate the used UC3525 Regulating Pulse Width Modulator and the IRS2001PBF Gate Drivers into a full bridge converter (the DC/AC step), while at the same time integrating the given overcurrent protection circuit in the correct way. Since connection schemes for both the UC3525 and the IRS2001PBF were given in their respective datasheets **uc3525a-datasheet**, **irs2001pbf-datasheet** this did not pose much of a problem. The focus was not on calculating the resistors and capacitors values, therefore we will not discuss the choices we made regarding these values. However, we will discuss our choice of the used MOSFET transistors and diodes. The most important factors in picking the correct transistor for our application were static and dynamic power dissipation.

1.1 MOSFET choice

All three of the MOSFETs (IPP50CN10N, IPP028N08N3G, PSMN017) were viable options, because our circuit parameters were well within their given margins. To pick one of the three, we calculated the power loss of each one, to see which one of them would do best. Static power dissipation can be calculated using

$$P_s = I_{DS} R_{DS(on)} D. \tag{1.1}$$

Where I_{DS} is the drain-source current through the transistor, $R_{DS(on)}$ is the transistors drain-source resistance, when switched on and D is the duty-cycle of the PWM control signal. We estimated I_{DS} to be approximately 2 A and chose D to be 0.5. $R_{DS(on)}$ is a transistor parameter which can be found in each datasheet. Dynamical power dissipation is the power that is lost charging the in- and output capacitances of the transistors (both found in transistor datasheets **IPP50CN10N-datasheet**, **IPP028N08N3G-datasheet**, **PSMN017-datasheet**) and is given by

$$P_d = (C_{in} V_{GS}^2 + C_{out} V_{DS}^2) f_s. \tag{1.2}$$

C_{in} and C_{out} are the transistor's in- and output capacitances, V_{GS} is the gate-source voltage on the transitor (estimated to be 15 V in our calculations), V_{DS} is the drain-source voltage on the transistor (also 15 V) and f_s is the switching frequency, which is 100 kHz. The total power dissipation thus becomes

$$P = P_s + P_d = I_{DS} R_{DS(on)} D + (C_{in} V_{GS}^2 + C_{out} V_{DS}^2) f_s. \tag{1.3}$$

Using this equation yields the results in Table 1.1 for each of the three transistors to pick from.

Table 1.1: MOSFET power loss calculations

MOSFET	$R_{DS(on)}$	C_{in}	C_{out}	Static loss	Dynamic loss	Total loss
IPP50CN10N	49 mΩ	822 pF	120 pF	0.098 W	0.021 W	0.119 W
IPP028N08N3G	2.8 mΩ	10 700 pF	2890 pF	0.006 W	0.306 W	0.311 W
PSMN017	13.7 mΩ	1573 pF	154 pF	0.027 W	0.039 W	0.066 W

From Table 1.1 we concluded the PSMN017 would be the best transistor to use.

1.2 Diode choice

In choosing one of the two given diodes (SB540 and SF61), we again considered the dynamic and static power loss. When assuming that the output voltage is near constant, the static dissipation, in context of the inverter, is given by

$$P_s = IV_{fw}D_d \tag{1.4}$$

in which I represents the current flowing through the diodes, V_{fw} the forward voltage drop and D_d the *diode duty cycle*. The diode duty cycle determines the percentage of time in which current flows through the diode with respect to the switching frequency. D_d is given by

$$D_d = \frac{1}{2} + arcsin\left(\frac{V_{min}}{V_{max}} - 1\right) \tag{1.5}$$

in which the minumum and maximum output voltage of the inverter is represented by V_{min} and V_{max}. The dynamic power dissipation is per diode given by

$$P_s = C_j V_{DS}^2 \tag{1.6}$$

in which the junction capacitance is represented by C_j. Combining equations 1.4, 1.5 and 1.6 yielded a total power loss of 0.0784 W for the SB540 and 0.139 W for the SF61, so we picked the SB540. **SB540-datasheet**, **SF61-datasheet**

1.3 Final design and testing

Implementing the PWM-generator, two gate drivers, the overcurrent protection circuit and the rectifier with overvoltage buzzer circuit resulted in the schematics found in Appendix . After soldering the PCB we got from our consultant we hooked it up to an oscilloscope, on which we then measured tidy square waves for the gate drivers and power outputs, whose frequency and duty-cycle could be varied by changing the values of the two potmeters in the design. While inspecting the rectifier output waveform, we obtained a nice DC-signal, with very little ripple, due to the high switching frequency (i.e. compared to for example the rectifier used during EPO1 at 50 Hz). Actual waveforms of the entire converter, including air transformer and compensation, can be found in Appendix .

2 | Assignment 2

Calculation

By using the online calculator located on `http://deepfriedneon.com/tesla_f_calcspiral.html`, we obtained acceptable inductances for our coils at the coil parameters as given in Table 2.1. Target parameters were an inner diameter of 50 mm for both coils and inductances of 22 µH for the secondary coil and 100 µH for the primary coil. The diameter of the given Litz-wire is 1.8 mm and we estimated an average wire spacing of 0.5 mm between each winding.

Table 2.1: Calculated coil parameters

Coil	Windings	Inductance	Outer diameter	Total wire length
Primary	30	101.6 µH	188 mm	11.2 m
Secondary	15	22 µH	119 mm	4 m

Measurements

After winding these coils we obtained the following inductances for the individual coils using an LCR-meter:

Table 2.2: Measured coil parameters

Coil	Inductance	DC-resistance
Primary	94.5 µH	250 mΩ
Secondary	25.2 µH	65 mΩ

Then, we calculated the coils' mutual inductance and coupling factor via the ostrich approach as given in the Student Manual. **epo4-manual** This meant measuring the inductance of both of the coils while connected in *series-aiding* and *series-opposing* at a varying distance between the coils. The results are shown in Table 2.3.

Table 2.3: Mutual inductance and coupling factor at varying distance

Distance	Aiding inductance	Opposing inductance	Mutual inductance	Coupling factor
0 cm	184.3 µH	58.6 µH	314.2 µH	0.64
2 cm	151.5 µH	86.8 µH	161.8 µH	0.33
4 cm	135.6 µH	100.0 µH	88.9 µH	0.18
6 cm	127.5 µH	107.0 µH	51.2 µH	0.11

By making use of an equivalent circuit we were able to calculate the theoretical power transfer to the load. The equivalent circuit translated to a mathematical relationship is given by

$$\vec{\mathbf{I}}\mathbf{Z} = \begin{bmatrix} I_{source} \\ I_{load} \end{bmatrix} \begin{bmatrix} R_1 + j\omega L_1 & j\omega M \\ j\omega M & R_2 + j\omega L_2 + R_L \end{bmatrix} = \vec{\mathbf{V}} = \begin{bmatrix} V_{source} \\ 0 \end{bmatrix}. \tag{2.1}$$

Here the internal resistances of the coils are denoted by R_1 and R_2, the mutual inductance by M, the inductances by L_1 and L_2, the voltage source current by I_{source} and the load current by I_{load}. By using this relationship, we tried to approximate the power transfer characterics. The calculated values are given in Table 2.4.

Table 2.4: Power transfer simulations

Distance	Source voltage	Source current	Source power	Load voltage	Load power	Efficiency
0 cm	20 V	0.1210 A	2.42 W	4.87 V	2.31 W	96 %
2 cm	20 V	0.0216 A	0.43 W	2.00 V	0.39 W	90 %
4 cm	20 V	0.0069 A	0.13 W	1.04 V	0.11 W	77 %
6 cm	20 V	0.0032 A	0.06 W	0.59 V	0.03 W	53 %

Our equivalent circuit only incorporates the losses of the internal resistances of the coils. We therefore expect the calculated efficiency and source power and consequently current to be inaccurate. Finally, we performed some measurements on the entire converter, including coils, to see how much power could be delivered to a 10.08 Ω load, with a distance of 2 cm between the coils.

Table 2.5: Power transfer measurements

Distance	Source voltage	Source current	Source power	Load voltage	Load power	Efficiency
2 cm	19.998 V	0.0835 A	1.67 W	2.02 V	0.405 W	24.2 %

As expected, the effiency and source power and current do not match the calculated values. However, the transferred power does match the result of the simulation.

Questions

1. The open and short circuit test is not well suited for the air core transformer, because that method depends on the coupling factor being very high and thus leakage flux being really low. For a ferrite-core transformer this assumption may hold, but for an air core transformer it does not, since the coupling factor decreases very fast, as the distance between the coils increases (this can be seen in Table 2.3).
2. To determine the mutual inductance of two coils, one can use the series-opposing and series-aiding method. This method makes use of the fact in both a series-aiding and series-opposing configuration, the influence of the inductance of the coils in the total inductance, that means also incorporating the mutual inductance, is the same. Thus, by substracting the measured values of the total inductance in a series aiding and series opposing configuration, one is able to substract the value of the mutual inductance because the influence of the inductances of the two coils is filtered out. However, the mutual inductance and the inductance of the two coils is heavily influenced by external factors. This should be kept in mind.
3. As the distance increases, the coupling factor k decreases. Because the magnetising inductance M is given by $k\sqrt{L_1 L_2}$, the magnetising inductance thus also decreases. Consequently, the leakage inductances L_{L1} and L_{L2} increase because they are given by $L_{Li} = (1-k)L_i$. This result can also be obtained by arguing that the leakage flux increases by increasing the distance between the coils. An increase in leakage flux corresponds with an increase of L_{L1} and a decrease of L_M.
4. As shown in Table 2.5, the power transfer of the transformer is very low. This is due to the low coupling factor, especially at higher distances between the two coils.

3 | Assignment 3

Design

The amount of power transferred to the load is desired to be as high as possible. One can see that by minimizing the impedance seen by a voltage source, the drawn power is maximized. It is therefore desired to compensate the impedance of the coils by making use of compensating capacitors. By equating the impedances of the coils and their capacitors, the capacitance of these capacitors can be calculated. This relationship is given by

$$C = \frac{1}{(2\pi f)^2 L}. \tag{3.1}$$

Using Equation 3.1 we obtain values of 26.8 nF for the primary side and 100.1 nF for the secondary side. Using a series combination of three times a parellel combination of two 22 nF and one 33 nF capacitor, all with a small deviation for the primary side and a parallel combination of a 33 nF and a 67 nF capacitor for the secondary side, we obtained real-world values of 26.4 nF for de primary side and 100.0 nF for the secondary side.

Expanding the model used in assignment 2 with the compensating capacitors we derive

$$\vec{\mathbf{I}}\mathbf{Z} = \begin{bmatrix} I_{source} \\ I_{load} \end{bmatrix} \begin{bmatrix} R_1 + j\omega L_1 + (j\omega C_1)^{-1} & j\omega M \\ j\omega M & R_2 + j\omega L_2 + (j\omega C_2)^{-1} + R_L \end{bmatrix} = \vec{\mathbf{V}} = \begin{bmatrix} V_{source} \\ 0 \end{bmatrix}. \tag{3.2}$$

The values of the compensating capacitors are denoted by C_1 and C_2. The results of the simulation are displayed in Table 3.1.

Table 3.1: Power transfer simulations - compensated

Distance	Source voltage	Source current	Source power	Load voltage	Load power	Efficiency
0 cm	20 V	0.5353 A	10.70 W	10.32 V	10.38 W	97 %
2 cm	20 V	1.9639 A	39.27 W	19.59 V	37.39 W	95 %
4 cm	20 V	5.6343 A	112.68 W	32.27 V	101.46 W	90 %
6 cm	20 V	9.4482 A	188.96 W	38.86 V	147.18 W	78 %

Rewriting Equation 3.2 results in the transfer function given by

$$|H(s)| = \frac{sMZ_L}{(sM)^2 - (sL_2 + R_2 + (sC_2)^{-1} + Z_L)(sL_1 + R1 + (sC_1)^{-1}))}. \tag{3.3}$$

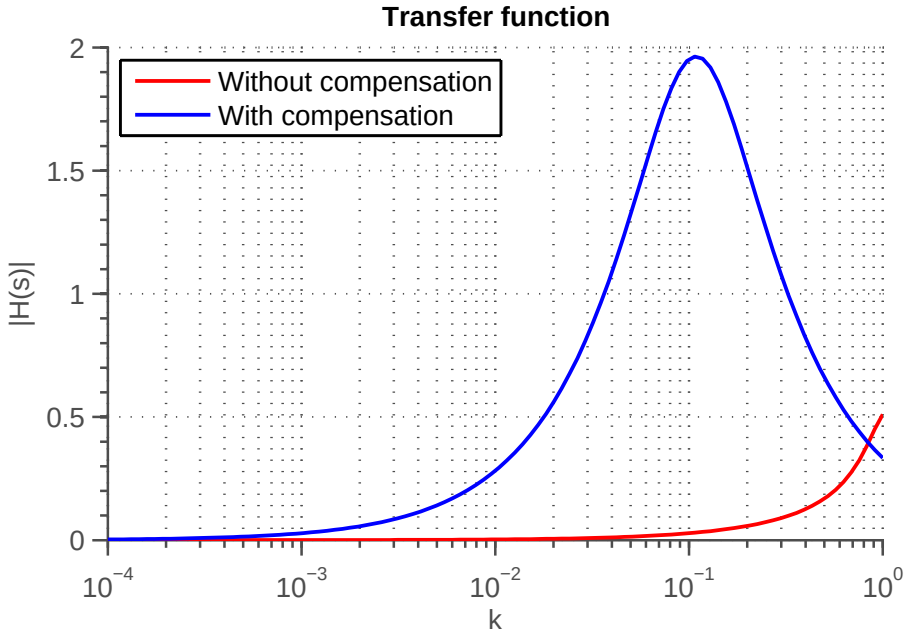

Figure 3.1: Transfer function with and without compensation

Graphically evaluating Equation 3.3 results in Figure 3.1. It is clear that one can maximize the power transfer after adding the compensating capacitors. This optimum is an equilibrium between the losses of the increasing leakage inductances and increased power drawn from the voltage source. The power drawn from the voltage source is proportional to the current drawn. The current drawn is proportional to the impedance seen by the voltage source, which decreases if the mutual inductance decreases. Therefore, the power drawn increases if the mutual inductance decreases.

Results

To test our design, we studied its waveforms using the oscilloscope. Screenshots of this are included in Appendix **??**. From this waveforms may be concluded that the inverter will generate a correct DC-signal when rectified. We also performed the same power transfer measurements as with the uncompensated converter, whose results are displayed in Table 3.2.

Table 3.2: Power transfer measurements - compensated

Distance	Source voltage	Source current	Source power	Load voltage	Load power	Efficiency
2 cm	19.998 V	1.2472 A	24.942 W	14.8 V	21.3 W	85.6 %

If we compare these results with Table 2.5 from the uncompensated converter, we see that the delivered power is more than fifty times higher, while the efficiency more than tripled. However, the measured values deviate a lot from the simulated values. This is due to the sensibility of the setup to external factors, such as mechanical placement. With the compensated converter, charging the supercapacitor bank took us little under three minutes.

Questions

1. Performing Fourier analysis to a square wave reveals that the fundamental sinus, which is a sinus with the same frequency of the square, is most influential. The system we are analysing is linear. Therefore, we can conclude that the reponse to the square wave can be approximated by the reponse to its fundamental sinus.
2. In a voltage oriented system, the power transfer can be maximized by maximizing the current. By compensating the impedance of the coils, we can minimize the impedance seen by the voltage source and consequently maximize the power transfer.
3. When the secondary coil is not present, the equivalent circuit reduces to a single loop with a tiny resistance, capacitance and inductance. Since the capacitance and inductance are designed to be in resonance, the impedance of the loop is very low. This allows for a very high current to flow, which could overload the converter and its power source.
4. To overcome this problem an overcurrent protection circuit is built in. This circuit measures the voltage over a shunt resistance and compares this to a reference voltage. When the shunt voltage (and thus the source current) exceeds the reference voltage, the circuit will trigger via positive feedback (being a Schmitt-trigger), so the output of the circuit becomes a logical '1'. This output signal is connected to the UC3525's *shutdown*-input, so it will stop generating the PWM-signal. This way the converter is turned off, until the reset button is pressed.

Assignment 4

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Appendices

Inverter Schematics

Inverter Waveforms