Electric Transport

Deliverable report 1

EPO-4

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Contents

Introduction

introduction

Assignment 1

The first step in designing our DC/DC converter meant we had to incorporate the used UC3525 Regulating Pulse Width Modulator and IRS2001PBF Gate Drivers into a full bridge converter (the DC/AC step), while at the same time integrating the given overcurrent protection circuit in the correct way. Since connection schemes for both the UC3525 and the IRS2001PBF were given in their respective datasheets [1], [2], this did not pose much of a problem. Because the focus was not on calculating resistor and capacitor values, we will not discuss our choice in this report. We will, however discuss our choice of the used MOSFET transistors and Diodes. The most important factors in picking the correct transistor for our application were static and dynamic power dissipation.

MOSFET choice

All three of the MOSFETs (IPP50CN10N, IPP028N08N3G, PSMN017) were viable options, because our circuit parameters were well within their given margins. To pick one of the three, we calculated the power loss of each one, to see which one of them would do best. Static power dissipation can be calculated using:

$$P_s = I_{DS} R_{DS(on)} D \tag{1}$$

Where I_{DS} is the drain-source current through the transistor, $R_{DS(on)}$ is the transistors drain-source resistance, when switched on and D is the duty-cycle of the PWM control signal. We estimated I_{DS} to be approximately 2 A and chose D to be 0.5. $R_{DS(on)}$ is a transistor parameter which can be found in each datasheet. Dynamical power dissipation is the power that is lost charging the in- and output capacitances of the transistors (both found in transistor datasheets [3]–[5]) and thus is given by:

$$P_d = (C_{in} V_{GS}^2 + C_{out} V_{DS}^2) f_s \tag{2}$$

Where C_{in} and C_{out} are the transistor's in- and output capacitances V_{GS} is the gate-source voltage on the transitor (estimated to be 15 V in our calculations), V_{DS} is the drain-source voltage on the transistor (also 15 V) and f_s is the switching frequency, which is 100 kHz. The total power dissipation thus becomes:

$$P = P_s + P_d = I_{DS} R_{DS(on)} D + (C_{in} V_{GS}^2 + C_{out} V_{DS}^2) f_s \tag{3}$$

Using this equation yields the following results for each of the three transistors to pick from:

Table 1: MOSFET power loss calculations

MOSFET	$R_{DS(on)}$	C_{in}	C_{out}	Static loss	Dynamic loss	Total loss
IPP50CN10N	49 mΩ	822 pF	120 pF	0.098 W	0.021 W	0.119 W
IPP028N08N3G	2.8 mΩ	10 700 pF	2890 pF	0.006 W	0.306 W	0.311 W
PSMN017	13.7 mΩ	1573 pF	154 pF	0.027 W	0.039 W	0.066 W

From Table 1 we concluded the PSMN017 would be the best transistor to use.

Diode choice

In choosing one of the two given diodes (SB540 and SF61), we decided that the forward voltage would be the most important factor, as all other parameters were well within their margins. Because the SB540 has a forward voltage of 0.55 V, which is lower than the forward voltage of the SF61 (0.975 V) we picked the SB540. [6], [7]

Final design and testing

Implementing the PWM-generator, gate drivers (2x), overcurrent protection circuit and rectifier with overvoltage buzzer circuit resulted in the schematics found in Appendix .
After soldering the PCB we got from our consultant we hooked it up to an oscilloscope, on which we then measured tidy square waves for the gate drivers and power outputs, whose frequency and duty-cycle could be varied by changing the values of the two potmeters in the design. While inspecting the rectifier output waveform, we obtained a nice DC-signal, with very little ripple, due to the high switching frequency (i.e. compared to for example the rectifier used during EPO1 at 50 Hz).
Actual waveforms of the entire converter, including air transformer and compensation, can be found in Appendix .

Assignment 2

Calculation

By using this calculator: `http://deepfriedneon.com/tesla_f_calcspiral.html`; we obtained acceptable inductances for our coils at the coil parameters as given in Table 2. Target parameters were an inner diameter of 50 mm for both coils and inductances of 22 µH for the secondary coil and 100 µH for the primary coil. The diameter of the given Litz-wire is 1.8 mm and we estimated an average wire spacing of 0.5 mm between each winding.

Table 2: Calculated coil parameters

Coil	Windings	Inductance	Outer diameter	Total wire length
Primary	30	101.6 µH	188 mm	11.2 m
Secondary	15	22 µH	119 mm	4 m

Measurements

After winding these coils we obtained the following inductances for the individual coils using an LCR-meter:

Table 3: Measured coil parameters

Coil	Inductance	DC-resistance
Primary	94.5 µH	250 mΩ
Secondary	25.2 µH	65 mΩ

Then, we calculated the coils' mutual inductance and coupling factor via the ostrich approach as given in the Student Manual. [8] This meant measuring the inductance of both of the coils while connected in *series-aiding* and *series-opposing* at a varying distance between the coils. The results are shown in Table 4.

Table 4: Mutual inductance and coupling factor at varying distance

Distance	Aiding inductance	Opposing inductance	Mutual inductance	Coupling factor
0 cm	184.3 µH	58.6 µH	314.2 µH	0.6443
2 cm	151.5 µH	86.8 µH	161.8 µH	0.3318
4 cm	135.6 µH	100.0 µH	88.9 µH	0.1823
6 cm	127.5 µH	107.0 µH	51.2 µH	0.1051

Lastly, we performed some measurements on the entire converter, including coils, to see how much power could be delivered to a 10.08 Ω load, with a distance of 2 cm between the coils:

Table 5: Power transfer measurements

Source voltage	Source current	Source power	Load voltage	Load power	Efficiency
19.998 V	0.0835 A	1.67 W	2.02 V	0.405 W	24.2 %

Questions

1. The open and short circuit test is not well suited for the air core transformer, because that method depends on the coupling factor being very high and thus leakage flux being really low. For a ferrite-core transformer this assumption may hold, but for an air core transformer it does not, since the coupling factor decreases very fast, as the distance between the coils increases (see table 4).
2. ?
3. As the distance between the two coils increases, less flux lines go through the secondary coil. Because of this, the magnetising inductance decreases while the leaking inductance increases.
4. As shown in Table 5, the power transfer of the transformer is very low. This is due to the low coupling factor, especially at higher distances between the two coils.

Assignment 3

Design

As stated in the Student Manual, the imaginary part of the impedance in each current loop (primary and secondary) is desired to be zero, for optimum power transfer. From this equation the following can be derived for both the primary and secondary side:

$$C = \frac{1}{\omega^2 L} \tag{4}$$

Using 4 we obtain values of 26.8 nF for the primary side and 100.1 nF for the secondary side. Using a series combination of three times a parellel combination of two 22 nF and one 33 nF capacitor, all with a small deviation for the primary side and a parallel combination of a 33 nF and a 67 nF capacitor for the secondary side, we obtained real-world values of 26.4 nF for de primary side and 100.0 nF for the secondary side.

Results

To test our design, we studied its waveforms using the oscilloscope. Screenshots of this are included in appendix From this waveforms may be concluded that the inverter will generate a correct DC-signal when rectified. We also performed the same power transfer measurements as with the uncompensated converter, the results are in Table 6

Table 6: Power transfer measurements - compensated

Source voltage	Source current	Source power	Load voltage	Load power	Efficiency
19.998 V	1.2472 A	24.942 W	14.8 V	21.3 W	85.6 %

If we compare these results with Table 5 from the uncompensated converter, we the delivered power is more than fifty times higher, while the efficiency more than tripled. With the compensated converter, charging the supercapacitor bank took us little under 3 minutes.

Questions

1. ?
2. The imaginary part of both of the converter's sides should equal zero. This way power transfer is maximized, because leakage inductances are compensated for, thus the power factor is increased. This can be accomplished by compensating both coils with a capacitance.
3. When the secondary coil is not present, the equivalent circuit reduces to a single loop with a tiny resistance, capacitance and inductance. Since the capacitance and inductance are designed to be in resonance, the impedance of the loop is very low. This allows for a very high current to flow, which could overload the converter and its power source.
4. To overcome this problem an overcurrent protection circuit is built in. This circuit measures the voltage over a shunt resistance and compares this to a reference voltage. When the shunt voltage (and thus the source current) exceeds the reference voltage, the circuit will trigger via positive feedback (being a Schmitt-trigger), so the output of the circuit becomes a logical '1'. This output signal is connected to the UC3525's *shutdown*-input, so it will stop generating the PWM-signal. This way the converter is turned of, until the reset button is pressed.

Assignment 4

bla

Bibliography

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[5] NXP Semiconductors. (Sep. 2011). N-channel 80 v 17 mΩstandard level mosfet in to220, [Online]. Available: http://www.nxp.com/documents/data_sheet/PSMN017-80PS.pdf.

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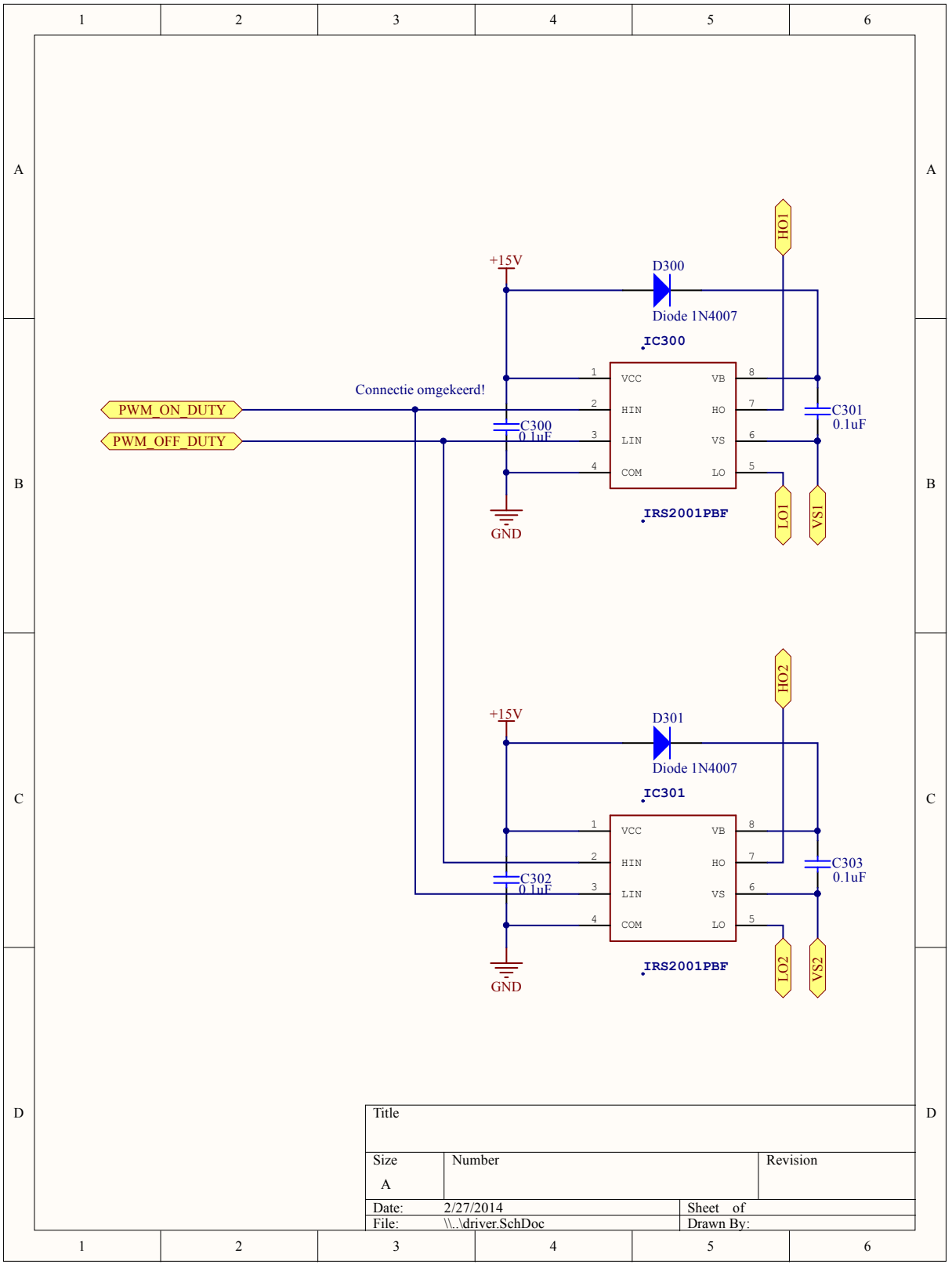
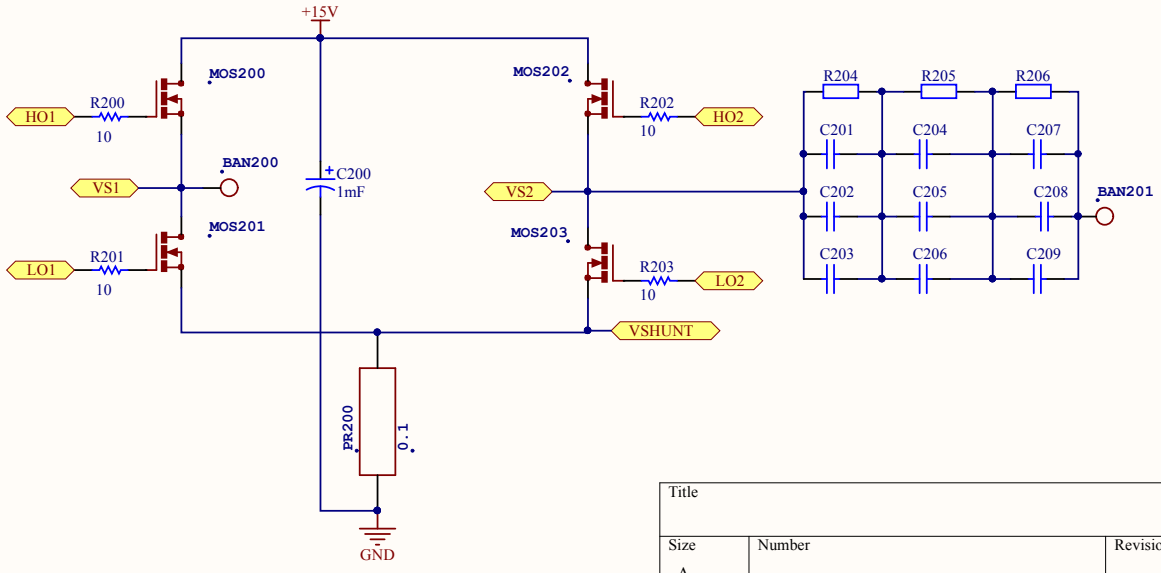
[8] P. Bauer, G. Delgado Lopes, G. Jansen, D. Jeltsema, B. Kooij, I. Lager, N. van der Meijs, J. van der Merwe, J. Popovic, E. Roeling, D. Tax, A. van der Veen, T. Velzeboer, and M. Weskin, *Electric Transport 2020 - Student Manual*. Delft University of Technology, 2014.

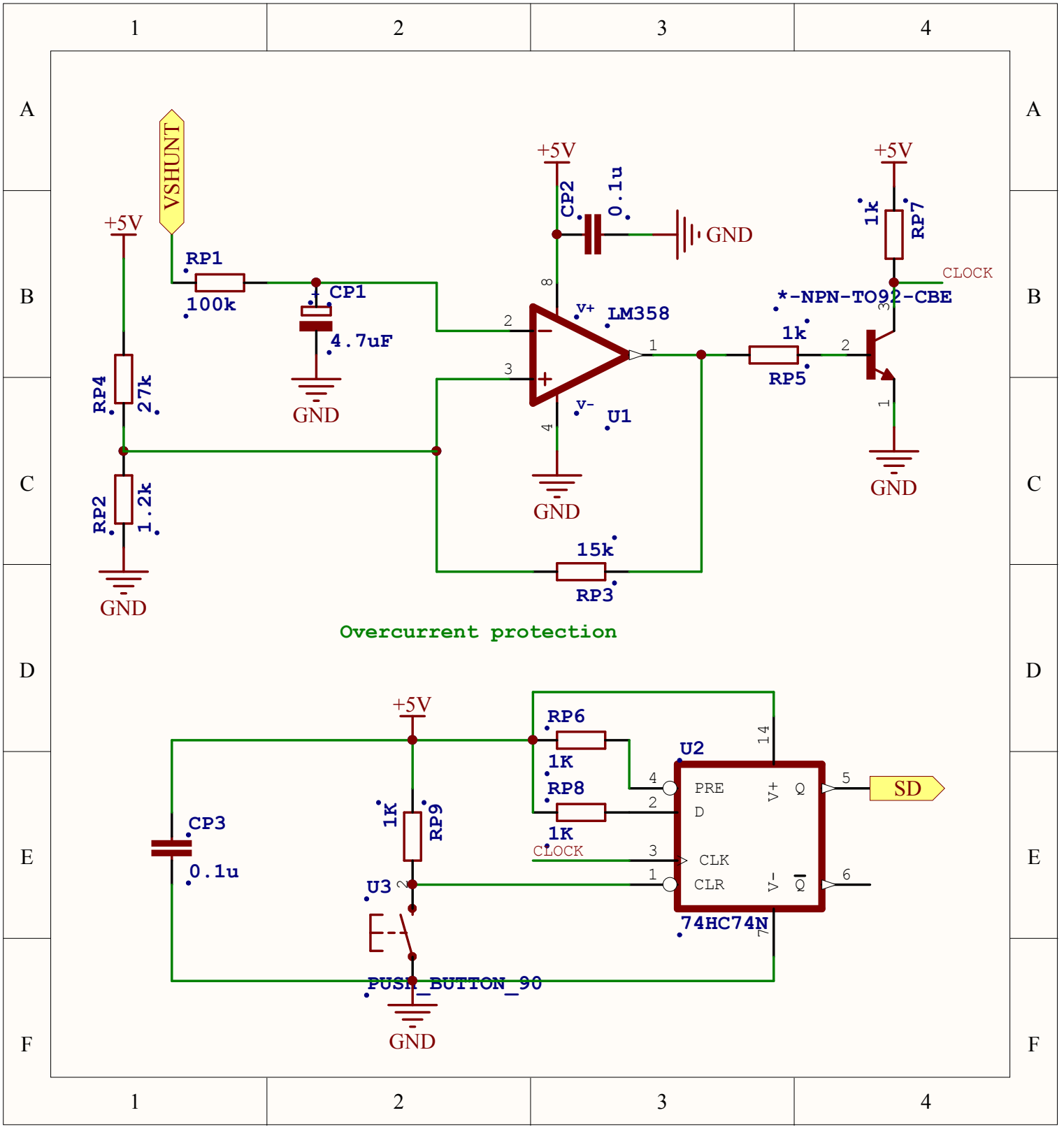
Appendices

Inverter Schematics


1
2
3
4
5
6
A
B
C
D
HO1
+15V
D300
Diode 1N4007
IC300
Connectie omgekeerd!
PWM_ON_DUTY
PWM_OFF_DUTY
C300
0.1uF
C301
0.1uF
VCC
HIN
LIN
COM
VB
HO
VS
LO
IRS2001PBF
GND
LO1
VS1
HO2
+15V
D301
Diode 1N4007
IC301
C302
0.1uF
C303
0.1uF
IRS2001PBF
GND
LO2
VS2
Title
Size
A
Number
Revision
Date: 2/27/2014
Sheet of
File: \\..\driver.SchDoc
Drawn By:



Title		
Size A	Number	Revision
Date: 2/27/2014		Sheet of
File: \\..\inverter.SchDoc		Drawn By:


VSHUNT
+5V
RP1
100k
CP1
4.7uF
GND
RP4
27k
RP2
1.2k
GND
+5V
CP2
0.1u
GND
8
V+
LM358
2
3
1
4
V-
U1
GND
15k
RP3
+5V
1k
RP7
CLOCK
*-NPN-TO92-CBE
3
1k
RP5
2
1
GND
Overcurrent protection
+5V
RP6
1K
RP8
1K
CLOCK
U2
14
4
2
3
1
PRE
D
CLK
CLR
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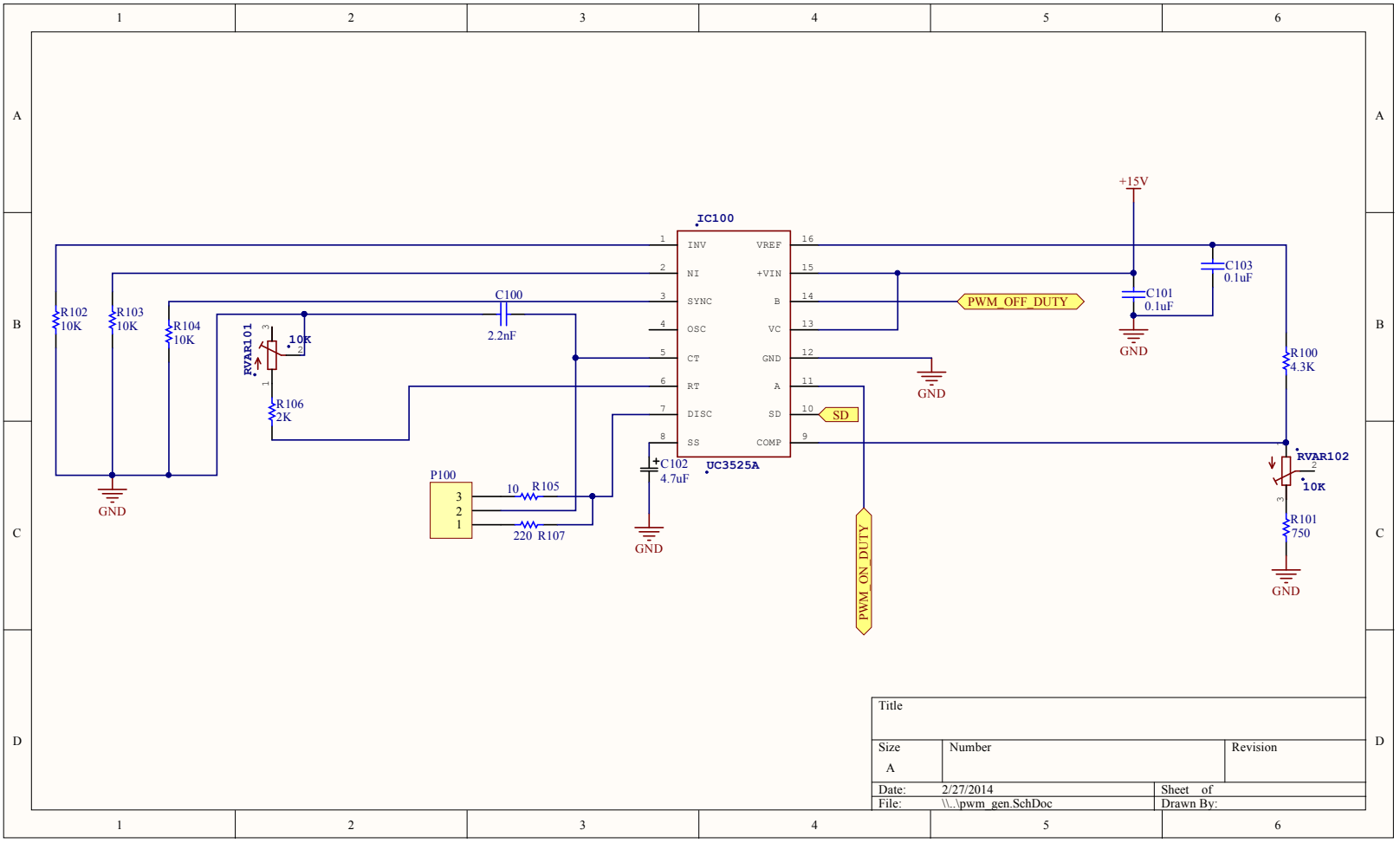
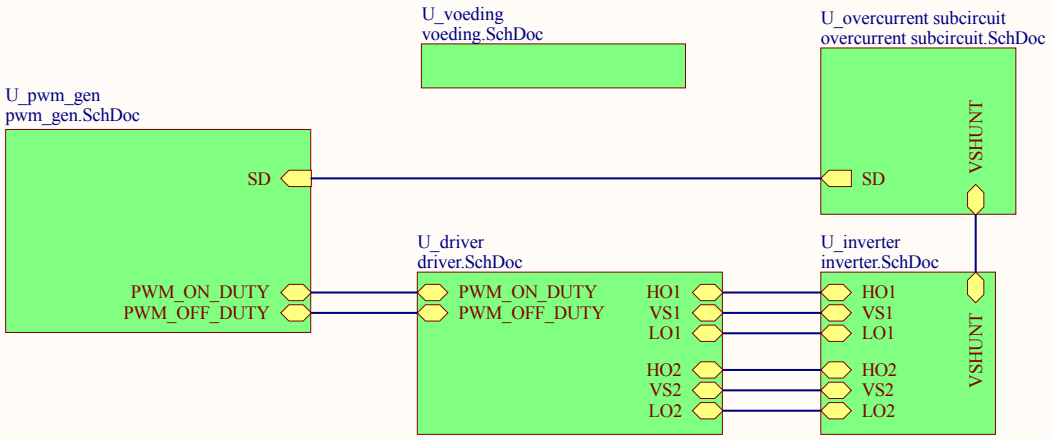
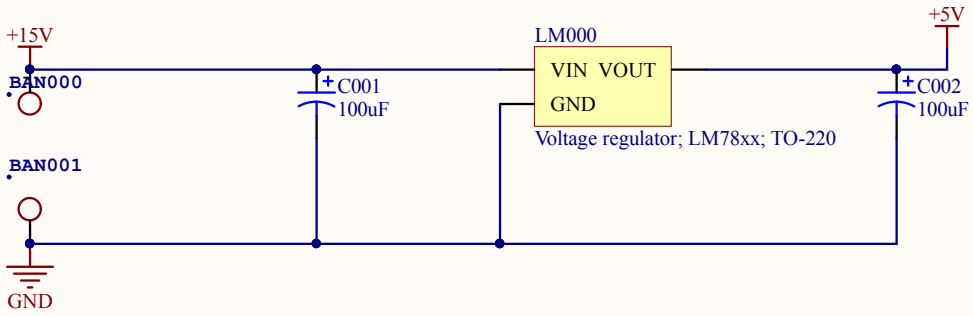
Q
V-
Q
5
6
7
SD
74HC74N
CP3
0.1u
1K
RP9
U3
2
PUSH_BUTTON_90
GND


IC100
UC3525A
INV
NI
SYNC
OSC
CT
RT
DISC
SS
VREF
+VIN
B
VC
GND
A
SD
COMP
R102 10K
R103 10K
R104 10K
RVAR101 10K
R106 2K
C100 2.2nF
C102 4.7uF
P100
R105 10
R107 220
PWM_OFF_DUTY
PWM_ON_DUTY
SD
+15V
C101 0.1uF
C103 0.1uF
R100 4.3K
RVAR102 10K
R101 750
GND
Title
Size A
Number
Revision
Date: 2/27/2014
Sheet of
File: \\..\pwm_gen.SchDoc
Drawn By:



Title			
Size: A	Number		Revision
Date:	2/27/2014	Sheet of	
File:	\\..\toplevel_inverter.SchDoc	Drawn By:	



Title			
Size A	Number		Revision
Date:	2/27/2014	Sheet of	
File:	\\..\voeding.SchDoc	Drawn By:	

Inverter Waveforms