1 | Assignment 1

The first step in designing our DC/DC converter meant we had to incorporate the used UC3525 Regulating Pulse Width Modulator and the IRS2001PBF Gate Drivers into a full bridge converter (the DC/AC step), while at the same time integrating the given overcurrent protection circuit in the correct way. Since connection schemes for both the UC3525 and the IRS2001PBF were given in their respective datasheets **uc3525a-datasheet**, **irs2001pbf-datasheet** this did not pose much of a problem. The focus was not on calculating the resistors and capacitors values, therefore we will not discuss the choices we made regarding these values. However, we will discuss our choice of the used MOSFET transistors and diodes. The most important factors in picking the correct transistor for our application were static and dynamic power dissipation.

1.1 MOSFET choice

All three of the MOSFETs (IPP50CN10N, IPP028N08N3G, PSMN017) were viable options, because our circuit parameters were well within their given margins. To pick one of the three, we calculated the power loss of each one, to see which one of them would do best. Static power dissipation can be calculated using

$$P_s = I_{DS} R_{DS(on)} D. \tag{1.1}$$

Where I_{DS} is the drain-source current through the transistor, $R_{DS(on)}$ is the transistors drain-source resistance, when switched on and D is the duty-cycle of the PWM control signal. We estimated I_{DS} to be approximately 2 A and chose D to be 0.5. $R_{DS(on)}$ is a transistor parameter which can be found in each datasheet. Dynamical power dissipation is the power that is lost charging the in- and output capacitances of the transistors (both found in transistor datasheets **IPP50CN10N-datasheet**, **IPP028N08N3G-datasheet**, **PSMN017-datasheet**) and is given by

$$P_d = (C_{in} V_{GS}^2 + C_{out} V_{DS}^2) f_s. \tag{1.2}$$

C_{in} and C_{out} are the transistor's in- and output capacitances, V_{GS} is the gate-source voltage on the transitor (estimated to be 15 V in our calculations), V_{DS} is the drain-source voltage on the transistor (also 15 V) and f_s is the switching frequency, which is 100 kHz. The total power dissipation thus becomes

$$P = P_s + P_d = I_{DS} R_{DS(on)} D + (C_{in} V_{GS}^2 + C_{out} V_{DS}^2) f_s. \tag{1.3}$$

Using this equation yields the results in Table 1.1 for each of the three transistors to pick from.

Table 1.1: MOSFET power loss calculations

MOSFET	$R_{DS(on)}$	C_{in}	C_{out}	Static loss	Dynamic loss	Total loss
IPP50CN10N	49 mΩ	822 pF	120 pF	0.098 W	0.021 W	0.119 W
IPP028N08N3G	2.8 mΩ	10 700 pF	2890 pF	0.006 W	0.306 W	0.311 W
PSMN017	13.7 mΩ	1573 pF	154 pF	0.027 W	0.039 W	0.066 W

From Table 1.1 we concluded the PSMN017 would be the best transistor to use.

1.2 Diode choice

In choosing one of the two given diodes (SB540 and SF61), we again considered the dynamic and static power loss. When assuming that the output voltage is near constant, the static dissipation, in context of the inverter, is given by

$$P_s = IV_{fw}D_d \tag{1.4}$$

in which I represents the current flowing through the diodes, V_{fw} the forward voltage drop and D_d the *diode duty cycle*. The diode duty cycle determines the percentage of time in which current flows through the diode with respect to the switching frequency. D_d is given by

$$D_d = \frac{1}{2} + arcsin\left(\frac{V_{min}}{V_{max}} - 1\right) \tag{1.5}$$

in which the minumum and maximum output voltage of the inverter is represented by V_{min} and V_{max}. The dynamic power dissipation is per diode given by

$$P_s = C_j V_{DS}^2 \tag{1.6}$$

in which the junction capacitance is represented by C_j. Combining equations 1.4, 1.5 and 1.6 yielded a total power loss of 0.0784 W for the SB540 and 0.139 W for the SF61, so we picked the SB540. **SB540-datasheet**, **SF61-datasheet**

1.3 Design and testing

Implementing the PWM-generator, two gate drivers, the overcurrent protection circuit and the rectifier with overvoltage buzzer circuit resulted in the schematics found in Appendix **??**. After soldering the PCB we got from our consultant we hooked it up to an oscilloscope, on which we then measured tidy square waves for the gate drivers and power outputs, whose frequency and duty-cycle could be varied by changing the values of the two potmeters in the design. While inspecting the rectifier output waveform, we obtained a nice DC-signal, with very little ripple, due to the high switching frequency (i.e. compared to for example the rectifier used during EPO1 at 50 Hz). Actual waveforms of the entire converter, including air transformer and compensation, can be found in Appendix **??**.

1.4 PCB design

After finishing the schematics, we implemented these on a printable circuit board (PCB). Figure 1.1 contains a 3D view of the developed PCB. More detailed information can be found in Appendix **??**. The PCB is designed with a feature size of 0.2 mm to deliver a nominal output current of 6 A.

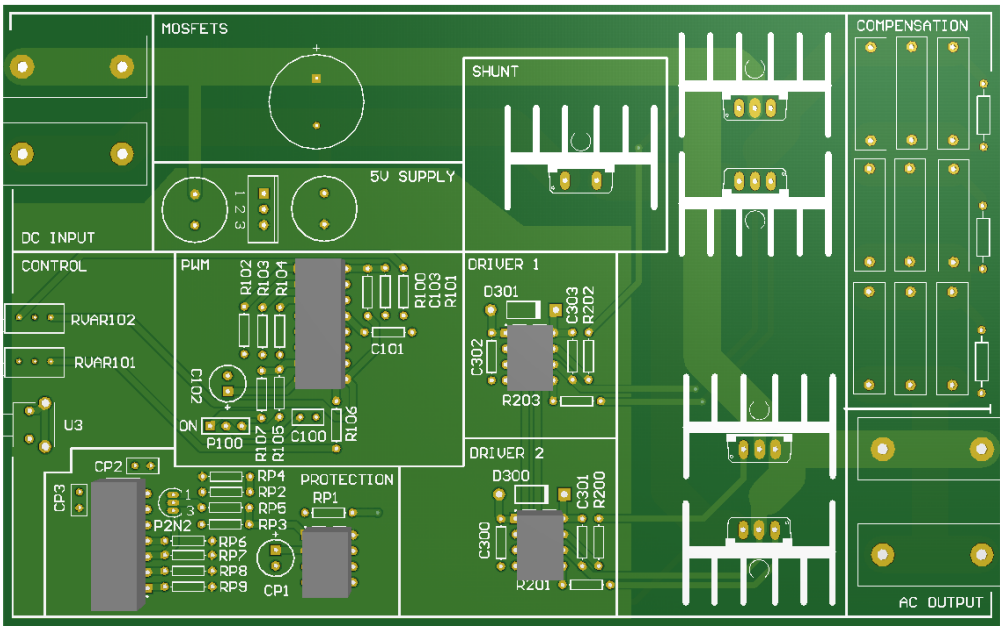

Figure 1.1: 3D view of the PDB