FACULTY OF SCIENCE
UNIVERSITY OF COPENHAGEN

Programming Massively Parallel Hardware – Optimising Tridag

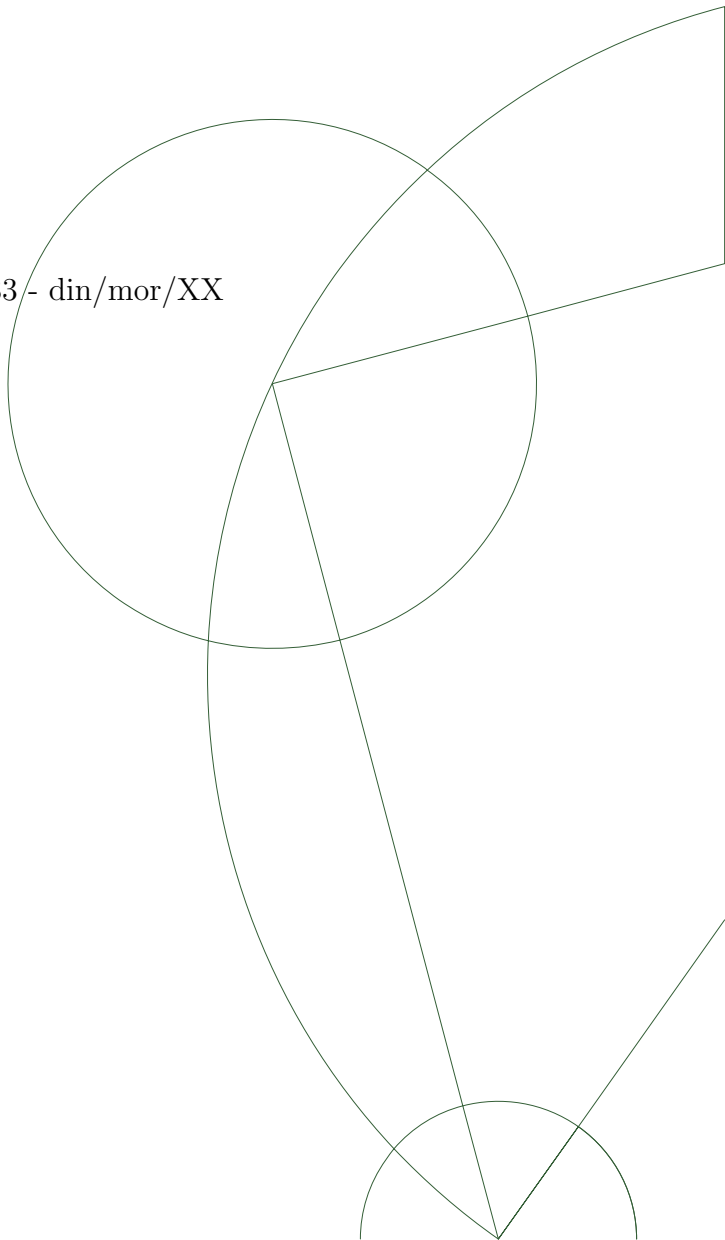
Group Project
Department of Computer Science

Written by:

Morten Espensen & Niklas Høj & Mathias Svennson
dzr440 - 19/06/1991 & nwv762 - 24/07/1991 & tpx783 - din/mor/XX
October 31, 2014

Supervised by:

Cosmin E. Oancea



Contents

Chapter 1

Transformations

Our initial approach to implementing a CUDA version in this project was just to get started with converting the different parts of the program into a CUDA ready format, thus simplifying parts and transforming parts which were not easily implemented in CUDA kernels.

1.1 Tridag Rewrite

1.2 Naive CUDA implementation

1.3 Propagating outer loop into rollback

1.4 Optimising coalesced memory access

Chapter 2

Will it validate?

Yes.

Chapter 3

Results

Data set size / Implementation	Small	Medium	Large
Sequential with flatten arrays	2162560μs	5652265μs	195845401μs
OpenMP	183016μs	241972μs	9680948μs
Naive CUDA	3956322μs	3639421μs	34980508μs
Optimised CUDA	183016μs	241972μs	9680948μs