Digital Systems

Homework 5

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14.10.2020

Contents

Task Description

I had to:

- *To modify the previous code so that it can determine the type of memory and branch instructions too. Also I had to use git source control.*

Solution

- *I only had to replicate the code that I did for data instruction..I have also created a repository on github and connected my local files to that repository. Here is the code:*

module datamodule(

input [31:0] inst,

output reg[1:0] instype,

output reg [2:0] datainstype,

output reg [1:0] meminstype,

output reg [1:0] branchinstype

*   );*

*   reg [1:0] bits;*

```verilog
    always @(inst)
begin
bits[0]=inst[26];
bits[1]=inst[27];
    case(bits)
    0: begin instype=1;
            if(inst[25]==1)
            datainstype=1;
            else if(inst[4]==0&&inst[25]==0)
            datainstype=2;
            else if(inst[7]==0&&inst[4]==1&&inst[25]==0)
            datainstype=3;
            else
if(inst[24]==0&&inst[6]==0&&inst[5]==0&&inst[7]==1&&inst[4]==1&&inst[25]==0)
            datainstype=4;
            else
            datainstype=0;


        end


    1: begin instype=2;
            if(inst[25]==1)
            meminstype=1;
            else if(inst[4]==1&&inst[25]==0)
            meminstype=2;
            else
            meminstype=0;
```

```
        end


2: begin instype=3;

        if(inst[25]==1&&inst[24]==0)

        branchinstype=1;  //branch

        else if(inst[25]==1&&inst[24]==1)

        branchinstype=2;  //branch and link

        else

        branchinstype=0;


    end
3: instype=0;
endcase
end
endmodule
```
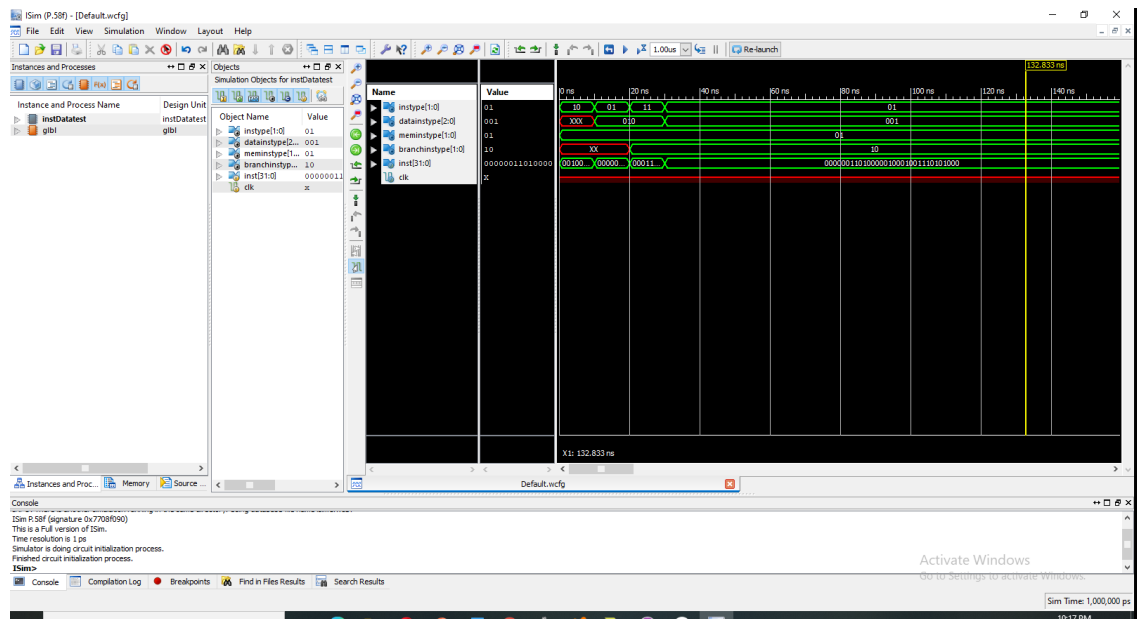
Simulation & Verification

- *Simulations of the code*

- *Here is the link to my github repository:*
https://github.com/NinoNonikashvili/DL475-instructions.git

Conclusion

- *The most important part of this homework was to get us familiar with git. I had a good practice of using github.*